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The Effect of Offcut Angle on Electrical Conductivity of Direct Wafer-Bonded n-GaAs/n-GaAs Structures for Wafer-Bonded Tandem Solar Cells

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Publication Date
2012

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The Effect of Offcut Angle on Electrical Conductivity of Direct Wafer-Bonded n-GaAs/n-GaAs Structures for Wafer-Bonded Tandem Solar Cells

A thesis submitted in partial satisfaction of the requirements for the degree of Master of Science in Materials Science and Engineering

By

King Wah Sunny Yeung

2012
ABSTRACT OF THE THESIS

The Effect of Offcut Angle on Electrical Conductivity of Direct Wafer-Bonded n-GaAs/n-GaAs Structures for Wafer-Bonded Tandem Solar Cells

By

King Wah Sunny Yeung
Master of Science in Materials Science and Engineering
University of California, Los Angeles, 2012
Professor Mark S. Goorsky, Chair

III-V compound semiconductors possess advantageous materials properties, such as direct bandgap and high carrier mobility, which make them attractive in optoelectronic, fiber optical communications and high-speed digital circuit applications. Integration of III-V heterostructures using direct wafer bonding has the added benefit of avoiding constraints in lattice parameter mismatch compared to epitaxially grown devices. As a result, wafer bonding is significant in its ability to integrate mismatched materials and circumvent the issues of inferior device performance due to a high density of threading dislocations.

In the solar industry, off-axis substrates are commonly used in the growth of III-V epitaxial layers to avoid the formation of antiphase boundaries, which act as deep level non-radiative recombination centers. Previously published studies from our research group showed
that an additional sulfur-based passivation technique can reduce the density of surface charge states and improve the conductivity across the interface. However, a research topic that has not been investigated is the effect that miscut substrates have on the performance of direct-bonded III-V devices. In this study, the effect of the wafer offcut angle on the electrical conductivity of III-V solar cell devices is investigated using n-GaAs/n-GaAs wafer-bonded structures.

GaAs (001) wafers misoriented towards <111>A are chosen and compared to nominal on-axis substrates. Prior to bonding, the surfaces are treated with either an oxide etch or additional 5-min treatment in aqueous (NH₄)₂S. Off-axis wafers are positioned face-to-face with a non-zero relative surface misorientation between the tilted (001) planes and low force bonding is initiated at room temperature. The highest degree of misorientation in this study is produced using 6° off-axis wafers and can be represented as a grain boundary with a twin defect at the (1 1 1 3) plane and a tilt angle of 12° about the common [110] direction. The samples are annealed at 400 °C for two hours to strengthen the bond. It is observed that the electrical conductivity improves considerably with a short rapid thermal processing (RTP) at 600 °C for 2 mins. However, the degree of miscut has a detrimental effect, as both the oxide-etched and sulfur-treated samples exhibit increasingly non-ohmic behavior with greater relative misorientations. A theoretical model that describes the electron tunneling across a grain boundary between semiconductor bicrystals is used to represent the bonded interface and estimate the barrier conduction height. Fitting the zero-bias conductance data over a range of temperatures reveals an increased barrier height for greater offcut angles, with 4° and 6° miscut sulfur-passivated wafers producing a 0.4 eV increase. When compared to on-axis structures, the interface resistance at room temperature increases from 0.01 Ω·cm² to 3.4 Ω·cm².
High resolution transmission electron microscopy (HRTEM) and scanning transmission electron microscopy (STEM) are used to compare the interface morphology across the range of relative misorientations after the 600 °C RTP. The ratio of well-bonded crystalline regions to amorphous oxide inclusions is consistent across all bonded samples, indicating that the degree of misorientation does not affect the level of interface recrystallization. It is also observed that regions adjacent to the interface undergo a process of atomic redistribution and recrystallize into the same lattice arrangement as the bulk semiconductor.

The effect of relative surface misorientation on conductivity is further investigated by fabricating zero-degree relative (001) misoriented bonded samples using 6° miscut substrates and subjecting to the same thermal and sulfur passivation treatment. This can be described as a grain boundary at the (1 1 13) plane without any twin defects about the [110] direction. Current-voltage (I-V) characteristics are comparable to nominal on-axis specimen with the interface resistance measured as 0.02 Ω·cm². It is concluded that the degree of relative misorientation of (001) planes across the bonded interface has a significant impact on the electrical properties, as illustrated by the two orders of magnitude difference in conductance.

Non-ohmic behavior has previously been discovered in direct-bonded n-type GaAs/GaAs structures. In order to pinpoint the source of this inferior conductance, several lines are physically cut into the surface with a diamond scribe to electrically isolate a portion of the metal contacts. I-V measurements are taken at various test points to compare the resistance across the different interfaces. The measured resistance across the metal-metal and metal-semiconductor-metal regions is found to be 0.8 Ω. However, the inclusion of the bonded interface results in a
significant increase in resistance to 770 $\Omega$ at zero-bias conditions. The non-ohmic behavior is confirmed to be solely attributed to the bonded interface.

These results demonstrate the potential usefulness of using off-axis substrates in the fabrication of direct wafer-bonded III-V heterostructures. More importantly, the primary effect on conductivity does not originate from the miscut substrates themselves. Instead, the out-of-plane relative misorientation of the tilted (001) planes is the critical parameter that needs to be controlled within a manufacturing environment in order to achieve acceptable electrical performance in multijunction solar applications.
The thesis of King Wah Sunny Yeung is approved.

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Mark S. Goorsky, Committee Chair

University of California, Los Angeles

2012
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Acknowledgements

I would like to thank Noah Bodzin from UCLA’s Electrical Engineering department for the cross-section TEM sample preparation on the FEI NOVA 600 Focused Ion Beam (FIB) system. Sergey Prikhodko was instrumental in performing the HRTEM/STEM imaging work of the bonded sample interfaces on the FEI TITAN S/TEM at the California NanoSystems Institute (CNSI). Dr. Yang Yang was generous in allowing me to use his research group’s thermal microprobe stage to evaluate my samples at various temperatures. Also, the CHA Mark 40 electron beam evaporation, RTP 650 and Dektak 6 Surface Profilometer at UCLA’s Nanoelectronics Research Facility (NRF) was used as a part of sample preparation. To Dr. Dwight Streit, Dr. Ya-Hong Xie, and Dr. Mark Goorsky, I appreciate your time and willingness to be on my thesis committee.

I would like to acknowledge my former and current research group colleagues: Mike Jackson, Caroline Moulet, Xiaolu Kou, Jeff McKay, David Fong, Christopher Roberts and Saurabh Sharma. They were very helpful in training me on the various laboratory equipment and providing advice on how to tackle various problems related to my thesis work. And to Professor Mark Goorsky, thank you for giving me the opportunity to join the Electronic Materials Integration Group in order to gain valuable research experience in semiconductor materials and apply my academic knowledge of material science & engineering towards a thesis project.

To my loving wife, Priya Dasgupta-Yeung, I owe a huge debt of gratitude for all her love and support in my decision to quit my previous job, move to a different city and return to graduate school to pursue another degree.
Chapter 1: Introduction

1.1 Motivation

III-V semiconductor materials are characterized by superior electronic properties when compared to more traditional elemental semiconductors such as silicon. Some of the major advantages include higher electron mobility, direct bandgap and the ability to modify its bandgap and lattice parameter by the synthesis of ternary or quaternary alloys in specific elemental proportions. In the solar industry, there is considerable motivation to design and manufacture higher efficiency devices in order to reduce the cost of solar electricity and achieve grid parity. In order to providing renewable energy at a cost comparable to the utility company, III-V materials have become increasingly utilized in the fabrication of high efficiency photovoltaic cells. The world record in solar cell efficiency is currently held by Solar Junction at 43.5%\(^1\) for their multijunction concentrators manufactured with GaAs substrates. Incident sunlight is concentrated by mirrors to 400 suns for this device to achieve the record efficiency, which is maintained up to even 1,000 suns.

Multijunction semiconductor heterostructures are the basis for the design of high efficiency solar cells due to the fact that the solar spectrum consists of photons spanning a wide range of wavelengths (approximately 250-2500 nm). The two major sources of inefficiency with a single-junction device are: (i) incident photons with energy less than the junction bandgap will not be absorbed, and (ii) photons with energy much greater than the bandgap will excite carriers to very high energy levels, leading to excess energy being released by the process of
thermalization. In order to reduce the amount of wasted energy and improve device efficiency, the concept of spectrum splitting is employed, whereby a stacked multijunction configuration is used to capture photons from a much wider range of the solar spectrum. This structure is manufactured such that the top cell possesses the highest bandgap in order to absorb short wavelength photons. Longer wavelength photons are transmitted through the top cell and instead, absorbed by the lower bandgap junctions. Power conversion efficiencies greater than the Shockley-Queisser limit of ~30% for single-bandgap devices under one sun \(^2\) can be achieved with this configuration.

The fabrication of multijunction devices typically involves the growth of epitaxial layers in a controlled environment using molecular beam epitaxy (MBE) or metal organic chemical vapor deposition (MOCVD). In order for researchers to determine the appropriate combination of junction bandgaps, computer simulations are employed to model the ideal efficiency of the device at certain operating conditions \(^3\). With this information, bandgap engineering techniques are applied to produce III-V and II-VI alloy compounds that target specific bandgaps. One of the side effects of bandgap engineering is that the overall lattice constant varies according to the relative elemental composition, leading to a mismatch in lattice parameter \(f\) and a corresponding build-up of strain energy between the epitaxial layer deposited on the substrate. Above a critical layer thickness \(h_c\) \(^4\), as defined in equation (1), the induced strain energy is released in the form of threading dislocations, which act as minority carrier recombination sites. Carrier diffusion length \(L_{TDD}\) is inversely proportional to the density of threading dislocations \(n_{TDD}\) \(^5\), as shown in equation (3), and these carriers recombine before they can contribute to the overall photocurrent. A typical solution to this problem is to grow a step-graded buffer layer in-between the
mismatched subcells in order to reduce the amount of induced strain\(^6\). However, this adds complexity and cost to the overall manufacturing process, leading some companies to adopt alternative methods of integrating mismatched subcells.

\[
h_c = \frac{b \cdot (1 - \frac{v}{4})}{4\pi \cdot |f| \cdot (1 + v)} \left[ \ln \frac{h_c}{b} + 1 \right]
\]  

\[
f = \frac{a_{epi} - a_{sub}}{a_{sub}}
\]  

where \(h_c\) is the critical film thickness, \(b\) is the magnitude of the Burgers vector of the dislocation, \(v\) is Poisson’s ratio, \(f\) is the lattice mismatch, \(a_{epi}\) is the lattice parameter of the epitaxial layer, and \(a_{sub}\) is the lattice parameter of the substrate.

\[
L_{TDD} \approx \frac{2}{\frac{3}{\pi^2} \cdot n_{TDD}^2}
\]

where \(L_{TDD}\) is the carrier diffusion length, and \(n_{TDD}\) is the threading dislocation density.

Direct wafer bonding/fusion is a technique that circumvents the limitation of epitaxial growth by allowing two lattice mismatched materials to be directly integrated via secondary Van der Waals forces without any induced strain\(^7\). A direct result of this fabrication method is the discontinuous edge between the bonded surfaces. This discontinuity can be treated as a grain boundary where interfacial charge states exist, leading to the formation of a double depletion region and a potential energy barrier to conduction\(^8\). For tandem solar devices, where conductance and optical transparency through multiple layers are important, it is critical to lower
the amount of charge trapping at the interface. In addition, III-V semiconductors are known to form unfavorable native oxides\textsuperscript{9} that are difficult to remove and would result in a highly resistive non-ohmic structure. Sulfur-based surface passivation techniques prior to hydrophobic direct bonding have been reported to reduce the density of interface charge states and enhance the electronic properties of the semiconductor surfaces\textsuperscript{10,11}. Several publications have demonstrated that sulfur is chemisorbed into the top 15-20 Å of the surface to form stable III-S and V-S bonds at the expense of undesirable oxide species\textsuperscript{11,12}.

In the solar industry, off-axis substrates are generally used in the epitaxial growth of III-V solar cells to avoid the formation of antiphase boundaries, which act as deep-level non-radiative recombination centers\textsuperscript{13}. Previous publications have reported on the degradation in linear transconductance and hence, inversion-layer electron channel mobility, for MOSFET transistors fabricated on off-axis silicon wafers\textsuperscript{14}. However, the effect of the offcut angle on the performance of direct-bonded III-V devices has not been investigated. The purpose of this research thesis is to analyze the electrical conductance with respect to the degree of offcut angle in GaAs substrates in order to understand the device performance implications of utilizing misoriented wafers in the fabrication of direct-bonded III-V structures for photovoltaic applications.
Chapter 2: Background and Theory

2.1 Wafer Bonding

Wafer bonding is an established materials integration technique in which two substrates are joined together by bringing their surfaces together and adhesion initiated by the application of a compressive force. This bonding technology has been used in the successful commercial manufacturing of devices for silicon-on-insulator (SOI) and micro-electro-mechanical systems (MEMS) applications and can be classified as either a hydrophobic or hydrophilic process. In hydrophobic bonding, a non-polar surface is established normally by soaking the sample in an oxide-etching solution such as hydrochloric acid (HCl) or hydrofluoric acid (HF). When exposed to moisture, polar water molecules do not form strong bonds with the non-polar surface. In hydrophilic bonding, the surface is terminated by a polar layer containing either oxide or hydroxide species that are formed from an extended air exposure or additional deposition processing. As a result, water molecules easily adhere to the surface due to hydrogen bonding. The level of surface hydrophilicity can be described by the equilibrium contact angle between water molecules resting on the surface. Hydrophobic surfaces are characterized by a high contact angle due to low adhesion, while the opposite is true for hydrophilic exteriors. For multijunction III-V solar applications, one of the major requirements of wafer bonding is to integrate large area semiconductor substrates together into heterostructures characterized by interfaces that possess low resistance and optical absorption. As a result, hydrophobic bonding is the appropriate processing method for our purposes, due to the removal of the native non-conductive oxide from the surface prior to bonding.
There are certain surface requirements that must be satisfied in wafer bonding. One of the most important prerequisites is a low surface micro-roughness in order to promote the formation of attractive molecular forces across the entire sample area in contact. The micro-roughness is commonly quantified by the root-mean-square (RMS) deviation of the surface about the mean height and can be measured by atomic force microscopy (AFM) considering a 40x40 μm² area. It is typically desirable for as much of the surface to be positioned within 1 nm of the opposite surface, leading to a maximum RMS roughness of 10 Å. In addition, the total thickness variation (TTV) and surface curvature are established semiconductor quality metrics used to characterize the wafer flatness, and must be maintained as low as possible to ensure the maximum amount of contact area without excessive bonding pressure.

Adhesion between the two surfaces is achieved by secondary Van der Waals forces between surface molecules as they are brought in close proximity to each other. This attractive force is rather weak and as a result, the bond strength is initially quite low at room temperature. Thermal energy initiates further surface reactions and transforms the weak Van der Waals bonds into strong covalent molecular bonds. However, high temperature thermal processing imposes a limitation on the combination of materials that can be used in the bonding procedure. For example, traditional silicon wafer fusion bonding techniques require a 1000 °C annealing step. This prevents the integration of certain combinations of materials that possess large differences in the coefficient of thermal expansion (CTE), as the mechanical stress induced by the thermal expansion of dissimilar substrates in contact would exceed the bond strength at high temperatures. Another limitation involves the over-diffusion of dopant species away from its intended junction regions under long processing times and/or temperatures. Wafers containing
electronic devices, such as CMOS integrated circuits, would also have to be excluded from these conventional bonding methods.

To circumvent these technological issues, research has been carried out to develop additional surface treatments to allow for low temperature wafer bonding that require lower temperature and shorter annealing time to achieve a sufficient bond strength. One of the more established procedures is a surface activation process that modifies the chemical bonds at room temperature and increases the overall surface energy. It can generally be categorized as: wet activation (soaking into a chemical solution) and dry activation (plasma exposure). For example, plasma-activated bonding in the fabrication of MEMS devices involves the exposure of plasma-enhanced chemical vapor deposition (PECVD) oxide to nitrogen or oxygen plasma. This allows for thermal annealing at significantly lower temperatures in the 100-300 °C range.

2.2 Off-Axis Surface Misorientation

2.2.1 Out-Of-Plane Relative Surface Misorientation

Both on-axis and offcut (001) n-GaAs wafers are used for these wafer bonding experiments. For off-axis substrates to produce a non-zero relative surface misorientation, the surfaces are positioned face-to-face prior to bonding such that the (001) planes on other side of the bonded interface are divergent, as shown in Figure 1(b). The total out-of-plane relative surface misorientation is the sum of each substrate's individual offcut angles. For off-axis substrates to produce a zero-degree relative surface misorientation, the surfaces are positioned face-to-face such that the (001) planes on adjacent sides of the interface are parallel to each
other, as shown in Figure 1(c). This can be achieved by rotating either top or bottom substrate in Figure 1(b) by 180° around the axis perpendicular to the surface prior to bonding.

![Diagram to show the various types of bonded samples: (a) zero relative surface misorientation with on-axis substrates, (b) non-zero relative surface misorientation with offcut substrates, and (c) zero relative surface misorientation with offcut substrates.](image)

2.2.2 In-Plane Rotational Misorientation

There also exists a non-zero in-plane rotational misalignment parallel to the sample surface after the substrates are bonded together, as depicted in Figure 2. The degree of twist misorientation can be measured using x-ray diffraction (XRD) by performing ω scans on the (004) plane for various ϕ stage angles, with the ϕ setting at the maximum separation ($\Delta\omega_{\text{max}}$) of the two (004) peaks corresponding to the in-plane misalignment. An example of the ω scan results is shown in Figure 3 for reference.

![Diagram of in-plane rotational misalignment of bonded samples.](image)
Figure 3. Example of x-ray diffraction (XRD) $\omega$ scan on (004) peak of offcut GaAs/GaAs bonded sample.

2.2.3 Bonded Interface Nomenclature

The bonded interface of each sample has been represented in previously published literature as a discontinuous grain boundary with a twin defect located at a certain $hkl$ plane and a tilt angle about the common [110] axis\textsuperscript{17}. The interface classification for each bonding combination is presented in Table 1.

<table>
<thead>
<tr>
<th>Wafer #1</th>
<th>Wafer #2</th>
<th>Relative Surface Misorientation (°)</th>
<th>$hkl$ plane</th>
<th>Tilt Angle (°)</th>
</tr>
</thead>
<tbody>
<tr>
<td>On-axis</td>
<td>On-axis</td>
<td>0°</td>
<td>(0 0 1)</td>
<td>0</td>
</tr>
<tr>
<td>2°</td>
<td>2°</td>
<td>4°</td>
<td>(1 1 40)</td>
<td>4</td>
</tr>
<tr>
<td>4°</td>
<td>4°</td>
<td>8°</td>
<td>(1 1 20)</td>
<td>8</td>
</tr>
<tr>
<td>6°</td>
<td>6°</td>
<td>12°</td>
<td>(1 1 13)</td>
<td>12</td>
</tr>
<tr>
<td>6°</td>
<td>6°</td>
<td>0°</td>
<td>(1 1 13)</td>
<td>0</td>
</tr>
</tbody>
</table>

2.3 Conductance Across Semiconductor Bicrystals

The discontinuous edge between the bonded surfaces can be treated as a grain boundary where interfacial charge states exist, leading to the formation of carrier traps at mid-gap energy levels. This results in the accumulation of charge, leaving behind immobile ionized dopants and
a depletion of majority charge carriers on either side of the interface. For direct-bonded n-type semiconductors, a double depletion region is formed and described by a potential energy barrier \( \phi_{BO} \) to ohmic conduction\(^8\), as shown in the energy band diagram in Figure 4. The width of this depletion region is determined by the dopant concentration, with high doping levels resulting in narrow depletion widths in order to balance the charge.

![Energy band structure for n-type semiconductor grain boundary containing interface states\(^18\).](image)

The Seager and Pike theoretical model for zero-bias conductance across semiconductor bicrystals\(^19\) is used to quantify the potential barrier height formed at the bonded interface. The conductance is derived from current-voltage (I-V) measurements across a wide range of temperatures and is fitted to this theoretical model. The electrical conductance across adjacent semiconductor bicrystals is mainly due to majority carrier transport and can be described by the following processes under forward bias: (i) activation energy-controlled thermionic emission of electrons over a potential barrier characterized by an Arrhenius relationship with respect to
temperature, (ii) quantum mechanical tunneling through the potential barrier, and (iii) diffusion of majority carriers in the depletion region. Electron tunneling can significantly dominate the overall conductance at low temperatures for heavily doped materials, due to the suppression of thermionic emission and a reduction in the depletion width. The diffusion component can be approximated by an n-type metal-semiconductor structure (ie. Schottky diode) under forward bias, where the current density is determined by both the electric field strength inside the depletion region and the concentration gradient. The Seager and Pike model is described by equation (4):

\[ \frac{G_0}{T} = \frac{qA_R}{k_b T} \int_0^\phi_{BO} \frac{2E_0}{E} \left[ \frac{1}{\sqrt{\phi_{BO} - E}} - \frac{1}{\sqrt{\phi_{BO} + E}} \ln \left( \frac{\sqrt{\phi_{BO} + E}}{\sqrt{\phi_{BO} - E}} \right) \right] \left( 1 + e^{\frac{(E+\xi)}{k_b T}} \right) dE \]

where \( G_0 \) is the zero-bias interface conductance (\( \Omega^{-1}\cdot\text{cm}^{-2} \)), \( A_R \) is the Richardson constant for GaAs, \( \phi_{BO} \) is the conduction band barrier height, \( \xi \) is the Fermi energy level relative to the conduction band edge, \( T \) is temperature, \( q \) is the charge of an electron, and \( k_b \) is Boltzmann constant. \( E_0 \) is a reference energy defined by equation (5) as:

\[ E_0 = \sqrt{\frac{\hbar^2 q^2 N_D}{4m_t \epsilon \epsilon_0}} \]

where \( N_D \) is the doping concentration, \( m_t \) is the electron tunneling effective mass for GaAs, \( \hbar \) is the reduced Planck constant, \( \epsilon_0 \) is the permittivity of free space, and \( \epsilon \) is the dielectric constant for GaAs.
of GaAs. In accordance with the fitting curves reported by Seager and Pike for experimental n-GaAs bi-crystals doped in the $10^{18}$ cm$^{-3}$ range, the $\phi_{BO}$ parameter is adjusted and the $A_R$ and $E_0$ parameters are scaled by individual pre-factors in order to obtain good correlation with the data.

2.4 Characterization

2.4.1 Atomic Force Microscopy (AFM)

Atomic force microscopy (AFM) is the primary tool for the high resolution evaluation of the sample’s surface topography and cleanliness. 40x40 $\mu$m$^2$ scan images are taken at evenly spaced regions across each wafer to measure the average surface roughness. In addition, AFM reveals the presence of any surface particle contamination to determine if additional surface cleaning is necessary before bonding. Small particulates located between adjacent surfaces form unbonded interface areas or voids$^7$, and can lead to unfavorable bonding results. A cantilever with a sharp tip is brought in close proximity to the specimen and a pre-defined area (typically 40x40 $\mu$m$^2$) is scanned. A laser is focused onto the top of the cantilever and the reflection is sensed by a position sensitive detector. As the tip travels across the surface, it interacts with the topographical features due to Van der Waals and electrostatic forces. The cantilever experiences a vertical deflection and this is registered by the change in the laser’s reflection angle$^{20}$. In most modern AFM systems, an additional feedback mechanism is included to maintain a constant force between the tip and surface as the scan is in progress. As a result, the tip-to-surface separation is adjusted accordingly to prevent the collision of the tip to the surface. The surface roughness is measured as the RMS deviation of the height from the average value and should be $< 10$ Å, as explained in Section 2.1.
2.4.2 Transmission Electron Microscopy (TEM)

Transmission electron microscopy (TEM) is required to observe the bonded interface morphology and the atomic arrangement within a very narrow (2-3 nm) region. This imaging tool consists of an electron gun that produces an electron beam of low angular and energy spread. The beam is accelerated down a vertical column and first encounters the condenser system, which consists of a series of condenser lenses and aperture. The lenses demagnify the electron beam and control its diameter as it is focused onto the specimen, while the aperture is located between the lenses and regulates the convergence angle of the beam. The condenser system therefore manipulates both the beam spot size and intensity. The electron beam transmitted through the very thin sample encounters the objective and intermediate lenses in succession, leading to the formation of either an enlarged image or diffraction pattern. Finally, the projector lens is needed to project the image or diffraction pattern onto a phosphor viewing screen, photographic film or digital charge-coupled device (CCD) camera. Overall system magnification is controlled by the combination of the individual magnifications of each lens and can achieve up to 1,000,000 times\(^{21}\).

The TEM image generally consists of contrasting dark and bright features that visually highlight subtle characteristics about the specimen under examination. One of the basic contrast mechanisms is mass-thickness contrast, where the energy and angular distribution of the primary electrons passing through the specimen are affected by both elastic and inelastic scattering. Thick or dense areas will scatter the electrons more, leading to dark features in the image. Thinner regions allow the majority of the electrons to pass through undeflected and result in brighter features. Typically, there is also an objective aperture positioned on the back focal
plane of the objective lens that prevents any electrons scattered greater than a certain angle from passing through to the detector. Therefore, both the objective aperture position and size, along with the electron beam accelerating voltage, and can be adjusted accordingly to improve image contrast.

When a crystalline material is being examined, diffraction contrast will also be present and contribute to the overall image contrast. The periodic nature of the atomic lattice leads to increased diffraction and intensity from elastic scattering at particular angles determined by the crystal orientation and structure. The diffraction pattern can also be recorded from this mechanism with its various peaks indexed to identify the $hkl$ miller indices and sample orientation. Examples of single crystal diffraction patterns for the face-centered cubic (FCC) crystal structure oriented along various zone axes are shown in Figure 5. The objective aperture can be used to allow either the undeflected beam at the origin or any of the multiple diffracted beams to form the image, thus controlling the amount of contrast due to electron diffraction.

![Figure 5. Single crystal diffraction pattern of FCC crystal structure for a) [001], b) [011], and c) [111] zone-axis orientations.](image-url)
In order to obtain atomic resolution of the bonded interface, high resolution TEM (HRTEM) is employed, where the sample is aligned to a major zone axis in order to obtain several reciprocal lattice points of similar intensity. A structure image is then formed by allowing several strongly diffracting beams to pass through the optical aperture and interfere with each other. The outcome of this interaction is a phase contrast mechanism, in which each diffracting beam contributes a pattern of light and dark lattice fringes to the image. These multiple fringes overlap to form a series of bright and dark spots corresponding to individual atoms arranged in a particular orientation that is dependent on the zone axis and substrate miscut direction.

In addition, some TEM imaging systems offer a scanning TEM (STEM) mode, where the magnetic coils inside the vertical column are constantly varying in order to raster the electron beam across the sample surface. As the beam travels across the specimen, the detector is collecting intensity information in synchronous and constructs an overall image. The detector is a ring-shaped detector that collects electrons from all radial directions that are scattered within a range determined by the detector width and camera length. For certain applications where one needs to distinguish between features of different atomic number, the high-Z contrast mode can be employed. The camera length is reduced such that the detector accepts electrons scattered through a much wider angle. The diffraction contrast is reduced in favor of atomic number contrast and this is known as a high-angle annular dark field (HAADF) image.
2.4.3 Bonded Interface Resistance

For each bonded n-GaAs/n-GaAs sample, the zero-bias resistance is calculated from the inverse slope of the I-V curve calculated at +/- 50 mV around zero voltage bias. The total resistance $R_{TOT}$ measured includes the bonded interface resistance $R_{INT}$, the equipment system resistance $R_{SYS}$, the metal contact resistance $R_{CON}$ and the intrinsic bulk semiconductor resistance $R_{SEMI}$, as illustrated in Figure 6.

![Figure 6. Diagram of bonded GaAs/GaAs sample showing all the resistance components.](image)

These individual resistances can be treated as separate components connected in series within an electrical circuit. In order to calculate the interface resistance, equation (6) is used:

$$R_{INT} = R_{TOT} - (2 \cdot R_{SEMI} + 2 \cdot R_{CON} + R_{SYS})$$

(6)

where $2 \cdot R_{SEMI} + 2 \cdot R_{CON} + R_{SYS}$ can be estimated from the I-V curve of a reference single on-axis (001) n-GaAs sample of similar doping concentration and subjected to the same metal contact
deposition and high temperature processing conditions as the bonded samples. The conductance data used to fit to the Seager and Pike theoretical model is attained from the inverse of the interface resistance $R_{\text{INT}}$. 
Chapter 3: Experiment

Epi-ready Si-doped 50 mm diameter n-type GaAs substrates with carrier concentration of approximately $3 \times 10^8$ cm$^{-3}$ from WaferTech LLC were used for all experiments.

3.1 Direct Wafer Bonding

Table 2 details the n-GaAs substrates used to evaluate the effect of offcut angle on the electrical conductance of direct-bonded III-V structures. Surface micro-roughness of all samples was measured using a Quesant Q-Scope 250 AFM to verify that RMS roughness was lower than 10 Å, with the average roughness across all substrates being approximately 5 Å. The wafers were cleaned by soaking in acetone and isopropyl alcohol for 3 min each and then rinsed in deionized water. Removal of the native oxide was initiated by etching the wafers in a 1:9 NH$_4$OH:H$_2$O solution for 5 min, followed by a 1:9 HCl:H$_2$O solution for the same amount of time, since there is still a native oxide at the bonded interface. The surface was passivated by soaking in a 20% aqueous (NH$_4$)$_2$S solution at room temperature for 5 min, then rinsed in deionized water and dried under N$_2$. The samples were oriented face-to-face and pressure manually applied at the center to allow the bonding front to propagate towards the periphery. Table 1 describes all the different bonding combinations that were constructed in this study. The bonded wafers were annealed at 400 °C for 2 hr with a ramp up/down rate of 3 °C/min in order to strengthen the bond. Transmission infrared (IR) images were taken after bonding and after annealing, as shown in Figure 10, in order to monitor the bonded areas and determine the presence of any interfacial voids. Subsequent annealing did not cause the existing voids to
significantly expand/contract or new voids to develop. Non-sulfur passivated versions were also prepared for comparison purposes, where low force bonding was initiated directly after the oxide etch step.

Table 2. Description of n-GaAs wafers used in bonding experiments.

<table>
<thead>
<tr>
<th>Orientation</th>
<th>Offcut Angle (°)</th>
<th>Miscut Direction</th>
</tr>
</thead>
<tbody>
<tr>
<td>(001)</td>
<td>0</td>
<td>On-axis</td>
</tr>
<tr>
<td>(001)</td>
<td>2</td>
<td>&lt;111&gt;A</td>
</tr>
<tr>
<td>(001)</td>
<td>4</td>
<td>&lt;111&gt;A</td>
</tr>
<tr>
<td>(001)</td>
<td>6</td>
<td>&lt;111&gt;A</td>
</tr>
</tbody>
</table>

The samples were prepared for electrical measurements by depositing metal contacts made of 2000 Å of AuGe, 400 Å of Ni, 1000 Å of Au on both sides of the bonded pairs by electron beam evaporation and alloyed at 400 °C for 2 min under N₂. Samples were diced into 2x2 mm² die using a DISCO 321 saw dicing machine and then subjected to rapid thermal processing (RTP) at 600 °C for 2 min, in accordance with previous journals that reported on improved conductance across bonded structures due to a reduction in amorphous interfacial regions. Reference samples were also fabricated by depositing the same front and back contacts on a single on-axis (001) n-GaAs wafer of similar carrier concentration and exposed to the same annealing conditions. The reference was used to eliminate the resistance added by the metal contacts, instrumentation and semiconductor material not associated with the bonded interface from the conductance calculations.


3.2 Current-Voltage Measurements

Current-voltage (I-V) measurements were performed with a Keithley 2400 digital sourcemeter under computer control and the zero-bias conductance was obtained from the slope at zero voltage bias. The resistance attributed solely to the bonded interface was calculated by subtracting the measured resistance from the 2x2 mm² reference on-axis n-GaAs sample, as explained in Section 2.3.2. A Linkam THM S600 thermal microprobe stage with liquid N₂ source was used to vary the chamber temperature and I-V curves were acquired at regular intervals between 90 K to 340 K. Graphs of zero-bias conductance divided by temperature were plotted against inverse temperature to fit the data to the Seager and Pike theoretical model¹⁹.

3.3 Source of Non-Ohmic Characteristics

Non-ohmic behavior was previously noticed in direct-bonded off-axis n-type GaAs/GaAs samples, regardless of RTP temperature. In order to identify the source of this non-ohmic conductance, a diamond scribe was used to electrically isolate a portion of the deposited metal contacts from the rest of the structure, as shown in Figure 7. The sample can essentially be divided into 3 components: metal contacts, bulk semiconductor and bonded interface. I-V measurements are taken across a variety of test points to compare the resistance across the various components.
3.4 Bonded Interface Morphology

Transmission electron microscope (TEM) samples were prepared by individually mounting 2x2 mm² die from each bonding combination to a disc grinder chuck using adhesive wax. The top portion of the bonded pair was mechanically thinned on SiC abrasive grit paper to less than 20 μm or until a portion of the top substrate started to de-bond, with the remaining thickness verified using a Dektak 6 surface profilometer. An example of the sample surface profile after de-bonding is shown in Figure 8. A FEI NOVA 600 Focused Ion Beam (FIB) system was used to extract a cross-section sample from the thinned surface and ion mill it to electron transparency. High resolution TEM (HRTEM) and scanning TEM (STEM) imaging were performed on a FEI TITAN S/TEM at an accelerating voltage of 300 kV. The camera length was shortened in STEM mode for better Z contrast and all samples were aligned to the [110] zone axis for HRTEM.
Figure 8. Example of measured profile across surface of bonded 2x2 mm$^2$ GaAs/GaAs sample after mechanical grinding.
Chapter 4: Results and Discussion

4.1 Source of Non-Ohmic Characteristics

Figure 9 shows I-V curves measured at various test points, as explained in Section 3.3, in order to compare the resistance across the various components of the bonded GaAs/GaAs sample after 600 °C RTP. The resistance of the metal-metal and metal-semiconductor-metal interfaces was found on average to be 0.8 Ω. However, the inclusion of the bonded interface resulted in a significant increase in resistance to 770 Ω at zero-bias conditions, as presented in Table 3. It was concluded that the non-ohmic behavior was attributed solely to the interface, with minimal contributions from the metal contacts and bulk semiconductor.

![Figure 9. Current vs voltage for various electrical test points of a direct-bonded GaAs/GaAs sample after RTP at 600 °C for 1 min.](image-url)
Table 3. Resistances across various components of a bonded GaAs/GaAs sample after RTP.

<table>
<thead>
<tr>
<th>Test Points</th>
<th>Components</th>
<th>Resistance (Ω)</th>
</tr>
</thead>
<tbody>
<tr>
<td>A-A’</td>
<td>Metal-metal</td>
<td>0.8</td>
</tr>
<tr>
<td>A-C, A-B</td>
<td>Metal-semiconductor-metal</td>
<td>0.9</td>
</tr>
<tr>
<td>C-D</td>
<td>Metal-semiconductor-interface-semiconductor-metal</td>
<td>770</td>
</tr>
</tbody>
</table>

4.2 Effect of Relative Surface Misorientation

As expected, the (NH₄)₂S-treated samples exhibited superior conductivity compared to the non-passivated structures, as depicted in the current density vs voltage (J-V) curves in Figure 11. Our observations indicated that sulfur passivation improves the electrical conductivity across the bonded interface and is consistent with previous studies on the benefits of using surface passivation techniques to reduce the potential barrier to conduction²⁴. Figure 10 illustrates the location of the 2x2 mm² bonded die with (NH₄)₂S passivation that were selected for electrical testing. IR and optical images were used to verify that all die chosen for this study are located away from non-bonded regions along the interface.

![Figure 10. Overlay of IR and optical images of bonded GaAs/GaAs quarter wafers with (NH₄)₂S passivation and diced into 2x2 mm² samples. Die highlighted in red were selected for I-V measurements.](image-url)
Comparing the J-V characteristics of sulfur-passivated specimen, the degree of substrate miscut had an adverse effect on conductivity, as the samples exhibited increasingly non-ohmic behavior for higher offcut angles, as shown in Figure 11(b). This trend can also be noticed within the non-passivated oxide-etched-only samples. The zero-bias interface resistance data at room temperature for surface passivated samples is presented in Table 4 and increased by two orders of magnitude (0.01 to 3.4 Ω·cm²) comparing on-axis to 12° relative misoriented samples.

![Figure 11](image)

**Figure 11.** Current density vs voltage for 2x2 mm² GaAs/GaAs structures after 2-min RTP at 600 °C with AuGe/Ni/Au contacts on front and back for various relative surface misorientations: (a) oxide etch only, and (b) additional (NH₄)₂S-passivation. (Note the difference in x-axis scale for the bias voltages.)

**Table 4.** Zero-bias interface resistance at room temperature for (NH₄)₂S passivated 2x2 mm² GaAs/GaAs structures after 2-min RTP at 600 °C.

<table>
<thead>
<tr>
<th>Substrate Offcut (°)</th>
<th>Relative Surface Misorientation (°)</th>
<th>Resistance (Ω·cm²)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0 (on-axis)</td>
<td>0</td>
<td>0.01</td>
</tr>
<tr>
<td>2</td>
<td>4</td>
<td>0.02</td>
</tr>
<tr>
<td>4</td>
<td>8</td>
<td>2.8</td>
</tr>
<tr>
<td>6</td>
<td>12</td>
<td>3.4</td>
</tr>
<tr>
<td>6</td>
<td>0</td>
<td>0.02</td>
</tr>
</tbody>
</table>
In order to investigate the precise effect that the wafer miscut angle had on electrical conductance, additional bonded samples were fabricated using 6° offcut n-GaAs substrates, aligned face-to-face to produce a zero-degree relative surface misorientation, as depicted in Figure 1(c), and subjected to the same thermal and sulfur passivation treatment. I-V characteristics were comparable to nominal on-axis samples, as shown in Figure 12, with the interface resistance calculated to be 0.02 Ω·cm². It is concluded that the out-of-plane relative surface misorientation of the tilted (001) planes has a major influence on the electrical conductivity across the interface of direct-bonded semiconductor structures.

Another significant observation from Figure 11(b) is the J-V curves were ohmic and conductive until the relative misorientation was greater than 4°. Above this upper limit, the electrical properties became significantly non-ohmic and the zero-bias interface resistance increased by two orders of magnitude. This behavior is consistent with data published by F. Kish et al.²⁵ that reported of a threshold value for the relative misorientation, below which resulted in low resistance ohmic conductance of wafer-bonded interfaces. For off-axis substrates used in the manufacturing of multijunction III-V solar cells by direct wafer bonding methods, these research findings are technologically significant in the establishment of process control margins for the out-of-plane relative misorientation of (001) planes across the bonded interface in order to obtain a high degree of electrical conductance from your solar device.
Figure 12. Current density vs voltage for 2x2 mm² GaAs/GaAs samples after 2-min RTP at 600 °C representing 0° and 12° relative surface misorientations using 6° offcut substrates.

4.3 Conduction Barrier Height

The zero-bias interface conductance with respect to temperature for each passivated sample was fitted to the Seager and Pike electron tunneling model (see Figure 13) in order to estimate the conduction barrier height of the double depletion region at the interface. At high temperatures, the conductance exhibits an approximately linear behavior with respect to inverse temperature. This can be characterized as an Arrhenius relationship, from which the slope is used to extract the activation energy of the conduction barrier, and is consistent with thermionic emission over the barrier being the primary electron transport mechanism across the bonded interface. At lower temperatures, the conductance deviates from the linear trend and becomes more independent of temperature, as all the curves saturate at 140 K. This observation is explained by the onset of electron tunneling through the barrier width and is reported to be the
dominant component of carrier transport across grain boundaries for highly doped semiconductors in the $10^{18}$ cm$^{-3}$ range.$^{19,26}$

Using the n-type Schottky diode under forward bias to approximate the diffusion transport mechanism across the double depletion region, the diffusion current can potentially make up a significant portion of the overall conduction, and is expressed as equation (7):

$$J_n = J_D \cdot \left[ e^{\frac{qV}{kT}} - 1 \right]$$

(7)

where $J_N$ is the diffusion current density, $J_D$ is the saturation current density, and $V$ is the voltage bias. $J_D$ is less dependent on temperature, when compared to the square power law current-temperature relationship in thermionic emission. As a result, the applied bias $V$ is the governing parameter in diffusion current$^{26}$. The Seager and Pike model derives the zero-bias conductance from the slope of the J-V curve within a narrow ±50 mV range about zero bias. Due to the relatively small voltages under evaluation, diffusion transport in the depletion region is not considered to be a significant factor in the overall electrical conduction across the bonded interface for these experiments.

A potential barrier height of 0.54 eV was obtained for on-axis (NH$_4$)$_2$S bonded pairs and matched fairly well with the 0.6 eV height reported by M. J. Jackson et. al. for similarly doped n-type GaAs/GaAs structures$^{24}$. As the relative surface misorientation angle is introduced, the barrier height increased accordingly. The 4° misorientation resulted in a height of 0.61 eV, while the most significant increase occurred for both 8° and 12° samples, each with a 1.0 eV barrier height. These results are consistent with our previous observations of the existence of a
misorientation threshold limit that leads to a substantial decrease in the conduction of charge carriers across the interface.

![Graph showing zero-bias conductance](image)

Figure 13. Zero-bias conductance of \((\text{NH}_4)_2\text{S}\)-passivated GaAs/GaAs structures vs inverse temperature after 2-min RTP at 600 °C for various relative surface misorientations.

4.4 HRTEM/STEM

STEM images with high Z contrast were taken of the bonded pairs to observe and compare the interface morphology across all the misoriented samples. F. F. Shi et al.\textsuperscript{27} described the direct correlation between the amount of well-fused crystalline regions to amorphous inclusions and the electrical conductivity of the bonded structure after high temperature processing. The conduction of charge carriers occurs through the crystalline regions, which formed along the previously entire amorphous layer due the kinetic processes of inter-atomic diffusion and surface tension reduction being initiated at high thermal treatments\textsuperscript{23}.
As presented in Figure 14, the amorphous inclusions are represented by the dark regions, with the areas in between corresponding to the crystalline material. The physical morphology is consistent across the different off-axis substrates, with the linear fraction of crystalline regions to the entire bonded interface estimated to be 65 ± 2%, as reported in Table 5. This suggests that the degree of misorientation does not have a significant effect on the level of interface recrystallization after high temperature RTP.

Figure 14. STEM images of interface morphology after 2-min RTP at 600 °C for various relative surface misorientations.
Table 5. Percentage of crystalline regions at the bonded interface for various relative surface misorientations.

<table>
<thead>
<tr>
<th>Bonded Sample</th>
<th>% Crystalline Region</th>
</tr>
</thead>
<tbody>
<tr>
<td>0° (on-axis)</td>
<td>63</td>
</tr>
<tr>
<td>4°</td>
<td>63</td>
</tr>
<tr>
<td>8°</td>
<td>68</td>
</tr>
<tr>
<td>12°</td>
<td>66</td>
</tr>
<tr>
<td>AVG</td>
<td>65</td>
</tr>
</tbody>
</table>

HRTEM images showed how the atoms are rearranged upon inter-atomic diffusion at high temperatures. Figures 15(a) and 16(a) provide an atomic view of the crystalline area for the 12° relative surface misorientation sample, in which the TITAN S/TEM was aligned to the [110] zone axis of the top and bottom substrates, respectively. The sample tilt and alignment with respect to both sides of the interface were performed due to the non-zero in-plane rotational misalignment as the quarter wafers were bonded together. The corresponding diffraction patterns are presented in Figures 15(b) and 16(b) to illustrate the {111} and {001} atomic planes in relation to the interface. As expected, the (001) plane is verified to be 6° offcut from the wafer surface. This can be characterized as a grain boundary with a twin defect at the (1 1 13) plane and a tilt angle of 12° about the common [110] axis, as explained in Section 2.2.3.

This analysis is repeated for the 8° relative surface misorientation sample to confirm the 4° tilt angle (see Figures 17 and 18), classified as a twin defect at the (1 1 20) plane and a tilt angle of 8° about the [110] direction. The in-plane rotational twist was measured by XRD to be 4°, which is significant enough to limit the atomic diffraction to only one side of the interface.
Figure 15. (a) HRTEM image of GaAs/GaAs interface with 12° relative surface misorientation for top portion aligned to [110] zone axis, and (b) corresponding diffraction pattern.

Figure 16. (a) HRTEM image of GaAs/GaAs interface with 12° relative surface misorientation for bottom portion aligned to [110] zone axis, and (b) corresponding diffraction pattern.
Figure 17. (a) HRTEM image of GaAs/GaAs interface with 8° relative surface misorientation for top portion aligned to [110] zone axis, and (b) corresponding diffraction pattern.

Figure 18. (a) HRTEM image of GaAs/GaAs interface with 8° relative surface misorientation for bottom portion aligned to [110] zone axis, and (b) corresponding diffraction pattern.
Figures 19 and 20 show the HRTEM images of the bonded die with the 12° relative surface misorientation at higher magnifications. Literature has reported the presence of a continuous amorphous oxide layer of 5-10 nm thickness at the interface for 400 °C-bonded GaAs/GaAs samples with HCl treatment. It is observed that certain regions of this amorphous layer develop into inclusions due to the diffusion of oxygen atoms into impurities and defects located at the interface, while the remaining areas recrystallize into the same zincblende lattice arrangement as the bulk semiconductor after the 600 °C RTP. As a result, the relationship between the offcut atomic planes and the substrate surface is preserved throughout the entire bonded structure.

Figure 19. (a) HRTEM image of GaAs/GaAs interface with 12° relative surface misorientation for top portion aligned to [110] zone axis, and (b) zoom view.
Figure 20. (a) HRTEM image of GaAs/GaAs interface with 12° relative surface misorientation for bottom portion aligned to [110] zone axis, and (b) zoom view.
Chapter 5: Conclusion and Future Work

Direct wafer-bonded n-GaAs/n-GaAs structures constructed from off-axis substrates with varying degrees of relative surface misorientation have been analyzed and compared with nominal on-axis wafers to determine the effect that the offcut angle had on the electrical conductance through the discontinuous interface. The samples exhibited increasingly non-ohmic behavior for greater relative surface misorientation angles, with the interface resistance increasing by two orders of magnitude to 3.4 Ω·cm² for the 12° misorientation sulfur-treated bonded pairs when compared to on-axis specimen. This progressively non-ohmic characteristic was noticed on both oxide-etched and (NH₄)₂S-passivated surfaces, even though sulfur-treated semiconductor surfaces possess improved electrical conductivity. A significant increase in resistance was measured for misorientation angles greater than the 4° limit, implying that bonded structures are able to endure small misorientations without significant performance degradation. In addition, zero-degree surface misorientation samples were fabricated using offcut substrates and demonstrated comparative resistance of 0.02 Ω·cm² to on-axis wafers. These findings establish that the out-of-plane relative surface misorientation is the key parameter to maintain when utilizing offcut wafers in the manufacture of direct-bonded tandem solar cells.

Fitting the non-linear zero-bias conductance with respect to inverse temperature to the Seager and Pike electron tunneling model revealed an increase in the potential barrier to conduction, due to the presence of charge trap states at the bonded interface. The 12° surface misoriented structures introduced as much as 0.4 eV increase in barrier height, corresponding to a more resistive interface. TEM characterization of the bonded interface after high temperature RTP revealed that the ratio of crystalline-to-amorphous regions was consistent across all
samples, eliminating the hypothesis of the misorientation angle having a kinetic effect on the interface morphology. High resolution imaging showed that atoms close to the interface redistributed into the same lattice arrangement as the offcut bulk semiconductor crystal after GaAs and impurity atomic inter-diffusion was initiated by high temperature treatment.

Future work on this research topic is still needed to better understand the effect of relative surface misorientation on the interface resistance. We have already proven that the offcut angle does not have a substantial impact on the interface morphology. Additional experiments and theoretical modeling are required in order to fully comprehend the quantum mechanical mechanisms behind the misorientation of tilted (001) planes and how this is linked to an increase in the potential barrier to conduction.

The effect of in-plane rotational misalignment between bonded miscut wafers on the electrical properties is another area of interest that should be examined. Previous publications have reported on this subject with on-axis substrates but the relative misorientation of off-axis atomic planes rotated away from each other adds another dimension of complexity that also needs to be precisely controlled within a manufacturing environment in order to produce high performance solar devices. Specialized direct bonding laboratory apparatus and procedures must be established to ensure that the degree of rotational twist can be accurately controlled to within 0.5° or better.

This thesis is based solely on the characteristics of bonded semiconductor n-GaAs/n-GaAs homostructures. A nature progression would be to manufacture direct-bonded heterostructures using different III-V materials to investigate the combined effects of sulfur passivation and offcut angle on electrical conductivity. This would align the research closer to
real world photovoltaic applications, as multijunction solar devices currently achieving world
record power conversion efficiencies typically consist of a multiple cell stacked structure
integrated using different semiconductor materials.
References


