All-optical logic gates based on vertical cavity semiconductor optical amplifiers

Author
Gauss, Veronica Andrea

Publication Date
2009

Peer reviewed|Thesis/dissertation
UNIVERSITY OF CALIFORNIA, SAN DIEGO

All-Optical Logic Gates based on Vertical Cavity Semiconductor Optical Amplifiers

A dissertation submitted in partial satisfaction of the requirements for the degree Doctor of Philosophy in

Electrical Engineering (Photonics)

by

Veronica Andrea Gauss

Committee in charge:

Professor Sadik Esener, Chair
Professor Andrew Kummel
Professor Yu-Hwa Lo
Professor Alex Orailoglu
Professor Charles Tu

2009
Copyright

Veronica Andrea Gauss, 2009

All rights reserved
The Dissertation of Veronica Andrea Gauss is approved, and it is acceptable in quality and form for publication on microfilm and electronically:

Chair

University of California, San Diego

2009
DEDICATION

To my family
# TABLE OF CONTENTS

Signature Page .................................................................................................................. iii

Dedication ......................................................................................................................... iv

Table of Contents ............................................................................................................... v

List of Tables and Figures .............................................................................................. viii

Acknowledgements .......................................................................................................... xii

Vita .................................................................................................................................. xiv

Publications ...................................................................................................................... xv

Abstract of the Dissertation ............................................................................................ xvi

1. INTRODUCTION ........................................................................................................ 1

   1.1 References .............................................................................................................. 7

2. ALL-OPTICAL FLIP-FLOP BASED ON VCSOAs ................................................... 10

   2.1 Introduction ............................................................................................................ 10

   2.2 Overview of SR Flip-Flops .................................................................................... 10

      2.2.1 Electrical SR flip-flops ................................................................................. 10

      2.2.2 All-Optical SR flip-flops .............................................................................. 15

   2.3 Properties of VCSOAs .......................................................................................... 22

   2.4 Background on VCSOA Inverters ......................................................................... 25

   2.5 VCSOA SR Flip-Flop ............................................................................................ 30

      2.5.1 Principles of operation .................................................................................. 30

      2.5.2 Experimental setup ....................................................................................... 34

      2.5.3 Results and discussion .................................................................................. 36
4.2 Review of Electrical and Optical Modulation of VCSELs ................................. 88
4.2.1 Significance of Relaxation Oscillation Frequency (ROF) .............................. 88
4.2.2 Design Considerations for Maximizing ROF in VCSELs ................................. 91
4.2.3 Maximizing ROF through Optical Injection .................................................... 94
4.2.4 VCSOA Inverter Modulation Bandwidth ......................................................... 96
4.3 Experimental setup ............................................................................................ 99
4.4 Modeling and simulation..................................................................................... 101
4.5 Results and discussion ...................................................................................... 103
4.6 Conclusion ......................................................................................................... 109
4.7 References ........................................................................................................ 112
5. CONCLUSION ...................................................................................................... 114
5.1 Summary ........................................................................................................... 115
5.2 Future Directions ............................................................................................... 117
5.3 References ........................................................................................................ 119
LIST OF TABLES AND FIGURES

Tables:

Table 2.2.1: Truth Table for NOR-Gate SR Flip-Flop ........................................................... 13
Table 2.5.1: Truth Table for VCSOA SR Flip-Flop ............................................................... 31
Table 2.5.2: VCSOA SR Flip-Flop Parameters ............................................................... 36
Table 3.2.1: XOR Truth Table ......................................................................................... 48
Table 3.2.2: Truth Table for Half-Adder ................................................................. 49
Table 3.2.3: NAND Truth Table ...................................................................................... 51
Table 3.3.1: VCSOA XOR Truth Table ........................................................................... 61
Table 3.3.2: VCSOA XOR Parameters ............................................................................ 64
Table 3.3.3: VCSOA XOR Truth Table for CW Optical Bias ......................................... 70
Table 3.4.1: VCSOA NAND Truth Table ........................................................................ 73
Table 3.4.2: VCSOA NAND Truth Table for CW Optical Bias ...................................... 81
Table 4.3.1: VCSOA Inverter Experimental Operating Conditions for Large and Small Signal Analysis ........................................................................................................ 101
Table 4.4.1: List of Parameters Used in Modeling VCSOA Inverter ......................... 102
Table 4.4.2: VCSOA Inverter Operating Conditions for Modeling of Large Signal Response ........................................................................................................ 103
Figures:

Figure. 1.1.1: Ratio of Optical to Electrical Performance versus Signaling Rate of Short-Haul Data Links ................................................................................................................ 3

Figure. 1.1.2: Schematic of a Generic VCSEL with Ion Implantation ....................... 4

Figure. 2.2.1: Latch (a) CMOS Implementation. (b) Logic Diagram. ...................... 11

Figure. 2.2.2: Voltage Transfer Curves for a CMOS Latch ..................................... 11

Figure. 2.2.3: SR Flip-Flop. (a) CMOS Implementation using NOR Gates. (b) Logic Diagram ........................................................................................................................... 12

Figure. 2.2.4: Noise Margins for a CMOS Inveter .................................................. 14

Figure. 2.2.5: Label Reading and Packet Routing with an All-Optical SR Flip-Flop .... 15

Figure. 2.2.6: All-Optical Flip-Flop Implementation with an SOA-MZI ..................... 16

Figure. 2.2.7: Multimode-Interference Bistable Laser Diode Implementation of an All-Optical Flip-Flop .............................................................................................................. 18

Figure. 2.2.8: SMRL Flip-Flop with Y-waveguide ..................................................... 19

Figure. 2.2.9: VCSEL Flip-flop using Polarization Bistability .................................... 21

Figure. 2.3.1: Nonlinear Gain Saturation with Increased Input Optical Power .......... 23

Figure. 2.3.2: Power Bistability with Increased Input Detuning .............................. 24

Figure. 2.3.3: Polarization Anisotropy for 2 Bias Currents ....................................... 25

Figure. 2.4.1: Logic Diagram of the VCSOA Inverter ............................................... 25

Figure. 2.4.2: Typical Gain Window Separation for a VCSOA Inverter .................... 26

Figure. 2.4.3: Signal Transfer Characteristic ............................................................. 27

Figure. 2.4.4: Optical Bias Transfer Characteristic with Signal Input ...................... 28

Figure. 2.4.5: VCSOA Inverter. (a) Dual-Wavelength Operation. (b) Single-Wavelength Operation. ................................................................................................................ 29

Figure. 2.5.1: Logic Diagram for VCSOA SR Flip-Flop ............................................ 30
Figure. 3.3.4: VCSOA XOR Experimental Results. (a) Oscilloscope Data. (b) Conversion to Optical Power. ................................................................. 65

Figure. 3.3.5: Inverter Transfer Characteristics as a Function of Increasing Optical Bias (Circles = 2uW, Squares = 3uW, Triangles = 7uW). ................................................................. 66

Figure. 3.3.6: VCSOA XOR with CW Optical Bias ............................................. 70

Figure. 3.3.7: High-Density Integration Scheme for XOR with CW Bias ............. 71

Figure. 3.4.1: VCSOA NAND ............................................................................. 73

Figure. 3.4.2: Experimental Setup for NAND Operation ..................................... 74

Figure. 3.4.3: VCSOA NAND Experimental Results. (a) Oscilloscope Data. (b) Conversion to Optical Power. ................................................................. 76

Figure. 3.4.4: VCSOA NAND with CW Optical Bias ............................................. 81

Figure. 3.4.5: High-Density Integration Scheme for NAND with CW Bias ............. 83

Figure. 4.2.1: Example of Relaxation Oscillations in a Semiconductor Laser ........... 89

Figure. 4.2.2: Modulation Transfer Function with Relaxation Oscillation Frequency and 3dB Bandwidth ................................................................................. 91

Figure. 4.3.1: Experimental Setup for Measurement of VCSOA Rise and Fall Times and Modulation Bandwidth ................................................................. 99

Figure 4.5.1: Experimentally measured (solid line) and simulated (dashed line) inverter transfer characteristics. (a) Below threshold and (b) above threshold. ....................... 104

Figure. 4.5.2: Transient Measurements at 200Mhz. (a) Below Threshold (rise time = 670ps, fall time = 140ps). (b) Above Threshold (rise time = 350ps, fall time = 100ps). Time scale = 500ps/div. Voltage scale = 5mV/div. Experimental (rough line) and model (smooth line). Model of injected signal is also shown in red. ................................. 105

Figure. 4.5.3: Modulation Bandwidth. Below threshold (squares). Above threshold (triangles). Dashed line is 3dB bandwidth. ........................................................................... 107
ACKNOWLEDGEMENTS

The work in this dissertation could not have been completed without the guidance and support of many individuals in both my professional and private life. Primarily, I would like to thank my advisor, Professor Sadik Esener, for giving me the opportunity to be involved in the exciting area of VCSEL research. Under his mentorship, I was able to explore new ideas but still remain focused and productive. I have learned a great deal from him, and I very much appreciate his patience and encouragement throughout my graduate studies.

In addition, I would like to thank the present and former members of Professor Esener’s research group, including Haijiang Zhang, Doug Jorgesen, Sanja Zlatanovic, Matthias Gross, Mark Hsu, Deqiang Song, Catherine Noble, Pengyue Wen, Chris Marki, Slaven Moro, Marta Sartor, and Hod Finkelstein. They have contributed significantly to this dissertation with helpful discussions and advice on experiments, and I will be forever indebted to them for their kindness and support.

I would also like to thank certain present and former graduate students of the ECE department at UCSD, including Meredith Draa, Clint Novotny, Jessica Godin, and Sourobh Raychaudhuri. Their light-hearted humor and vigorous encouragement made a tremendous difference in keeping me sane and motivated, and their uncanny ability to save my experiments with exquisitely-timed equipment loans was invaluable!

I would also like to thank Antonio Hurtado and Professor Michael J. Adams at the University of Essex, Colchester, U.K. for their model of the VCSOA inverter, and for the many fruitful discussions which resulted from our collaboration.
I owe perhaps the greatest debt of gratitude to my family—my husband, Tom Marsilje III, my daughter Amelie, my parents, Dr. Arthur and Maria Gauss Jr., and sister, Carla-Maria Gauss-Arora, her husband, Professor Paramjit Arora, and their son Adais, for their incredible patience and support throughout my graduate school career. Without their love and encouragement, this work would never have been possible.

Lastly, I would like thank DARPA for their financial support of this work.

The contents of Chapter 2 are in part a reprint of the material in: Deqiang Song, Veronica Gauss, Haijiang Zhang, Matthias Gross, Pengyue Wen, and Sadik Esener, “All-optical flip-flop based on vertical cavity semiconductor optical amplifiers,” Optics Letters, 32, 2969-2971 (2007). The contents of Chapter 3 and 4 contain material which has been submitted to Optics Express, but has not yet been accepted. The material in Chapter 3 is from Veronica Gauss, Haijiang Zhang, Doug Jorgesen, Matthias Gross, and Sadik Esener, “All-Optical XOR and NAND gates based on Vertical Cavity Semiconductor Optical Amplifiers (VCSOAs),” to be submitted to Optics Express, 2009. The material in Chapter 4 is from Veronica Gauss, Antonio Hurtado, Doug Jorgesen, Michael J. Adams, and Sadik Esener, “Static and Dynamic Analysis of an All-Optical Inverter based on a Vertical Cavity Semiconductor Optical Amplifier (VCSOA),” to be submitted to Optics Express, 2009
# VITA

<table>
<thead>
<tr>
<th>Year</th>
<th>Experience and Education</th>
</tr>
</thead>
<tbody>
<tr>
<td>1995</td>
<td>B.S., Electrical Engineering, Virginia Polytechnic Inst. &amp; State Univ., Blacksburg, VA</td>
</tr>
<tr>
<td>1995-1996</td>
<td>Engineering Co-op, Jet Propulsion Laboratory-NASA, Pasadena, CA</td>
</tr>
<tr>
<td>1996-1997</td>
<td>Research Assistant, Department of Electrical and Computer Engineering, VPI&amp;SU, Blacksburg, VA</td>
</tr>
<tr>
<td>1997</td>
<td>M.S., Electrical Engineering (Robotics), VPI&amp;SU, Blacksburg, VA</td>
</tr>
<tr>
<td>1997-2000</td>
<td>Engineer, Electrical Board Design and Software, Computer Motion, Inc., Santa Barbara, CA</td>
</tr>
<tr>
<td>2000-2003</td>
<td>Engineer, Electrical Board Design, Sun Microsystems, Inc., San Diego, CA</td>
</tr>
<tr>
<td>2003-2004</td>
<td>Teaching Assistant, Department of Electrical and Computer Engineering, U.C. San Diego</td>
</tr>
<tr>
<td>2004-2008</td>
<td>Research Assistant, U.C. San Diego</td>
</tr>
<tr>
<td>2009</td>
<td>Ph.D., Electrical Engineering (Photonics), U.C. San Diego</td>
</tr>
</tbody>
</table>
PUBLICATIONS

**Journal Articles**

Veronica Gauss, Haijiang Zhang, Doug Jorgesen, Matthias Gross, and Sadik Esener, “All-Optical XOR and NAND gates based on Vertical Cavity Semiconductor Optical Amplifiers (VCSOAs),” to be submitted to Optics Express, 2009

Veronica Gauss, Antonio Hurtado, Doug Jorgesen, Michael J. Adams, and Sadik Esener, “Static and Dynamic Analysis of an All-Optical Inverter based on a Vertical Cavity Semiconductor Optical Amplifier (VCSOA),” to be submitted to Optics Express, 2009


**Conference Articles**


ABSTRACT OF THE DISSERTATION

All-Optical Logic Gates based on Vertical Cavity Semiconductor Optical Amplifiers

by

Veronica Andrea Gauss

Doctor of Philosophy in Electrical Engineering (Photonics)
University of California, San Diego, 2009
Professor Sadik Esener, Chair

This dissertation focuses on the three most significant logic elements which can be formed from Vertical Cavity Semiconductor Optical Amplifier (VCSOA) inverters for the purpose of all-optical communication systems. These logic elements are the Set-Reset (SR) flip-flop, XOR gate, and NAND gate, and together with the basic building block VCSOA inverter, they hold promise for performance improvement in all-optical signal processing. This dissertation investigates the theory and implementation of these gates, and also provides a study of the dynamic properties of the VCSOA inverter in an effort to understand the overall performance improvement that may be provided by VCSOA logic gates.

An all-optical Set-Reset (SR) flip-flop based on VCSOAs is demonstrated experimentally and theoretically. It is shown that the flip-flop can be constructed from 2
cross-coupled VCSOA inverters using the principles of cross-gain modulation, polarization anisotropy, and nonlinear gain to achieve flip-flop functionality. The flip-flop is also shown to be cascadable, have low switching power (~10µW), have the potential to be integrated on a small footprint (100µm²), and have the potential for single-wavelength operation.

An all-optical exclusive-OR (XOR) and Not-And (NAND) gate are demonstrated experimentally and theoretically. Based on a similar platform as the flip-flop, the XOR and NAND also demonstrate the same advantages in terms of cascadability, low switching power, and high-density integration. The demonstration of XOR and NAND functionality, however, proves the versatility of the VCSOA inverter platform, and the similarity to electrical inverters highlights a key advantage of VCSOAs for developing more complex circuits.

Finally, the dynamic behavior of the VCSOA inverter is studied experimentally and theoretically. The similarity between VCSOAs and VCSELs indicate that the response time of both are limited by the same factors, and thus may have the same possible solutions. Large signal analysis indicates a discrepancy in the speed of positive (rising edge) versus negative (falling edge) logic transitions which can be attributed to differences in the carrier recombination time that result from nonlinearity in the intensity-dependent gain. Small signal measurements indicate that the modulation bandwidth of the inverter approximates that of electrically modulated VCSELs, which supports the conclusion that carrier recombination time is the primary limiting factor.
1. INTRODUCTION

All-optical logic gates have been the subject of extensive research in recent years because of the myriad of potential applications in short-haul optical data communication networks and high performance computing (HPC)[1-12]. For example, in the late 1990's and early 2000's when the internet was experiencing explosive growth, optical solutions were increasingly in demand to improve performance of telecommunications network switches [13]. Switching of optical fibers was typically done by converting to electrical signals and then back into fiber, incurring a conversion delay. Many types of all-optical switches were developed to overcome this problem, but signal processing, when necessary, was still done electronically. Many types of all-optical flip-flops and exclusive-OR (XOR) gates were proposed for various signal processing tasks, including label reading, regeneration, header recognition, insertion, and extraction, and packet routing[14-18].

Recently, all-optical switching has found other applications, such as reconfigurable patch panels and optical switches for automated Fiber-to-the-Premises (FTTP) network testing[19]. Large-scale optical switching is still the benchmark of achievement in the industry, however, and researchers are making progress towards this as well. Recently, an innovative integrated optical switch and dense wavelength division multiplexing (DWDM) transport platform was unveiled at the 2005 Optical Fiber Communications Conference and Exposition (OFC). This platform supports 256 wavelengths, with each wavelength running at 10 Gbps (gigabits per second) for a total capacity of 2.5 Tbps (terabits per second)[19]. It outperforms current switching products on the market by almost an order of magnitude. While all-optical logic gates are not
currently a part of optical network switches, processing data exclusively in the optical domain is still a natural next-step to further improvements in performance. It only remains to be seen how quickly market forces propel product development in this area.

In addition to telecommunication network switches, all-optical logic may find applications in high-performance computing (HPC). The driving force appears to be 2-fold: (1) the presence of optics already in HPC environments, and (2) the performance limitations of copper traces. Optics are already well-established in Ethernet, which is the dominant form of data communication in HPC environments[20]. However, like telecommunications network switches, signal processing is still done electronically, which results once again in an O-E-O conversion delay. HPC environments cannot afford such limitations if they are to compete for increasingly high bandwidth applications such as high energy physics, climate forecasts, and genomics data and computation which could require aggregate bandwidths in excess of 100 Gbps [20].

One solution proposed for this problem is to replace electrical interconnects with optical interconnects. In current HPC environments, parallel interconnects longer than 50m with data rates of at least 2.5 Gbps are already handled exclusively with optics[20]. However, optical interconnects may also be preferable in short-haul data links- the so-called 'chip-to-chip' and 'rack-to-rack' interconnects which are less than 10m. Researchers at IBM have shown that when lane speeds exceed 10 Gbps for short-haul data links, power consumption, density, and cost considerations of optical interconnects become preferable to electrical interconnects (see Figure 1.1)[20].
In terms of power consumption, optics outperforms electronics as bitrate is increased because optics does not require equalization. Equalization is necessary in electronics to circumvent many sources of frequency-dependent loss, including dielectric loss, skin-effect losses, impedance discontinuities, and cross-talk[20]. Electronic interconnects are also inferior to optics in terms of cost since they must be redesigned as bitrate is increased. Finally, the increase in density of electrical traces as bitrate is increased has been known for some time to be a problem[20-21]. At higher data rates, electrical interconnects suffer from increased cross-talk, heat-dissipation issues, and RC delay as trace widths are reduced to meet density requirements[20-21]. The 2007 International Technology Roadmap for Semiconductors specifically lists optical interconnects among the technology solutions that will "be needed to overcome the delay, power, and bandwidth limitations of traditional interconnects" in order to meet the bandwidth
demands of the future[21]. As with telecommunications network switches, if O-E-O conversion delay can be removed in HPC through the introduction of all-optical logic gates, even greater performance should be expected.

As stated previously, for short reach and local area ethernet networks, optical technology is already dominant. In these networks, the transmitter of choice is the 850nm wavelength Vertical Cavity Surface-Emitting Laser (VCSEL)[20, 23]. Their small size, low electrical and optical power consumption, and ease of integration make VCSELs ideal for short distance high density applications. As shown in Figure 1.2,

![Figure 1.1.2: Schematic of a Generic VCSEL with Ion Implantation [22]](image)

VCSELs are layered semiconductor structures that form a Fabry-Perot cavity with a high optical gain light-emitting structure (i.e., quantum-wells) inside. Alternating high index and low index of refraction layers, with appropriate carrier doping, produces a pair of highly-reflective (>99.9%), low electrical resistance, Distributed Bragg Reflector (DBR) mirrors. Together, these mirrors form the Fabry-Perot cavity, with light emission normal to the substrate. The high mirror reflectivity results in a high-Q cavity with narrow
wavelength selectivity. A top and bottom contact provide a means of injecting carriers, and a confinement structure (ion implantation is shown in Figure 1.2) provides a means of directing the flow of carriers through the active region. VCSELs can be pumped both electrically and optically. The wavelength of the device is determined by the materials (for 850nm, GaAs/AlGaAs is commonly used) and the cavity length, which is determined by the thickness of the DBR layers and the active region.

In this dissertation, the focus is on all-optical logic gates which can be formed from Vertical Cavity Semiconductor Optical Amplifiers (VCSOAs). VCSOAs are simply VCSELs that are biased below threshold. Given the prevalence of VCSELs in today's ethernet market, VCSOAs have an advantage over other all-optical technologies in that industry is already familiar with many of their specifications through the use of VCSELs.

In Chapter 2, a Set-Reset (SR) flip-flop made from two cross-coupled VCSOA inverters is discussed. A brief review of SR flip-flops is provided to emphasize the merits and impetus for our design. The basic building block of all VCSOA optical logic-the VCSOA inverter- is reviewed in order to apply the concepts of optical nonlinearity, cross-gain modulation, and polarization gain anisotropy to the case of the VCSOA flip-flop. Experimental demonstration of a VCSOA flip-flop is shown, and the specifications for the flip-flop are outlined in terms of optical and electrical power requirements, operating wavelength, and wavelength detuning. It is shown that an SR flip-flop that is cascadable, has low optical switching power (~10µW), has the potential to be integrated on a small-footprint (~100µm²), and has the potential for single-wavelength operation, can be produced from 2 VCSOA inverters.
In Chapter 3, the VCSOAs logic family is expanded to include an exclusive-OR (XOR) gate and a Not-AND (NAND) gate. A brief review of XOR and NAND gates is provided to emphasize the merits and impetus for our designs. Experimental demonstration shows that both gates can be implemented in a platform very similar to the flip-flop, indicating the versatility of the platform to realize new logic gates. In addition, analysis of VCSOA logic diagrams shows that the VCSOA inverter forms complex logic in much the same way as electrical inverters. This similarity may allow VCSOA inverters to use the same circuit design principles as electronics. Similar to the flip-flop, specifications for both gates are determined for optical and electrical power, operating wavelength, and wavelength detuning. Single wavelength operation is demonstrated for the first time, as are novel designs for programmable logic elements, and the added advantages of cascadability, low optical switching power, and high-density integration are further emphasized.

In Chapter 4, the performance of VCSOA inverters is examined to assess the practicality of all-optical logic gates designed from VCSOA inverters. The results of large and small signal experiments are discussed and compared to simulation. The results indicate that the inverter modulation bandwidth is limited by the same carrier transport, parasitic capacitance, and heating issues which limit the modulation bandwidth of VCSELs. Although the modulation bandwidth measured for our inverter is a modest ~1.4Ghz, advances in VCSEL design have demonstrated that modulation bandwidth can be increased to meet the demands of the future[23-24].

Chapter 5 concludes the dissertation by summarizing the work and providing future directions.
1.1 References


5. V. Gauss, Electrical and Computer Engineering Department, University of California, San Diego, 9500 Gilman Dr., La Jolla, CA 92093, and H. Zhang, D. Jorgesen, M. Gross, and S. Esener are preparing a manuscript to be called “All-Optical XOR and NAND gates based on Vertical Cavity Semiconductor Optical Amplifiers (VCSOAs)”.


2. ALL-OPTICAL FLIP-FLOP BASED ON VCSOAs

2.1 Introduction

This chapter is an in-depth discussion of an all-optical Set-Reset (SR) Flip-Flop which can be created from VCSOAs. The chapter begins with a review of SR Flip-Flops to provide background and context for the discussion. The fundamentals of VCSOA inverters are then reviewed to explain the underlying physical mechanisms which result in Flip-Flop operation. The principles of operation of the VCSOA SR Flip-Flop are presented, followed by discussion of the experimental demonstration, and finally a summary of the conclusions.

2.2 Overview of SR Flip-Flops

2.2.1 Electrical SR Flip-Flops

In order to understand how the VCSOA SR flip-flop structure was developed, it is important to review the origins of the SR flip-flop, or SR latch, in electronics. The fundamental element for storing binary data in electronics is called a latch. The latch is implemented using two cross-coupled inverters made from complimentary metal-oxide semiconductor (CMOS) transistors. Figure 2.2.1 illustrates this design, and the associated logic diagram[1]. As can be easily observed by applying a binary logic 1 or 0 to the input of the latch (Vil), the output state of the latch (Vo2) is held by the cross-coupled inverters. A more detailed analysis can be obtained by plotting the inverse of the voltage transfer curve for inverter 2 with the voltage transfer curve of inverter 1.
As shown in Figure 2.2.2[1], two stable states are achieved when inverter 1 output high is the same as inverter 2 output low, and vice versa.

In addition, an unstable state occurs at the third intersection of the two voltage transfer curves. This state is unstable because any noise in the circuit will trigger the state to change one way or another. Thus, the latch is always in either the high or low state. A circuit element which exhibits this behavior is known as a bistable element. Bistable
elements are frequently referred to as flip-flops in the literature, and this terminology will be used in this dissertation from this point forward.

The problem with the flip-flop in Figure 2.2.1 is that flip-flop functionality cannot be realized in practice. There is no way to Set or Reset the state of the flip-flop since that would require Vi1 and Vo2 to have different voltages simultaneously, which would cause a short on one of the transistors. The simplest way to solve this problem is through the well-known SR (Set-Reset) flip-flop configuration. Figure 2.2.3 shows an SR flip-flop implementation using CMOS inverters as part of two cross-coupled NOR gates[1]. The corresponding truth table for this SR flip-flop is shown in Table 2.2.1.

![Figure 2.2.3: SR Flip-Flop. (a) CMOS Implementation using NOR Gates. (b) Logic Diagram. [1]](image)

The truth table is realized as follows: When the Set input (S) is low and Reset input (R) is high, the transistors M1 and M2 are both off, and the transistors M3 and M4 are both on. This means that the flip-flop inverted output (/Q) is pulled high and the flip-flop output (Q) is pulled low. This is the flip-flop Reset state. Conversely, when the Reset
input (R) is low and Set input (S) is high, the transistors M1 and M2 are both on, and the transistors M3 and M4 are both off. This means that the flip-flop inverted output (/Q) is pulled low and the flip-flop output (Q) is pulled high. This is the flip-flop Set state. When Set and Reset inputs are both low, M1 and M4 are both off, and M2 and M3 are either on or off depending on the previous state of Q and /Q. In this way, the previous state of the flip-flop is held indefinitely. This allows the Set and Reset lines to be released without losing the information stored in the flip-flop. The final case where Set and Reset are high is not allowed since it would result in Q and /Q both low, which violates the complementarity of the output states.

Table 2.2.1: Truth Table for NOR-Gate SR Flip-Flop

<table>
<thead>
<tr>
<th>Set Input (S)</th>
<th>Reset Input (R)</th>
<th>Q Output</th>
<th>/Q Output</th>
<th>State</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>x</td>
<td>x</td>
<td>HOLD</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>RESET</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>SET</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>-</td>
<td>-</td>
<td>NOT ALLOWED</td>
</tr>
</tbody>
</table>

The discussion of electrical SR flip-flops would not be complete, however, without mentioning the importance of noise margins. In electronics, noise margins are a commonly used figure of merit for CMOS inverters which give a measure of the cascadability and immunity to noise of the inverter. The larger and more positive the noise margins are, the better the performance of the inverter. Figure 2.2.4 illustrates a typical CMOS inverter transfer characteristic[24]. The transfer characteristic shows the transition from high to low output voltage levels as input voltage is increased.
Figure 2.2.4: Noise Margins for a CMOS Inverter [24]

The input voltages $V_{IL}$ and $V_{IH}$ mark the maximum low and minimum high voltages, respectively, that will generate a proper output logic high or low. $V_{IL}$ and $V_{IH}$ are themselves defined as the points on the transfer curve where the slope is -1. The region between $V_{IL}$ and $V_{IH}$ is the transition region and should be avoided for proper logic operation. A key feature of the transfer characteristic is the slope of the transition, which must be steeper than -1 in order to maintain positive noise margins. The noise margins are defined graphically in terms of the four voltage levels, $V_{IL}$ (Input Low Voltage), $V_{IH}$ (Input High Voltage), $V_{OL}$ (Output Low Voltage), and $V_{OH}$ (Output High Voltage):

$$NMH = V_{OH} - V_{IH}$$
$$NML = V_{IL} - V_{OL}$$

where $NMH$ and $NML$ are the noise margins for high and low logic levels, respectively. The noise margins are a measure of the amount of noise that can be tolerated by the system and still maintain correct logic operation. Thus for electrical, and optical, flip-flops, the inverter transfer curves should have a transition slope steeper than -1 in order to maintain correct logic operation.
2.2.2 All-Optical SR Flip-Flops

In telecommunications, all-optical SR flip-flops can be used for such applications as label reading and packet routing. Figure 2.2.5 illustrates an all-optical flip-flop implementation of this function [2].

\[ \text{Figure 2.2.5: Label Reading and Packet Routing with an All-Optical SR Flip-Flop[2]} \]

In this example[2], the header/label is extracted and compared to a look-up table containing reference addresses which assign a unique wavelength to the packet payload. In this way, the information can be routed through the network according to its wavelength. The flip-flops are all initially Set through an external optical pulse, so that each flip-flop outputs a unique wavelength \( \lambda_i \) provided by a second external source. The XOR correlators then perform the comparison of extracted header/label to reference
addresses. The result of the comparison is that the XOR correlators will Reset all flip-flops (i.e., prevent them from transmitting) except for the one flip-flop which corresponds to the address match. The wavelength of this flip-flop is then used in a wavelength converter to convert the packet payload wavelength to the new designated wavelength. Each XOR compares 1 bit of address information, and will either Reset its corresponding flip-flop by toggling the Reset line if the comparison is false, or do nothing if the comparison is true. In this way, the XORs can select a single designated wavelength to send to the wavelength converter.

All-optical flip-flops have been demonstrated using various technologies, including Semiconductor Optical Amplifiers (SOAs)[3-4], Multimode Interference Bistable Laser Diodes (MMI-BLDs)[5-7], ring resonators[8-11], photonic crystal and quantum dots[12], and Vertical Cavity Surface Emitting Lasers (VCSELs)[13-14]. An example of a flip-flop implementation using SOAs is shown in Figure 2.2.6[3].

![Figure 2.2.6: All-Optical Flip-Flop Implementation with an SOA-MZI][3]

In this implementation[3], a Mach-Zehnder Interferometer (MZI) architecture is used with one SOA in each arm. Flip-flop state changes are induced at the output (port #5) by
changing the phase experienced by the continuous-wave (CW) injected signal Pbias (port #1) as it travels through the two arms of the MZI. This change in phase selects between constructive and destructive interference at the flip-flop output, alternating the state from Set to Reset. The phase is changed by altering the carrier density of the SOAs using optically injected Reset and Set signals at ports #3 and #4, respectively. Altering the carrier density changes the gain and phase experienced by Pbias, changing the state of the MZI from balanced to unbalanced and causing the state of the flip-flop to change from Set to Reset. The feedback loop maintains the state change when no Set or Reset pulse is applied.

While all-optical flip-flops can be designed from SOA-MZIs, the large size of SOAs (2mm for the design in [3]) makes them unsuitable for practical applications. Larger aspect ratios translate to slower speed from increased capacitance and resistance, and difficulty with high-density integration. In addition, SOAs typically suffer from higher power consumption from the need to overcome poor carrier confinement with larger bias current. Optical amplifiers have been designed to have large bandwidths for broadband amplification; however, the larger bandwidth comes at the price of lower gain and poor carrier confinement.

Figure 2.2.7 shows a flip-flop implementation using a Multimode-Interference Bistable Laser Diode (MMI-BLD)[7]. In this case, an MMI coupler is designed as a cross-coupler for two optical lasing modes, and uses cross-gain saturation (XGS) between the modes to switch the state of the flip-flop. In the MMI-BLD, two-mode bistability occurs when the modes overlap completely and there is strong coupling between the modes. By itself, the MMI-BLD does not have strong enough coupling, and so saturable
absorbers (SAs) are typically used to increase coupling[15]. Initially, the MMI-BLD is switched ON by increasing the bias current appropriately, resulting in a lasing mode (Mode 1). In [7], single-mode operation is achieved by using distributed Bragg-reflector (DBR) structures which can be tuned by applying a bias current to the DBRs. If a weak Set pulse is applied at the wavelength of Mode 2, it is insufficient to saturate the absorption to Mode 2 but still able to saturate the absorption to Mode 1, so Mode 1 will lase.

![Multimode-Interference Bistable Laser Diode Implementation of an All-Optical Flip-Flop](image)

**Figure 2.2.7: Multimode-Interference Bistable Laser Diode Implementation of an All-Optical Flip-Flop[7]**

This realizes the Set function of the flip-flop. If a stronger Reset pulse is then applied at the wavelength of Mode 2, the absorption to Mode 2 becomes saturated, and Mode 2 begins to lase. At the same time, due to cross-gain saturation, Mode 1 is suppressed, resulting in the Reset function of the flip-flop. The flip-flop state is held by the SAs when no Set or Reset pulse is applied.

The flip-flop implementation in [7] has reasonably fast response times (~280ps rise time); however, there are still several issues with MMI-BLDs. As with the SOA-
MZI, they have high power consumption ($I_{bias} \sim 100\text{’s mA}$), and large overall dimensions ($\sim 2.5\text{mm}$) which could make high-density integration difficult. In addition, fabrication of MMI-BLDs is non-standard, indicating they would not be able to take advantage of existing semiconductor manufacturing processes. Finally, it is impossible to cascade MMI-BLD flip-flops [5-7] since XGS is by nature a lossy process and MMI-BLDs flip-flop outputs use 2 different wavelengths, although some progress has been made towards solving the wavelength problem[7].

Figure 2.2.8 illustrates a flip-flop implementation using ring resonators[11].

![SMRL Flip-Flop with Y-waveguide](image)

**Figure 2.2.8: SMRL Flip-Flop with Y-waveguide[11]**

In semiconductor micro-ring lasers (SMRLs), there are 2 modes- one in the clockwise direction (CW) and one in the counter-clockwise direction (CCW). These modes are degenerate and thus have the same frequency. Past flip-flop implementations have used cross-gain modulation between these modes to change the state of the flip-flop[8-9]. A
bus waveguide placed along-side the SMRL is used to input the Set and Reset signals. The inputs are launched into the waveguide from opposite directions so that one will excite the CW mode and suppress the CCW, and the other will excite the CCW mode and suppress the CW mode. The output power of one mode is monitored as the state of the flip-flop.

Traditional SMRL flip-flops suffer from several problems related to bus waveguide reflections, including periodic oscillations, chaotic behavior, and linear combinations of the CW and CCW modes[11]. The solution proposed by [11] is to find the new modes of the SMRL in the presence of bus waveguide reflections. The traditional SMRL flip-flop is then modified to include a new y-waveguide structure to take advantage of the new modes. These new modes occur when the CW and CCW modes combine in constructive and destructive interference at the output of the y-waveguide. They can be controlled using Set and Reset signals on opposite sides of the bus waveguide, as is done in traditional SMRL flip-flops. However, in the new case, the Set and Reset signals have different frequencies corresponding to the two new modes. Launching a Set or Reset pulse causes one or the other mode to be suppressed, resulting in either constructive or destructive interference of the CW and CCW modes at the output of the y-waveguide. The constructive and destructive interference is interpreted as the high and low states of the flip-flop, respectively.

In practice, SMRL flip-flops have been demonstrated to be fast (suitable for 10 Gbps operation) and have the small dimensions necessary for high-density integration[10]. However, in addition to the problem of bus waveguide reflections, SMRL flip-flops face a variety of challenges. They are difficult to fabricate, and like
MMI-BLDs, would not be able to utilize standard semiconductor manufacturing processes. In addition, they require high bias currents in order to overcome lossy waveguide coupling, and the output states use two different wavelengths, making implementation in circuits more challenging. Finally, due to their inherently lossy nature, ring lasers are not cascadable[8-10].

Figure 2.2.9 shows a flip-flop implementation using Vertical Cavity Surface-Emitting Lasers(VCSELs)[14]. In this implementation, the VCSEL has 2 lasing modes of 0º and 90º polarizations. Cross-gain-saturation (XGS) between the two modes results in bistable switching. When a Set pulse is applied at 0º, the lasing polarization is changed from 90º to 0º. Similarly when a Reset pulse is applied at 90º, the lasing polarization is changed from 0º to 90º. If the applied pulse has the same polarization as the lasing polarization, no change in state is observed. When no pulse is applied, the state is held because the VCSEL is injection locked. In this way, flip-flop operation is achieved.
The VCSEL flip-flop is a promising technology—especially since it takes advantage of semiconductor fabrication processes that are readily available. Flip-flop operation can be fast (~3Ghz), and power consumption low (tens of µW)[14]. This implementation, however, is intended for 1.55µm-wavelength operation where VCSEL technology is still immature. Gain tends to be lower in 1.55µm VCSELs, which results in logic devices which are either not cascadable[14] or only weakly so[16]. Lastly, the implementation in [14] results in an output with different wavelength and polarization than the input signaling which could make circuit design more complicated.

2.3 Properties of VCSOAs

Vertical Cavity Semiconductor Optical Amplifiers (VCSOAs) have several unique properties which lend themselves nicely to optical logic design. The first is nonlinear gain which results from the complex index of refraction of the active material[17]. This nonlinearity is intensity dependent, as shown in Figure 2.3.1. As input optical power is increased on the long-wavelength side of the cavity resonance, peak gain shifts to the long wavelength side, and gain saturates more quickly[17]. The slope of the gain curve on the long-wavelength side also becomes increasingly sharp. This optical nonlinearity is the result of a rapid shift in cavity resonance towards the input wavelength. When an optical input detuned to the long-wavelength side of the cavity is injected, there is a resulting carrier depletion which modifies the phase in the cavity and therefore the cavity resonance. The cavity resonance is pulled towards the input wavelength, which causes further amplification of the input optical injection, and thus
further pulling of the resonance towards the input wavelength[18]. This feedback effect results in the sharp optical nonlinearity of the gain characteristic on the long-wavelength side.

![Graph showing nonlinear gain saturation with increased input optical power.](image)

**Figure 2.3.1: Nonlinear Gain Saturation with Increased Input Optical Power [17]**

If input power is increased further, the optical nonlinearity becomes a hysteresis. This optical bistability is another manifestation of the effects of intensity-dependent index of refraction[19]. In general, bistability is defined as the case where 2 output states exist for the same range of inputs. Optical bistability in VCSOAs is observed in both wavelength and power, and both are related through the intensity-dependent nonlinear index of refraction[20]. In order to observe wavelength bistability curves, input power is held constant while input wavelength (i.e., detuning from cavity resonance) is swept. For power bistability, input detuning is held constant while input power is swept. Figure 2.3.2 illustrates an example of power bistability, with detuning defined in terms of phase. A sharp optical nonlinearity- whether bistable or not- is very useful for logic gates because it helps define the sharp transfer curve characteristics necessary for logic regeneration and positive noise margins.
The second property of VCSOAs which is useful in the construction of logic gates is polarization anisotropy. It has been known for some time that VCSELs experience a splitting of polarization degeneracy due to material birefringence, and that these polarizations are linear and orthogonal. This splitting is caused in large part by the electro-optic effect[21].

Figure 2.3.2: Power Bistability with Increased Input Detuning[18]

Polarization anisotropy can be observed in the gain characteristics of the VCSOA, where each polarization has its own gain curve (i.e., gain window). An example of this is illustrated in Figure 2.3.3 for 2 different bias currents (6.1mA and 6.4mA)[21]. The separation of the gain window peaks can vary between VCSOAs, and is a measure of the degree of birefringence in the device. For the VCSOAs discussed in this dissertation, the separation ranges from 8 to 40pm. The separation has been referred to as Intrinsic Polarization Peak Separation (IPPS)[22]. The size of the gain window separation is an important factor in determining how a VCSOA is used for a given logic application. The
most important aspect of polarization anisotropy, however, is that it provides a natural means for creating inverting logic. This idea is explained in detail in the next section.

![Figure 2.3.3: Polarization Anisotropy for 2 Bias Currents[21]](image)

### 2.4 Background on VCSOA Inverters

The VCSOA inverter is the basic building block of all VCSOA logic elements. As shown in the logic diagram of Figure 2.4.1, two optical inputs, called the Signal and the Optical Bias, are injected into the VCSOA, and two optical outputs are obtained: the amplified Signal and the inverted Signal imprinted on the Optical Bias. The Signal and Optical Bias are injected at the two linear orthogonal polarizations which are intrinsic to

<table>
<thead>
<tr>
<th>Input</th>
<th>Output</th>
</tr>
</thead>
<tbody>
<tr>
<td>Signal (\lambda_s, \text{S-Pol})</td>
<td>Amplified Signal (\lambda_s, \text{S-Pol})</td>
</tr>
<tr>
<td>Optical Bias (\lambda_p, \text{P-Pol})</td>
<td>Inverted Signal on Optical Bias (\lambda_p, \text{P-Pol})</td>
</tr>
</tbody>
</table>

![Figure 2.4.1: Logic Diagram of the VCSOA Inverter](image)
the device. These polarizations are labeled ‘S’ and ‘P’ in Figure 2.4.1. The designations ‘S’ and ‘P’ are defined as vertical and horizontal polarizations, respectively, in a Cartesian coordinate system of an optical table (i.e., vertical is perpendicular to the table and horizontal is in the plane of the table perpendicular to the direction of VCSOA emission). S and P polarizations can be mapped to the intrinsic VCSOA polarizations using a half-wave plate as a linear polarization rotator. In Figure 2.4.1, the Signal and Optical Bias are arbitrarily assigned the S- and P-polarizations, respectively.

The VCSOA is electrically pumped at 95-97% of threshold to provide appropriate gain for the two polarizations. Figure 2.4.2 illustrates a typical gain window separation for a VCSOA inverter[23].

![Figure 2.4.2: Typical Gain Window Separation for a VCSOA Inverter[23]](image)

The gain windows are measured separately for each polarization by injecting a probe beam with small optical power (~100nW) and measuring the output of the VCSOA. The gain windows are then plotted together to show the gain window separation (i.e., IPPS).
As discussed previously, the gain of the VCSOA has a sharp nonlinearity, or bistability, which is due to the intensity-dependent nonlinear index of refraction of the active region. This nonlinearity is critical in realizing the sharp transfer characteristic necessary for logic regeneration and positive noise margins (see Appendix A). If the Signal input wavelength is detuned to the long-wavelength side of its cavity resonance, the nonlinearity may be observed in the output optical power by sweeping the Signal input optical power. As detuning is increased, the observed nonlinearity in the power transfer curve becomes sharper. Figure 2.4.3 illustrates a typical power nonlinearity for a strongly detuned Signal[23].

![Figure 2.4.3: Signal Transfer Characteristic[23]](image)

When both the Optical Bias and Signal are injected in the cavity, cross-gain modulation occurs. The inverse of the Signal transfer characteristic can thus be imprinted on the output Optical Bias. If the Signal is strongly detuned, the Optical Bias transfer characteristic will have the same sharp nonlinearity as the Signal transfer characteristic. Figure 2.4.4 illustrates this effect[23].
Figure 2.4.4: Optical Bias Transfer Characteristic with Signal Input[23]

The VCSOA inverter can be operated in both a dual-wavelength and single-wavelength mode, as shown in Figure 2.4.5. As can be readily observed, the Signal and Optical Bias are detuned to different wavelengths in dual-wavelength mode, and the same wavelength in single-wavelength mode. In dual-wavelength mode, the S and P polarizations are arbitrarily assigned to the Signal and Optical Bias, respectively, and that configuration, which is shown in Figure 2.4.5, would work equally well if the polarization designations were reversed. One of the advantages of dual-wavelength mode is that the detuning can be adjusted independently for the Signal and Optical Bias. This allows the Signal detuning to be optimized for sharp nonlinearity in the transfer curve, while Optical Bias detuning can be adjusted to maximize the extinction ratio. The extinction ratio (ER) is defined as the ratio of the Optical Bias output high to output low power levels, and governs the cascadability of the inverter. In general, an extinction ratio of > 6dB is preferred since the extinction ratio must be able to compensate for losses in the optical circuit in order to properly drive the inputs to the next optical logic stage.
Extinction ratio can be optimized by increasing the Optical Bias input power and detuning to maximize the output high logic level, while simultaneously increasing the Signal input optical power and detuning to minimize the output low logic level. Typically this is realized when the Optical Bias has a smaller input power and detuning than the Signal.

For single-wavelength mode, assigning the S-polarization to the Signal beam is strategic because it means the Signal detuning will be greater than the Optical Bias detuning, realizing a sharp nonlinear inverter transfer curve. In this case, the balance
between a sharp transfer curve and a high extinction ratio is dependent on the IPPS of the VCSOA. Thus, careful consideration must be given to the selection of the VCSOA in this case. Single wavelength operation has the obvious advantage, however, that it reduces complexity and cost of circuits designed from VCSOA inverters.

2.5. VCSOA SR Flip-Flop

2.5.1 Principles of Operation

The structure of VCSOA SR flip-flops are very similar to electrical SR flip-flops in that they are both based on cross-coupled inverters. Figure 2.5.1 shows the logic diagram of the VCSOA SR flip-flop.

Unlike the electrical flip-flop, however, the VCSOA flip-flop does not need any additional circuitry beyond the cross-coupled inverters to realize flip-flop functionality. This is simply due to the difference in mechanism of action of electrical and optical circuits. In electronics, digital switching is performed between two voltage levels, and the mixing of these voltage levels at a node (i.e., a short) can have deleterious effects on circuitry. In photonics, the equivalent case would be mixing of two optical power levels
which has no adverse impact on optical circuits. In this way, the VCSOA inverter realizes a simpler implementation of the SR flip-flop than its electrical counterpart.

As discussed in Section 2.4, the designations S and P are assigned to the intrinsic orthogonal polarizations of the VCSOA. In Figure 2.5.1, the Signals (Set and Reset) for the 2 inverters have opposite polarizations and different wavelengths, as do the Optical Bias for each inverter. Two-wavelength operation is not required, however, and an alternative, single-wavelength, implementation will be discussed in section 2.5.4. Opposite polarizations for the Signals and Optical Bias of each inverter become necessary when a two-wavelength implementation is used, however.

The logic diagram of Figure 2.5.1 implements the truth table in Table 2.2.1 when the Optical Bias of both inverters is a continuous wave (CW) logic high. The Optical Bias is not expected to be modulated, and should be treated much the same as electrical bias (e.g., Vdd). The one significant difference is that cross-gain modulation (XGM) between the Signal and Optical Bias is what produces the output states of the flip-flop. This difference can be understood using Table 2.5.1, where the polarizations of each signal are included in the truth table.

**Table 2.5.1: Truth Table for VCSOA SR Flip-Flop**

<table>
<thead>
<tr>
<th>Set (P-Pol)</th>
<th>Reset (S-Pol)</th>
<th>Optical Bias (P-Pol)</th>
<th>Optical Bias (S-Pol)</th>
<th>/Q (S-Pol)</th>
<th>Q (P-Pol)</th>
<th>State</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>/Q</td>
<td>Q</td>
<td>Hold</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>Reset</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>Set</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>N/A</td>
<td>N/A</td>
<td>N/A</td>
<td>Invalid</td>
</tr>
</tbody>
</table>
The Set and Reset states of the flip-flop are obtained via XGM between the Signal and Optical Bias of each inverter. As discussed in Section 2.4, the output of each inverter is the inverted Signal imprinted on the Optical Bias. Thus the output of each inverter, Q and /Q, have the same wavelength and polarization as their Optical Bias. It should be noted that the last case, where Set=Reset=1, as in electronics, is also not allowed for the VCSOA flip-flop because it would set the flip-flop outputs to the same state, violating their complementarity.

The configuration of VCSOA inverters for an SR flip-flop involves several steps. First, two VCSOAs must be selected such that one (VCSOA1) has a much larger difference in Intrinsic Polarization Peak Separation (IPPS) than the other (VCSOA2). This enables the gain windows of VCSOA1 to be positioned in-between the gain windows of VCSOA2, as shown in Figure 2.5.2.

The relationship between the detuning of the two inverters must satisfy the following equation:

\[ IPPS_2 - IPPS_1 = \Delta P_1 - \Delta P_2 + \Delta S_2 - \Delta S_1 \]  

The gain windows of VCSOA1 can be moved relative to those of VCSOA2 by adjusting the temperature of either VCSOA’s laser diode mount. The purpose of this reconfiguring of the gain windows is to optimize the optical input power and wavelength detuning of the Signal and Optical Bias for each inverter, while at the same time ensuring that the Signal of one inverter matches the wavelength and polarization of the Optical Bias of the other inverter.
In this way, the two inverters can be cascaded. As stated previously, optimizing optical power and detuning is important in ensuring that an inverter has a transfer curve that exhibits high extinction ratio and sharp nonlinearity. Cascading inverters, as is done in the two-wavelength version of the flip-flop, has the added complexity of ensuring that the output of one inverter optimizes the transfer curve of the other. This involves ensuring that the output optical power of each inverter can compensate for loss in the feedback loop in order to match the input optical power requirements of the cascaded inverter.
2.5.2 Experimental Setup

Figure 2.5.3 shows the experimental setup for the VCSOA SR flip-flop (after [22]).
The VCSOAs that are used in this setup are commercially available Emcore 8085-1100 proton-implanted VCSELs with 20 \( \mu \)m apertures and 850nm wavelength emission. They are electrically pumped and biased at 95% of threshold, using a Keithley 236 Source Measure Unit current controller for each VCSOA. The temperature of each VCSOA is controlled by an ILX Lightwave LDT-5910B temperature controller. The Set and Reset signals and Optical Bias are generated by two New Focus 6316 tunable lasers, and the optical power and polarization of the beams is set by attenuators and polarizers along the beam paths. The detuning of the beams is set by tuning the New Focus lasers to \( \lambda_s = 841.564 \text{nm} \) and \( \lambda_p = 841.581\text{nm} \), and the wavelengths are monitored using a Hewlett-Packard 86120B wavelength meter. The Set and Reset signals are modulated by a chopper which is inserted across the optical paths of the two beams. The beams are combined with their corresponding Optical Bias using beam-splitters, and coupled into the appropriate VCSOAs using high quality numerical objectives. The VCSOAs are cascaded through a combination of regular beam splitters and polarization beam splitters (PBS). The PBS and optical isolators along the feedback paths ensure that only the Optical Bias output of each inverter is used as the input to its cascaded stage. Half-wave plates are used as linear polarization rotators in the feedback loop to correct for the 45 degree rotation caused by the isolators, and at the inputs to the VCSOAs to match the intrinsic orthogonal polarizations. Finally, the inputs and outputs of the flip-flop are extracted using appropriately aligned polarizers, and measured using two Newport 2832-C dual-channel optical power meters and a Tektronix TK11400 oscilloscope.

Table 2.5.2 lists the parameters used in the experiment.
Table 2.5.2: VCSOA SR Flip-Flop Parameters

<table>
<thead>
<tr>
<th>VCSOA</th>
<th>Temp (°C)</th>
<th>95% Ith (mA)</th>
<th>IPPS (pm)</th>
<th>ΔS (pm)</th>
<th>ΔP (pm)</th>
<th>Optical Bias Input Power (µW)</th>
<th>Signal Input Power (µW)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>24.4</td>
<td>6.268</td>
<td>6</td>
<td>14</td>
<td>25</td>
<td>7.3</td>
<td>13 (Set)</td>
</tr>
<tr>
<td>2</td>
<td>19.1</td>
<td>6.086</td>
<td>35</td>
<td>28</td>
<td>10</td>
<td>5.8</td>
<td>11 (Reset)</td>
</tr>
</tbody>
</table>

2.5.3 Results and Discussion

Figure 2.5.4 shows the transfer curves for the two VCSOA inverters used in the experiment. These transfer curves were obtained by sweeping the Set and Reset input optical powers, and measuring the corresponding Optical Bias outputs. The feedback path between the inverters was temporarily blocked in order to take the measurements, as otherwise the transfer curves were distorted.

Figure 2.5.4: VCSOA SR Flip-Flop Transfer Curves
As can be seen, the transfer curve for VCSOA1 is not optimized in comparison to VCSOA2. This discrepancy was caused by two factors: (1) the IPPS of the two devices which did not permit simultaneous optimization of both inverter transfer characteristics, and (2) alignment tolerances in the free-space optical setup which caused slight misalignment into VCSOA1. The second factor was easily eliminated by simple optimization of the alignment into the VCSOA. This was done by another student, and the improved transfer characteristics were subsequently published in [22]. However, the transfer curves in Figure 2.5.4 were sufficient to generate flip-flop operation since the modulation speed was limited by hand-modulation of the chopper.

As can be seen in Figure 2.5.4, the stable points of operation were A: $Pin(VCSOA1) = Pout(VCSOA2) = 13\mu W$ and $Pout(VCSOA1) = Pin(VCSOA2) = 2.5\mu W$, and B: $Pin(VCSOA1) = Pout(VCSOA2) = 2.5\mu W$ and $Pout(VCSOA1) = Pin(VCSOA2) = 11\mu W$. The extinction ratio was thus between 6 and 7dB. This extinction ratio, while sufficient for cascadability, leaves little margin for error in terms of the optical loss that could be sustained in actual optical circuit implementations. Higher quality transfer characteristics would almost certainly be needed for high speed applications, and these could be obtained in the single-wavelength flip-flop implementation which will be discussed shortly.

Figures 2.5.5 and 2.5.6 show the oscilloscope data for flip-flop operation. Figure 2.5.5 shows that when a Set pulse is applied, the flip-flop output $Q$ is set and $\overline{Q}$ is reset, and that when both Set and Reset are released, the state is held.
Figure 2.5.5: VCSOA SR Flip-Flop: Set and Hold

Figure 2.5.6 shows that when a Reset pulse is applied, the flip-flop output Q is reset and /Q is set, and that when both Set and Reset are released, the state is held.

Figure 2.5.6: VCSOA SR Flip-Flop: Reset and Hold
Both figures also show that when the same input is applied twice, no change in state is observed. The voltage on the y-scale of the figures reflects the voltage conversion of the power meters from optical power to voltage. The large overshoots are the result of improper setting of the optical power measurement range on the power meter. Referring to the truth table in Table 2.5.2, the data from these figures shows that correct flip-flop operation was achieved.

The discussion on the VCSOA SR Flip-Flop would not be complete, however, without one final note regarding integration. Figure 2.5.3 is obviously not usable in a high-speed application since it would be limited by the time of flight of the feedback path which is on the order of 3ns. Figure 2.5.7 shows a possible scheme for miniaturizing our design[22]. In this scheme, two transmissive VCSOA inverters are fabricated on transparent substrates, and aligned in the direction of emission. The Set and Reset signals and Optical Bias are applied from the back side of each substrate. A unidirectional polarization rotator (UPR) is used which is composed of a half-wave plate stacked on top of a Faraday rotator. The purpose of the UPR is to convert the output polarizations of each inverter to the input polarization needed by its cascaded inverter. It operates by rotating the polarization of an incoming beam by 90° if the incoming beam is injected into the Faraday rotator before passing to the half-wave plate. In the reverse direction, no polarization rotation is applied to the beam. The S-polarizer is used to ensure that only the proper inverter output reaches its cascaded inverter.

If the scheme in Figure 2.5.7 were implemented in practice, it is estimated based on current VCSEL dimensions that the flip-flop would occupy a footprint of ~100μm² and dissipate ~1mW of electrical power. Using these calculations, a 10kb all-optical
frame buffer dissipating 10W of power could be realized in 1cm²[22]. Further investigation would be necessary to determine the dimensions of the half-wave plate, Faraday rotator, and S-polarizer. In addition, some consideration would need to be given to determining how to control the output optical power of each inverter to match the input requirements of its cascaded gate.

Figure 2.5.7: High-Density Integration Scheme for VCSOA SR Flip-Flop[22]
2.5.4 Single-Wavelength Operation

Figure 2.5.8 shows the logic diagram for a VCSOA flip-flop operating in single-wavelength mode.

![Logic Diagram for Single-Wavelength Mode](image)

**Figure 2.5.8: Logic Diagram for Single-Wavelength Mode**

In this case, all inputs and outputs would have the same wavelength. The Set and Reset signals would have the same polarization, and the Optical Bias would have the same polarization. A Unidirectional Polarization Rotator (UPR), as described in section 2.5.3, would be used at the output of each inverter to convert the output polarization to the input polarization of the next stage. Figure 2.5.9 illustrates the single-wavelength implementation in terms of gain windows. Two identical VCSOAs would have two identical gain windows which could be positioned such that they overlap in wavelength. Optimizing the inverter optical power and detuning of either inverter would simultaneously optimize the other. The polarization of the inverted output of one VCSOA could be converted to match the input polarization of its cascaded stage using a UPR, and the optical power of the output could be attenuated to match the necessary
input optical power using a simple attenuator. In this way, two identical inverters could be used to create a single-wavelength flip-flop.

Figure 2.5.9: Positioning of Inverter Gain Windows for Single-Wavelength Operation

Figure 2.5.10 illustrates this new design in terms of the high-density integration idea discussed in section 2.5.3. The function of all components is the same. The notable difference between the two designs is simply that one UPR is flipped.

There are multiple benefits of single-wavelength operation. First, as discussed previously, optimization of the inverter transfer characteristics (TC) will be significantly less complicated since it will require that only one inverter TC is optimized, not both simultaneously. Second, the use of identical VCSOAs greatly simplifies the selection process. Finally, the inputs of each inverter and the outputs of each inverter will be the same polarization and the same wavelength, which would greatly simplify circuit design.
Figure 2.5.10: High-Density Integration Scheme for Single-Wavelength Operation
2.6 Conclusion

In this chapter, a novel cascadable all-optical Set-Reset flip-flop based on VCSOAs operated at 850nm wavelength was presented. The flip-flop was shown to realize the same truth table as electrical SR flip-flops, but have easier implementation due to inherent advantages in optical versus electrical signaling. Comparison of VCSOA SR flip-flops to other all-optical flip-flop technologies demonstrated the superiority of VCSOA flip-flops in terms of low electrical and optical power consumption, high-density integration, manufacturing, cascadability, and single-wavelength operation. The mechanism of action for flip-flop functionality was shown to have its origins in the physical processes employed by VCSOA inverters, namely cross-gain modulation, highly nonlinear gain characteristics, and polarization anisotropy. A simple method for alignment of the gain windows and determination of the optical input powers and detunings was specified. Experimental demonstration of the flip-flop showed that the inverter transfer characteristics have sharp transition regions, reasonable extinction ratios (∼6dB), and low switching powers. In addition, new designs were presented which showed potential for high-density integration and single-wavelength operation. This work clearly demonstrates the exciting potential of VCSOA flip-flops to realize real-world all-optical memories.

ACKNOWLEDGEMENT

2.7 References


3. ALL-OPTICAL XOR AND NAND GATES BASED ON VCSOAs

3.1 Introduction

This chapter continues the discussion of all-optical logic gates which can be created from VCSOAs. The chapter begins with a review of XOR and NAND gates to provide background and context for the discussion. The principles of operation of the VCSOA XOR and NAND gates are presented, followed by discussion of the experimental demonstrations, and finally a summary of the conclusions.

3.2 Overview of XOR and NAND Gates

3.2.1 Electrical XOR and NAND Gates

In electronics, exclusive-OR (XOR) and Not-AND (NAND) gates are used extensively for a variety of digital logic applications[1]. XOR gates implement exclusive disjunction, meaning that the output is a logic 1 only when both inputs are different. This is also modulo-2 addition, where addition is performed between binary numbers, and no numbers are carried or borrowed. Table 3.2.1 shows this function.

Table 3.2.1: XOR Truth Table

<table>
<thead>
<tr>
<th>Input A</th>
<th>Input B</th>
<th>Output (A XOR B)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
</tbody>
</table>

The symbol for an XOR gate is shown in Figure 3.2.1 with its associated logic function.
XOR gates are used in digital circuits to perform binary addition and subtraction in computers. One such digital circuit which is also important in optical logic circuits is the half-adder. Figure 3.2.2 shows an example of a half-adder implemented with an XOR gate and an AND gate. The half-adder takes the binary inputs A and B and performs modulo-2 addition with a carry and then places the results in the Sum (S) and carry (C) outputs. The associated truth table is shown in Table 3.2.2. The half-adder cannot sum large numbers since it does not have an input for a carry, and this is why it is called a half-adder. A full-adder is needed for addition of larger numbers.

<table>
<thead>
<tr>
<th>Input A</th>
<th>Input B</th>
<th>Output C</th>
<th>Output S</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
</tbody>
</table>

Figure 3.2.1: XOR Logic Symbol[1]
Figure 3.2.2: Half-Adder Implemented with XOR and AND Gates[2]
XOR gates can be implemented with CMOS transistors as shown in Figure 3.2.3(a) and (b)[1]. As can be readily observed by applying binary inputs to inputs A and B, these schematics realize the XOR function in Table 3.2.1. Figure 3.2.3(a) is the simplest realization of the XOR gate, and requires that the electrical bias is modulated as an input signal A or B. In contrast, Figure 3.2.3(b) depicts a real-world implementation of the XOR in which the electrical bias is a constant DC voltage.

Figure 3.2.3: CMOS Implementations of an XOR Gate. (a) Modulated Electrical Bias[16]. (b) Constant DC Electrical Bias[1].

Figure 3.2.3(b) is obviously a more complicated realization of the XOR functionality than Figure 3.2.3(a), and the added complexity is the direct result of the need to maintain a DC electrical bias. This problem will also be observed in the VCSOA XOR, but from the perspective of using a continuous-wave (CW) optical bias.
Not-AND (NAND) gates implement the inverse of the AND function, meaning that the output is only a logic low when both inputs are at a logic high. Table 3.2.3 shows the truth table for this logic gate. A unique feature of the NAND gate is that it has functional completeness, meaning that any gate can be made from a combination of NAND gates. NAND gates are also the most compact of all the digital logic gates, and so more cost-effective to use in digital circuit design. These qualities make the NAND gate the basic building block of digital logic.

Table 3.2.3: NAND Truth Table

<table>
<thead>
<tr>
<th>Input A</th>
<th>Input B</th>
<th>Output (A NAND B)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
</tbody>
</table>

The symbol for the NAND gate is shown in Figure 3.2.3 along with its associated logic function.

![NAND Logic Symbol][1]

NAND gates can be implemented from CMOS transistors as shown in Figure 3.2.5. As can be readily observed by applying binary inputs to inputs A and B, this schematic realizes the NAND function in Table 3.2.3. Unlike the XOR, the NAND CMOS implementation is already in its simplest form and cannot be simplified further by using a modulated electrical bias. This is not the case for VCSOA NAND gates, as will be shown in section 3.4.
3.2.2 All-Optical XOR and NAND Gates

All-optical logic gates have attracted significant attention in recent years because of their potential applications in packet switching[3], error detection[4-7] and differential phase-shift keying (DPSK) modulation[8-9]. In particular, the development of all-optical XOR gates is critical for realizing the complex optical circuits necessary for these applications. As discussed previously, the NAND gate is capable of forming all other digital logic gates, including the XOR, and thus is inherently important as the fundamental building block for optical, as well as electrical, digital logic. All-optical XOR and NAND gates have been proposed using a variety of technologies including semiconductor optical amplifiers integrated with Mach-Zehnder interferometers (SOA-MZIs)[3, 7], semiconductor ring lasers (SRLs)[10, 13], periodically-poled lithium niobate
(PPLN) waveguides[4, 6, 8, 12, 14], highly nonlinear fiber (HNLF)[9], and vertical cavity semiconductor gates (VCSGs)[11] and VCSOAs[15].

Figure 3.2.6 shows an error detection scheme implemented with an XOR using two SOAs in each arm of an MZI[7].

![Figure 3.2.6: XOR Gate implementation with SOA-MZI[7]](image)

The error-detection scheme is based on convolutional code which is commonly used to achieve reliable data transfer. The convolutional code employed in this case involves comparing an information bit-string with a check symbol to determine whether the data has been corrupted during a transfer. XOR operations are used to generate the check symbol at the transmitter and to compare the check symbol to the information bit string at the receiver.

The XOR is implemented using an SOA-MZI structure. As discussed in Chapter 2, SOAs are used to change the phase in each arm of an MZI, resulting in constructive or destructive interference at the output. In this case, if both inputs A and B are the same, there is destructive interference (or a logic 0) at the output. Similarly, if the inputs are
different, there is constructive interference (or a logic 1) at the output. In this way, the truth table of the XOR is realized.

As discussed in Chapter 2, SOA-MZIs have several problems. First, the larger size of SOAs necessitates higher bias current in order to overcome poor carrier confinement and achieve proper gain[3,7]. This translates into higher overall power consumption. In addition, large size usually results in slower speed[3]; however, in [7], a push-pull geometric system of 3dB couplers, variable optical attenuators (VOA), and optical delay lines compensates for the slow carrier recover time. This new system allows the SOA-MZI XOR to operate at very high data rates (40 Gbps) and reasonable extinction ratios ~9dB[7]. In addition, the SOA-MZI design in [7] can be cascaded, as is shown in experiment. However, cascading SOA-MZI XORs is not practical since they inherently require the inputs to have different wavelengths in order to achieve constructive/destructive interference at the output. This requirement necessitates that alternate XOR stages must have their own tunable laser source[7], which is simply not a practical solution. Finally, there is some question as to the feasibility of scaling SOA-MZIs for high-density integration. These designs tend to be larger (dimensions in millimeters) which is not be suitable for on-chip integration[3,7].

Figure 3.2.7 shows an XOR implementation using two SRLs[10]. As discussed in Chapter 2, the operational principle of SRLs is injection locking to one of two modes (clock-wise (CW) or counter clock-wise (CCW)) using an external optical injection while monitoring the output state of one of the modes. In [10], the authors deviate from the operational principle to include the effects of four-wave mixing (FWM). Two SRLs, SRL1 and SRL2, are initially set to lase in the CW direction. A Tunable Filter (TF) is
placed at the output of SRL1 to select only the wavelength of input A. Similarly, a TF is placed at the output of SRL2 to select only the wavelength of input B. If no input is applied, the lasing wavelength of the SRLs is filtered by the TFs, and the output is a logic 0.

Figure 3.2.7: Semiconductor Ring Laser (SRL) implementation of an XOR[10]

If input A is applied, both SRLs are injection locked to input A, and the TF of SRL1 allows this output to pass, resulting in a logic 1. Similarly, if input B is applied, both SRLs are injection locked to input B, and the TF of SRL2 allows this output to pass, resulting again in a logic 1. If both input A and B are applied, FWM occurs and both A and B are reduced since other SRL modes are excited and take energy from A and B. This is interpreted as a logic 0.

As discussed in Chapter 2, SRLs have many advantages, including fast response times and compact designs suitable for high-density integration. However, problems such as high coupling loss, high bias current, and back-reflections continue to limit the practical applications of SRLs[10, 13]. The XOR implementation in [10] exhibits further problems in that the use of FWM results in poor extinction ratio, difficulty in cascading
devices due to multiple output wavelengths, and the inconsistency of logic 0 levels when no input is applied versus both inputs applied.

Figure 3.2.8 shows a design for DPSK using a 3-input XOR implemented using PPLN waveguides[8].

Figure 3.2.8: XOR implementation of a DPSK System using PPLN Waveguides[8]

Three DPSK signals, A, B, and C, are created by passing the outputs of three tunable lasers through a system of Mach-Zehnder modulators with appropriate bit-pattern generators attached, and then bit-delaying the signals using two optical delay lines. After being amplified by a high-power EDFA, the signals are launched into the PPLN waveguide. A and B mix through sum-frequency generation (SFG), and produce a sum-frequency wave. The sum-frequency wave, as the name implies, has a frequency that is the sum of the frequencies of A and B. This wave is then mixed with input C, and through difference frequency generation (DFG), an idler wave is produced which has a frequency that is the difference of the frequencies of C and the sum-frequency wave. When the coupled mode equations for the cascaded SFG-DFG system are analyzed, the
phase relation shown in equation 3.1 between the idler wave and the 3 inputs A, B, and C becomes clear.

\[ \phi_i = \pi + \phi_A + \phi_B + \phi_C \]  

(3.1)[8]

If the periodicity of \(2\pi\) for optical phases is taken into consideration, and it is further understood that data in DPSK is carried in terms of binary phase (i.e., 0 and \(\pi\)), equation 3.1 shows that the phase of the idler wave is an XOR operation of the phases of A, B, and C. Thus, this system is capable of performing XOR operations on 3 DPSK signals.

XOR gates implemented using PPLN waveguides have the potential to be extremely fast—160 Gbps operation has been demonstrated in simulation[12]. However, they suffer from multiple problems. The first is that coupling to PPLN waveguides is extremely lossy, and so high-power optical preamplifiers must be used to compensate[4, 6, 8]. This results in overall high power consumption for the gate. In addition, due to their inherently lossy nature, PPLN XOR gates are not cascadable[4, 6, 8]. Finally, while there are certainly applications for 3-input XOR gates, the use of cascaded SFG-DFG restricts the use of these XOR gates to 3-input applications only.

Figure 3.2.9 shows a NAND implementation using a vertical cavity semiconductor gate (VCSG)[11]. The design in [11] is similar to VCSELs and VCSOAs in that it is formed from a vertical semiconductor Fabry-Perot cavity. However, VCSGs operate on the principle of absorption rather than amplification. Instead of a gain medium, these devices have a saturable absorber formed from quantum wells or quantum dots. The operational principle of the NAND, however, is very similar to that reported for NANDs designed from single VCSOAs[15].
In VCSGs, the Fabry-Perot resonator is constructed such that the typical saturable absorber nonlinear resonator reflectivity characteristic is inverted. This means that, rather than transition from low to high reflectivity with increased input energy, as is standard for nonlinear resonators with saturable absorbers, VCSGs exhibit a high to low transition in reflectivity with increased energy, as shown in Figure 3.2.9(b).

![Diagram of VCSG structure and reflectivity transfer curve](image)

**Figure 3.2.9: NAND Implementation. (a) VCSG Structure. (b) Reflectivity Transfer Curve for Increasing Input Power. [11]**

This inverted characteristic is achieved by designing an asymmetric resonator with a larger bottom mirror reflectivity than top mirror reflectivity.

The inverted reflectivity characteristic allows NAND functionality if 3 beams are used. The first- a probe beam ($P_{pb}$) - is injected at the resonance of the VCSG and with a power that is slightly below the transition power of the reflectivity characteristic in Figure 3.2.9(b). The probe beam will be monitored as the output of the NAND gate. A second and third beam- called pump beams ($P_{pmp}$) - are injected at a wavelength slightly detuned from resonance. The detuning must be selected carefully- too large and the sharpness of the transition in the reflectivity transfer curve degrades; too little, and undesirable effects from bistability are observed which can cause failure in the NAND gate.
functionality. The pump beams correspond to the inputs of the 2-input NAND gate. As shown in Figure 3.2.9(b), the power of each pump beam added to the probe by itself is not enough to cause a transition in the reflectivity characteristic; however, when both pump beams are applied together, a transition occurs, and output power is reduced. In this way, the NAND functionality is achieved—the probe output is a logic high unless both pump inputs are present.

VCSG and single-VCSOA NANDs have several attributes, including their potential for high speed (10 Gbps), low optical power consumption, and the fact that they are single-device solutions[11, 15]. In addition, these devices take advantage of well-understood semiconductor fabrication processes since they are based on VCSELs. VCSG and single-VCSOA NANDs face a variety of challenges however, including the requirement of 3-inputs for a 2-input device, inability to cascade since the maximum output optical power is less than the input power needed for switching, and poor extinction ratio.

3.3 VCSOA XOR

3.3.1 Principles of Operation

The structure of VCSOA XORs is very similar to electrical XORs in that they are both based on inverter architectures. Figure 3.3.1 shows the logic diagram of the VCSOA XOR. As can be seen from the figure, the VCSOA XOR is composed of 2 VCSOA inverters whose outputs are connected together. In this configuration, the Optical Bias is modulated similar to the electrical XOR illustrated in Figure 3.2.3(a) and, as in the electronics, is also the simplest implementation of the XOR using inverter
architecture. Since the bias is modulated, the inverter inputs are renamed “In” for Input Signal and “Ctrl” (Control) for the modulated Optical Bias.

In Figure 3.3.1, S and P polarizations have the same meanings as in Chapter 2, and S and P polarizers are understood to produce the polarizations of the inputs and outputs shown. The inverter Input signals are S-polarized, the Control signals are P-polarized, and the outputs are P-polarized. As in the VCSOA SR Flip-Flop, the VCSOAs can be identical, and therefore single-wavelength operation is assumed. It should be noted that the XOR gate inputs, Input A and Input B, are different than the inverter inputs (In and Ctrl). This is also the case in electronics, as shown in Figure 3.2.3(a).

The logic diagram of Figure 3.3.1 implements the truth table in Table 3.2.1 when the Input and Control lines of opposite inverters are modulated simultaneously. This is shown in Table 3.3.1 for the conditions when Sig1A and Sig2A are modulated simultaneously as gate input A, and Sig2B and Sig1B are modulated simultaneously as gate input B. As discussed in Chapter 2, the output of each inverter is the result of cross-gain modulation between the Input signal and the Optical Bias (or Control, in this case),
and thus the inverted Input is imprinted on the Control. Consequently, the output of each inverter, Out1 and Out2, has the same polarization as its Control.

Table 3.3.1: VCSOA XOR Truth Table

<table>
<thead>
<tr>
<th>Input A (In1) Sig1A (S-Pol)</th>
<th>Input B (In2) Sig2B (S-Pol)</th>
<th>Input B (Ctrl1) Sig1B (P-Pol)</th>
<th>Input A (Ctrl2) Sig2A (P-Pol)</th>
<th>Out1 (P-Pol)</th>
<th>Out2 (P-Pol)</th>
<th>Out (P-Pol)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

Since the VCSOAs are assumed to be identical, the inverter gain windows are positioned exactly as in the SR Flip-Flop for single-wavelength operation. This is illustrated in Figure 3.3.2 for the XOR case.

Figure 3.3.2: Positioning of the Inverter Gain Windows for XOR Operation
As in the flip-flop, IPPS corresponds to the intrinsic peak polarization separation of the gain windows, and $P_{\text{SIG}1A/1B/2A/2B}$ correspond to the input optical powers for the inverter inputs and controls, and $\Delta S1/ S2/ P1/ P2$ correspond to the wavelength detuning. $\lambda_{\text{op}}$ is the operating wavelength. Since the inverters are decoupled in this case, there is no need to convert the output polarization of one to the input polarization of the other as was done in the flip-flop. In addition, since the inverters are identical, optical power and detuning only need to be adjusted for a single inverter to optimize the transfer curve of both inverters simultaneously in terms of extinction ratio and nonlinearity.

### 3.3.2 Experimental Setup

Figure 3.3.3 shows the experimental setup for the VCSOA XOR (after[16]). The VCSOAs that are used in this setup are commercially available Emcore 8085-1100 proton-implanted VCSELs with 20 µm apertures and 850nm wavelength emission. They are electrically pumped and biased at 97% of threshold, using a Keithley 236 Source Measure Unit current controller for each VCSOA. The temperature of each VCSOA is controlled by an ILX Lightwave LDT-5910B temperature controller. The XOR gate inputs A and B are generated by two New Focus 6316 tunable lasers, and are modulated by choppers inserted across the optical paths of each beam. The detuning of the beams is set by tuning the New Focus lasers to $\lambda_s = \lambda_p = 841.561\text{nm}$, and the wavelengths are monitored using a Hewlett-Packard 86120B wavelength meter. The optical power and polarization of the VCSOA inverter Input and Control beams is set by attenuators and polarizers along the beam paths. The Input and Control beams are combined using beam-splitters, and coupled into the appropriate VCSOAs using high quality numerical
objectives. Finally, the inverter inputs and P-polarized outputs are extracted using a system of beam-splitters, mirrors, and appropriately aligned polarizers, and measured using a Newport 2832-C dual-channel optical power meter, a Newport 1830-C single-channel optical power meter, and a Tektronix TK11400 oscilloscope.

![Diagram](image-url)  

**Figure 3.3.3: Experimental Setup for XOR Operation (after [16])**
Referring to Figures 3.3.2 and 3.3.3, Table 3.3.2 lists the parameters used in the experiment. It should be noted that the VCSOAs that were actually implemented in the experiment were not identical since our experiment was limited to the use of commercially available VCSELs. However, as will be shown shortly, the IPPS of the two VCSOAs were close enough to achieve both single-wavelength operation and the output optical power requirements needed for cascadability.

**Table 3.3.2: VCSOA XOR Parameters (from [16])**

<table>
<thead>
<tr>
<th>VCSOA</th>
<th>Temp (°C)</th>
<th>97% Ith (mA)</th>
<th>IPPS (pm)</th>
<th>ΔS (pm)</th>
<th>ΔP (pm)</th>
<th>P_{Control} (µW)</th>
<th>P_{Input} (µW)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>24.8</td>
<td>6.204</td>
<td>8</td>
<td>10</td>
<td>2</td>
<td>1.4 (P_{Sig1B})</td>
<td>1.4 (P_{Sig1A})</td>
</tr>
<tr>
<td>2</td>
<td>23.6</td>
<td>6.178</td>
<td>16</td>
<td>25</td>
<td>9</td>
<td>8.3 (P_{Sig2A})</td>
<td>13.8 (P_{Sig2B})</td>
</tr>
</tbody>
</table>

**3.3.3 Results and Discussion**

Figure 3.3.4 (a) and (b) show the functionality of our VCSOA XOR. As can be seen in Figure 3.3.4, our VCSOA XOR implements the truth table in Table 3.3.1. The inverter inputs, Sig1A and Sig2B, were selected to illustrate the functionality because they were modulated as gate inputs A and B and were readily available in experiment (see Figure 3.3.3); however, Sig2A and Sig1B could just as easily have been used for the same reasons.

From Figure 3.3.4 it can be seen that there is an inconsistency in the logic low levels of the gate output Out. This is due to the fact that the Control lines of each inverter are modulated. If the Control lines were not modulated but instead held at a constant CW logic 1 (as in the flip-flop), there would only be a single mechanism for producing a logic 0- namely cross-gain modulation between the Control and a logic 1 Input signal.
Figure 3.3.4: VCSOA XOR Experimental Results. (a) Oscilloscope Data. (b) Conversion to Optical Power. [16]
When the Control lines are modulated, however, there is a second way for a logic 0 to be produced. If the Control line input is a logic 0, the VCSOA inverter will not have a transfer characteristic. This is best understood by reviewing the behavior of VCSOA inverter transfer characteristics as Control (or Optical Bias) is changed. When the Optical Bias power is reduced, the overall output power of the inverter is reduced because the Optical Bias gain at the operating wavelength is reduced. This is shown in Figure 3.3.5.

![Figure 3.3.5: Inverter Transfer Characteristics as a Function of Increasing Optical Bias (Circles = 2uW, Squares = 3uW, Triangles = 7uW).]

The Optical Bias power can be reduced to a point where no transfer curve exists. This occurs when the Optical Bias input power is so low that the gain characteristic is blue-shifted past the inverter operating wavelength. In this case, the Optical Bias gain is virtually extinguished, and thus there is no transfer curve. The output power of the
Optical Bias is virtually zero. The above discussion applies to modulators that do not have infinite contrast. In the experiment shown in Figure 3.3.3, modulation is performed using a chopper which results in an extreme case. With the Control input at a literal zero, there is nothing to amplify, and so the Control output (gate output) is a true zero. In contrast, when the Control input is at a logic 1, the only mechanism for producing a logic 0 is cross-gain modulation with a logic 1 Input signal. Cross-gain modulation will necessarily result in a higher logic 0 because the gain of the Control is not completely extinguished in this process. Thus, modulating the Control causes an inconsistency in the gate output logic 0.

One solution to the problem of inconsistent logic levels would be to increase the effectiveness of cross-gain modulation between the Control and the Input, such that the logic 0 produced through XGM would be closer to true logic 0. This could be accomplished by increasing the inverter Input signal power while keeping the Control power the same. In addition, if a VCSOA with larger IPPS were selected, the detuning for single-wavelength operation would be optimized for a minimized Control power and a maximized Input power. This would increase the effectiveness of cross-gain modulation by allowing the Input to extinguish the gain of the Control more thoroughly, and therefore produce a logic 0 closer to true logic 0.

In Figure 3.3.4, the output power levels of the XOR gate were Out (HIGH) = 18µW and Out (LOW) = 6µW. The extinction ratio is therefore less than 6dB, which is due to two factors: (1) the output logic 0 due to cross-gain modulation is not true 0, and (2) while the inverters never output a logic 1 at the same time, they do output a logic 0 at the same time, and these happen to be cross-gain modulation logic 0’s which add. Thus,
while each inverter has a respectable ~7.8dB extinction ratio, the overall gate is reduced
to less than 6dB. This problem could be addressed in several ways: (1) by selecting 2
identical VCSOA inverters which have better extinction ratios (e.g., the inverter in
Figure 3.3.5 has ER >11dB for the operating characteristic marked with circles), (2) by
minimizing the logic 0 from cross-gain modulation, as recently discussed, and (3)
increasing the bias current above threshold, which has the effect of increasing the overall
gain of the devices, and as a result, the overall extinction ratio. The last option, of course,
indicates that the VCSOAs would not be operating as amplifiers but as VCSELs.

While not ideal, the extinction ratio obtained indicates that this implementation of
the XOR could be cascaded with other similar logic gates. Since the output logic 1 of the
gate is greater than the Input switching power of either inverter (see Table 3.3.2), these
gates are technically cascadable. However, the losses from optical components such as
beam-splitters and polarizers in Fig. 3.3.3, incurred between the gate inputs (Input A and
B) and the VCSOA inverter Inputs, would need to be mitigated through the use of lower
loss components such as polarizing beam-splitters and half-wave plates. This could be
accomplished in a high-density structure such as the one shown in the next section.

Lastly, as can be observed from Figure 3.3.4, XOR functionality was
demonstrated at a very slow speed, on the order of Hz. This is not a measure of the
performance of the gate, but was simply due to speed limitations of the chopper which
had to be modulated manually. The actual speed of these gates exceeds 1Ghz, as will be
shown in Chapter 4.
3.3.4 Operation with Continuous Wave Optical Bias

In section 3.2.1, an implementation of the electrical XOR was shown which uses a DC voltage bias, rather than a modulated bias. Since the fundamental building block of electronic gates is the NAND gate which requires the use of a DC voltage bias, it follows that more complex electronic logic would also use this convention. This convention facilitates electronic circuit design by providing structure and uniformity to electronic logic gates. A similar convention can be applied to VCSOA optical logic by using a continuous wave (CW) optical bias. As with its electrical counterpart, the structure of a VCSOA XOR under this convention would be more complicated. Four VCSOA inverters are used in this case, which neatly parallels the design of the electronic XOR in Figure 3.2.3(b) which uses 8 transistors (or the equivalent number of transistors in 4 CMOS inverters). Figure 3.3.6 illustrates the VCSOA implementation. In this implementation, the VCSOA inverters are expected to be identical and have identical operating conditions (i.e., the same optical power and detuning requirements). They are also assumed to have S-polarized inputs and P-polarized outputs. The XOR logic inputs-Input A and Input B- are injected into the first two inverters (VCSOA Inv 1 and VCSOA Inv 2), along with the CW optical bias. The output of each inverter is passed through a P-polarizer, and then split into 2 paths by a beam-splitter. The P-polarization along one path is converted to S-polarization using a half-wave plate. This S-polarized output is then combined with the P-polarized output from the opposite inverter at VCSOA inverters 3 and 4. Finally, the P-polarized outputs of VCSOA Inv 3 and 4 are selected using P-polarizers at the XOR gate output.
Figure 3.3.6: VCSOA XOR with CW Optical Bias

Note that the P-polarized outputs of VCSOA Inv1 and Inv2 act as the Control for Inv3 and Inv4. Even though these Control lines are modulated, the XOR gate is considered to operate with a CW Optical Bias since the Optical Bias input to the gate (at Inv1 and Inv2) is separate from the logic inputs of the gate and is not modulated.

Table 3.3.3 shows the flow of the XOR truth table in terms of the gate inputs and outputs of each inverter, and the polarizations of each beam.

Table 3.3.3: VCSOA XOR Truth Table for CW Optical Bias

<table>
<thead>
<tr>
<th>InputA (S-Pol)</th>
<th>Input B (S-Pol)</th>
<th>Bias (P-Pol)</th>
<th>Out1 (P-Pol)</th>
<th>Out1 (S-Pol)</th>
<th>Out2 (P-Pol)</th>
<th>Out2 (S-Pol)</th>
<th>Out3 (P-Pol)</th>
<th>Out4 (P-Pol)</th>
<th>Out (P-Pol)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>
The primary advantage of using a continuous wave optical bias is that the XOR gate inputs are now the same as the inputs to VCSOA Inv1 and Inv2. This makes it possible to develop a design for high-density integration in which the gate inputs can be applied to separate substrates, as shown in Figure 3.3.7. This would not be the case for the design in Figure 3.3.1, where both inputs would have to be applied to both substrates.

In Figure 3.3.7, an array of transmissive VCSOA inverters are fabricated on transparent substrates, and aligned in the direction of emission. The gate Input signals and Optical Bias are applied from the back side of each substrate into VCSOA #1 and VCSOA #2, and the gate Output is obtained in the same manner through VCSOA #3 and VCSOA #4.
A system of polarizing beam-splitters (PBS), normal beam-splitters (NBS), half-wave plates, and absorbers realize the design in Figure 3.3.6. Redundant (and unbiased) VCSOAs complete the design to provide structure and symmetry. Interestingly, with a simple adjustment in output polarization, this design could be coupled with the VCSOA SR Flip-Flop in Figure 2.5.10 to create the label-reading and packet-routing circuit shown in Figure 2.2.5.

3.4 VCSOA NAND

3.4.1 Principles of Operation

Figure 3.4.1 shows the logic diagram of the VCSOA NAND. As can be seen from the figure, the VCSOA NAND is composed of 2 VCSOA inverters whose outputs are connected together. Inverter outputs cannot be connected together like this in electronics without causing a short, and so this scheme is not an option in electronics (see Figure 3.2.5). However, when implemented with VCSOAs, this scheme allows the use of a modulated Optical bias which can greatly simplify logic design.

In Figure 3.4.1, the Optical Bias is modulated for inverter 2. As with the VCSOA XOR, the inverter inputs are also named “In” for Input Signal and “Ctrl” (Control). The S and P polarizations have the same meanings as in Chapter 2, and S and P polarizers are understood to produce the polarizations of the inputs and outputs shown. The same I/O polarization convention is assumed for the NAND as the XOR: the inverter Input signals are S-polarized, the Control signals are P-polarized, and the outputs are P-polarized. As in the case of the XOR, the VCSOAs can be identical and therefore single-wavelength
operation is assumed. In addition, it should be noted that, as with the VCSOA XOR of Figure 3.3.1, the NAND gate inputs, Input A and Input B, are different than the inverter inputs (In and Ctrl).

![Logic Diagram](image_url)

**Figure 3.4.1: VCSOA NAND[16]**

The logic diagram of Figure 3.4.1 implements the truth table in Table 3.2.3 when the Input of Inverter 1 and Control line of Inverter 2 are modulated simultaneously, and the Input of Inverter 2 is modulated separately. This is shown in Table 3.4.1 for the conditions when Sig1A and Sig2A are modulated simultaneously as gate input A, and Sig2B is modulated separately as gate input B.

**Table 3.4.1: VCSOA NAND Truth Table**

<table>
<thead>
<tr>
<th>Input A</th>
<th>Input B</th>
<th>Bias</th>
<th>Input A</th>
<th>Out1</th>
<th>Out2</th>
<th>Out</th>
</tr>
</thead>
<tbody>
<tr>
<td>Sig1A</td>
<td>Sig2B</td>
<td></td>
<td>Sig2A</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>
As discussed in Chapter 2, the output of each inverter is the result of cross-gain modulation between the Input signal and the Optical Bias (or Control, in this case), and thus the inverted Input is imprinted on the Control. Consequently, the output of each inverter, Out1 and Out2, has the same polarization as its Control.

### 3.4.2 Experimental Setup

![Experimental Setup for NAND Operation](image)

Figure 3.4.2: Experimental Setup for NAND Operation (after [16])
As shown in Figure 3.4.2, the same experimental platform was used for the NAND as the XOR shown in Figure 3.3.3. The VCSOAs used in the NAND logic gate were identical to those used in the XOR, and therefore, the positioning of the gain windows and the operating conditions were the same as in Figure 3.3.2 and Table 3.3.2. The functional difference between the two experimental platforms was the placement of the chopper for gate Input B, which was moved to the output of the beam-splitter in order to obtain both a modulated input (Sig2B) into VCSOA 2 and a CW Optical Bias into VCSOA 1. Since the same experimental platform was used for both gates, all components and measurement equipment for the NAND were the same as those for the XOR and are outlined in section 3.3.2.

3.4.3 Results and Discussion

Figure 3.4.3 (a) and (b) show the functionality of our VCSOA NAND. As can be seen in Figure 3.4.3, our VCSOA NAND implements the truth table in Table 3.4.1. The inverter inputs, Sig1A and Sig2B, were selected to illustrate the functionality because they were modulated as gate inputs A and B and were readily available in experiment (see Figure 3.4.2).

From Figure 3.4.3 it can be seen that there is an inconsistency in the logic high levels of the gate output, Out. This is due to the discrepancy in the inverter logic low produced from XGM versus switching the Control line off. As explained in the XOR, the logic low produced from XGM cannot be true zero since the gain of the Control can never be completely extinguished in this process. By contrast, if the inverter is off because the Control line is off, the output is a true zero. In the case where Sig1A and
Figure 3.4.3: VCSOA NAND Experimental Results. (a) Oscilloscope Data. (b) Conversion to Optical Power. [16]
Sig2B are both logic low, Inverter 1 outputs a logic high since its Control has a constant CW optical bias input, but Inverter 2 outputs a true zero because its Control is off. However, when Sig1A is a logic high and Sig2B is a logic low, Inverter 1 outputs a logic low from XGM, and Inverter 2 outputs a logic high. Since the outputs of the two inverters are summed as the gate output, the case where Sig1A = 1, Sig2B = 0 results in a higher output logic high than the case when Sig1A = Sig2B = 0. This is not considered a serious issue, however since it has the same solutions as the logic low inconsistency observed in the XOR.

Of more serious concern, however, are the spikes that are observed in Figure 3.4.3 when Sig1A transitions between logic states and Sig2B is at logic 0. These are the result of modulating the Control line of the inverter, and thus have much more serious implications for the practical implementation of these gates. As shown in Figure 3.3.5, inverter transfer characteristics are obtained for fixed CW Optical Bias optical power levels. When the Optical Bias is modulated as a Control line, the idea of a single inverter transfer characteristic no longer applies. The transfer characteristic and optical power switching threshold of the inverter that is obtained by switching the Control line from off to on may be significantly different than that obtained by switching the Input Signal from on to off when the Control is a fixed CW optical bias. This problem is further complicated in our implementation of the NAND because the VCSOAs have different operating characteristics, which could lead to different response times and optical power switching thresholds regardless of whether the Control lines are modulated. The end result, however, is that mismatch in inverter transfer characteristics causes one inverter to
switch states before the other, resulting in the observed spikes at the transition edges of the gate output.

When the NAND is operated at higher speeds, it is expected that another problem may also contribute to the appearance of spikes at the transition edges of the gate output. This is the result of inconsistencies in the speed of transitions of the VCSOA inverter, operated with a CW optical bias, as the inverter switches between logic levels. The speed of the logic 0 to 1 transition is dependent on the gain recovery time of the Optical Bias which is governed by both electrical and optical pumping. Since the optical injection in the Optical Bias is weak, there is little benefit in terms of performance enhancement in comparison to electrical pumping alone. As will be shown in Chapter 4, the speed of electrical modulation is limited by carrier recombination time, and thus, the speed of the 0 to 1 transition is also expected to be limited in the same manner.

In contrast, the speed of the 1 to 0 transition is dependent on the feedback mechanism discussed in Section 2.3 that pulls the cavity resonance towards the wavelength of an input optical injection, thereby amplifying the input. As discussed in Section 2.3, this phenomenon is intensity dependent, and as intensity is increased, sharp nonlinearity is observed on the long-wavelength side of the gain characteristic. The Input optical power and detuning are set to take advantage of this nonlinearity, which translates to a sharp increase in photon density that can significantly reduce the carrier recombination time. This results in rapid amplification of the Input, and a corresponding rapid extinction of the Optical Bias through cross-gain modulation. Thus, the speed of the 1 to 0 transition is expected to be faster than the speed of the 0 to 1 transition. This
difference in transition rate between rising and falling transitions is expected to manifest as undershoots in the output of the NAND gate.

Several solutions can be presented for the problem of mismatched inverter logic transitions. The most obvious is to use identical VCSOAs to reduce the possibility of mismatched transfer characteristics between inverters. In addition, increasing the Optical Bias input power would help to increase the gain recovery time; however, this comes at the expense of extinction ratio since the larger the Optical Bias input power, the more difficult it is for the Input signal to pull the Optical Bias low through cross-gain modulation. A better solution might be to increase the bias current, which would then increase the overall gain of the device and thus gain recovery time of the Optical Bias. The disadvantage here is that higher electrical power consumption is required. A third option would be to use faster VCSELs since faster electrical modulation indicates faster modulation of the carrier density which results in faster gain recovery time. If the gain recovery of the device could be as fast as the nonlinear transition in the Input gain, then symmetric logic transitions might emerge. With the current VCSOAs, however, the best solution would be to use clocked operation in which the output of the gate would only be sampled at stable logic levels.

In Figure 3.4.3, the output power levels of the NAND gate were Out (HIGH) = 18µW and Out (LOW) = 6µW. As in the case of the VCSOA XOR, this extinction ratio is non-ideal, and has the same causes and solutions as outlined for the XOR in Section 3.3.3. Also as in the case of the XOR, the NAND gate may be considered cascadable since the output optical power of the gate exceeds the input switching power of each
inverter. The same caveats apply, however, regarding the need for low-loss optical components at the inputs to the inverters.

Lastly, as can be observed from Figure 3.4.3, NAND functionality was demonstrated at a very slow speed, on the order of Hz. As in the case of the XOR, this is not a measure of the performance of the gate, but was simply due to speed limitations of the chopper which had to be modulated manually. The actual speed of these gates exceeds 1Ghz, as will be shown in Chapter 4.

3.4.4 Operation with Continuous Wave Optical Bias

As discussed in Section 3.3.4, all electronic gates use a DC voltage bias, rather than a modulated bias. This convention facilitates electronic circuit design by providing structure and uniformity to electronic logic gates. Unlike electronic NAND gates, however, applying this convention to VCSOA NAND gates results in a more complicated structure. Three VCSOA inverters are used in this case, whereas only 4 transistors are used in the electrical NAND in Figure 3.2.5. The equivalent number of transistors in 3 electrical inverters would be 6. Figure 3.4.4 illustrates the VCSOA NAND implementation. In this implementation, the VCSOA inverters are expected to be identical and have identical operating conditions (i.e., the same optical power and detuning requirements). They are also assumed to have S-polarized inputs and P-polarized outputs. The NAND logic inputs- Input A and Input B- are injected into the first two inverters (VCSOA Inv 1 and VCSOA Inv 2), along with the CW optical bias. The output of each inverter is passed through a P-polarizer, but only Out2 is split into 2 paths by a beam-splitter. One half of Out2 is converted to S-polarization using a half-
wave plate. This S-polarized output is then combined with the P-polarized output, Out1, at VCSOA inverters 3. Finally, the P-polarized output of VCSOA Inv 3 is selected using a P-polarizer at its output, and then combined with the P-polarized output, Out2, at the NAND gate output.

Figure 3.4.4: VCSOA NAND with CW Optical Bias

Note that the P-polarized output of VCSOA Inv1 acts as the Control for Inv3. Even though this Control line is modulated, the NAND gate is considered to operate with a CW Optical Bias since the Optical Bias input to the gate (at Inv1 and Inv2) is separate from the logic inputs of the gate and is not modulated.

Table 3.4.2 shows the flow of the NAND truth table in terms of the gate inputs and outputs of each inverter, and the polarizations of each beam.

Table 3.4.2: VCSOA NAND Truth Table for CW Optical Bias

<table>
<thead>
<tr>
<th>Input A (S-Pol)</th>
<th>Input B (S-Pol)</th>
<th>Bias (P-Pol)</th>
<th>Out1 (P-Pol)</th>
<th>Out2 (P-Pol)</th>
<th>Out2 (S-Pol)</th>
<th>Out3 (P-Pol)</th>
<th>Out (P-Pol)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>
As with the VCSOA XOR, the primary advantage of using a continuous wave optical bias is that the NAND gate inputs are now the same as the inputs to VCSOA Inv1 and Inv2. This makes it possible to develop a design for high-density integration in which the gate inputs can be applied to separate substrates, as shown in Figure 3.4.5. This would not be the case for the design in Figure 3.4.1, where both inputs would have to be applied to both substrates.

In Figure 3.4.5, an array of transmissive VCSOA inverters are fabricated on transparent substrates, and aligned in the direction of emission. The gate Input signals and Optical Bias are applied from the back side of each substrate into VCSOA #1 and VCSOA #2, and the gate Output is obtained in the same manner through an unused VCSOA and VCSOA #3. A system of polarizing beam-splitters (PBS), normal beam-splitters (NBS), half-wave plates, and absorbers realize the design in Figure 3.4.4. Redundant (and unbiased) VCSOAs complete the design to provide structure and symmetry. Of key interest is that this is the exact same design as for the high-density VCSOA XOR in Figure 3.3.7, with the exception that VCSOA #4 is turned off. This means that this design could be an equivalent optical implementation of an electronic programmable logic element (PLE) by simply turning on/off VCSOAs as necessary to implement logic functions. One example of a circuit which could be made from this PLE is the half-adder circuit shown in Figure 3.2.2, with an additional inverter needed at the output of the NAND gate to form the AND function.
Figure 3.4.5: High-Density Integration Scheme for NAND with CW Bias
3.5 Conclusion

In this chapter, novel cascadable all-optical XOR and NAND gates based on VCSOAs operated at 850nm wavelength were presented. These gates were shown to realize the same truth tables as electrical XOR and NAND gates, and have similar degrees of complexity when implemented with a modulated bias. As with their electrical counterparts, the VCSOA XOR and NAND designs can be modified to make use of a DC (or CW) bias convention. These new designs are more complex, but allow the development of a common high-density integration platform which could result in a novel all-optical programmable logic element. Comparison of VCSOA logic gates to other all-optical gate technologies demonstrated the superiority of VCSOAs in terms of low electrical and optical power consumption, high-density integration, manufacturing, cascadability, and single-wavelength operation. The mechanism of action for the VCSOA gates was shown to be the same as for VCSOA SR Flip-Flops, namely cross-gain modulation, highly nonlinear gain characteristics, and polarization anisotropy. Single-wavelength operation was demonstrated for the first time by using VCSOAs with very similar properties, and this was shown to facilitate the alignment of the inverter gain windows and the selection of input optical powers and detunings.

Experimental demonstration also brought to light several serious issues, however, including inconsistencies in the timing of the inverter logic level transitions, and inconsistencies in the logic levels of the gates. The inconsistencies in the timing were attributed to mismatch in the inverter transfer characteristics resulting from different operating conditions and modulation of the Control. This results in unequal transition rates between VCSOA inverters which results in undershoots in certain NAND gate logic.
level transitions. Inconsistencies in the logic levels of the gates were found to be the result of the difference in logic 0 obtained through cross-gain modulation of the Optical Bias and Input signal versus simply switching the inverter on and off through modulation of the Optical Bias. Inconsistencies in logic levels caused lower extinction ratio and the appearance of 3 logic levels in the output for both gates. Both the transition and logic level inconsistencies may be improved by increasing the bias current above threshold and by using devices with closer operating characteristics. Increasing the bias current has the effect of increasing the overall gain, thus improving the gain recovery time of the Optical Bias and the extinction ratio of the inverter. Using devices with closer operating characteristics will also improve extinction ratio, and may help to better match the transfer characteristics of the inverters.

ACKNOWLEDGEMENT

The material in Chapter 3 is from Veronica Gauss, Haijiang Zhang, Doug Jorgesen, Matthias Gross, and Sadik Esener, “All-Optical XOR and NAND gates based on Vertical Cavity Semiconductor Optical Amplifiers (VCSOAs),” to be submitted to Optics Express, 2009.
3.6 References


   http://en.wikipedia.org/wiki/Adder_(electronics)


16. V. Gauss, Electrical and Computer Engineering Department, University of California, San Diego, 9500 Gilman Dr., La Jolla, CA 92093, and H. Zhang, D. Jorgesen, M. Gross, and S. Esener are preparing a manuscript to be called “All-Optical XOR and NAND gates based on Vertical Cavity Semiconductor Optical Amplifiers (VCSOAs)”.
4. DYNAMIC BEHAVIOR OF A VCSOA INVERTER

4.1 Introduction

In this chapter, large signal and small signal analysis of a VCSOA inverter are studied in order to understand the factors which may affect the speed of all-optical logic gates designed from VCSOA inverters. The chapter begins with a review of physical properties which limit the modulation bandwidth of VCSELs, and parallels are drawn to VCSOA inverters. A model is presented which calculates the large signal response based on the nonlinear interactions of the Input and Optical Bias inside the VCSOA. An experimental platform is presented for studying both large and small signal responses, and the results of the experiment are analyzed and compared to the model predictions. Finally, the factors which have the greatest impact on modulation speed are identified and assessed to understand how their effects can be mitigated in the development of high-speed VCSOA all-optical logic gates.

4.2 Review of Electrical and Optical Modulation of VCSELs

4.2.1 Significance of Relaxation Oscillation Frequency (ROF)

As stated previously, VCSOAs are VCSELs that are biased below threshold, but otherwise are structurally identical. This strong relationship between VCSOAs and VCSELs indicates that factors which limit the modulation bandwidth of VCSELs could also impact the modulation bandwidth of VCSOA inverters. The modulation bandwidth of VCSELs and semiconductor quantum-well lasers has been studied extensively, and it
is generally accepted that the frequency of relaxation oscillations plays a significant limiting role[1-11]. Relaxation oscillations are an intrinsic resonance that arise from energy exchange between photons and carriers in the laser cavity. They arise when the laser is first initialized and electrical pumping of the carrier density causes population inversion to overshoot threshold, causing a corresponding overshoot in the photon number. The overshoot in photon number then causes an undershoot in population inversion and the process repeats, oscillating the energy in the system back and forth between photons and carriers. At each repetition, the oscillation is damped because neither photon number nor population inversion drops all the way to zero. Thus, each oscillation begins from initial conditions which increasingly approximate steady-state behavior until the laser at last reaches steady-state operation. Figure 4.2.1 illustrates this process in a 1.3\(\mu\)m InGaAsP laser where \(N\) is carrier density and \(P_{0-3}\) are photon number of each mode under multimode operation[1].

![Figure 4.2.1: Example of Relaxation Oscillations in a Semiconductor Laser[1].](image-url)
A mathematical expression for the relaxation oscillation frequency (ROF) for VCSELs can be derived from small-signal analysis of the rate equations [4]:

\[
f_R = \frac{1}{2\pi} \left[ \eta_i \frac{\Gamma v_g}{qV} \frac{\delta g}{\delta N} (I - I_{th}) \right]^{1/2}
\]

(4.1)[4]

In equation 4.1, \( \eta_i \) is injection efficiency, \( \Gamma \) is confinement factor, \( v_g \) is group velocity, \( q \) is electron charge, \( V \) is the volume of the active region, \( \delta g/\delta N \) is the differential gain, \( I \) is bias current, and \( I_{th} \) is threshold current. Equation 4.1 can be used to give an approximation of the modulation bandwidth of the VCSEL, \( f_{3dB} \), for the case where damping is neglected[2, 4]:

\[
f_{3dB} = 1.55 f_R
\]

(4.2)[2, 4]

The modulation bandwidth is typically larger than the ROF for small damping since the ROF is measured close to the peak resonance, while modulation bandwidth is measured at the frequency where the response drops to half its DC value. This is shown in Figure 4.2 where \( \omega_p \) is the frequency of peak resonance, \( \omega_r \) is relaxation oscillation frequency, \( \omega_{3dB} \) is the modulation bandwidth, and \( \gamma \) is the damping factor[2]. As shown in Figure 4.2, as damping is increased, the modulation bandwidth approximates the ROF.

The relationship between the ROF and modulation bandwidth can be understood physically by considering the ROF as a limit on the speed at which energy can be exchanged between photons and carriers in the laser cavity. Thus, any electrical or optical modulation applied to the VCSEL can only modulate the carrier density on the order of the ROF which therefore limits the response time of the VCSEL by the same factor.
4.2.2 Design Considerations for Maximizing ROF in VCSELs

Since the frequency of relaxation oscillations is an intrinsic limit to the modulation bandwidth of VCSELs, many strategies have been devised to increase it. One method is to reduce the impact of nonlinearities inside the quantum-well active region of the VCSEL which adversely affect differential gain[4, 6]. Since ROF is proportional to differential gain (see equation 4.1), minimizing the affects of these nonlinearities can greatly enhance the performance of VCSELs. Nonlinearities which cause reduction in differential gain include spatial hole burning (SHB), carrier transport, carrier heating, and self-heating of the laser cavity[6].

SHB is the result of the standing-wave nature of the transverse optical modes inside the cavity. Transverse optical modes have different field distributions across the active region. As carriers are depleted at the peak of the standing wave of the
fundamental mode, the gain is decreased, allowing power to increase in higher order modes. SHB is only significant if the VCSEL is being used at very high output power, however, and therefore has less influence than other nonlinearities in the dynamic response of VCSELs[6].

Carrier transport issues refer to carrier dynamics between the quantum-well (QW) active region and the separate confinement heterostructure (SCH) layer. The SCH is composed of two semiconductor layers which sandwich the QW active region and help to confine carriers to the active region. Carrier transport issues involve carrier diffusion time across the SCH, and carrier capture and escape times in and out of the QWs[13]. These factors affect differential gain by controlling the interaction time of photons with carriers in the active region. Decreasing the diffusion and capture times means that carriers will reach the QWs faster. Increasing the escape time means that carriers will exist in the QWs longer, thereby increasing the interaction time with photons and the probability of stimulated emission. Carrier diffusion time is affected by the size of the SCH (i.e., the larger the SCH, the larger the diffusion time)[13]. Escape time is affected by carrier heating which adds energy to the carriers, increasing the probability that the carriers will escape the QW[13]. Carrier capture time is affected by the width of the quantum wells, which must meet or exceed the longitudinal optical (LO) phonon scattering limited carrier mean free path for the quantum well to efficiently capture carriers[14]. In order for a QW to capture a carrier, the carrier must be able to lose the energy difference between the barrier and the QW confined state. This is accomplished when the carrier scatters and emits a LO phonon which then relaxes its energy into a
lattice phonon[6]. Thus, the carrier mean free path must be less than or equal to the QW width in order to ensure that scattering with LO emission occurs within the well.

Another factor which can be considered a carrier transport issue is parasitic capacitance which, together with series resistance in the distributed Bragg reflector (DBR) mirrors, acts as a low pass filter for the flow of carriers into the active region. Parasitic capacitance can build up around pad electrodes and across the oxide aperture of index-guided VCSELs, and can be adjusted using novel planarization techniques and double-oxide apertures[7,8,12].

Heating also contributes to lower differential gain. Two types of heating can be identified in VCSELs- carrier heating and self-heating. Carrier heating results from various forms of carrier scattering and relaxation inside the QW active region which result in increase in carrier temperature. Increases in temperature reduce the differential gain by increasing the overall energy of carriers in the QWs and making it more difficult to confine them and more difficult for them to relax into the lowest energy subbands where they can participate in stimulated emission. P-doping the active region has been suggested as a possible method for reducing carrier heating as it has been shown to decrease the LO phonon relaxation time which increases differential gain[6].

Self-heating is due to the high thermal resistance of the distributed Bragg reflector (DBR) mirrors which prohibits dissipation of heat from the active region. As with carrier heating, the effect of self-heating is to compromise the ability of the active region to confine carriers and involve them in stimulated emission, thus reducing optical differential gain. Self-heating is considered more serious than carrier heating as it limits
the response time of VCSELs more severely[6]. Solutions for self-heating involve using modulation doping and graded interfaces to reduce DBR resistance[4, 12].

Lastly, differential gain may also be enhanced through the use of strained QWs[2, 12]. Under no strain, inversion is typically much smaller in the valence band than in the conduction band, which leads to the quasi-Fermi level for the valence band being higher than the valence band edge. Compressive strain increases the curvature of the valence band which decreases the effective mass, causing light and heavy hole bands to separate, and causing the quasi-Fermi level of the valence band to drop below the band edge. Both conduction band and valence band quasi-Fermi levels are then more symmetric about the band-gap, and inversion is increased in the lowest energy levels of the valence band. The differential gain will increase when both quasi-Fermi levels are as close to their respective band edges as possible, maximizing inversion[2].

4.2.3 Maximizing ROF through Optical Injection

Another method for improving differential gain, and therefore ROF, is to reduce the impact of carrier transport issues by using optical pumping[3, 5, 9-11]. Optical pumping at the energy of the absorption range of the active region produces photon-generating carriers directly in the active region of the VCSEL. This can greatly reduce the need for electrically pumped carriers, which reduces the effects of carrier transport, parasitic capacitance, and self-heating. Consequently, ROF, and therefore, modulation bandwidth, can be greater for optical modulation than for electrical modulation[3, 5].

Optical pumping cannot completely eliminate the effects of carrier transport issues, however, since the QW active region is still coupled to the SCH[3]. So other
methods of improving ROF through optical injection have been investigated. One such method which has been demonstrated to dramatically improve the ROF and modulation bandwidth is optical injection-locking (OIL)[9-11]. In OIL, a master laser is used to optically lock a follower laser (the VCSEL) which causes the VCSEL to lase at the same wavelength as the master. The VCSEL is then electrically modulated, and the ROF and modulation bandwidth of the VCSEL are measured as a function of injection ratio and detuning. Injection ratio is defined as the ratio of optical power incident on the VCSEL to the output power of the free-running VCSEL, and detuning is defined as the difference in wavelength between the master laser and the free-running VCSEL. The ROF and modulation bandwidth of injection-locked VCSELs have been observed to increase dramatically under high injection ratio (i.e., several times the ROF of the free-running VCSEL)[9-11]. This dramatic increase has been attributed to beating between the detuned optical injection frequency and the cavity resonance frequency which results in a new resonant frequency that is the difference of the injection and cavity resonance frequencies[9]. This new frequency is the modified ROF because it causes energy exchange between the intracavity field and carrier population at that frequency[9]. It should be noted that the detuning of the optical injection is significant in OIL because without it, constructive interference between the optical injection and cavity resonance would deplete the steady-state population to such a degree that relaxation oscillations would become overdamped[9].

While OIL is a very promising technique for improving the modulation bandwidth of VCSELs, it is not well-suited for optical logic. This is because OIL uses high injection ratios which makes OIL logic inherently not cascadable. Recently, our
group used a variant of OIL in a 1550nm wavelength VCSEL inverter logic gate[15]. In this case, the authors took advantage of the polarization anisotropy of VCSELs to injection lock the orthogonal polarization mode, rather than the lasing polarization mode. The injection-locked orthogonal polarization mode (OP) was used as the output of the inverter, and the lasing polarization (LP) was the input. When no light was injected at the LP (i.e., input was logic 0), the output of the inverter was the injection-locked OP which was considered a logic 1. When light was injected in the LP (i.e., input was logic 1), the OP mode was suppressed through gain competition between orthogonal and lasing modes, and the output of the inverter was a logic 0. This method avoids the high-injection ratio problem of OIL since the input optical power needed to injection-lock the OP mode is considerably less than for the LP mode. However, when the modulation bandwidth of the inverter is compared to the modulation bandwidth of the electrically modulated VCSEL as specified by manufacturer, it appears that the inverter does not perform better than the VCSEL. The reason this design does not benefit from ROF enhancement is not clear since the injection power into the OP mode is not specified, and neither is the detuning. It could be speculated that the injection power into the OP mode, or the detuning, is not sufficient to produce significant change in the ROF.

4.2.4 VCSOA Inverter Modulation Bandwidth

Relaxation oscillations, by definition, are a phenomenon of lasers operating above threshold. They describe the frequency of energy exchange between stimulated emission photons and the carrier population above threshold from turn-on until the laser reaches steady-state. This idea of energy exchange between carriers and photons applies below
threshold as well, however, when the VCSEL acts as an amplifier for coherent optical injection. This is the case for VCSOA inverters, and it follows, then, that the same methods for increasing the response time of VCSELs above threshold will also increase the response time of VCSOAs.

The speed of energy exchange between photons and carriers in the VCSOA inverter can be described in terms of photon relaxation time and carrier recombination time. Photon relaxation time (or photon lifetime) refers to the time it takes a photon to exit the cavity through mirror facets or be absorbed through stimulated emission processes. In this context, carrier recombination time refers to the time it takes a carrier to reach the active region and combine into stimulated emission. In previous chapters it has been stated that inverter transitions are the result of cross-gain modulation between the S-polarized Input signal and the P-polarized Optical Bias. This cross-gain modulation involves energy exchange between S-polarized and P-polarized photons through modulation of the carrier density. For a 0 to 1 transition, S-polarized photons must either exit the cavity by transmission through the mirror facets or relax into carriers. These carriers must then get pumped into gain for P-polarized stimulated emission. This process can be referred to as the gain recovery of the P-polarized Optical Bias, and the limiting factor is the recombination time of the carriers since photon relaxation time is shorter than carrier recombination time. Even though pumping of carriers is partly done by optical injection, carrier transport, parasitic capacitance, and self-heating issues will still be significant limitations on the response time of the inverter. There are 2 reasons for this: (1) the optical injection is weak, and thus the amount of carriers created in the active region is not large enough to dismiss the need for electrically injected carriers, and
(2) the coupling of the quantum-well active region to the separate confinement heterostructure (SCH) means that carriers generated by optical injection will continue to experience diffusion, capture, and escape, and these factors will contribute to an increase in the carrier recombination time[3]. Since carrier recombination time determines the gain recovery time of the Optical Bias, it also determines the response time of the inverter to the 0 to 1 transition. Thus, the speed of these transitions can be expected to approximate electrically-modulated VCSEL transitions.

The case for a 1 to 0 transition is more complex because it involves nonlinearity in the gain. In a 1 to 0 transition, P-polarized photons must either be transmitted from the cavity or relax into carriers, and these carriers must get pumped into S-polarized photons. The limiting factor is again carrier recombination time since photon relaxation time is much shorter. However, in this case, because the optical injection in the S-polarized mode is strong and the detuning is large, there is a sharp nonlinearity observed in the S-polarized gain. This leads to a rapid increase in S-polarized photons in the cavity as input power is increased due to the cavity resonance which exists at the detuning. This results in a corresponding rapid decrease in P-polarized photons, as the overabundance of S-polarized photons induces carriers to produce stimulated emission of S-polarized photons rather than P-polarized photons. The stimulated emission of P-polarized photons declines at the conversion rate of P-polarized photons to S-polarized photons, which is limited by the recombination time of carriers into S-polarized photons. The recombination time is faster than in the 0 to 1 transition, however, due to the rapid increase in S-polarized photon density from the sharp nonlinearity in the gain. The rapid increase of S-polarized photons means the probability of recombination is higher which
means the carrier recombination time is shorter. Thus, the speed of the inverter 1 to 0 transition is expected to be faster than the electrically modulated VCSEL. However, since the inverter 0 to 1 transition is the limiting factor, overall the modulation bandwidth of the inverter is expected to approximate that of the electrically modulated VCSEL.

4.3 Experimental Setup

In order to prove the conclusions in section 4.2.4 regarding the speed of the VCSOA inverter transitions versus the electrically-modulated VCSEL transitions, an experiment was conducted to determine the rise and fall times of the inverter and the modulation bandwidth. The experimental setup is shown in Figure 4.3.1.

Figure 4.3.1: Experimental Setup for Measurement of VCSOA Rise and Fall Times and Modulation Bandwidth[16]

A hybrid fiber/free-space design was used in order to interface the free-space VCSOA to a high-speed fiber-coupled modulator and measurement equipment. The VCSOA was an Emcore 8085-1100 proton-implanted VCSEL with 20 µm aperture and 850nm wavelength emission. It was electrically pumped and biased at 97% of threshold, using a
Keithley 236 Source Measure Unit current controller. The temperature of the VCSOA was controlled by an ILX Lightwave LDT-5910B temperature controller. Two New Focus 6316 tunable lasers were used for the Optical Bias and Input beams, and optical isolators were positioned at the output of each laser to eliminate back-reflections. The Input was fiber-coupled into a Photline/Keopsys NIR-MX800-LN-05 850nm 5Ghz modulator using a high-quality diode objective, and was modulated with either a sine wave, for small-signal modulation bandwidth measurements, or an NRZ PRBS pattern for rise/fall time measurements. For small-signal measurements, pattern generation was provided by an Agilent 8703A Lightwave Component Analyzer. For large signal measurements, an Anritsu MP1632A Data Analyzer was used with a Rhode & Schwartz SM1Q03B Signal Generator to provide the frequency for the Data Analyzer. The Input was then split using an 80/20 fiber coupler, and the smaller optical power was routed to an HP 86120B wavelength meter to monitor the Input wavelength detuning. The Optical Bias wavelength detuning was also monitored by the wavelength meter via a free-space 50/50 beam-splitter and fiber coupling. The Input was then coupled back into free-space and routed to the VCSOA. The intensity and polarization of both beams were controlled by variable attenuators and individual polarizers along each path as in [17]. The Input and Optical Bias optical power to the VCSOA were monitored using a Newport 2832-C Dual Channel power meter, and the output Optical Bias was monitored using an Electro-Optics Technology ET-4000AF fiber-coupled high-speed photodetector and either an Agilent Infinium DCA 86100A oscilloscope for large signal measurements or the Agilent 8703A Component Analyzer for small signal measurements.
Measurements were also taken above and below threshold to observe the impact of bias current. Table 4.3.1 lists the operating conditions for these two cases. The threshold current was 6.3mA at a temperature of 23.6°C.

Table 4.3.1: VCSOA Inverter Experimental Operating Conditions for Large and Small Signal Analysis [16]

<table>
<thead>
<tr>
<th>I_{BIAS} (mA)</th>
<th>Operating Wavelength (nm)</th>
<th>Δλ_{S} (pm)</th>
<th>Δλ_{P} (pm)</th>
<th>P_{Optical Bias} (µW)</th>
<th>P_{Input *} (µW)</th>
</tr>
</thead>
<tbody>
<tr>
<td>6.15</td>
<td>841.562</td>
<td>23</td>
<td>6</td>
<td>2</td>
<td>1 to 15</td>
</tr>
<tr>
<td>6.5</td>
<td>841.575</td>
<td>19</td>
<td>3</td>
<td>2</td>
<td>1 to 15</td>
</tr>
</tbody>
</table>

*For Large-Signal Analysis Only

4.4 Modeling and Simulation

In addition to experiment, a model was developed to predict the results of large signal analysis of the VCSOA inverter. The model was developed by Dr. Antonio Hurtado and Professor Michael J. Adams (both at the Department of Computing and Electronic Systems, University of Essex, Wivenhoe Park, CO4 3SQ Colchester, U.K) to simulate the large signal experimental results obtained by this author at UCSD. Details of the model will be published elsewhere. Simply stated, however, this model is an extension of the model in [18] which has its origins in the well-known semiconductor laser Fabry-Perot model proposed by Adams, Collins, and Henning [19] in which average intensity in the cavity, rather than the photon rate equation, is used to model photon density. The model is similar to [18] except that now the VCSOA is assumed to have two orthogonal polarization states, rather than a single dominant polarization.
Table 4.4.1 summarizes the parameters used to model the VCSOA, and Table 4.4.2 summarizes the model operating conditions for inverter operation in terms of phase detuning. The calculated threshold current was 6.336 mA[16].

**Table 4.4.1: List of Parameters Used in Modeling VCSOA Inverter[16]**

<table>
<thead>
<tr>
<th>VCSOA Parameter</th>
<th>Value</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Wavelength of resonant mode, ( \lambda )</td>
<td>841.53 nm</td>
<td>---</td>
</tr>
<tr>
<td>Top DBR reflectivity, ( R_t )</td>
<td>0.9955</td>
<td>---</td>
</tr>
<tr>
<td>Bottom DBR reflectivity, ( R_b )</td>
<td>0.9995</td>
<td>---</td>
</tr>
<tr>
<td>Cavity refractive index, ( n_c )</td>
<td>3.2</td>
<td>---</td>
</tr>
<tr>
<td>Cavity length, ( L_i )</td>
<td>(3)( \lambda/n_c )</td>
<td>( \mu m )</td>
</tr>
<tr>
<td>Circular active region radius, ( r )</td>
<td>10 ( \mu m )</td>
<td>---</td>
</tr>
<tr>
<td>DBR high/low refractive index</td>
<td>3.45/2.89</td>
<td>---</td>
</tr>
<tr>
<td>Substrate refractive index, ( \mu_s )</td>
<td>3.45</td>
<td>---</td>
</tr>
<tr>
<td>Top DBR periods number</td>
<td>16</td>
<td>---</td>
</tr>
<tr>
<td>Bottom DBR periods number</td>
<td>26</td>
<td>---</td>
</tr>
<tr>
<td>Longitudinal confinement factor, ( \Gamma_l )</td>
<td>0.05</td>
<td>---</td>
</tr>
<tr>
<td>Lateral confinement factor, ( \Gamma )</td>
<td>1</td>
<td>---</td>
</tr>
<tr>
<td>Linear material gain coefficient, ( a )</td>
<td>( 2.7 \times 10^{-20} ) m(^2)</td>
<td></td>
</tr>
<tr>
<td>Linewidth enhancement factor, ( b )</td>
<td>3.2</td>
<td>---</td>
</tr>
<tr>
<td>Linear recombination coefficient, ( A )</td>
<td>( 2 \times 10^{9} ) 1/s</td>
<td></td>
</tr>
<tr>
<td>Bimolecular recombination coefficient, ( B )</td>
<td>( 1 \times 10^{-16} ) m(^3)/s</td>
<td></td>
</tr>
<tr>
<td>Auger recombination coefficient, ( C )</td>
<td>( 2 \times 10^{11} ) m(^6)/s</td>
<td></td>
</tr>
<tr>
<td>Transparency carrier density, ( n_0 )</td>
<td>( 1.6 \times 10^{24} ) 1/m(^3)</td>
<td></td>
</tr>
<tr>
<td>Internal quantum efficiency, ( \eta )</td>
<td>1</td>
<td>---</td>
</tr>
<tr>
<td>Fixed internal loss parallel mode, ( \alpha_1 )</td>
<td>990</td>
<td>1/m</td>
</tr>
<tr>
<td>Fixed internal loss orthogonal mode, ( \alpha_2 )</td>
<td>995</td>
<td>1/m</td>
</tr>
<tr>
<td>Spontaneous emission factor</td>
<td>( 2 \times 10^{-5} )</td>
<td>---</td>
</tr>
</tbody>
</table>
Table 4.4.2: VCSOA Inverter Operating Conditions for Modeling of Large Signal Response[16]

<table>
<thead>
<tr>
<th>$I_{BIAS}$ (mA)</th>
<th>$\Delta \phi_S$ (mrad)</th>
<th>$\Delta \phi_P$ (mrad)</th>
<th>$P_{Optical Bias}$ (µW)</th>
<th>$P_{Input}$ (µW)</th>
</tr>
</thead>
<tbody>
<tr>
<td>6.15</td>
<td>-.245π</td>
<td>-.09π</td>
<td>2</td>
<td>1 to 15</td>
</tr>
<tr>
<td>6.5</td>
<td>-.255π</td>
<td>-.075π</td>
<td>2</td>
<td>1 to 15</td>
</tr>
</tbody>
</table>

4.5 Results and Discussion

Figure 4.5.1 shows the measured and simulated DC transfer characteristics for the VCSOA inverter above and below threshold obtained using the operating conditions in Tables 4.3.1 and 4.3.2. In the experiment, the Optical Bias input optical power was held constant at 2µW, and the Input optical power was increased incrementally using a variable optical attenuator. The Input and Optical Bias output of the VCSOA were measured at the 50/50 beam-splitter in front of the VCSOA, and the Optical Bias output was plotted versus the Input to obtain the transfer curves in Figure 4.5.1[16].

Figure 4.5.1 shows that this VCSOA inverter exhibits high on/off extinction ratio (below threshold = 11.4dB, above threshold = 12.8dB), low switching power (below threshold = 6.5µW, above threshold = 8.5µW) and the positive noise margins which have come to be associated with these devices[17]. In general, the simulation results are in good agreement with the experimental results. It should be noted, however, by comparison of Tables 4.3.1 and 4.4.2, that the detuning does not trend the same with increasing bias current between the model and the experiment. The cause of this discrepancy is under investigation.
Figure 4.5.1: Experimentally measured (solid line) and simulated (dashed line) inverter transfer characteristics. (a) Below threshold and (b) above threshold. [16]

The results of the large signal modulation experiments are shown in Figure 4.5.2[16]. The modulation input was an NRZ pseudorandom $2^{15}-1$ bit pattern from an Anritsu MP1632A, and an Agilent 86100A digital communication analyzer was used in oscilloscope mode to capture the inverter output.
Figure 4.5.2: Transient Measurements at 200Mhz. (a) Below Threshold (rise time = 670ps, fall time = 140ps). (b) Above Threshold (rise time = 350ps, fall time = 100ps). Time scale = 500ps/div. Voltage scale = 5mV/div. Experimental (rough line) and model (smooth line). Model of injected signal is also shown in red.
The original purpose of the PRBS was to obtain eye-diagrams for our inverter; however, the small output optical power levels of the inverter made eye-diagram measurements difficult to resolve from the noise floor of the high-speed photodetector and DCA oscilloscope. Rise and fall time measurements were more accurate because the DCA averaging feature could be employed to significantly reduce the effect of noise. Transient measurements were taken at a frequency of 200Mhz since performance predictions for our inverter were in the range of 1Ghz. These predictions were based on performance predictions from the VCSEL vendor, and independently verified using equations 4.1 and 4.2 and the parameters in Table 4.4.1 with the above-threshold bias current (I_{bias} = 6.5mA). The Optical Bias optical power was held constant at 2\mu W, and the Input optical power was modulated between 0 and 15\mu W. Detuning for both optical inputs was the same as for the DC transfer characteristics experiment.

As shown in Figure 4.5.2, below threshold, rise time was 670ps and fall time was 140ps. If the rise time were used exclusively to create the modulation waveform, the frequency would be \sim 750Mhz. In contrast, if the fall time were used, the modulation frequency would be much higher: 3.5Ghz. Above threshold, rise time was 350ps (1.4Ghz) and fall time was 100ps (5Ghz). Several points are worth noting here. First, the rise times are on the order of the VCSEL modulation bandwidth. This would indicate that the gain recovery time for the Optical Bias, which determines the rise time, is limited by the same carrier transport issues that limit the VCSEL modulation bandwidth. Second, the fall times are significantly shorter than the rise times, indicating that fall time could be governed by nonlinearity in the gain. Finally, both rise and fall time exhibit improvement with bias current, as does the on/off extinction ratio. Improved inverter
performance is expected as bias current is increased since gain increases with bias current. However, self-heating will also increase with bias current, and will eventually limit the modulation response[4]. Lastly, Figure 4.5.2 shows our model and experimental data in very good agreement.

The measured small signal frequency response (S21) of the VCSOA inverter is shown in Figure 4.5.3 for the above and below threshold cases.

![Figure 4.5.3: Modulation Bandwidth. Below threshold (squares). Above threshold (triangles). Dashed line is 3dB bandwidth.]

The small-signal waveform on the Input was created by passing an electrical sine wave from an Agilent 8703A component analyzer to the RF input of the modulator, and observing the average input optical power to the VCSOA on the Newport 1830-C power meter and the output of the VCSOA on the Agilent 86100A DCA oscilloscope. The optical power offset of the waveform was adjusted using the modulator's DC bias to produce the average input optical power necessary to position the waveform in the center of the linear region of the VCSOA inverter's DC transfer characteristic. The modulation
depth was then adjusted to fit the amplitude of the waveform in the linear region of the inverter's DC transfer characteristic. This was accomplished by setting the biasing conditions on an RF amplifier at the RF input to the modulator to produce an undistorted sine wave at the output of the VCSOA. The small-signal response was then measured using the Agilent 8703A component analyzer. The Optical Bias optical power was held constant at 2µW, and the detunings of both beams were the same as in the previous experiments.

The results of the small-signal experiments compare quite favorably to the results of the large signal experiments. Below threshold, large signal experiments predict the modulation bandwidth of the inverter to be limited by the rise time (670ps), which translates to a modulation bandwidth of 750Mhz. This is exactly the modulation bandwidth measured using small-signal experiments. Above threshold, large signal experiments predict the modulation bandwidth will be 1.4Ghz and small-signal experiments show ~1.85Ghz. The discrepancy between these results versus the below threshold case can be attributed to the slope of the transfer function in each case. The slope will increase with bias current since the gain will increase, which means the amplitude of the modulated input must be smaller to fit in the linear region. Small-signal analysis is always an approximation of the theoretical limit rather than a measure of what can be attained in practice, and therefore, if the amplitude of the input is decreased, the modulation bandwidth can be expected to increase.

As with the large signal experiments, modulation bandwidth was observed to increase with bias current for the same reasons discussed previously. These results
further support the conclusion that the VCSOA inverter modulation bandwidth is limited by carrier transport issues in the same manner as electrical modulation of VCSELs.

### 4.6 Conclusion

In this chapter, the response time of an 850nm VCSOA inverter under optical modulation was investigated. Since VCSOAs are VCSELs that are biased below threshold, they are subject to the same limiting factors in regard to modulation bandwidth. VCSEL modulation bandwidth is limited by the relaxation oscillation frequency (ROF) which is a measure of the rate of energy transfer between photons and electrons above threshold at the onset of lasing[1]. The ROF is limited by carrier transport, parasitic capacitance, and heating, and can be improved through modifications to the VCSEL structure which minimize these effects[4, 6-8, 12]. In addition, the ROF can be enhanced through optical injection which minimizes the effects of carrier transport, parasitic capacitance, and heating by creating stimulated emission carriers directly in the active region[3, 5]. If optical-injection locking is used with high optical injection ratio and detuning, the ROF can experience an almost limitless performance enhancement[9-11]. However, the use of a high injection ratio means that injection-locked VCSELs cannot be cascaded, and therefore have limited use, if any, in optical logic[15].

The ROF does not apply, by definition, to the VCSOA since the VCSOA is operated below threshold. However, the principles of energy transfer between photons and carriers is still applicable when the VCSOA is used to amplify coherent optical injection. The speed of energy transfer between photons and carriers in the VCSOA
inverter can be described in terms of photon relaxation time and carrier recombination time. The inverter 0 to 1 transition was shown to be limited by carrier recombination time since this is the limiting factor in the gain recovery time of the Optical Bias. Carrier recombination time was also shown to be limited by carrier transport, parasitic capacitance, and heating issues. Thus, the inverter 0 to 1 transition was expected to approximate the response time of electrically modulated VCSELs.

The inverter 1 to 0 transition was shown to also be limited by carrier recombination time. However, in this case, the sharp increase in photon-density resulting from nonlinearity in the Input gain made the recombination time faster than the 0 to 1 transition. Overall, however, the modulation bandwidth of the VCSOA inverter was limited by the speed of the 0 to 1 transition. Therefore, the modulation bandwidth of the VCSOA inverter was expected to approximate that of electrically modulated VCSELs.

Experimental and theoretical results of large and small signal analysis of the VCSOA inverter verified the above conclusion. In addition, they demonstrated that the inverter performance can be expected to improve with increased bias current due to the increase in gain. These results support the conclusion that improvements in VCSEL design and optical injection to mitigate carrier transport, parasitic capacitance, and heating, may result in significant performance improvement for the inverter, and that operation above threshold (i.e., as a VCSEL instead of VCSOA) would result in further performance improvement.

ACKNOWLEDGEMENT

The material in Chapter 4 is from Veronica Gauss, Antonio Hurtado, Doug Jorgesen, Michael J. Adams, and Sadik Esener, “Static and Dynamic Analysis of an All-
Optical Inverter based on a Vertical Cavity Semiconductor Optical Amplifier (VCSOA),”
to be submitted to Optics Express, 2009.


4.7 References


16. V. Gauss, Electrical and Computer Engineering Department, University of California, San Diego, 9500 Gilman Dr., La Jolla, CA 92093, and A. Hurtado, D. Jorgesen, M.J. Adams, and S. Esener are preparing a manuscript to be called “Static and Dynamic Analysis of an All-Optical Inverter based on a Vertical Cavity Semiconductor Optical Amplifier (VCSOA)”.


5. CONCLUSION

This dissertation is an in-depth analysis of all-optical logic gates based on Vertical Cavity Semiconductor Optical Amplifier (VCSOAs). These type of logic gates may provide a solution to the optical-electrical-optical conversion delay problem in telecommunications network switches and high-performance computing environments since their logic operations are performed exclusively in the optical domain. They are particularly well-suited to these applications since they are based on mature 850nm-wavelength Vertical Cavity Surface-Emitting Laser (VCSEL) technology which is already prevalent in short reach and local area ethernet networks[1, 2]. Three types of VCSOA all-optical logic gates- the Set-Reset flip-flop, Exclusive-OR (XOR), and Not-AND (NAND) gates- were demonstrated in this dissertation using pairs of 850nm proton-implanted VCSOA inverters. Advantages of these VCSOA logic gates include low electrical and optical power consumption, high-density integration and modular design, manufacturing, cascadability, and single-wavelength operation. Performance analysis of the VCSOA inverter, which is the fundamental building block of all VCSOA logic gates, suggests that faster operation is possible when the VCSOA is biased above threshold (i.e., operates as a VCSEL). In addition, while the speed has been shown to be limited on the order of the modulation bandwidth of the VCSEL, new advances in VCSEL design[2] and optical injection[3] show promising avenues for considerably advancing the response time of the inverter. These results indicate that future logic gates based on VCSEL technology have the potential to not only meet but exceed the requirements of future ethernet networks[1].
5.1 Summary

In Chapter 1, the problem of optical-electrical-optical (O-E-O) conversion delay in telecommunications network switches and high-performance computing (HPC) was presented. The main limitation stems from the bandwidth limitation of electrical interconnects as the speed of data transfer increases[1, 4]. Studies have shown that when lane speeds exceed 10 Gbps for short-haul data links, power consumption, density, and cost considerations favor optical interconnects over electrical interconnects[1]. This, in turn, necessitates the development of all-optical circuits and associated all-optical logic gates. Logic gates based on VCSELs may be the preferred solution since VCSELs are a mature technology that is already well-established in short reach and local area ethernet networks[1, 2]. This dissertation studies the closely related VCSOA (i.e., VCSEL biased below threshold) in order to assess its potential in the development of all-optical logic gates.

In Chapter 2, an all-optical Set-Reset (SR) flip-flop was demonstrated from two cross-coupled 850nm VCSOA inverters[5]. Comparison to electrical SR flip-flops showed that the VCSOA design had simpler implementation in terms of number of discrete components due to inherent advantages in optical versus electrical signaling. Comparison to other all-optical flip-flops demonstrated additional advantages including low electrical and optical power consumption, high-density integration, manufacturing, cascadability, and single-wavelength operation. The principle of operation was observed to have the same physics as the VCSOA inverter, namely cross-gain modulation, highly nonlinear gain, and polarization anisotropy. Experimental demonstration showed the high extinction ratio and low switching power which have come to be associated with
VCSOA inverters[6]. Finally, new designs were presented which demonstrate the exciting potential for high-density integration and single-wavelength operation.

In Chapter 3, all-optical VCSOA XOR and NAND gates were demonstrated using two 850nm VCSOA inverters[7]. Designs were presented for both continuous wave (CW) and modulated optical bias in order to compare the electrical paradigm with the simplest implementation, respectively. While CW XOR and NAND gates are more complex, as they are in DC biased electronic gates, they may permit the development of a common high-density integration platform which would result in a novel all-optical programmable logic element. In addition, comparison of VCSOA XOR and NAND gates to other all-optical gate technologies demonstrated the same advantages as the SR flip-flop. Finally, experimental demonstration brought several issues to light, including inconsistent timing of logic level transitions and the existence of multiple logic levels. These issues could be improved by increasing the bias current which increases overall gain, and by using inverters with more similar operating characteristics.

In Chapter 4, the response time of an 850nm VCSOA inverter to high-speed optical modulation was investigated in order to understand the performance limitations of VCSOA logic gates[8]. The similarity of the VCSOA and VCSEL structures indicated that the inverter modulation bandwidth would be limited by the same factors as the electrically modulated VCSEL. Large and small signal experiments showed that the response time of the inverter did indeed approximate that of the electrically modulated VCSEL, and simulations provided further support for this conclusion. Large signal experiments showed that rising and falling transitions had different transition times due to nonlinearity in the Input gain, and the rising transition was found to be the limiting factor
in the response time of the inverter. Experiments were also conducted both below and above threshold to determine the impact of bias current on the performance of the inverter. As expected, higher performance was observed as bias current was increased due to the increase in overall gain. These results support the conclusion that improvements in VCSEL design[2] and optical injection[3] could result in significant performance improvement for the inverter.

5.2 Future Directions

In this dissertation it has been demonstrated that VCSOA logic gates have great potential to materialize real-world all-optical circuits. They have been shown to far outperform comparable all-optical logic technologies, and have many additional advantages in terms of their similarity to electrical logic gates and the prevalence of VCSEL technology already in use. Many issues remain to be addressed, however, including how to realize high-density integration designs and interfaces to external optical circuitry, temperature dependence of individual VCSOAs on the operating characteristics of optical circuits, and methods for increasing the modulation bandwidth of the inverter.

The high-density integration designs presented in this dissertation provide exciting prospects for programmable logic elements of VCSEL-based logic gates; however, issues such as input/output polarization mismatch, coupling to external waveguides, and the availability and alignment of small passive components such as beam-splitters and half-wave plates still need to be examined. In addition, because of the processes used to fabricate VCSEL arrays, non-uniformity will exist in the operating
characteristics of VCSELs across the wafer. Therefore, some investigation would be required to understand the operating tolerances involved when creating optical circuits from these VCSELs.

Another issue of VCSEL-based logic is the temperature dependence of VCSELs which can cause operating characteristics to drift with temperature. Once again, some investigation would be required to determine how operating characteristics vary with temperature, and whether there would be sufficient tolerance between logic gates to maintain correct operation.

Finally, exciting prospects exist in the issue of response time of VCSEL-based inverters. Recent improvements in VCSEL design[2] and optical injection[3] hold promise for significant improvements in the response time of VCSEL-based inverters. However, the actual benefit to VCSEL-based inverters remains to be seen.
5.3 References


7. V. Gauss, Electrical and Computer Engineering Department, University of California, San Diego, 9500 Gilman Dr., La Jolla, CA 92093, and H. Zhang, D. Jorgesen, M. Gross, and S. Esener are preparing a manuscript to be called “All-Optical XOR and NAND gates based on Vertical Cavity Semiconductor Optical Amplifiers (VCSEOs)”.

8. V. Gauss, Electrical and Computer Engineering Department, University of California, San Diego, 9500 Gilman Dr., La Jolla, CA 92093, and A. Hurtado, D. Jorgesen, M.J. Adams, and S. Esener are preparing a manuscript to be called “Static and Dynamic Analysis of an All-Optical Inverter based on a Vertical Cavity Semiconductor Optical Amplifier (VCSOA)”.