The Materials Science of Titanium Dioxide Memristors

by

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Abstract

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This dissertation describes the materials science of memristive switching in titanium dioxide. It discusses the structural changes of the oxide that take place and provides a phenomenological model for the dynamical behavior during switching. Further, the dissertation describes a two-state variable nanoscale device based on metal insulator transitions and memristive switching. It concludes with a discussion of various applications of titanium oxide memristive devices.
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Chapter 1

Introduction to resistive switching in oxides

1.1 Description of the phenomenon

Nonvolatile resistance switching is a seemingly universal phenomenon exhibited by metal oxide insulators when they are fabricated into metal-oxide-metal thin-film capacitor structures. The qualitative behavior is straightforward: apply a sufficient voltage across the metal electrodes and the resistance of the oxide permanently changes, typically by several orders of magnitude. The resistance can be reversed back to the original value by applying another voltage across the electrodes. A resistance decrease is called a ‘SET’ or ‘ON’ switching operation and an increase is called a ‘RESET’ or ‘OFF’ switching operation. Some oxides can be switched ON and OFF by applying the same voltage polarity and are consequently labeled as unipolar, while others, labeled as bipolar, require opposite polarities for ON and OFF switching. For both types, a so-called electroforming step is frequently required to initiate switching from a highly resistive as-fabricated state to a less resistive OFF/ON switching regime. This electroforming is typically achieved by applying a voltage larger than either of the subsequent OFF or ON switching voltages.

1.2 Literature survey

Resistive switching in oxides was discovered and identified for applications in solid state memory in the early 1960s. The first reports on the phenomenon came from Hickmott and Hiatt at GE [1, 2] and Gibbons and Beadle at Stanford [3]. The potential applications of this type of switching drove a flurry of study on the materials science of oxide conduction phenomena. However, by 1971 a lack of consensus remained regarding the following three questions:

1. Is the switching effect due to localized or uniform conduction pathways?
2. Is the switching due to charge trapping or ionic motion?

3. Is the effect occurring in the bulk of the oxide or at the interface with the electrodes?


Concurrently, in 1971 Dov Frohman-Bentchkowsky at Intel produced the first practical implementation of MOSFET-based floating gate charge storage memory (EPROM) [6, 7]. EPROM technology and its descendants, EEPROM and FLASH, have since dominated the solid state memory market mainly because they have been tied to the blistering speed of innovation and device scaling of silicon MOS technology. It is perhaps unsurprising that research activity into oxide switching tapered off in the early seventies and the phenomenon was regarded as a scientific curiosity for three decades.

Resistance switching in oxides regained interest from the scientific community in the early 2000s when a new generation of researchers observed the phenomenon while studying the ferroelectric [8, 9], high dielectric constant (\(\kappa\)) [10, 11] and magnetoresistive [12, 13] properties of thin film perovskite oxides. At around the same time, nanoscale crossbar circuits [14, 15] and novel computing architectures [16, 17, 18] based on two-terminal resistive switching emerged as possible candidates to replace conventional CMOS. In 2006 Szot et al. demonstrated that resistive switching in oxides could be confined to a single dislocation in SrTiO\(_3\) [19] implying that the ultimate scalability for the phenomenon is beyond 10 nm. These results indicate that resistive switching in oxides could be the go-forward technology for nonvolatile memory after FLASH hits its impending scaling floor at the 16 nm node in 2016 (see e.g. the Emerging Research Devices section of the 2009 ITRS Report [20]). Although there are still technical problems to be worked out, the promise of extending memory scaling by several generations has spurred a resurgence of research on oxide switching in the past five years.

During this time a variety of groups around the world have employed the advent of new analytical techniques and improved electrical equipment to more directly answer the questions left over from the seventies. The first question of whether or not the conduction is localized in switching oxides has been answered for a broad range of oxide phases ranging from the complex, such as single crystal epitaxial Ruddlesden-Popper phases, to the simple, such as amorphous sputtered binary oxides. There is now consensus that for both unipolar and bipolar switching the switching effect is almost always located to a small region of the device which is typically defined by electroforming. By employing electron beam induced current (EBIC) measurements, Rossel et al. showed localized conduction pathways in switching SrZrO\(_3\) epitaxial films [21]. Choi et al. used conductive atomic force microscope (AFM) measurements to demonstrate that switching is localized in atomic layer deposition (ALD) grown polycrystalline TiO\(_2\) films [22]. Szot et al. also used conductive AFM to demonstrate the localized dislocation switching mentioned above in SrTiO\(_3\) [19]. Jeong et al. inferred from impedance spectroscopy of polycrystalline TiO\(_2\) that the conduction pathway was localized [23]. Janousch et al. employed synchrotron-based x-ray absorption measurements to directly map a locally reduced pathway between
the electrodes of a planar Cr: SrTiO$_3$ device [24]. Kim et al. inferred that switching in ALD grown TiO$_2$ films is localized from DC current-voltage ($i-v$) measurements [25]. Sato et al. inferred a ‘thermal filament’ model from pulsed switching measurements of sputtered NiO and TiO$_2$ films [26]. Chae et al. proposed that unipolar switching in sputtered NiO can be modeled as local breakdown in a resistive network based on their observation in that between switching events the threshold voltages appear to be randomly distributed [27]. The observation of localized features with AFM led Yang et al. to conclude that the electroforming step creates a locally reduced channel [28]. This observation was later confirmed by synchrotron-based spatially resolved photoemission spectroscopy by Strachan et al. [29]. Kwon et al. [30] reported direct observation of the localized channel with cross-sectional TEM for unipolar TiO$_2$ switches while Strachan et al. [31] reported direction observation in bipolar TiO$_2$ switches.

The fact that there is some universality to the localization of switching for vastly different oxide compositions and structures indicates that the switching effect is more likely to be related somehow to the oxygen ions in the lattice, rather than electronic structure or trapping effects. Indeed, there seems to be broad consensus in the community now that switching is related to the motion of oxygen or oxygen vacancies, as determined by the application of advanced techniques. Fujimoto et al. used electron energy loss spectroscopy (EELS) to demonstrate that TiO$_2$ is reduced, or has a high vacancy concentration, in the switching region [32]. Karg et al. used temperature dependent electron transport measurements to infer that resistance changes were related to the presence of vacancies which act as hopping centers [33] in SrTiO$_3$. Fujii et al. and Jameson et al. respectively came to a similar conclusion using similar techniques for epitaxial SrTi$_{1-x}$Nb$_x$O$_3$ [34] and bulk single crystals of TiO$_2$ [35]. As mentioned above, Janoush et al. was able to directly image a reduced channel in SrTiO$_3$ using XAS mapping [24]. Hirose et al. [36] and Phan et al. [37] used impedance spectroscopy to infer that vacancy motion was responsible for switching in SrTiO$_3$. Hasan et al. also used pulsed electrical measurements to conclude that vacancy migration is responsible for switching in La$_{0.7}$Ca$_{0.3}$MnO$_3$ [38]. Jeong et al. [39] and Yang et al. [28] showed with AFM that electroforming of TiO$_2$ materials causes features to appear on top electrodes, reportedly due to oxygen evolution during the forming process. Yang et al. used conductive AFM and electrical measurements to demonstrate that electrical switching is also mediated by vacancy motion in Ca doped BiFeO$_3$ grown on SrTiO$_3$ [40]. Strukov et al. developed the first complete quantitative model for bipolar switching in oxides based on vacancy drift/diffusion [41] and showed that this model is equivalent to the memristor element predicted theoretically by Chua [42]. Strukov et al. later expanded this simple model to account for non-linearities in electronic and ionic [43, 44] transport. Jeong et al. published a similar model for switching in TiO$_2$ based on vacancies modulating the barrier height of an interface Schottky barrier [45].

The relationship between vacancy motion and total device resistance was the third remaining question for the switching mechanism and turns out to be the main difference between the material mechanisms for bipolar and unipolar switching in oxides. For
bipolar switching in thin films the consensus that exists now points to a modification of the contact resistance between the oxide and the electrodes rather than the oxide bulk. Various researchers have come to this conclusion from transport and impedance spectroscopy measurements on epitaxially grown Schottky barriers of the model systems Pr_{0.7}Ca_{0.3}MnO_3 [46], SrTi_{1−x}Nb_{x}O_3/SrRuO_3 [47, 34] La_{1−x}Sr_{1+x}MnO_4 [48] and SrTiO_3[37]. Other researchers came to similar conclusions for Schottky barriers fabricated from ceramic SrTiO_3[36], sputtered La_{0.7}Ca_{0.3}MnO_3 [38], SrTiO_3 bicrystals [49], bulk single crystals of Rutile TiO_2 [35, 50] and sputtered TiO_2 [50]. Miao et al. used the more direct method of pressure modulated conductance microscopy to demonstrate that barrier width modulation is the likely switching mechanism in Pt/sputtered TiO_2/Pt devices [51]. Borghetti et al. used temperature dependent transport measurements to strengthen this model [52]. As discussed above, Strukov et al. [41, 43, 44] and Jeong et al. [45] have developed quantitative models based on vacancy modulation of interface barriers in bipolar devices.

For unipolar switching the original model of Gibbons and Beadle [3], based on current-driven creation/rupture of reduced shunt channels through the bulk of the film, remains largely intact. Chae et al. have updated the model in the context of random resistor networks to account for switching variability [27]. Kwon et al. have shown direct TEM evidence that a metallic reduced oxide of Ti_4O_7 channel bridges the two electrodes in the ON state, but is incomplete in the OFF state of a unipolar Pt/TiO_2/Pt switch [30].

1.3 Dissertation summary

In this dissertation I report the results of five research efforts that I either advanced or contributed significantly to during the past three years. Chapter 2 shows the results of an effort to directly characterize the material structure of switching centers in a functioning device using TEM and synchrotron-based scanning transmission x-ray microscopscopy (STXM) and is based on reference [31]. The results unambiguously demonstrate that the switching effect is localized and that the conduction channel is composed of a reduced metallic phase. Chapter 3, based on reference [53], reports a dynamical electrial characterization of oxide switching and presents a state-variable based memristive model to accurately and quantitatively predict device behavior. This work elucidates the highly nonlinear processes taking place in the oxide during switching for both the electronic and ionic motion. Chapter 4, based on reference [54], builds upon the previous memristive model and knowledge of conduction channel phase analysis to experimentally demonstrate a nanoscale device that exhibits both memristance and metal-insulator transition. This device is shown to produce self-sustained oscillations when biased with a DC voltage based on a threshold instability of the metal-insulator transition which, when coupled with the memristance, can be used for tunable oscillators. The final chapter shows the experimental demonstration of two circuit applications enabled by the memristive properties of metal-oxide-metal devices: the defect-tolerant demultiplexer, based on reference
[55], and the nonvolatile latch, based on reference [56].
Chapter 2

Microscopic characterization of functioning memristors

A full understanding of the atomic-scale mechanism and identification of the material changes within titanium oxide during memristive switching remains an important goal. In this chapter (previously published in part in reference [31]), we report the characterization of a functioning TiO$_2$ memristor using synchrotron-based x-ray absorption spectromicroscopy and transmission electron microscopy (TEM). We observed that electroforming of the device generated a crystallite of the Magnéli Ti$_4$O$_7$ phase within the initially sputter-deposited TiO$_2$ matrix. In an attempt to describe microscopically the source of the resistance change, many physical models have been put forth, including generation and dissolution of conductive channels [57, 58], electronic trapping and space-charge current limited current effects [59], strongly correlated electron effects such as a metal-insulator transition [60], and changes localized to the interface of the metal electrode and the oxide [46, 19]. Identifying the correct model and quantifying its physical parameters using exclusively electrical characterization has not entirely eliminated the ambiguity between these available models. Meanwhile, direct physical characterization [24] requires the capability of observing subtle material changes, such as vacancy creation, occurring in a nanoscale volume buried between two metal contacts. Recently, Kwon, et al. [30] performed cross-sectional TEM studies of the unipolar resistive switching in TiO$_2$, revealing the presence of nanoscale Magnéli phase conductive channels following device operation and extraction of a region of interest. A Ti$_4$O$_7$ phase was confirmed from the temperature dependence of the conductance. Concurrently, we have investigated the bipolar memristive switching mode of TiO$_2$, using non-destructive transmission-geometry spatially-resolved x-ray absorption and electron diffraction to report on the associated chemical and structural changes of a functioning device.
2.1 Experiment description

To enable the transmission measurements, a vertical metal-insulator-metal (MIM) crosspoint device was fabricated on a thin free-standing Si$_3$N$_4$ window, as illustrated in Figure 2.1a. The device stack consisted of Cr(5)/Pt(15)/TiO$_2$(30)/Pt(30 nm) grown on a Si/Si$_3$N$_4$ (20 nm) substrate. The device consisted of a 2 $\mu$m wide bottom electrode and a 3 $\mu$m wide top electrode patterned perpendicular to each other with their overlap defining the active junction area. The junction was centered within the 60×60 $\mu$m$^2$ free-standing window (Figure 2.1b). The TiO$_2$ switching layer, which extends across the entire substrate, was sputter deposited from a titania source onto the substrate held at 250 $^\circ$C.

Following an initial electroforming step, the device exhibited reversible bipolar resistance switching (Figure 2.1c) between a low resistance of 20 k$\Omega$ (ON) and a high resistance of 1 M$\Omega$ (OFF), as measured at low bias. One issue of concern was whether devices fabricated on thin windows would behave similar to devices on thicker substrates; strain effects and the inability to sink the significant Joule heating generated during operation [29, 52] might change the device electrical characteristics. A comparison of the electrical switching in Figure 2.1c shows that window devices have similar switching behavior to standard devices fabricated on a silicon oxide substrate. The latter have been extensively characterized electrically [53], and show bipolar, non-volatile switching down to sizes of 50 nm (half-pitch) and speeds 10 ns.

Electrical characterization of the device was performed in a four-probe geometry using an HP4155 semiconductor parameter analyzer, with the bottom electrode grounded at all times. The electroforming step (inset to Figure 2.1c) was performed as a slow (~1 sec) 0 to -8 V sweep, leaving the device roughly 10$^6$ times more conductive. The comparison in Figure 2.1c shows a standard device (red, dashed) which has an identical materials stack, except uses a Ti adhesion layer rather than Cr. Transmission devices studied in this paper used Cr in order to avoid any Ti background signal. After performing 6 ON/OFF switching cycles, the device was characterized by STXM and TEM.

2.2 STXM characterization

X-ray measurements were performed using the Scanning Transmission X-ray Microscope (STXM) at the Advanced Light Source in Lawrence Berkeley National Laboratory\textsuperscript{1}. STXM allows spatially-resolved x-ray absorption spectroscopy (XAS) to be performed on a sample by raster-scanning a focused, monochromatic x-ray beam that can be tuned in energy with better than 100 meV resolution [61]. Focusing of the x-rays is accomplished using a diffraction-based Fresnel zoneplate lens, which can give a spatial resolution of

\textsuperscript{1}STXM measurements and analysis were performed on this sample exclusively by John Paul Strachan, but are included here with permission because they are complementary to the TEM data analysis performed by the author.
Figure 2.1: Illustration of the device geometry for transmission characterization. a) A cross-bar device is aligned to a free-standing silicon nitride window in which the underlying silicon substrate has been fully etched away in a 60×60 µm² area. A bottom and top electrode are defined in separate photo-lithography steps, with an unpatterned titanium dioxide layer in between. b) Optical micrograph of a completed device. c) Electrical characterization of the titanium dioxide memristor before physical measurements. Following an electroforming step (inset), the device shows bipolar resistance switching (solid green trace) to an ON state with positive bias and to an OFF state with negative bias. Comparison to a standard, non-window device fabricated atop a silicon/silicon oxide substrate is also shown (red, dashed).
roughly 35 nm. The absorption of x-rays by the sample is measured in a transmission geometry. In our study, a sequence of images of the device junction area was acquired at incremental photon energies and spatially localized spectra were generated by post processing this absorption versus energy data set within various regions of the sample.

After electroforming and switching of the device, STXM measurements were performed within the junction area while scanning the incident monochromatic x-ray energy. With this technique, the switching layer can be isolated from the Pt electrodes and other materials in the stack by tuning the x-ray energy to a Ti resonance, in this case the Ti L\textsubscript{2,3} absorption edge (455 - 475 eV). The observed absorption intensity is proportional to the unoccupied density of states, broadened by the core-hole lifetime, and can act as a fingerprint to identify the phase and chemical state of the titanium [62, 63, 64]. Figure 2.2a shows an x-ray image of the junction taken at a single energy within the Ti edge, illustrating the absorption contrast within the device. In this image, increased absorption corresponds to darker regions, and the main contrast observed here is primarily based on material thickness and elemental mass, with the Pt electrodes dominating in absorption. However, a region near the center of the device possessing chemical contrast is already evident. Full processing of the energy-dependent stack of images across the Ti L-edge revealed the presence of three distinct states of the titanium oxide switching layer and the corresponding absorption spectra are shown in Figure 2.2c. Figure 2.2b provides a spatial mapping for the three states of the oxide, with regions labeled i, ii, and iii. For similar devices with no prior electrical treatment ("virgin state"), no such chemical features are observed.

Region i is outside of the junction area and is most similar to the as-deposited TiO\textsubscript{2}, which is known from X-ray Diffraction (XRD) to be an amorphous phase. Within the junction (region ii), the spectrum strongly matches the known XAS for anatase, one of the crystalline polymorphs of TiO\textsubscript{2} [63, 64]. This crystalline phase shows a noticeable sharpening of the absorption peaks, particularly the first and third main peaks (near 458 and 463 eV) and an increased crystal field splitting. Additionally, a prominent splitting of the second main peak (near 460.5 eV) is observed due to the distortion [62, 63, 64] of the Ti site from octahedral to tetragonal symmetry. This crystallization of the deposited titanium dioxide has been observed [29] in resistance switching devices and is driven by Joule heating, which can raise the device temperature above 350 °C in spatially localized regions [52]. Figure 2b indicates that the crystallized region extends along the bottom electrode, possibly because of the reduced thickness and width compared to the top electrode.

Most striking is region iii, an approximately 200×300 nm\textsuperscript{2} area that has a qualitatively different absorption spectrum (Figure 2.2c, blue spectrum) from those of regions i and ii. Here, the spectrum exhibits a pronounced shift in density to lower energies (new features at 456 eV and 461.3 eV), as well as a merging of the crystal-field split doublet pairs. These changes result from core-level shifts, [65, 66, 67, 68] indicating a mixed-valence composition in region iii of Ti\textsuperscript{+3} and Ti\textsuperscript{+4}, and closely matching the spectral shape and trend [68, 69] for deliberately reduced titanium oxide layers. This is a direct
Figure 2.2: Chemical and structural mapping of a functioning memristor by Scanning Transmission X-ray Microscopy (STXM) following electroforming and ON/OFF cycling. 

a) STXM image of the device junction area, taken at an x-ray energy of 460.0 eV within the Ti L$_3$ edge. Absorption contrast is observed within the junction. 
b) Chemical and structural mapping of the three observed phases of titanium oxide. Region i (green) is the as-grown amorphous TiO$_2$, region ii is the anatase phase, and region iii shows a stoichiometrically reduced suboxide TiO$_{2-x}$, or equivalently a mixed-valence oxide with Ti$^{+3}$ and Ti$^{+4}$ ions. The color mapping of each pixel is derived from the Ti L$_{2,3}$ x-ray absorption spectrum using singular value decomposition procedures. 
c) The corresponding Ti L-edge x-ray absorption spectra.
observation of a locally reduced region within the functioning bipolar resistance switch. Since reduction of titanium dioxide leads to metallic conductivity, and is not present in a virgin device, it follows that this observed region is responsible for the dramatic conductivity increase after electroforming of the junction.

2.3 TEM characterization

Complementing the chemical analysis, localized structural information was acquired by transmission electron microscopy (TEM) and nanobeam diffraction on the same device. TEM measurements were performed on a JEOL 2100F equipped with a Gatan Imaging Filter operating at 200 kV. At various locations within the device, electron diffraction images were acquired using a nanobeam spot sizes of 50 to 200 nm. Diffraction pattern images were calibrated to a Si [100] zone axis pattern measured on the same sample at the edge of the window.

The upper right corner of the device was first characterized in order to determine the structure of the oxide in the regions i and ii of the STXM map in Figure 2.2b. A transmission image of the corner region is included as Figure 2.3a with the four circles indicating where the nanobeam diffraction measurements were taken. The position of the diffraction spots were chosen to determine the phases present in the top electrode region, bottom electrode region, junction region, and the window or TiO$_2$ only region. As demonstrated by the radially-integrated diffraction data of Figure 2.3b, the top electrode shows only Pt diffraction spots since the TiO$_2$ is amorphous. Both the bottom electrode and the junction regions show the signature of Pt and anatase crystals. These results are identical to those obtained from STXM which determined that region i is amorphous and region ii is anatase. Diffraction data from the TiO$_2$ in the window spot is not shown because it is amorphous and there were no spots in the diffraction image.

The electron diffraction pattern observed within the reduced region iii of Figure 2.2b is shown in Figure 2.4a and revealed a single crystal of Ti$_4$O$_7$, consistent with the spectroscopic results of the previous section. The phase of this crystallite was identified by reconciling the strongly diffracting spot positions with possible diffractions from all known phases in the Ti-O binary phase diagram. The diffraction spot positions were initially identified by comparing the magnitudes of the observed scattering vectors in the measured pattern to all possible scattering vector magnitudes of 17 phases we considered plausible. We used the database in the Phillips Analytical X’Pert software to generate a list of possible scattering vector magnitudes from the following crystal structures: the Anatase, Rutile and Brookite polymorphs of TiO$_2$, the series of Magnéli phases Ti$_n$O$_{2n-1}$ for n=3-10, the corundum structure Ti$_2$O$_3$, the cubic and hexagonal polymorphs of TiO, and the electrode metals Ti, Pt and Cr. Ti$_4$O$_7$ emerged as the only consistent structure.

The phase identification was confirmed by simulation of the Ti$_4$O$_7$ diffraction pattern using the reported structure [70] with SingleCrystal from Crystal-Maker Software. We found excellent agreement when the simulated zone axis is taken to be the lattice vector.
Figure 2.3: (a) TEM image showing a zoom on the upper right corner of the device with white circles indicating the positions of nanobeam diffraction measurements. (b) Radially integrated diffraction patterns from the spots of interest with vertical lines indicating possible scattering vector magnitudes for Pt and anatase. Comparison of the integrated profiles and possible peak positions shows that the TiO$_2$ is amorphous beneath the top electrode, but is in the anatase phase above the bottom electrode and in the junction region. These spots correspond to regions i and ii respectively of the STXM map of Figure 2.2b.
$[uvw] = [1.1, 1.7, 0.3]$, as indicated by the alignment of calculated (blue circles) and measured spot positions indexed in Figure 2.4a. The lateral size and shape of the crystallite was revealed to be $\sim 100 \times 50 \text{ nm}^2$ by dark field imaging with an aperture around the 10T spot as shown in Figure 2.4b.

Since the measurement was done on a device buried underneath platinum electrodes and embedded in an anatase matrix, the electron beam also transmitted through crystallites of Pt and anatase. Additional diffraction spots not associated with the reduced crystallite of interest are thus visible on the same pattern. The red and grey rings superimposed on the diffraction pattern indicate possible diffraction positions from anatase and Pt, respectively, showing that these other observed spots are likely background from these phases.

The observation of the Ti$_4$O$_7$ phase is consistent with the localized reduction seen in STXM, but also reveals an ordering of the oxygen vacancies in region iii of Figure 2.2b. Ti$_4$O$_7$ is a member of the homologous series of stable reduced TiO$_2$ phases, frequently referred to as the Magnéli phases, and has a metallic conductivity at room temperature [71]. The crystallographic structure is similar to that of the common rutile phase of TiO$_2$, but with ordered periodic planes of oxygen vacancies. The small area observed for the Ti$_4$O$_7$ crystallite (Figure 2.4b) indicates that ordering of the vacancies occurred within a sub-region of the reduced area (blue region of Figure 2.2b), possibly where Joule heating was highest during electroforming. Additional crystals of Ti$_4$O$_7$ and even higher order Magnéli phases may also be present in this region, but were not obvious from the measurements that we performed.

A more complete picture describing the mechanism for bipolar resistive switching thus emerges when the results of both the physical and electrical characterization are combined. Prior studies [52] of titanium dioxide memristors have shown that the electrical data is best modeled as a metallic element in series with a tunneling gap or other non-linear transport barrier. Additionally, studies using the technique of pressure modulated conductance with an AFM tip [51] show that insulating barrier width modulation is responsible for the switching mechanism. By applying this model to dynamical measurements [53] we have additionally suggested that ON and OFF switching involves the contraction or expansion, respectively, of this gap width by less than 1 nm. In the present device, the non-linear $i-v$ curve and low currents observed in both the ON and OFF states (Figure 2.1c) indicate that the observed metallic Ti$_4$O$_7$ phase does not entirely span between the bottom and top electrodes. Given the geometry of our transmission measurements, a resulting model (Figure 2.4c) is that resistive switching consists of a modulation of a barrier between Ti$_4$O$_7$ and the contacting electrodes. The modulation can either be of the barrier width (thickness of un-reduced titanium oxide) or height [45]: drift of oxygen vacancies from the Ti$_4$O$_7$ by an applied electric field reduces the barrier and increases the conductivity (ON switching), while the reverse motion induced by the opposite polarity field increases the barrier (OFF switching). Directly observing such a barrier modulation remains a future goal, but is exceptionally difficult for devices in the metal-insulator-metal geometry.
Figure 2.4: TEM characterization of the same memristive device as in Figure 2.2. a) Electron diffraction pattern taken within the reduced region (Figure 2.2b, region iii) of the device with a 50 nm nanobeam spot. Red and gray circles are superimposed on the diffraction pattern indicating possible diffraction rings from polycrystalline anatase TiO$_2$ and Pt, respectively. Indexed blue circles are the results of simulation by Single-Crystal software. b) Dark field imaging of the Ti$_4$O$_7$ Magnéli crystallite using the 104 diffraction spot showing a size of less than 50×100 nm$^2$. c) Resulting physical model for bipolar resistance switching of Pt/TiO$_2$/Pt memristors. The Ti$_4$O$_7$ acts as a source and sink of oxygen vacancies; application of an electric field pushes vacancies into or out of a thin barrier layer, thus modulating the barrier and switching between the ON and OFF states.
The observation of a Magnéli crystallite in a titanium dioxide matrix shows that bipolar resistance switching in an electroformed Pt/TiO$_2$/Pt memristive system is related to a localized partial reduction of titanium dioxide and crystallization of a metallic conducting channel. Inside a titanium dioxide matrix, the Magnéli phases are thermodynamically favored over a high concentration of randomly distributed vacancies [72], and thus they can act as a source or sink of vacancies in the matrix material depending on the electrochemical potential within the device. The application of an electrical bias can control vacancy motion into and out of this sub-oxide phase, modulating a transport barrier and leading to the dramatic conductivity change.
Chapter 3
Dynamics of memristive switching

A significant challenge to the widespread adoption of memristive oxide switches by circuit designers has been the lack of a predictive compact model that can be integrated into a time domain simulation package like SPICE. The desired circuit element model should abstract, parameterize, and predict the behavior of the device under an arbitrary voltage and current bias, at least under some restricted domain of state and/or excitation. Such a model has not been available for bipolar oxide switches, despite the significant progress in understanding their physical switching mechanism in the context of coupled electronic and ionic conductors.[57, 58, 24, 73, 74, 45, 43, 44]. As discussed in detail below, the memristive system [75] is the most appropriate framework for achieving the goal of quantitatively modeling these bipolar switches in the simplest way possible.

In this chapter (previously published in part in Reference [53]), we propose a dynamical electrical testing protocol and we establish a quantitative memristive model of bipolar switching for Pt-TiO$_2$-Pt crosspoint devices from the results. We analyze both the static electronic conduction behavior and the switching dynamics that arise from ionic motion in the device. Our analysis quantitatively establishes that electronic conduction in these devices can be parameterized by a single dynamical state parameter: an insulating barrier width $w$ that varies with time under an applied voltage or current. We see that the dynamical behavior for OFF and ON switching is highly nonlinear and asymmetric. We interpret these observations in terms of a moving phase boundary which is mediated by an exponential dependence of the drift velocity of ionized dopants on the applied current or voltage, and the competing or cooperative behavior of ionic drift and diffusion, depending on the switching voltage polarity.

3.1 The canonical memristive system

The framework of a single state variable memristive system was defined by Chua and Kang [75] as two coupled equations of the form:

$$ v = R(w, i) \cdot i $$

(3.1)
The generalized memristive system is a natural way to model oxide bipolar switches because it can reproduce the four important phenomena exhibited by these devices. These phenomena include the zero-crossing property, a time dependent $i-v$ shape, an amplitude dependent $i-v$ shape, and a continuous set of possible states. These four properties are shown for OFF switching in the time-sampled $i-v$ data of Figure 3.1 for a typical TiO$_2$ device under the application of a triangular voltage waveform with a variable amplitude and period. In this data the applied voltage is not equal to the measured device voltage because the series resistance of the nanowire electrodes holds a majority of the voltage. This voltage drop is removed from the data by performing four-wire measurements.

The first memristive property is obvious, but not trivial: all $i-v$ curves cross the
origin, or equivalently all curves exhibit ‘pinched hysteresis’. This means that no energy is stored in a purely memristive device, which is the case for all bipolar switches that we studied. The second memristive property is illustrated by the two 7 V amplitude curves: when the voltage is swept quickly, there is no change in device state and consequently no hysteresis in the $i-v$. However, when the voltage is swept slowly the device is able to change state and the loop opens up. The third memristive property is illustrated by the two 50 $\mu$s sweeps: when the applied voltage amplitude is increased from 7 V to 10 V the hysteresis loops open up. The fourth property is embodied in the two $i-v$ curves which exhibit switching: the device proceeds though a continuum of states while it switches until the current level is too low to cause further switching. This data makes it clear that these devices must be modeled as continuous dynamical systems and that the memristive system is an appropriate framework to use for that task.

3.2 The stress-test protocol

In order to track the state of the device throughout the switching process and obtain quantitative dynamical information, we have performed a quasi-static stress-test protocol summarized schematically in Figure 3.2. Using a two-step iterative process, we first apply a low voltage amplitude (too low to result in observable switching or hysteresis) triangular external voltage sweep to interrogate the state of the device as defined by its $i-v$ characteristic, and then apply a constant voltage time-sampled stress pulse to change the state of the device. This process is iterated until the junction has fully switched or the maximum test time has been reached.

In order to study the switching dynamics over six orders of magnitude in time, we fixed the amplitude of the applied voltage during each pulse but exponentially increased the pulse widths from one step to the next. This protocol required that the state be invariant when the device was not under a voltage pulse intended to change the state, i.e. it must be nonvolatile and the applied test waveform must be non-perturbative. This was a good assumption for our devices and our measurement protocol, since in our experience the devices stay at an arbitrary state without changing for at least a year in air at room temperature and we did not observe any hysteresis in the state-interrogation $i-v$ characteristics.

In the study presented here we examined the applied voltage dependence of OFF-switching dynamics for the device by applying a set of six state tests with pulse heights ranging from 3.0 V to 5.5 V. Additionally, we examined the applied voltage dependence of the ON-switching behavior at -1.25 V and -1.4 V. Each test had a total of 40 voltage pulses, which gave a total time under the applied voltage of 33 seconds. After each application of the state test, we reset the device to its initial condition with a quasi-dc triangular voltage sweep of the opposite polarity.

Although we held the applied or external voltage fixed during the state tests, there was an appreciable voltage dropped on the 2 k$\Omega$ electrodes. The actual or internal
Figure 3.2: The stress-test protocol is designed to slightly push the state of a memristive device with a time-sample stress pulse (blue) and test for resulting changes in the $i - v$ shape. In general it is necessary to make four-wire measurements and use full $i - v$ test sweeps in order to precisely observe changes in the nonlinear conductivity over time. This protocol implicitly assumes there is no state relaxation between stress pulses, an assumption that we have validated for our TiO$_2$ devices.
voltage, \( v \), seen by the device was lower than the applied voltage and evolved continuously throughout the switching process because of the voltage divider it formed with the series resistance of the electrodes. The current seen by the device during a test, \( i \), also changed throughout the switching process. The electrode series resistance and the nonlinearity of the conductivity yield a complicated relationship between the current and the external and internal voltages throughout the switching process. This behavior highlights the necessity of a four-wire time-sampled measurement scheme to completely characterize the state evolution during memristive switching. We accounted for these measured changes in stress voltage and current in our analysis and determination of the characteristic memristive equations for the device.

### 3.3 Device description and characteristics

For our experiments, we fabricated single crosspoint metal-oxide-metal switches on thermally oxidized silicon substrates with the following vertical structure: Si / SiO\(_2\)\((100)\) / Ti(5) / Pt(15) / TiO\(_2\)(50) / Pt(30), where the numbers in parentheses are the layer thicknesses in nanometers. The TiO\(_2\) was grown by sputter deposition from a rutile target onto a substrate held at 250\(^\circ\)C. X-ray diffraction (XRD), transmission electron microscopy (TEM) and Rutherford backscattering spectrometry (RBS) analyses on sister films of TiO\(_2\) grown with the same process showed that the layers are amorphous or nanocrystalline (TEM/XRD) and the as-grown stoichiometric ratio (RBS) of oxygen to titanium is 2.00\(\pm\)0.1.

In order to minimize the series resistance and the parasitic resistance-capacitance (RC) time constant of the wires and contact pads for time-sampled measurements, we present here the results from a large-area 5×5 \( \mu \)m\(^2\) crosspoint device. We performed similar experiments and analyses on a total of 5 devices with 4 different areas on 5 independently fabricated samples, including 50×50 nm\(^2\) devices defined by imprint lithography. The dynamical switching behavior was relatively insensitive to device size, presumably because the electroformation process creates the localized conduction channel described in the previous chapter.

We electroformed the TiO\(_2\) devices by applying a voltage sweep from 0 V to +6 V over 5 ms. As discussed in the previous chapter, electroforming causes localized heating and oxygen vacancy formation in these materials and produced an irreversible decrease in the resistance from the \( \sim 1 \) G \( \Omega \) as-fabricated state to the \( \sim 1-100\)k\( \Omega \) ON/OFF switching regime. Based on the characterization outlined in the previous chapter, we believe that the result of electroforming was a conducting channel with a resistance in the hundreds of Ohms that shunts most of the oxide film. The electroforming also produced a remnant insulating gap between the conducting channel and the opposite Pt electrode. Here we assume that the width, \( w \), of the insulating gap can be modulated by applying a voltage across the device which induces the motion of ionized defects. A schematic of this switching model and a representative switching \( i - v \) characteristic for these devices
Figure 3.3: The material model that we use to understand TiO$_2$ memristive systems is shown in (a). An electroformed reduced channel bridges the majority of the oxide region with a residual insulating region of width $w$. Four-wire stress test measurements are performed by attaching a voltage source $S$ to the top electrode, a current amplifier $A$ to the bottom, and a voltage amplifier $V$ between the two. The memristive state $w$ is modulated by applying a stress voltage for a fixed amount of time. A quasi-static $i-v$ curve (b) qualitatively demonstrates the memristive switching hysteresis with OFF switching occurring for positive voltages and ON switching occurring for negative voltages.

are included in Figure 3.3. The series resistance intrinsic to the channel can be obtained directly from the switching $i-v$ by fitting the differential resistance at high bias. For the device reported in detail here, the value obtained was $R_s = 215 \pm 6 \Omega$.

3.4 Quasi-static transport model

As discussed above, the generation of the memristive model from stress-test data is possible because the state of the device is tracked with low-voltage $i-v$ sweeps while the stress pulses step the state by a small amount. The test $i-v$ data gives information on the instantaneous memristive curve shape, but no direct information about the state.
Direct information is obtained by fitting the $i-v$ curve to a conduction model in order to reduce the data into a single state parameter. Based on our previous understanding of the phenomenology of switching and in order to simplify the model as much as possible while still maintaining phenomenological accuracy and physical relevance, we assume that the only material parameter that changes during switching is the width of the insulating gap. We also assume that the only electron conduction mechanisms that are important here are electron tunneling through the gap and ohmic conduction in the channel. These assumptions allow us to generate a particular form for the first memristive equation: the static transport relation of Equation (3.1). Here we use the Simmons simplification for tunneling which accounts for image charges barrier lowering [76] because it provides a relatively simple but accurate closed-form expression for the $i-v$ curve shape. The combination of this tunneling expression plus the channel series resistor (as shown in Figure 3.3) yields a coupled set of equations for the conduction model:

$$i = \frac{j_0 A}{\Delta w^2} \left[ \phi_I \exp \left( -B \phi_I^{1/2} \right) - (\phi_I + e v_g) \exp \left( -B (\phi_I + e v_g)^{1/2} \right) \right]$$ \hspace{1cm} (3.3)

$$v_g = v - v_R = v - i R_s$$ \hspace{1cm} (3.4)

with simplification terms in the equations defined by Simmons as:

$$j_0 = e/(2\pi h)$$ \hspace{1cm} (3.5)

$$\phi_I = \phi_0 - e v_g \left( \frac{w_1 + w_2}{2w} \right) - \left( \frac{1.15\lambda}{\Delta w} \right) \ln \left[ \frac{w_2(w - w_1)}{w_1(w - w_2)} \right]$$ \hspace{1cm} (3.6)

$$B = 4\pi \Delta w \sqrt{2m/\hbar}$$ \hspace{1cm} (3.7)

$$\Delta w = w_2 - w_1$$ \hspace{1cm} (3.8)

$$w_1 = \frac{1.2\lambda}{\phi_0}$$ \hspace{1cm} (3.9)

$$w_2 = w_1 + w \left[ 1 - \frac{9.2\lambda}{3\phi_0 + 4\lambda - 2ev_g} \right]$$ \hspace{1cm} (3.10)

$$\lambda = \frac{e^2 \ln 2}{8\pi \kappa \epsilon_0 w}$$ \hspace{1cm} (3.11)

Here $v$ is the internal voltage across the whole device, $v_g$ is the voltage across the insulating gap, $v_R$ is the voltage across the metallic channel series resistance, the state variable $w$ is the barrier thickness, $\kappa$ is the dielectric constant, $\phi_0$ is the effective barrier height, $R_s$ is the channel series resistance, and $A$ is the cross-sectional area of the tunneling gap. The other symbols have their usual meanings as physical constants. Due to the series coupling between the gap and the channel and the complexity of the transport equation, $i-v$ curves can only be solved by a numerical root finding procedure.

Figure 3.4 shows the test results of a 4.5 V OFF-switching stress-test on the device studied in detail in this chapter. The evolution of the $i-v$ curve shape during
Figure 3.4: A series of test $i - v$ curves demonstrates the nonlinear change in curve shape as the device is continually turned OFF with positive stress pulses of increasing width. The markers show experimental transport data for a given total time under stress, from which a particular value of the state variable $w$ is extracted. The solid lines indicate the results of the tunneling transport model which is used to infer the $w$ values.
OFF-switching is shown in detail: the device is shown to become more resistive but also qualitatively more nonlinear, a phenomenon that must be accounted for in an accurate memristive model. We successfully reduced the $i - v$ characteristic for each state of the device to a single variable by fitting to the above conduction model. The tunneling gap width $w$ as a single state variable was able to successfully reproduce the full nonlinear evolution, as shown by the model fits of Figure 3.4. For completeness we also considered the tunneling barrier height $\phi_0$ as a plausible single state variable, but could not accurately reproduce the experimental data by varying only the barrier height during the fitting procedure. Thus, we believe that the switching effect is primarily due to an effective tunneling distance modulation.

For the $i - v$ fitting we implemented an orthogonal distance regression procedure, based on ODRPACK [77]. We used a nested loop regression procedure in order to optimize the parameters $A$, $\phi_0$ and $\kappa$ for the entire data set simultaneously while $w$ was fit individually for each of the forty $i - v$ characteristics. Invariant device parameters that resulted were: barrier height $\phi_0 = 0.95 \pm 0.03\text{eV}$, dielectric constant $\kappa = 5 \pm 1$ and channel area $A = 10,000 \pm 2,500\text{nm}^2$. The series channel resistance, $R_s = 215\Omega$ was kept fixed during the fitting procedure because it was measured directly. The barrier width $w$ varied from 1.1 nm to 1.9 nm, with typical fitting uncertainty $\pm 0.1$ nm. Typical relative errors in the current and voltage measurements were 1%, but for the sake of clarity error bars are omitted from Figure 3.4. Assuming a cylindrical geometry for the conduction channel, the best fit area $A$ corresponds to a diameter of $110 \pm 10$ nm, which is consistent with previous direct measurements of the channel width in similar devices using the technique of pressure-modulated conductance mapping [51] as well as the results presented in the last chapter. This channel geometry yields a resistivity estimate of $4 \times 10^{-3} \Omega \text{cm}$ which is significantly more resistive than metallic Pt or Ti but reasonable for reduced TiO$_2$ [78] [79].

We assumed that the tunneling effective mass was equal to the free electron mass, because we do not have an independent means to measure this value. This could produce a systematic error in the above parameters and the reported barrier widths. For this reason the numerical results should be considered as effective values, although they nonetheless provide a good idea of the measurement precision. Invariant parameter values were obtained from a first regression analysis, e.g. at a particular voltage pulse amplitude, after which only $w$ was allowed to vary in subsequent fits. This procedure enabled us to track the width of the tunnel barrier as a function of time and applied voltage and consequently determine the dynamical behavior of these devices.

### 3.5 Dynamical model

By reducing each state $i - v$ to a value of $w$ we were able to examine the voltage-dependent dynamics of the effective barrier width during switching. Figure 3.5a shows the time evolution of $w$ during six OFF-switching tests with external voltages ranging
from 3.0 V to 5.5 V. Figure 3.5c shows the results of five ON-switching tests with voltages of -1.25 V and -1.4 V. We chose to study only two biases for ON-switching because the switching speed was much faster and more sensitive to the magnitude of the applied bias and we had a $RC$-limited time resolution of ($\sim 1\mu s$) in our test setup. ON-switching repeatability was therefore demonstrated via multiple stress tests at the same voltage. The device state evolved in a continuous but highly nonlinear manner between the ON and OFF states, and the switching speed was strongly dependent on the current magnitude and polarity. In order to determine a particular form for the second memristive equation (dynamical state evolution Equation 3.2) for OFF- and ON-switching, we again applied a orthogonal distance regression technique.

The end result was a set of consistent parameters for the full range of applied voltages studied, with the following analytical expressions for OFF switching:

$$\dot{w}_{OFF} = f_{OFF} \sinh \left( \frac{i}{i_{OFF}} \right) \exp \left[ -\exp \left( \frac{w - a_{OFF}}{w_c} - \frac{|i|}{b} \right) - \frac{w}{w_c} \right]$$  \hspace{1cm} (3.12)

and ON switching:

$$\dot{w}_{ON} = f_{ON} \sinh \left( \frac{i}{i_{ON}} \right) \exp \left[ -\exp \left( \frac{w - a_{ON}}{w_c} - \frac{|i|}{b} \right) - \frac{w}{w_c} \right]$$  \hspace{1cm} (3.13)

with fitting parameters: $f_{OFF} = 3.5 \pm 1 \mu m/s, f_{ON} = 40 \pm 10 \mu m/s, i_{OFF} = 115 \pm 4 \mu A, i_{ON} = 8.9 \pm 0.3 \mu A, a_{OFF} = 1.2 \pm 0.02 nm, a_{ON} = 1.8 \pm 0.01 nm, w_c = 1.07 \pm 0.003 \AA, b = 500 \pm 80\mu A$. Figures 3.5a and 3.5c show the time series fits to these dynamical expressions as solid curves, indicating that they represent the data accurately and thus qualify as a predictive compact model. Figures 3.5b and 3.5d show the numerical time derivatives of the time series plotted against the instantaneous values of the barrier width, and demonstrate the agreement between the form of the model and the data set.

These nonlinear functions of $i$ and $w$ were determined ad hoc through a combination of physical insight from theoretical analyses and trial-and-error modifications. For the dynamics fitting, at each step of the outer regression, we numerically solved Equations 3.12 and 3.13 using the Runge-Kutta method as implemented in IGOR Pro software for each $w$ time series. At each time step in the numerical integration, we explicitly used the experimentally measured current from the four-wire data for that stress test, to account for the fact that the current changes during the switching process. These experimental internal voltages $v(t)$ and the currents $i(t)$ are shown in Figure 3.6 for OFF switching in (a) and (b), and for ON switching in (c) and (d).

The memristive model embodied by Equations (3.4), (3.3), (3.12) and (3.13) is a predictive formulation for gaining intuition into these strongly nonlinear dynamical systems. As examples, two quantities of interest, the time and the energy required to switch a device between two arbitrary states, can be computed from Equations 3.12 and 3.13 for times that were not experimentally accessible. Figure 3.7 shows the switching time and energy as a function of constant applied current, calculated by numerical integration of
Figure 3.5: The stress-test protocol yields time series data for the state variable of the conduction model, $w$. The experimentally inferred evolution of $w$ as a function of total time under stress is shown as markers for OFF switching in (a) and ON switching in (c). There is a significant dependence of the switching rate on the applied external voltage of the stress pulses. (b) and (d) respectively show the numerically differentiated time series of (a) and (c), from which an analytical form of the dynamical memristive equation can be obtained. The analytical dynamical models of Equations 3.12 (for (a) and (c)) and 3.13 (for (b) and (d)) are plotted as solid lines. The lines show discontinuities because the dynamical fitting procedure uses measured current values which also changes during switching.
Figure 3.6: Although the external voltage is kept constant during the entire stress-test protocol, the actual internal voltages and currents passing through the device during the stress steps do not remain constant because of the changing device impedance and its interaction with the electrode as a load line. As such, an accurate memristive model can only be constructed if the real currents and/or voltages of the stress pulses are measured and fed into the fitting process. Here we show the measured voltages (a, OFF) and (c, ON) and currents (b, OFF) and (d, ON) which correspond to the stress tests of Figure 3.5. The currents and voltages change by up to a factor of 2, a fact which highlights the necessity of measuring time-sampled stress data to fully understand the memristive dynamics.
Figure 3.7: Calculations of switching time and energy using the memristive model. Constant-current magnitude switching times and energies are presented for ON- and OFF-switching events. The ON and OFF states were chosen as $w_{ON} = 1.2 \text{ nm}$ and $w_{OFF} = 1.8 \text{ nm}$ to reflect a resistance switching ratio of 500. The plots were evaluated by numerical integration of Equations (3.14) and (3.15). These results demonstrate the asymmetry between the on and off switching behavior and show that the switching energy decreases exponentially with the applied current because of the highly nonlinear switching dynamics.

the following formal expressions between the limits $w_{ON} = 1.2 \text{ nm}$ and $w_{OFF} = 1.8 \text{ nm}$ for both ON and OFF switching:

$$\Delta t = \int \frac{dw}{\dot{w}(i, w)}$$

$$E = \int \frac{iv(w)dw}{\dot{w}(i, w)}$$

(3.14)
(3.15)

The series resistances of the wires is not included in this calculation of the switching energy since they are external to the device and it is in principle possible to effectively eliminate them with short wires in an integrated circuit. These simulations show that the switching time and energy decrease exponentially with increasing applied current, a counterintuitive property that is due to the nonlinearity of the governing differential equations. Additionally, the asymmetry between OFF and ON switching is clearly ob-
served, a property that must be accounted for in circuit designs that utilize TiO$_2$-based memristive systems.

### 3.6 Discussion and conclusion

These results confirm the picture that is emerging of the structure of an electroformed metal-oxide memristive device, as illustrated by Figure 3.3. In this model the electro-forming process creates a localized conducting channel that extends most of the way across the 50 nm titanium dioxide film, leaving a $\sim 2$ nm wide insulating gap. The state variable of the device $w$ is the effective width of the insulating gap, and the electrical current transport process is limited primarily by tunneling through this gap, represented in Equations (3.3) and (3.4) by the simplified Simmons tunneling equation in series with the Ohmic conduction channel. $w$ is changed by an applied voltage, with a positive bias applied to the top electrode pictured in Figure 3.3 leading to an increase in the state variable $w$ and a corresponding exponential increase in the resistance of the device. A negative bias leads to a decrease in $w$ and a corresponding exponential decrease in resistance. This bipolar behavior is in agreement with the identification of the mobile dopants in the gap being positively charged oxygen vacancies [58]. Switching between selected OFF and ON states with resistance ratios of approximately 500 is accomplished by changing the width of the tunneling gap by less than one nanometer. A completely independent analysis of similar devices by the technique of pressure-modulated conductance microscopy [51] yielded similar results in terms of the sub-nanometer change of the width of a tunneling gap during switching.

The switching dynamics are complex but are reproduced well by the phenomenological differential equations (3.12) and (3.13), the physical basis of which can be understood qualitatively. The $\sinh(i/i_0) \exp[-w/w_c]$ dependence of the switching rate may have two contributions: a nonlinear drift at high electric fields [43, 80] and local Joule heating of the junction that speeds up the thermally activated drift of oxygen vacancies [24, 52]. A similar exponential dependence of switching rate on applied voltage has been reported by Tamura et. al [81] in cation migration based sulfide bipolar switches, which they attributed to device self-heating. Both effects produce similar behavior and are likely present simultaneously; the nonlinearity of either effect could account for the observed storage to switch time ratio of greater than $10^{13}$.

The absolute rates of OFF- and ON-switching were observed to be dramatically different, with the OFF-switching several of orders of magnitude slower than ON-switching for an equivalent applied voltage. This behavior was previously attributed to the interaction of diffusion and drift in a net internal electric field [44]. For a positive bias applied to the top electrode of Figure 3.3, positively charged oxygen vacancies are repelled toward the conducting channel, and thus the insulating gap width $w$ increases. This increases the concentration of the vacancies near the channel and results in both an increased vacancy diffusion current acting in the opposite direction to the drift by Fick’s Law and also an
internal electric field opposite to the applied field, which slows down the vacancy drift. Eventually, the total drift velocity goes to zero, and there is a bias-dependent maximum value that \( w \) can attain. However, when a negative bias is applied to the top electrode in Figure 3.3 the externally applied field, the internal field of the concentrated vacancies and the diffusion all act in the same direction, thus dramatically speeding up ON-switching compared to OFF-switching for the same applied voltage.

We have introduced and utilized a test protocol that explicitly maps the time evolution of state to analyze the behavior of a dynamical electronic device. We have determined a compact memristive model for an electroformed TiO\(_2\) bipolar switch that utilizes the Simmons tunneling equation for the static transport expression, the width of the tunnel gap in the device as the state variable, and a phenomenological differential equation for the dynamical expression. The model provides a physical picture of the transport, imparts significant insight into the device dynamics, and enables the switching properties to be predicted over a wide range of operating currents and times.
Chapter 4

Two state variable metal-insulator transition systems

The literature on conduction phenomena in metal-oxide-metal systems is often confusing because the word 'switching' is used indiscriminately for two very different phenomena: memristance, or nonvolatile resistance change, and negative differential resistance (NDR), which causes current-voltage oscillations. The confusion is compounded because both phenomena are independently reported in seemingly identical samples and there are many different physical mechanisms proposed for both. Here we present an analytical model that describes each effect in terms of independent properties of the same material system: dynamical memristance based on the drift of charged dopants in a semiconductor, and instantaneous NDR based on a metal-insulator transition (MIT). We experimentally demonstrate that both phenomena can be simultaneously realized in a single nanoscale device, and that this device can be used as a continuously tunable voltage-controlled oscillator. We derive a new state-variable treatment that provides quantitative insight into oscillation dynamics driven by a MIT instability.

Memristive devices are nonlinear dynamical systems [75] that exhibit continuous, reversible and nonvolatile resistance changes that depend on the polarity, magnitude and duration of an applied electric field. The memristive properties of thin film metal oxide materials systems were discovered [3, 2] in the 1960s and studied without reaching a consensus [82, 4, 83] on the physical mechanism until recently. Recent studies on the mechanism revealed that memristive switching is due to electric field-driven motion of charged dopants which define the interface position between conducting and semiconducting regions of the film [19, 24, 57, 41, 50, 58]. In titanium dioxide, a prototypical system, independent researchers have recently shown [30, 31] that two different phases are present in electroformed devices: a metallic Magnéli phase Ti$_4$O$_7$ [84, 70] (an ordered solution of oxygen vacancies in rutile [72]) and a stoichiometric semiconducting TiO$_2$ polymorph. The Ti$_4$O$_7$ can act as a source or sink of oxygen vacancies, donors in TiO$_2$, which are injected into or withdrawn from the TiO$_2$ layer thus modulating the width of the semiconducting region. This Magnéli phase inclusion can be produced by electrofor-
mation via localized reduction of TiO$_2$ or controllably grown as an oxygen poor layer in a device structure [28].

There have been many reports of current-controlled NDR (CC-NDR) in thin film metal-oxide-metal (MOM) devices since the early 1960s (e.g. binary oxides of V [85, 86, 87, 88, 89], Nb [90, 91], Ta [92], Ti [92, 93, 94, 95] and Fe [96]) but, like memristance, there have been many proposals for the physical mechanism of the NDR in the literature. The more recent work of Chudnovskii et al. [97] and Kim et al. [98] presents persuasive evidence that CC-NDR is always due to a Joule-heating induced metal-insulator transition (MIT) in binary oxide films of V, Nb, Ti and Fe. Electroforming is often a prerequisite for CC-NDR in these oxides. This treatment can chemically reduce an initially fully oxidized film to form a localized channel of a partially-reduced mixed-valence phase that exhibits MIT. MITs arise because of competing ground states in correlated electron systems and are common in transition metal oxides[99]. An MIT can be induced in a two-terminal MOM device at fixed ambient temperature by passing sufficient current through it to cause local Joule heating, a feature first intentionally demonstrated in vanadium oxide [85, 86]. In these devices, a discrete drop in resistivity, which occurs when the device self-heats past the critical MIT temperature, has an unstable positive feedback effect on the current. This results in the formation of a metallic phase conductive filament [87, 88], a necessary condition [100] of bulk CC-NDR.

Here we present an analytical model for and demonstrate the controllable coexistence of memristance and a MIT-driven CC-NDR in a single nanoscale TiO$_2$-based MOM device. We show that the coexistence of both phenomena yields a rich behavior described by two state variables, one dynamical and one instantaneous. We analyze the electrical oscillations that arise from the CC-NDR of the device in order to characterize the dynamics of the MIT. Finally, we demonstrate an interesting application of such a device: a tunable voltage-controlled oscillator with efficiency greater than 1% capable of injecting AC energy into nanoscale oxide-based circuits.

4.1 Description of Models

As shown in Figure 4.1a, we have observed that electroformed titanium dioxide MOM devices will frequently exhibit both memristance and CC-NDR when immersed in liquid He. Based on the conclusions of previous authors [85, 86, 97, 98], we hypothesized that the low temperature CC-NDR effect was due to a Joule heating controlled MIT in the electroformed channel of the device. This hypothesis was reinforced by the recent observation that the electroformed channel in similar devices was composed of the Magnéli phase Ti$_4$O$_7$ [30, 31], which is known to exhibit a metal-insulator transition at 155 K [71, 101, 79].

In this picture, there are two physical state variables that describe the device behavior: (a) for the memristance, the width $w$ of the highly resistive TiO$_2$ layer that is essentially free of vacancy dopants and (b) for the CCNDR, the normalized radius $u$ of the metallic
Figure 4.1: Current-voltage behavior and model schematic. (a) Room temperature and liquid He temperature switching I-V curves of a device on sample A that exhibits memristive switching at both temperatures and CC-NDR at low temperature. (b) and (c) Schematics and (d) equivalent circuit illustrating the thermal and electrical conduction models we use for a memristive MIT device.
phase within the Ti_4O_7 channel. Schematic diagrams and an equivalent circuit of this model are presented in Figure 4.1. The width \( w \) of the resistive layer is essentially static (the memristance state is nonvolatile) in the absence of large applied fields at normal temperatures, but it can be changed dynamically (in other words, the amount of change depends explicitly on the time duration[53]) by the application of electric fields that result in currents greater than 100 \( \mu \)A in the devices studied here. The radius of the MIT boundary is volatile, since it depends on the instantaneous power dissipated in the channel as well as the ambient temperature, but generally results in CC-NDR current thresholds of 5-10 \( \mu \)A in these devices.

### 4.1.1 Memristive barrier model

The conduction behavior of the memristive barrier is now considered in order to have a complete model for device transport across the range of experimental temperatures and currents. Although there is broad agreement that the memristance of oxides is due to vacancy transfer between an insulating and conducting region, the exact state parameter that changes in the insulator when it is partially reduced is still under debate. There are two state parameters that are typically invoked: insulating barrier height [45] or barrier width [53, 52, 44, 51] modulation. As discussed in the previous chapters, we believe that width modulation is the more likely case.

The state variable formulation for the memristive system (now included within the previously more restrictive term ‘memristor’) introduced by Chua and Kang[75] is especially useful for both understanding the physical behavior of the device and for constructing compact models, such as for SPICE, to enable accurate circuit simulations. This approach utilizes two coupled equations, the instantaneous conduction equation (Equation 4.1) to relate the current and voltage at any particular instant as a function of a state variable or variables \( w \), and the dynamical equation (Equation 4.2), which is written in differential form to explicitly reveal the time (or charge or flux) dependence of the state variable:

\[
v = \frac{i}{G(w,i)} \tag{4.1}
\]

\[
\dot{w} = f(w,i) \tag{4.2}
\]

In the previous chapter we presented a detailed description of the electrical measurements required to characterize a memristor and the analytical model we obtained for \( w(t) \). We apply the same model here to describe the memristive barrier in series with an MIT material, but with a small modification. Because we examine the devices in this chapter over a very broad range of temperatures, here we modified the conduction equation to incorporate a thermally activated leakage current in parallel with the tunnel barrier. This behavior more accurately reflects temperature dependence of the conductivity and is consistent with previous studies on conduction through thin TiO_2 films [102].
For calculation purposes, we used the following phenomenological form for the insulator leakage:

\[ i_{\text{leak}} = \alpha \sinh \left( \frac{v_{\text{mem}}}{\beta} \right) \] (4.3)

which has a thermally activated conductance dictated by:

\[ \alpha = \beta G_a \exp \left( -\frac{E_a}{k_b T_{\text{amb}}} \right) \] (4.4)

Here the parameters \( \alpha \) and \( \beta \) control the conductivity while \( G_a \) and \( E_a \) are determined by the thermal activation behavior. \( v_{\text{mem}} \) is the voltage dropped on the memristive barrier. In parallel to the leakage pathway, we use the following empirical form of the Fowler-Nordheim equation\[103\] to describe the tunneling behavior of the device exhibited at high field:

\[ i_{\text{tun}} = C v^2 \exp \left( -\frac{B}{v_{\text{mem}}} \right) \] (4.5)

with \( C \) and \( B \) representing the parameters that control the tunneling behavior, since in this case the state of the memristor is fixed for any given set of measurements.

The five TiO\(_2\)-related conduction parameters (\( \beta, G_a, E_a, C \) and \( B \)) that are dictated by material properties in this device can be inferred from the current-voltage-temperature (I-V-T) sweeps. The I-V behavior at low voltage and moderate temperature is dominated by leakage because in this regime tunneling is less important and the channel is still metallic and highly conductive. Thus, the leakage parameters \( G_a \) and \( E_a \) can be determined by fitting to an Arrhenius plot of the low voltage conductivity (\( G_0 \)) as a function of temperature. As shown in Figure 4.2, this process yields an activation energy of 58 ± 2 meV with a prefactor of 1.6 ± 0.2 mS. The phenomenological nonlinearity parameter \( \beta \) is obtained by inspection of the voltage at which conduction deviates from linearity in the leakage dominated regime. This occurs at roughly 130 mV, so we take this as the value of \( \beta \). The Fowler-Nordheim parameters are obtained by least-squares fitting of the full conduction model to the \( i-v-T \) dataset above the metal-insulator transition temperature, where the channel resistance does not have a significant impact on the \( i-v \) shape. This procedure yields the following values for the parameters: \( C=(1.2 \pm 0.7) \times 10^7 \) A/V\(^2\) and \( B = 9.4 \pm 0.4 \) V. Note that these parameters depend on the memristive state of the device which changes in time under the application of large currents.

### 4.1.2 Metal-insulator transition instability model

When the ambient temperature was below the MIT temperature, the Ti\(_4\)O\(_7\) channel was modeled as a two-phase system of length \( L \) consisting of a warm metallic core (with radius \( r_{\text{met}} \) and resistivity \( \rho_{\text{met}} \)) surrounded by a cool insulating shell (with outer radius \( r_{\text{ins}} \) and resistivity \( \rho_{\text{ins}} \)). This model is a 3D generalization of previous models for planar-geometry CC-NDR MIT devices\[87\] and conforms with the thermodynamic condition
Figure 4.2: Arrhenius plot of the low voltage conductivity, which is used to extract the conduction parameters for the thermally activated leakage current. There is some deviation from ideal behavior because of the presence of multiple conduction mechanisms in the device, but an approximate form is sufficient for device modeling.

That CC-NDR must result from locally conductive filaments[100] oriented parallel to the current flow. In this picture, the thermal environment is cylindrically symmetric and heat flow parallel to the channel is neglected. Since the resistance in the insulating regime is high, we assume that the power dissipated within the shell provides negligible heating. We also assume that the heat capacity of the nanoscale volume is sufficiently small that the thermal profile is always in a steady state on the experimental time scales, an assumption validated by results presented later. These assumptions allow us to use the source-less heat equation to determine the temperature profile within the insulating shell:

\[
\frac{\partial}{\partial r} \left( r \frac{\partial T}{\partial r} \right) = 0 \tag{4.6}
\]

in the domain

\[
\text{met} \leq r \leq \text{chan}. \tag{4.7}
\]

For the first (Neumann) boundary condition, we assume that Joule heat generated in the metallic core flows radially through the insulating shell, which results in the following heat flux boundary condition, with \( \kappa \) being the effective thermal conductance of the insulator:

\[
\left. \frac{\partial T}{\partial r} \right|_{r=r_{\text{met}}} = -\frac{-r^2 \rho_{\text{met}}}{2\pi^2 \kappa r^3_{\text{met}}} . \tag{4.8}
\]

For the second (Dirichlet) boundary condition, we assume that the temperature is clamped
to ambient at the edge of the channel: \( T(r_{\text{chan}}) = T_{\text{amb}} \). Combining the differential equation with the boundary conditions yields a complete expression for the temperature profile. The radius of the metallic core can then be found in terms of the fixed parameters of the system by recognizing that the phase boundary occurs at the point where the temperature is equal to the MIT temperature, \( T(r_{\text{met}}) = T_{\text{MIT}} \).

We now introduce the reduced radius state parameter \( u \) which acts as a simple way of visualizing the instantaneous position of the phase boundary for a given ambient temperature and current.

\[
u(i, T_{\text{amb}}) := \frac{r_{\text{met}}}{r_{\text{chan}}} \tag{4.9}\]

Solution of the above ordinary differential equation and boundary conditions is straightforward and, when combined with the definition for \( u \) yields the transcendental solution:

\[
u^2 \left( \ln \frac{1}{u} \right)^{-1} = i^2 \rho_{\text{met}} \frac{2\pi^2 \kappa r_{\text{chan}}^2 (T_{\text{MIT}} - T_{\text{amb}})}{A} \tag{4.10}\]

Using a temporary simplification for the right hand side,

\[
A = \frac{i^2 \rho_{\text{met}}}{2\pi^2 \kappa r_{\text{chan}}^2 (T_{\text{MIT}} - T_{\text{amb}})} \tag{4.11}\]

Equation 4.10 can be rearranged algebraically to:

\[-2 \ln u \exp(-2 \ln u) = \frac{2}{A} \tag{4.12}\]

This expression is invertible by using the transcendental Lambert W function which satisfies

\[
W(z) \exp([W](z)) = z \tag{4.13}\]

Equation 4.12 can be inverted to

\[
W \left( \frac{2}{A} \right) = -2 \ln u \tag{4.14}\]

or

\[
u = \exp \left[ -\frac{1}{2} W_0 \left( \frac{4\pi^2 \kappa r_{\text{chan}}^2 (T_{\text{MIT}} - T_{\text{amb}})}{i^2 \rho_{\text{met}}} \right) \right] \tag{4.15}\]

The argument of the W function here is always real and positive which restricts the domain such that we only need to consider the single valued positive branch of the Lambert W function, denoted \( W_0 \). It is easy to see from this form of the \( u \) function that \( u \) is bounded between 0 for small currents and 1 for large currents, an intuitively necessary constraint on the model.

Corless et al. [104] have provided a detailed description and fascinating history of the Lambert W function. For real values \(-1/e < z < 0\), Equation 4.13 yields a curve that
is double-valued. In order to define functions, the curve is broken into two parts, $W_0(z)$ for $W(z) > -1$ and $W_{-1}(z)$ for $W(z) < -1$. Thus, the Lambert W function turns what can be a time-consuming numerical solution of a differential equation or a laborious expansion in basis functions, such as Bessel functions for the cylindrically symmetric heat equation, into a simple analytical form. Many popular computer mathematics packages include $W_0(z)$ and $W_{-1}(z)$ as standard functions. The Lambert W function provides convenient analytical solutions to a wide variety of problems besides CC-NDR, including combinatorial applications, iterated exponentials, linear constant-coefficient delay equations, population growth, epidemics and many other applications. Thus, the mathematical formalism for CC-NDR shares common ground with many other fields, and the further theoretical development may benefit from analyzing the mathematical advances that have grown out of these other applications.

Using Equation 4.15, the total conductance of the MIT material has a simple analytical form when $T_{amb} < T_{MIT}$:

$$G_{chan}(i, T_{amb}) = \frac{\pi r^2_{chan}}{L} \left( \frac{u^2}{\rho_{met}} + \frac{(1 - u^2)}{\rho_{ins}} \right)$$

which is nonlinear in current and temperature and results in the emergence of CCNDR below $T_{MIT}$. In this case, the resistance of the $\text{Ti}_4\text{O}_7$ channel is a function of the state variable $u$, but unlike the dynamical state variable $w$ of the memristive barrier, $u$ is not an explicit function of time; thus the CC-NDR state is volatile and we call $u$ an instantaneous state variable. In this model, $u$ is fixed to unity when the ambient rises above the MIT temperature. The values of the parameters required in this model can be estimated from the geometry of the device and from the materials literature: $\rho_{met} = 3 \times 10^{-6} \Omega \cdot m$, $\rho_{ins} = 3 \times 10^{-3} \Omega \cdot m$ and $T_{MIT} = 155$ K. We assume that the channel is essentially the size of the device and that it bridges most of the oxide film thickness, so we take $r_{chan} = 25$ nm for sample A, $r_{chan} = 50$ nm for sample B and $L = 25$ nm for both.

In the absence of literature values for the thermal conductance of the insulating phase of $\text{Ti}_4\text{O}_7$, we estimate an average value of $\kappa = 1.5$ W m$^{-1}$ K$^{-1}$ for the range of temperatures from 77-300 K based on the thermal conductivities of sputtered TiO$_2$ films reported by Lee et al. [105]. Because of its simplicity and the analytical nature of this model, it can be easily incorporated into a SPICE time-dependent circuit simulation package, allowing accurate simulations of circuits incorporating the device, including oscillating behavior.

### 4.2 SPICE model for time domain simulations

We implemented our analytical thermal and conduction models in SPICE in order to build an equivalent circuit for the experimental test setup and perform transient oscillation simulations. The first step was to build a subcircuit element that reproduces the full device model, which includes both the thermal and electronic conduction components. The thermal model was implemented in the subsystem labeled “LambertW calculation.
Figure 4.3: SPICE schematic of the memristive NDR element subcircuit, which incorporates both the thermal Joule heating model (instantaneous state variable) and the electronic conduction model.

circuit”, which uses a piecewise linear voltage-controlled source (element EW) to compute the Lambert $W_0$ function. The resistor (RW2) and capacitor (C1) at the output of the $W_0$ function are added to help the stability of computation in SPICE and are not part of the physical model. These components force the state variable $u$ to be continuous in time, otherwise $u$ would jump discontinuously, causing convergence problems in the SPICE simulator. The $RC$ time constant of 1 ns was chosen to be faster than the time resolution of our experiments, so that this computational aide would not perturb the simulation compared to the experimental time scales.

The conduction model was incorporated into the SPICE circuit by including four arbitrary behavior current sources (BRins, BRmet, Bleak, Btunnel) to account for the four conduction mechanisms: Ohmic conduction in the two parts of the electroformed channel (warm metallic and cool insulating) to simulate the CC-NDR, as well as the nonlinear leakage and tunneling currents across the memristive barrier. We additionally added some independent output channels for monitoring the internal state variable $u$ throughout the circuit operation.

In order to understand and simulate the oscillatory behavior of the device at $T_{amb} = 4$ K, we placed the memristive NDR subcircuit described above in a broader SPICE model designed to be equivalent to the test circuit that we used to characterize the device. We tested the device in four-wire configuration with a DC source attached to one side of the top electrode through a series resistor (Rext), two 1 MΩ input impedance oscilloscope channels attached respectively to one side of the top and bottom electrodes, and a 50 Ω input impedance channel attached to one side of the bottom electrode. This enabled
us to measure the true voltage across the device and the current through the device in real time. The series resistor Rext acted as the loadline, which is necessary to obtain oscillation from CC-NDR circuits.

Attaching the 10 feet of cable from the scope to the bottom of the He Dewar added a parasitic capacitance, which must be incorporated into the model to understand the oscillations since it is this capacitance that stores and supplies charge during oscillation. The capacitors in the simulation circuit (CcableN, N=1-4) are used to model the parasitic cable capacitance, the value of which was measured with an impedance meter. The final components of the test circuit that need to be accounted for are the resistances of the nanowire electrodes. We measured the total resistance of the wires from end to end before measuring the oscillation behavior and, since the wires cross roughly at their half-way points, placed half the value on either side of the memristive NDR element for simulation (RelectN N=1-4). In order to demonstrate that a capacitance external to the device was determining the oscillation period, we attached a 10 nF capacitor at the source (Cext) and performed an additional simulation.

4.3 Transport and switching characterization

In order to study the coexistence of memristance and MIT in titanium oxide, we fabricated two sets of crossbar-geometry MOM devices with a three-step process. First,
we patterned 3 nm Ti/9 nm Pt metal bilayer bottom nanowire electrodes with a liftoff-based nanoimprint lithography process. Second, we sputter-deposited a 30 nm thick blanket layer of amorphous TiO$_2$. Finally, we patterned 12 nm thick Pt top nanowire electrodes perpendicular to the bottom electrodes. The two sets of samples were identical except for the length and width of the nanowire electrodes. Sample A had 50 nm wide, 300 µm long wires ($R_s = 30$ kΩ), while sample B had 115 nm wide, 100 µm long wires ($R_s = 2$ kΩ). In this study, we used the two different wire geometries in order to control the nanowire resistance between the contact pads and the MOM device. The large wire resistance of sample A quenched CC-NDR oscillations, and thus it was possible to characterize the quasi-static current-voltage ($i - v$) curve in the NDR regime. The small series resistance of Sample B was used to allow free-running oscillations.

In order to characterize the temperature dependence of CC-NDR in the devices, we collected current-voltage-temperature ($i - v - T$) data for both the memristive ON and OFF states in multiple devices of sample A. We performed the quasi-DC ($i - v - T$) characterization using an Agilent B1500 Semiconductor Device Analyzer. Temperature was controlled by either a liquid nitrogen cooled sample-in-vacuum cryostat for temperature sweeps between 78 K and 300 K or by immersion in liquid He to obtain data at 4.2 K. We eliminated the electrode series resistance from our measurements by connecting the device in a four-wire geometry. In this configuration, we applied voltage to one end of the top electrode, grounded and measured current at one end of the bottom electrode, and measured the voltage across the device by probing voltage at the opposite ends of each wire. Before exhibiting memristance or CC-NDR, these devices required a pulsed electroforming step of +5V for 10 µs, which was performed with the B1500 pulse generator. For the CC-NDR datasets presented here, we used an applied current sufficiently low to ensure that no memristive switching occurred during an entire $i - v - T$ sweep. We checked this condition by sweeping the current up and down at each temperature and the temperature down and up for each experiment and making sure that we saw no hysteresis. We changed memristive states by pulsing the device with +5 or -5 V for 10 µs at room temperature in between $i - v - T$ sweeps.

A representative $i - v - T$ dataset for the memristive ON state is included in Figure 4.5a. Two qualitative features are evident: (a) the conductivity around zero bias, $G_0$, is thermally activated and (b) there is a critical temperature at which CC-NDR initiates. The second feature is more obvious when the $i - v$ data are numerically differentiated to obtain the differential resistance $dV/dI$, which is plotted as a function of current and temperature in Figure 4.5b. We observed a CC-NDR critical temperature between 150-160 K on four separate devices, which were driven to both the memristive ON and OFF states. This critical temperature is due to the onset of the MIT in the Ti$_4$O$_7$ channel, which has a reported transition temperature in the range 150-155 K[71, 101, 79]. This conclusion is consistent with the experiments reported by Chudnovskii et al.[97] on MIT related CC-NDR and the recent observation by Kwon et al.[30], who observed an MIT (albeit without reporting CC-NDR) in a formed Ti$_4$O$_7$ channel that bridged the two electrodes of an MOM device. Two other devices displayed CC-NDR critical
temperatures at about 120 K; it is possible that the electroforming process resulted in a crystalline inclusion of the Magnéli phase Ti$_5$O$_9$, which has been reported to exhibit an MIT at 120 K\cite{79}.

With the model described above, we calculated the $i - v - T$ behavior of the devices, and compare the experimental results for the device of Figs. 4.5a and 4.5b to the model results of Figs. 4.5c and 4.5d. The agreement between the model and experiment is notable. Qualitatively, the shape of the CC-NDR $i - v$ curves (which is primarily determined by the Lambert W function in the model) match extremely well, and quantitatively, the values of the differential resistance and the positions of the inflection points in the $i - v$ curves are accurate. Thus, the instantaneous state variable $u$ is appropriate for quantitatively understanding the origin of CC-NDR in MIT oxides.

### 4.4 Characterization of the MIT oscillator

Along with the first independent reports of CC-NDR in MOM devices\cite{90, 91}, Chopra additionally reported the observation of free-running relaxation oscillations. A concise theoretical treatment of CC-NDR-based relaxation oscillators by Shaw et al.\cite{106} demonstrated that an appropriate bias applied to a parallel connection of any CC-NDR device and a reactive element will behave as a van der Pol oscillator. Oscillations are frequently reported in studies of CC-NDR devices, because in most electrical test configurations there is sufficient parasitic capacitance in the cabling to meet the necessary conditions.

Here we utilize these oscillations and our analytical model to characterize the dynamical behavior of the MIT phase transformation and apply the results to demonstrate continuously-tunable voltage controlled oscillators. Figure 4.6a displays a typical experimental output voltage waveform for devices on sample B when $V_{DC} = 0.74$ V. The frequency was partly controlled in this experimental configuration by the parasitic capacitance of the 10 ft long cables (with parasitic capacitance $\sim 650$ pF) that connected the device at the bottom of the He Dewar to the electronic test equipment. When a 10 nF capacitor was added to the test circuit after the source, the oscillation period increased. Figure 4.6b displays a SPICE simulation of the voltage output using the analytical model presented above placed in an accurate equivalent circuit for the experimental setup (see below for details of the SPICE implementation). The observed oscillatory behavior was quantitatively reproduced with the SPICE model.

The SPICE simulation reveals important information about the dynamics of the MIT transition. As shown in Figure 4.6c, the MIT state variable $u$ jumps nearly instantaneously at the crest of the voltage wave when the parallel capacitor changes from charging to discharging. This change occurs because the MOM device is driven to a voltage that corresponds to the lower inflection point of the 'S' on the NDR curve. Since the voltage on the capacitor must remain continuous, the current, and consequently $u$, jumps effectively discretely. Although there is a finite time required for the temperature increase and phase transformation to occur ($u$ must be continuous), a current transient
Figure 4.5: Experimental and theoretical current-voltage-temperature results. (a) Temperature dependent current voltage ($i - v - T$) measurements performed on a device from sample A in the memristive ‘ON’ state. The emergence of current-controlled negative differential resistance (CC-NDR) is apparent as the device is cooled. (b) Numerically differentiated ($dV/dI$) data from (a) showing the current and temperature dependence of the differential resistance. The critical temperature for the observation of CC-NDR coincides with the metal-insulator transition temperature of the expected channel phase Ti$_4$O$_7$ ($T_{MIT} = 155$ K). (c) and (d) Temperature dependent current-voltage calculations for this device using the analytical instantaneous state-variable model of Eqs. 4.15 and 4.16 plotted for comparison to the experimental data of (a) and (b), respectively.
Figure 4.6: Oscillation characterization of MIT instability. (a) Measured oscillations from a device on sample B under DC voltage with the relaxation capacitance provided by the background capacitance of the measurement cables (red) and an added 10 nF capacitor (blue). (b) SPICE simulation of the oscillations using the analytical memristive metal-insulator transition model attached to a circuit equivalent to the experimental setup. (c) The corresponding oscillations of the MIT state variable $u$ from the simulations. (d) Measured current oscillations from the device, which should exhibit abrupt jumps if $u$ is an instantaneous state variable on the experimental time scale. (e) A zoom on the current waveform shows that the transition time is less than or equal to the 2 ns measurement resolution of our test setup.
measurement during an oscillation is the best way to check our assumption that this time dependence is negligible on the experimental time frame. Figures 4.6d and 4.6e show that the current transients at the inflection points of oscillation are less than or equal to the time resolution of our test setup, 2 ns.

This upper limit on the current transition time is important for two reasons. First, it directly demonstrates that the nanoscale volume of these memristive devices can be heated at least 150 K above ambient temperature in the nanosecond time frame. This is an important issue for understanding switching dynamics independent of the MIT effect, because local Joule heating can also play a role in memristive switching speeds. Second, it allows us to calculate an upper limit on the volume ($Vol$) of the Ti$_4$O$_7$ region by using the measured power, $P$, and literature values of the average specific heat ($c_p = 30 \text{ cal/mol K}$)[101], enthalpy of transformation ($h=563 \text{ cal/mol}$)[101] and the molar volume ($\nu=70 \text{ cm}^3/\text{mol}$)[70] with the relation:

$$Vol = P \cdot \Delta t \frac{\nu}{h + c_p \Delta T}$$  \hspace{1cm} (4.17)

which yields $Vol = 5 \times 10^{-17} \text{ cm}^3$, corresponding to a 25 nm long cylinder with a radius smaller than 25 nm, consistent with our model.

The efficiency of the oscillator can be defined as the ratio of the rms AC power coupled to a load to the total power input by the DC source. In the experimental measurements shown in Fig. 4.6, the load was the 1 MΩ input impedance of the oscilloscope that was used to measure the oscillations. Using the SPICE model to calculate the DC/AC efficiency and comparing it with the experimental data yielded a value of 0.05% when the load was 1M. However, this load impedance is poorly matched to the device and the efficiency can be increased to 1.3% if the load were reduced to 40 kΩ in a circuit.

### 4.5 The configurable voltage-controlled oscillator

We observed that the frequency and amplitude of the oscillations were dependent on both the applied DC voltage and the memristive state of the device. In order to demonstrate a simple application of the two state variable MOM nanodevice, we studied the oscillatory behavior of a single device on sample B that was configured into different memristive states. The results, shown in Figure 4.7, demonstrate that for a given memristive state, $w$, there is a characteristic curve that relates the CC-NDR driven oscillation period to the applied DC voltage. The memristive state can be pushed back and forth with a large applied voltage (5 V), which changes the voltage threshold for CC-NDR since more or less voltage is dropped on the series insulating barrier. Thus, by changing $w$ the characteristic curve is shifted back and forth along the $V_{DC}$ axis in a continuous manner, since $w$ is continuously tunable. The presence of two controllable state parameters, one instantaneous and one nonvolatile, along with the small-signal gain of the CC-NDR region, provides a range of possible applications for this type of MOM nanodevice.
Figure 4.7: Tunable characteristics of a memristive oscillator. The oscillation period of the device is dependent on the DC operating point applied to the circuit and exhibits a characteristic curve with low and high cutoff voltages. This characteristic curve can be continuously tuned back and forth by modulating the memristive state variable $w$.

4.6 Conclusion

We have derived a simple analytical model and experimentally demonstrated a two-state-variable, two-terminal metal oxide nanodevice. The two state variables correspond to a dynamical memristive film thickness perpendicular to current flow and an instantaneous MIT boundary parallel to current flow, with in this case Ti$_4$O$_7$ acting as the source/sink of mobile dopants for the semiconductor film and providing the MIT. The coexistence of memristance and an MIT in an MOM nanodevice provides rich electrical behavior, including small-signal gain and oscillations with a continuously tunable threshold. We expect that this class of device can be fabricated with different materials systems to provide CC-NDR at room temperature, and that applications could include a variety of reconfigurable AC circuits.
Chapter 5

Circuit applications of titanium dioxide memristors

Regardless of the particular material or switching mechanism, memristive devices have a broad range of possible circuit applications due to their ability to store information over time in a nonvolatile fashion and the possibility of extremely large scale integration [14, 107]. The most straightforward application is an ultra-dense crossbar memory [18] with information stored in the form of a nonvolatile resistance value. Because memristive devices are fabricated from simple metal-oxide-metal structures which do not require a particular substrate for fabrication, the devices can be integrated on top of CMOS electronics during the back-end of the line process [108]. This property enables multiple layers of devices to be stacked in 3 dimensions and consequently, new approaches to memory topology [109]. In addition to nonvolatile memory blocks, nanoscale memristive crosspoints can be used for reconfigurable CMOS wiring in dense field programmable gate arrays (FPGAs) [110, 111], self-programming logic circuits [112] and circuits which perform nonvolatile stateful logic operations [113]. A longer-term goal is to employ memristive devices as the synaptic weight component of neuromorphic circuits [114, 115, 116].

In this chapter we experimentally demonstrate two of the many possible applications of titanium dioxide memristors. First we show the construction and operation of a nonvolatile latch which can potentially be used to store the entire state of a microprocessor within a single clock cycle of losing power. Secondly, we show a proof-of-principle for crossbar demultiplexers with hard-coded error correction.

5.1 The nonvolatile latch

Flip-flops enable synchronous sequential logic operations and are ubiquitous in digital circuitry. CMOS-based flip-flops are volatile so additional nonvolatile memory circuits are typically used to store processor states between power cycles of flip-flop based circuits.
such as microprocessors. The data storage process is complicated and takes many clock cycles because it requires the encoding, communication, decoding, and writing of the data in each register to the external nonvolatile memory. Powering down a system gracefully consequently requires a maintained power source during this storage procedure.

With the conceptualization [110, 111] and recent demonstration [108] of nanoscale memristive devices integrated directly on top of CMOS logic, it is conceivable that a bit of nonvolatile memory can be connected directly to each flip-flop in a microprocessor with minimal area overhead. This integration may enable cost-effective, miniature single-chip platforms which can store their state in a single clock cycle for applications in small devices with intermittent power sources. Here we use discreet logic and memristive components to demonstrate an architectural concept that will be enabled by the development of this memristive integration: the nonvolatile latch.

The nonvolatile latch implemented here consists of a master/slave flip-flop (FF) configuration with a memristive device directly wired to the master FF output. The circuit is designed to store the master FF state within one clock cycle of power loss. A variety of resistance switching materials could be used for vertically integrated memory bits including the phase change materials [117], metallic bridge materials [118, 57] and metal oxides [58]. For this implementation we used 50 × 50 nm² titanium dioxide memristors because of their process compatibility with CMOS [108], process simplicity, < 10 ns switching speed, > 1 year nonvolatility, high yield, and small device size.

The memristors were fabricated utilizing a Pt-TiO₂-Pt metal-insulator-metal structure, patterned by nanoimprint lithography in the 17 × 1 device array shown by the atomic force microscope (AFM) image in Figure 5.1 (a). The fabrication was carried out on an oxidized Si substrate with a 200 nm thick oxide with adequate smoothness to permit the imprint lithography process. The 50 nm wide bottom electrode was fabricated by a nanoimprint liftoff procedure and consisted of a 2 nm Ti adhesion layer and 9 nm Pt layer. The blanket 25 nm thick TiO₂ switching layer was then deposited followed by the nanoimprint liftoff fabrication of 50 nm wide, 11 nm thick Pt top electrodes perpendicular to the bottom electrode.

The devices were packaged, wire-bonded and characterized by measuring the 2-wire current-voltage (i − v) characteristics with an Agilent B1500 semiconductor parameter analyzer. Typical swept current-voltage (i − v) characteristics are shown in Figure 5.1 (b) which demonstrates an OFF (100 MΩ) to ON (50 kΩ) ratio exceeding 1000 at 0.1 V. Low level current measurements were limited in the bonded package by a 1 GΩ leakage pathway between package pads, an issue which results in 100 pA of leakage current in the measurements. The 50 kΩ series resistance of the nanowire electrodes is visible in the linear regime of the i − v above 1V. The i − v also shows an ON switching current of −200 µA and an OFF switching current of +300 µA with positive polarity defined as being applied from the top to bottom electrodes of the device.

A schematic of the non-volatile latch circuit that was designed and constructed for this experiment is included as Figure 5.2. The components of the circuit include a master flip-flop (FF1), a slave flip-flop (FF2), write circuit switches (S1, S2) a restore circuit
Figure 5.1: (a) Atomic force microscope micrograph of the 50×50 nm$^2$, 1×17 TiO$_2$ memristor crossbar studied in this work. (b) Representative quasi-DC current-voltage ($i − v$) switching plot of the devices demonstrating a switching ratio greater than $10^4$. 


Figure 5.2: Block diagram of the discrete component nonvolatile latch circuit. The master-slave flip-flop (FF) configuration operates normally until the write enable channel is activated, copying the master FF state to the memristor. Upon receiving the read enable signal, the memristor state is copied to the slave FF.
switch (S3) and a read comparator (C0). The circuit concept for the NV latch is that the circuit operates as a conventional CMOS master-slave flip-flop during normal powered operation, with all data flowing through conventional CMOS digital circuits, and with the memristor sitting dormant. When a PowerDown signal is received, the state of the master flip-flop is copied into the memristor (M1) by activating the write enable switch (S2). Later, when a PowerUp signal is received, the saved state is copied from the memristor to the slave flip-flop, and computation resumes. After PowerUp is complete, the flip-flops hold the same state they had at PowerDown. This switched design (a) limits the number of write operations to the memristive memory element, and (b) does not slow down the latch during normal (powered) operation. In this test setup we do not pass data directly from one flip-flop to another since this is a trivial operation and only test data transfer by means of copying the master flip-flop state Q1 to and from the memristor. Thus, we have created a nonvolatile latch circuit that demonstrates the saving of a flip-flop state to a memristor, and the restoration of this state from the memristor to a second flip-flop.

An array of programmable source/measurement units (SMUs) were utilized as control hardware in order to provide the following control signals to the circuit: Digital Control Signals: D1 (Data In, master flip-flop), C1 (Clock, master flip-flop), D2 (Data In, slave flip-flop), C2 (Clock, slave flip-flop), WE (Write-Enable: save state to memristor), RE (Read-Enable: restore state to slave flip-flop); Analog Control Signals: VR (read voltage applied to top of resistor/memristor divider), VW0 (Voltage to write a zero), VW1, (Voltage to write a one), VR/2 (reference voltage input at the comparator). The control hardware was also used to simultaneously measure the voltage output of the circuit at the nodes: VOUT, (Voltage at the output of the comparator) and Q2, (State, slave flip-flop).

The control program running the hardware simulated integration of the NV latch circuit into a larger system by forcing and measuring a clocked sequence of voltages at each of the control nodes in the circuit. The clock period was set to 10 ms due to the time resolution of the SMUs. The sequence of signals for a single cycle of the program was as follows:

1. Power up the circuit
2. Set master flip-flop to state 1
3. Power down the circuit and copy master flip-flop state to memristor
4. Power up the circuit and copy memristor state to slave flip-flop
5. Read and store the voltage outputs of the comparator and the slave flip-flop
6. Set master flip-flop to state 0
7. Power down the circuit and copy master flip-flop state to memristor
8. Power up the circuit and copy memristor state to slave flip-flop
9. Read and store the voltage outputs of the comparator and the slave flip-flop

This cycle was repeated 2000 times in order to determine the performance of the circuit and the memristor during many operations.

The NV latch circuit operated successfully for 1500 cycles with an error rate less than 1%, as shown by the sequence of slave flip-flop outputs in Figure 5.3. As the number of cycles increased, failure was observed in that the circuit was no longer able to store the ON state of the master flip-flop through power cycles for the chosen threshold values for ON and OFF. Failure of the memristor after 1500 cycles was a relatively slow and continuous event as shown by the progression of the voltage output of the comparator in Figure 5.3. This output slowly increases because the ON state of the memristor steadily becomes more resistive relative to the voltage divider resistor, causing the divider output to steadily increase. Failure of laboratory fabricated memristors has previously been attributed to the failure of nanowire electrodes which could be possibly be improved by oxide passivation, improvements in device planarity, or utilization of refractory metal electrodes [119].

In summary, we demonstrated that a memristor can be used as a memory element in a nonvolatile latch circuit. This circuit could be used in a nonvolatile processor. The feasibility of the tight integration of memristors with conventional CMOS circuitry was shown by the recent hybrid memristor/CMOS SNIC chip. In normal powered operation of this circuit, there is no speed penalty, since the memristor is not used for this function. The use of the memristor is limited to the times at which power fails, or is restored. Since this circuit was built and tested, the endurance of memristors has been improved to the range of $10^9 - 10^{10}$ write operations which is a figure that enables effectively unlimited operation if the power even once a second.

### 5.2 A defect-tolerant crossbar demultiplexer

Demultiplexer (demux) circuits are needed for interfacing micro- to nano-circuitry in order to electronically access highly integrated nanowire-based circuits. In a demultiplexer a small number of address wires control a much larger number of nanowires through a selection matrix which must be of roughly the same feature scale as the nanowires in order to minimize area overhead. Previously it was been shown that a crossbar of nanowires can be used as a demultiplexer [120], making it reasonable to envision microscale components wired to vast crossbars of nanoscale components. As the size of the features decrease it is likely that manufacturing defects in the nano-circuitry will inevitably increase, causing the demultiplexer to malfunction under conventional architecture design. To deal with this issue, approaches towards defect tolerant computer architectures have been developed theoretically, primary based on coding theory [121]. In this work, we show the fabrication of a 50 nm half-pitch nanowire crossbar array with electrically switching titanium oxide memristors and demonstrate how to reliably address a specific nanowire in
Figure 5.3: Circuit test results demonstrating the output voltage of the voltage divider during the READ operation after the master FF was in the OFF (a) and ON (b) states. The total number of write errors (c) starts to increase sharply at around 1200 cycles reaching 1% at around 1500 cycles.
a nano-crossbar array with a partially defective nano-crossbar demultiplexer by utilizing the error-correcting coding theory.

A fully addressable $17 \times 17$ nano-crossbar circuit at 50 nm half-pitch was designed for this study. Figure 5.4 shows three microscopic images of the crossbar including an optical image including the electrode fanout and pads (a) as well as high magnification AFM (b) and SEM (c) images of the crossbar itself. A sub-array of this crossbar was used to demonstrate the defect tolerance. The general fabrication process was reported extensively in previously [107] but is briefly described here. Two sequential steps of UV-based nanoimprint liftoff process produced crossbar arrays fabricated on silicon wafers with a 100 nm thermal oxide overlayer. The first imprint step generated the bottom electrodes which were composed of 2 nm of Ti and 9 nm of Pt. After the first imprint process a blanket layer of TiO$_2$ was prepared by five cycles of 1.5 nm Ti deposition immediately followed by oxygen plasma exposure in order to create a TiO$_2$ switching film. The top electrode of 2 nm Ti / 9 nm Pt, orthogonal to the bottom electrode, was then fabricated by the second nanoimprint process. After the formation of the top electrode, the device was subjected to O$_2$/CHF$_3$ plasma in a RIE for 1 min to remove the TiO$_2$ that was not directly under the top electrodes. This step not only exposed the bottom electrode fanouts for ohmic electrical contact, but also reduced the possibility of cross-talk between neighboring nanowires.

The multilayer TiO$_2$ deposition process described above was designed to exhibit antifuse type switching with a large resistance change between the as-grown state and the written state. It was written to the low resistance state from its initial insulating state by applying a voltage of about 3 V and exhibited an on/off ratio of greater than $10^4$. The multilayer oxide could subsequently be switched off by applying a negative voltage bias, but the following switching event in these films usually has small on/off ratio, typical of less than 10. This type of behavior is not useful for nonvolatile memory devices, but is very useful for demultiplexers which only need to be programmed once in the lifetime of the circuit.

Although most of the junctions showed reliable switching during the programming test, we observed a small fraction of the junctions in the nano-crossbar arrays which could not be turned on, a defect know as a “stuck open” defect. In order to deal this somewhat common stuck-open defect, we adopted the defect-tolerant approach based on coding theory which was previously worked out [122, 121] in simulation. The basic purpose of these codes is to convert raw addresses into longer-bit-length codewords such that the resulting codewords are substantially different from each other. This “substantial difference” is quantitatively defined as the minimum number of different bits between any two codewords and is referred to as the minimum Hamming distance, denoted as $d$. In this scheme, a minimum Hamming distance of $d$ allows for $d - 1$ stuck open defects per output line in the demultiplexer because it requires $d$ errors to make a mistake when using codewords $d$ bits apart. In coding theory nomenclature, the number of bits in the codeword is typically denoted by $n$, the number of bits in the original address by $k$, a set of codes defined by these parameters is denoted as an $[n, k; d]$ code, and the matrix used
Figure 5.4: Optical (a), atomic force (b), and scanning electron (c) micrographs of a 50×50 nm$^2$ 17×17 memristor crossbar used to demonstrate a defect tolerant resistor logic demultiplexer. The crossbar columns were used for the balance input address which selected a single output row.
Figure 5.5: Schematic of the ideally programmed demultiplexer with conductive cross-points indicated by the blue dots. As discussed in the text, the error correcting codes used here allow each output line to contain a maximum of two errors while still operating correctly.

to generate the codewords is denoted by $g$.

For experimental characterization of the defect-tolerant demultiplexer on our nanocrossbar devices, we generated a $[6, 3, 3]$ code and laid it out on a $12 \times 8$ crossbar sub-array for selecting an output line when its respective encoded address (a codeword) is input. The generating matrix that we used was:

$$
\mathbf{g} = \begin{pmatrix}
1 & 0 & 0 & 1 & 1 & 0 \\
0 & 1 & 0 & 1 & 0 & 1 \\
0 & 0 & 1 & 0 & 1 & 1
\end{pmatrix}
$$

(5.1)
which resulted in the generation of the following set of codewords:

\[
\begin{align*}
  c_0 &= 0 \quad 0 \quad 0 \quad 0 \quad 0 \quad 0 \\
  c_1 &= 0 \quad 0 \quad 1 \quad 0 \quad 1 \quad 1 \\
  c_2 &= 0 \quad 1 \quad 0 \quad 1 \quad 0 \quad 1 \\
  c_3 &= 0 \quad 1 \quad 1 \quad 1 \quad 1 \quad 0 \\
  c_4 &= 1 \quad 0 \quad 0 \quad 1 \quad 1 \quad 0 \\
  c_5 &= 1 \quad 0 \quad 1 \quad 1 \quad 0 \quad 1 \\
  c_6 &= 1 \quad 1 \quad 0 \quad 0 \quad 1 \quad 1 \\
  c_7 &= 1 \quad 1 \quad 1 \quad 0 \quad 0 \quad 0
\end{align*}
\]  

(5.2)

The codewords were balanced by taking their complement and appending it to the codeword. This set of balanced codewords was then programmed into the crossbar in order to enable each line to be selected when the appropriate codeword is input at the address lines. A schematic of the ideally programmed demultiplexer is shown in Figure 5.5. Since the Hamming distance, \(d\), of this code is 3 the demultiplexer should be able to tolerate up to two defects per line.

The crossbar was contacted with a probe card and initially tested for nanowire continuity and shorts between nanowires to rule out the other defects. Typical resistances of the nanowires from end to end was about 40 k\(\Omega\). After a suitable 12 \(\times\) 8 nanocrossbar sub-array with good nanowires was identified, the desired crossbar junctions were programmed by applying a switching bias of 4.5-6V across the junctions. During the programming process we formed two different configurations, one with \(\leq 3\) stuck-open defects per line and one with \(\leq 2\) defects per line. A map of the programmed crossbar resistance states measured at low bias of 0.5V for both configurations is shown in Figure 5.6. The junctions were considered to be switched ‘ON’ if the resistance was less than 20 M\(\Omega\), whereas the junctions were considered to be un-programmed or stuck-open if the resistance was greater than 500 M\(\Omega\).

After programming the demultiplexer configurations, we tested their ability to select the proper output line in the presence of the intentional defects. The device was again contacted with the probe card and was tested by applying all of the codewords to the crossbars with a logical 1 (bias of 1 V) and logical 0 (bias of 0 V). The application of one volt did not cause the resistance of the switches to change significantly. When each codeword was applied we recorded the voltage on each output line to see the output bias. The results of the test showed that the demultiplexer worked as expected from previous theoretical analysis. As shown in Figure 5.7 (a), the demultiplexer with \(\leq 3\) stuck-open defects per line had a high output on the appropriate output line for each input code. However there are also two erroneous output lines selected when they are not supposed to be, including line seven for code 000000 and line two for code 101101. These errors are consistent with the model because lines seven and two are the ones that contain 3 defects as shown in Figure 5.6. The demultiplexer programmed with \(\leq 2\) defects per line (Figure 5.7 (b)) selects all of the correct lines and does not select any incorrect lines. The voltage margin between selected and unselected lines was measured to be 0.2 V under
Figure 5.6: Ideally programmed (a) map of the junction resistance where dark cross-points indicate the programmed or conductive state. Maps of the junction resistance as-programmed into the crossbar demultiplexer for (b) \( \leq 3 \) errors per output line and (c) \( \leq 2 \) errors per output line. Intentionally introduced errors in the demux programming are indicted by the red circles.
Figure 5.7: Output line selection maps for the ≤ 3 (a) and the ≤ 2 (b) as-programmed states of the crossbar demux. These plots indicate the output voltage on each line for each encoded address generated by the coding scheme. As expected, in the leq 3 configuration output lines 2 and 7 are erroneously selected because they contain 3 errors. the ≤ 2 configuration selects all output lines correctly.
Figure 5.8: The margin between selected and unselected output lines for a resistor logic demultiplexer is a function of the input voltage placed on the address lines. As the voltage increases, the absolute margin also increases.

the current input level of 1 V, which is well above the noise floor of the measurement system.

In order to determine the margin as a function of input bias, the nano-crossbar demultiplexer with up to two-defect configuration in Figure 5.7 (b) was tested at 0.5 V, 0.75 V, and 1 V, respectively. The results, shown in Figure 5.8, demonstrate that the margin increases with increasing applied voltage for our crossbar demultiplexer device. It is worth to note that even though the margin increased slightly at 1 V input, the voltages on the selected wires are also more scattered than that tested at 0.5 and 0.75 V. This may be attributed to the non-linearity of the $i - v$ characteristics of the titanium dioxide junctions, at higher input voltage the junction resistance will decrease and cause more potential sneaking current path inside the resistor-only cross-bar array. Further improvement of the switching characteristics of the oxide junction as well as the incorporation of diode-like behavior into the junction will likely to provide more stable demultiplexer operation. Nevertheless, this first physical demonstration of defect-tolerant demultiplexer will be useful in designing nano-crossbar circuits for addressing other nano-crossbar memory, logic, routing circuits as well as nanowire-based sensor arrays.
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