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High Linearity 1.5-2.5 GHz RF-MEMS and Varactor Diodes Based Tunable Filters for Wireless Applications

A dissertation submitted in partial satisfaction of the requirements for the degree Doctor of Philosophy in Electrical Engineering

by

Mohammed Ahmed El-Tanani

Committee in charge:

Professor Gabriel M. Rebeiz, Chair
Professor Peter M. Asbeck
Professor Gert Cauwenberghs
Professor Bill Hodgkiss
Professor Kevin Quest

2009
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The dissertation of Mohammed Ahmed El-Tanani is approved, and it is acceptable in quality and form for publication on microfilm and electronically:

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Chair

University of California, San Diego

2009
DEDICATION

To my parents, Ahmed and Zeinab
My wife, Yasmeen and our son, Ahmed
and
to my brother and sisters
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Appendix B is mostly the fabrication process that is a result of a joint effort with other researchers in Prof. Rebeiz’s group, mainly Isak Reines, Rashed Mahameed and Alex Grichner.
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PUBLICATIONS


Mohammed A. El-Tanani, and Gabriel M. Rebeiz, “Capacitively Compensated 1.4-2.2 GHz Comline Tunable Filters,” to be submitted for publication in *IEEE Transactions on Microwave Theory and Techniques*, June 2009.


ABSTRACT OF THE DISSERTATION

High Linearity 1.5-2.5 GHz RF-MEMS and Varactor Diodes Based Tunable Filters for Wireless Applications

by

Mohammed Ahmed El-Tanani
Doctor of Philosophy in Electrical Engineering
University of California San Diego, 2009
Professor Gabriel M. Rebeiz, Chair

The dissertation presents tunable bandpass filters in the 1.5-2.5 GHz frequency range targeted for wireless applications. The tunable filters are designed for size miniaturization, good linearity and constant absolute bandwidth characteristics while maintaining low insertion loss. The improved linearity has been demonstrated using back-to-back varactor diodes and using RF MEMS devices. The constant absolute bandwidth characteristics was achieved using a novel corrugated-coupled lines approach and also using a localized capacitive compensation concept.

In the improved linearity varactor diode design, two miniaturized tunable filters with two zeros were developed at 1.4-2.0 GHz on. The filters were built using single and back-to-back varactor diodes and compared for linearity characteristics. The single diode filter has a 1-dB bandwidth of 5 ± 0.5 % and an insertion loss of 2.5-1.8 dB. The back-to-back diode filter has a 1-dB bandwidth of 4.9 ± 0.5 % and an insertion loss of 2.9-1.25 dB (resonator $Q$ of 56-125). A detailed Volterra series analysis is done on the back-to-back diode including the effect of the bias network and diode mismatches. The measured $IIP_3$ for the back-to-back diode tunable filter is 22-41 dBm depending on the bias voltage and is 13-15 dB better than the single diode design. The power handling capabilities of both designs is explored using large signal $S_{21}$ measurements. To our knowledge, these planar tunable filters represent state-of-the-art insertion loss and linearity characteristics.
performance with varactor diodes as the tuning elements.

In the corrugated coupled-lines design, miniaturized fixed and tunable microstrip bandpass filters were developed t 1.4-1.9 GHz. The novel approach uses microstrip corrugated coupled-lines concept to synthesize a coupling coefficient which maintains a nearly constant absolute bandwidth across the tuning range. In addition, a miniaturized 2-pole varactor tuned filter is demonstrated with a frequency coverage of 1.44-1.89 GHz and an insertion loss < 2.92 dB with a constant 1-dB bandwidth of 70±4 MHz across the tuning range. In addition, a 3-pole combline 4.7% fixed filter at 1.94 GHz shows a 3:1 resonator spacing reduction over the conventional approach, with an insertion loss of only 1.1 dB. This technique will allow the design of miniaturized small bandwidth fixed and tunable microstrip filters.

In the localized capacitive compensation design, the approach was used to design 3-poles combline tunable filter with an electrical length of 42° at the mid band. The frequency coverage of the tunable filter is 1.4-2.2 GHz with a 1-dB bandwidth of 157±7 MHz across the tuning range. Detailed design equation as well as the design procedure were presented.

In order to get substantial improvement in linearity and achieve a high resonator $Q$, high $Q$ RF MEMS devices are used to demonstrate tunable filters with constant absolute bandwidth for the 1.5 – 2.5 GHz wireless band. The filter design is based on corrugated coupled-lines and ceramic substrates ($\epsilon_r = 9.9$) for miniaturization, and the 3-bit tuning network is fabricated using a digital/analog RF MEMS device so as to provide a large capacitance ratio and continuous frequency coverage. Narrowband (72±3 MHz) and wideband (115±10 MHz) two-pole filters result in a measured insertion loss of 1.9 – 2.2 dB at 1.5 – 2.5 GHz, with a power handling of 25 dBm and an $IIP_3 \gg 33$ dBm. The filters also showed no distortion when tested under wideband CDMA waveforms up to 24.8 dBm. The designs can be scaled to higher dielectric-constant substrates to result in even smaller filters.
Chapter 1

Introduction

1.1 Motivation

Low-loss bandpass filters are basic components of transceivers, either as band select or image-reject units. The increased rejection to out-of-band interferes eases the dynamic range requirement of the receiver low noise amplifier (LNA) and mixer in the presence of interferers. In multi-band communication systems, a single bandpass filter generally cannot fulfill the filtering requirements for all bands especially in today crowded RF environments. Therefore a filter-bank followed by switching network is used which results in a large area and an increased complexity of the system. An ideal solution is to replace the switched filter-bank by a tunable filter which tunes to different bands without degradation in the filter performance (Fig. 1.1).

Common applications for tunable band-pass filters include multi-band wireless communication systems, frequency hopped receivers, wide-band radars, and microwave instrumentation. Historically, the invention of radar in World War II led to dramatic improvement in tunable filter technology for applications in ESM (electronic support measures) and ECM (electronic counter measure systems) [2]. In these applications, wide band receivers are used together with low-loss fast tuning tunable filters to split the complete microwave band of interest into smaller sub-bands. This results in a wide-band receiver which has barely the same sensitivity as narrow-band system (except for the filter loss).
In wireless communication systems, tunable filters have the potential to reduce the system size and complexity. Fig. 1.2 presents a cell phone front-end, with multiple GSM, CDMA and data-channels covering 800 MHz to 2400 MHz, and shows that a single silicon transceiver chip requires 19 different fixed filters or diplexers. These are implemented using fixed SAW (surface acoustic waves) and BAW (bulk acoustic waves) filters, a large SP9T switch matrix and an RF distribution network. In fact, the passive part of a multi-band cell phone or a defense radio occupies 65-80% of the RF board area, depending on the number of channels, and with an RF loss of 3-6 dB between the silicon chip and the antenna(s). It is therefore imperative to combine several of these filters into single units using tunable filters and antennas.

Cognitive radios are also currently an active area of research in which the radios themselves sense the available spectrum and decide on the communications channel to use [3]. Unlike conventional systems, this system does not have fixed frequency bands which are already allocated and the use of a switched bank that cover the whole band will tremendously increase the system complexity and size. Therefore, tunable filters can be a key components in such an architecture and will
1.2 Tunable Filter Technology

Most tunable filters described in the literature fall into three basic types: mechanically tunable, magnetically tunable, and electronically tunable filters [4]. Electronically tunable filters are mainly based on varactor diodes, PIN diodes, BST (Barium Stronium Titanate) and RF-MEMS. Mechanically tunable filters have large power handling capability and low insertion loss. However, their low tuning speed and large size prevent the possibility of using them in modern communication systems [5].
YIG filters are the most popular example of magnetically tunable filters. The filter uses ferromagnetic resonators and gyromagnetic coupling. The tuning is done utilizing the variation in the ferromagnetic resonant frequency of Yttrium-Iron-Garnet spheres by applying an external DC magnetic field [5]. YIG filters have the advantage of multi-octave tuning range, spurious-free response, low insertion loss and high quality factor resonators [5] [6]. However, YIG have moderate tuning speed (ms), large power consumption (0.1-1W). Also, YIG filters are not planar structures which limits their use in modern wireless communication systems.

BST tunable filters are based on ferroelectric thin-film barium strontium titanate tunable capacitors. The ferroelectric materials have two phases of operations: ferroelectric phase and paraelectric phase. In the paraelectric phase, the relative dielectric constant is high ($\epsilon_r \approx 300$) and can be changed with the applied electric field [7]. BST filters are planar, easy to integrate and can be tuned with a 2-5 V applied dc voltage and zero power consumption [7]. On the other side, BST filters have moderate $Q$ and limited linearity.

Varactor diode based tunable filters utilize the change in capacitance due to change in the depletion region width with the applied reverse-bias DC voltage. The main advantage of this technology is the fast tuning speed, zero power consumption, low cost and proven reliability [8]. However, these devices have moderate $Q$ and suffer from poor linearity due to the non-linear $C-V$ curve of the varactor diodes. At large signal power, the diode can also be forward biased resulting in harmonic distortion and a distorted filter response. In part of this dissertation, considerable improvements in varactor-based tunable filter linearity characteristics are achieved using the back-to-back configuration. The linearity of this configuration is discussed and modeled in detail using Volterra series analysis with full comparison over the single diode case.

RF MEMS (Micro-Eletro-Mechanical System) tunable filters employ RF MEMS based capacitance network as a tuning element. RF MEMS devices utilize micrometer level movement to result in a changing capacitance with the applied DC voltage. Typical devices include metal-contact switches, shunt switches ($C_r=20-100$), continually tuned varactors ($C_r < 1.5$) and switched capacitors ($C_r=3-10$).
### Table 1.1: Typical performance parameters of microwave tunable bandpass filters.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>YIG</th>
<th>BST</th>
<th>Schottky Diode</th>
<th>PIN Diode</th>
<th>RF MEMS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Resonator Q</td>
<td>5000 – 2000</td>
<td>30 – 150</td>
<td>30 – 150</td>
<td>$R_s = 1 , \Omega$</td>
<td>50 – 400</td>
</tr>
<tr>
<td>Tuning Range</td>
<td>2 – 18 GHz</td>
<td>$C_r = 2-3$</td>
<td>$C_r = 3-5$</td>
<td>High</td>
<td>$C_r = 2-100$</td>
</tr>
<tr>
<td>Tuning Speed</td>
<td>$ns$</td>
<td>$ns$</td>
<td>$ns$</td>
<td>$ns$</td>
<td>0.2-0.5 μs</td>
</tr>
<tr>
<td>IIP$_3$ [dBm]</td>
<td>≈ 20</td>
<td>10-35</td>
<td>10-35</td>
<td>&gt; 33</td>
<td>&gt; 60</td>
</tr>
<tr>
<td>Power Consumption</td>
<td>1 – 5 W</td>
<td>0</td>
<td>0</td>
<td>20 – 30 mA</td>
<td>0</td>
</tr>
<tr>
<td>Temperature Sensitivity</td>
<td>High</td>
<td>High</td>
<td>Low</td>
<td>Low</td>
<td>Low</td>
</tr>
<tr>
<td>Biasing</td>
<td>Magnet</td>
<td>High R</td>
<td>High R</td>
<td>LC choke</td>
<td>High R</td>
</tr>
<tr>
<td>Palnar</td>
<td>No</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td>Cost</td>
<td>High</td>
<td>Low</td>
<td>Low</td>
<td>Low</td>
<td>Medium</td>
</tr>
</tbody>
</table>

Switched capacitors have analog, digital or analog/digital tuning capabilities. In part of this research, an RF MEMS switched capacitor network is used to design a low-loss, wide tuning range and high linearity tunable filter with constant absolute bandwidth characteristics.

The main advantages of RF-MEMS devices include [9]:

1. **Very Low Insertion Loss**: Since metals are used for conduction instead of semiconductors, RF MEMS switches show very low loss, about 0.05-0.2 dB from 1-100 GHz. This corresponds to $R_s = 0.5-3 \, \Omega$ in metal contact switches and $R_s = 0.1-0.5 \, \Omega$ in capacitive switches.
2. **Very High Linearity**: Beyond their mechanical resonance frequency (20-1000 kHz), RF MEMS devices are extremely linear and are 30-50 dB better than GaAs or CMOS varactors [10].
3. **Very High Q**: A device resistance of $0.1 – 2 \, \Omega$ results in a $Q > 50-400$ at 2-100 GHz. This is essential for tunable filters and reconfigurable networks.
4. **High Power Handling**: Power handling of 1-10 W has been achieved for both capacitive and metal-contact switches and varactors (with proper designs) [mac1,
RF MEMS devices can be designed to handle large RF voltage swings (> 30 – 50 V$_{rms}$), or better yet, can be designed to be a three or four-terminal device where the RF terminals are independent from the DC actuation pads.

5. **Extremely Low Power Consumption:** Although a high voltage (20-100 V) is needed for the electrostatic actuation of MEMS switches, there is very little current consumption leading to very low DC power dissipation.

6. **Very High Isolation:** MEMS metal-contact switches are fabricated in an air dielectric, and therefore have very small off-state capacitance ($C_{up}$) about 2-10 fF, which leads to an excellent isolation up to 40 GHz.

On the other side, RF MEMS also has some concerns, and they are [9]:

1. **Hermetic Packaging:** All reliable RF MEMS switches require a hermetic package which tends to increase cost. A hermetic wafer-cap is been developed by several companies and labs which will greatly reduce the packaging cost.

2. **High Voltage Drive:** Most reliable RF MEMS switches operate at 25-90 V, and therefore require high-voltage drive circuits.

3. **Reliability:** Research on reliability is a very high priority, and better dielectrics, metal-contacts, actuator design and packaging are all contributing to vastly improved reliability results.

Table I summarizes the performance characteristics of the serval tunable filter technologies.

### 1.3 Literature Survey

A literature review in tunable filters in the 0.8-3 GHz range results in few papers even of the 20$^{th}$ years of work in this area. The reason is that earlier design suffered a lot of loss (Schottcky varactor had too much series resistance, no BST or RF MEMS technology, etc), and the only available tunable filter was the YIG based design.

Hunter *et al.* [8] demonstrated varactor-diode 2-pole strip-line tunable comb-line filter (based on λ/4 resonators) at 3500-4500 MHz with a 3-5 dB insertion loss.
and a $200 \pm 20$ MHz absolute-bandwidth. The analysis showed that constant absolute bandwidth filters can be achieved for resonators having $53^\circ$ electrical length at the mid-band frequency. However, the analysis is based on strip-line technology, and this is not applicable to microstrip-line case on high dielectric constant substrates. In addition, the $53^\circ$ electrical length requirement has the drawback of requiring a high capacitance ratio to achieve wide tuning range.

Sanchez et al. [11] demonstrated bandwidth control of comb-line filters by inserting a coupling reducer between the combline resonators. This however increases the complexity and size of the filter. In his work, mechanical capacitors are used as frequency tuners in the resonators. The filter shows a tuning range, insertion loss, and fractional-bandwidth of 450-850 MHz, 14-3 dB, and 2-18%, respectively.

Park et al. [12] recently demonstrated varactor-diode 2-pole tunable filters with predefined bandwidth characteristics at 850-1300 MHz. The insertion loss was 3-1 dB for an absolute bandwidth of $43 \pm 3$ MHz. However, this work cannot be extended to higher order tunable filter in a planar technology.

Young et al. developed an RF MEMS 2-pole tunable bandpass filter using a 3-bit switched capacitance bank on a ceramic substrate [13]. Both the coupling and resonator capacitance is tuned with RF MEMS devices to achieve center frequency and bandwidth tunability. The inductors were off-chip air-coil type with $Q > 100$ at 1.3 GHz, and were assembled next to the RF MEMS chip. The measured performance shows frequency tunability of 900-1600 MHz, fractional bandwidth tuning of 7-42% bandwidth, and an associated insertion loss of 1-4 dB. The estimated filter tunable $Q$ is 60-90.

Reines et al. demonstrated suspended 3-pole combline RF MEMS tunable filter with a frequency coverage of 1.6-2.4 GHz [14]. Both the resonators and the input/output capacitance networks are tunable. The filter is built on a quartz substrate and results in an insertion loss of 1.34-3.03 dB over the tuning range and a 1-dB bandwidth of 144-253 MHz. A tunable $Q$ of 50-150 was achieved over this frequency range. Since the filter is based on a suspended structure, it results in large size and require special housing as part of the design and this limits it use.
in compact wireless communications system. The tunable filter also suffers from increasing bandwidth as the filter is tuned.

Palego *et al.* demonstrated a 2-pole tunable filter with bandwidth and center frequency tuning. This filter is built on ceramic and exploits five 3-bit capacitor banks controlled with MEMS ohmic switches. The filter has a tuning range of 1.512.26 GHz, an insertion loss of 2.9-5.9 dB. The filter suffers from high insertion loss, poor selectivity, and increased bandwidth even with the RF MEMS tuning elements used to control the bandwidth due to the lumped-element components used in the capacitive inter-resonator coupling network.

Park *et al.* developed a 4-6 GHz 3-bit tunable filter using a high-\(Q\) 3-bit orthogonally-biased RF-MEMS capacitance network [15]. The filter is built on a quartz substrate and is based on capacitively-loaded \(\lambda/2\) resonators. In this design, both the resonators and the input/output matching capacitance networks are tunable. The measured filter has an insertion loss of 1.5-2.8 dB with a 1-dB bandwidth of 4.35+/−0.35\% over the 4-6 GHz tuning range with a tunable \(Q\) of 85-170. The filter, however, suffers from increasing bandwidth as the frequency tune and since it is based on \(\lambda/2\) resonators, it results in a large size if designed for at the 1.5-2.5 GHz.

### 1.4 Thesis Goals

Varactor diode-based tunable filters have been an active area of research but very little attention was given to improve the linearity issue of these filters. The increased bandwidth as the filter is tuned is another main drawback of tunable filters (both RF MEMS and varactor diode based) presented in the literature.

The main goal of this dissertation is to develop novel topologies for size miniaturization, while keeping low insertion loss, maintaining constant absolute bandwidth characteristics and achieving at least 10-20 dB linearity improvement over the current state-of-the-art. Silicon and GaAs varactor diodes are used in part of this work as tuning elements which are highly non-linear devices. Two uniformly doped varactor diodes connected in back-to-back configuration with a high-value
biasing resistor can significantly improve the linearity characteristics of the tunable filter (by $\sim 13$ dB in IIP3 and $\sim 7$ dB in $P_{1dB}$) over conventional designs. The 1.5-2.0 GHz tunable filter presented are based on loaded shorted resonator that is folded to result in further size miniaturization. To improve the rejection in the stop-band, two additional zeroes were added to the transfer function which also tune as the center frequency tunes.

The absolute bandwidth is an important characteristic of the RF filter and from system level analysis it is desired to keep it constant as the filter tunes in frequency. In this work, a novel mixed-coupling mechanism using corrugated coupled-lines to maintain constant absolute bandwidth across the tuning range. This novel approach was also applied to conventional combline 1.94 GHz fixed-filters and gave another design freedom which resulted in size miniaturization. Localized capacitive compensation was also introduced to overcome the increased bandwidth drawback in conventional combline tunable filters and maintain constant absolute bandwidth characteristics. This approach was demonstrated for three pole filter at 1.4-2.1 GHz.

The novel corrugated coupled-lines topology was also used to develop highly linear 1.5-2.5 GHz RF MEMS tunable filter. The design is built on alumina for further size miniaturization while still maintaining low loss. The filters deployed wide-bandwidth tuning without the need of variable switching network in the input/output matching network which is challenging in wide-band tunable filters. Unlike conventional RF-MEMS designs which use the RF MEMS as a switch, the switching network used in this approach is based on switched capacitance RF MEMS with digital/analog tuning capabilities. This resulted in a high $Q$ switching network with continuous $> 16$ states tuning across the tuning range. The filters demonstrated $< 2$ dB insertion loss with resonator $Q$ of 85-125 for wide-band tuning design (1.5-2.5 GHz) and a $Q$ of 125-165 for an improved design of 1.5-2.0 GHz.
1.5 Thesis Overview

Chapter 2 presents two miniaturized tunable filters with two zeros to result in sharp skirts developed at 1.4-2.0 GHz on $\epsilon_r = 6.15$ substrate. The filters were built using single and back-to-back varactor diodes and compared for linearity characteristics. The single diode filter has a 1-dB bandwidth of $5 \pm 0.5 \%$ and an insertion loss of 2.5-1.8 dB. The back-to-back diode filter has a 1-dB bandwidth of $4.9 \pm 0.5 \%$ and an insertion loss of 2.9-1.25 dB (resonator $Q$ of 56-125). The back-to-back diode filter was designed for improved linearity characteristics using two uniformly doped varactor diodes and biased with a high impedance circuit. A detailed Volterra series analysis is done on the back-to-back diode including the effect of the bias network and diode mismatches. The measured $IIP_3$ for the back-to-back diode tunable filter is 22-41 dBm depending on the bias voltage and is 13-15 dB better than the single diode design. The power handling capabilities of both designs is explored using large signal $S_{21}$ measurements. To our knowledge, these planar tunable filters represent state-of-the-art insertion loss and linearity characteristics performance with varactor diodes as the tuning elements.

Chapter 3 presents corrugated coupled-lines for miniaturized fixed and tunable microstrip bandpass filters. The novel approach uses microstrip corrugated coupled-lines concept to synthesize a coupling coefficient which maintains a nearly constant absolute bandwidth across the tuning range. A miniaturized 2-pole varactor tuned filter is demonstrated with a frequency coverage of 1.44-1.89 GHz and an insertion loss $< 2.92$ dB with a constant 1-dB bandwidth of 70±4 MHz across the tuning range. In addition, a 3-pole combine 4.7% fixed filter at 1.94 GHz shows a 3:1 resonator spacing reduction over the conventional approach, with an insertion loss of only 1.1 dB. This technique will allow the design of miniaturized small bandwidth fixed and tunable microstrip filters.

Chapter 4 presents detailed analysis of conventional combine tunable filters and show that the electrical length proposed by [8] for strip-lines is not valid for microstrip case. Capacitively compensated coupled-lines were therefore analyzed and showed that with proper design they can result in a constant absolute bandwidth tunable filters. The technique is applicable to strip-lines, CPW lines as well
as microstrip lines and for resonator with arbitrary electrical lengths. The technique was used to design 3-poles combline tunable filter with an electrical length of 40° at the mid band. The frequency coverage of the tunable filter is 1.4-2.2 GHz with a 1-dB bandwidth of 157±7 MHz across the tuning range.

Chapter 5 presents high performance RF MEMS tunable filters with constant absolute bandwidth for the 1.5 – 2.5 GHz wireless band. The filter design is based on corrugated coupled-lines and ceramic substrates ($\epsilon_r = 9.9$) for miniaturization, and the 3-bit tuning network is fabricated using a digital/analog RF MEMS device so as to provide a large capacitance ratio and continuous frequency coverage. Narrowband (72±3 MHz) and wideband (115±10 MHz) two-pole filters result in a measured insertion loss of 1.9 – 2.2 dB at 1.5 – 2.5 GHz, with a power handling of 25 dBm and an $IIP_3 \gg 33$ dBm. The filters also showed no distortion when tested under wideband CDMA waveforms up to 24.8 dBm. The designs can be scaled to higher dielectric-constant substrates to result in even smaller filters. To our knowledge, these filters represent the state-of-the-art at this frequency range using any planar tuning technology.

Chapter 6 is the conclusion and future work. The bandpass tunable filters can be designed for 1.5-2.5 GHz frequency range using novel topologies where many multi-band wireless communication systems are operating. RF MEMS based tunable filters showed substantially improved performance in term of insertion loss and linearity characteristics. The capacitively compensated tunable filter topology can be further extended to result in bandwidth as well as center frequency tunability.

Appendix A presents a single-stage 5.5-6.0 GHz reflection-type phase shifter based on a complex load design and Schottky varactor diodes. The measured phase shift is $> 360^\circ$ at 5.8 GHz with an average insertion loss of 1.7 dB. The measured reflection coefficient is better than 17 dB at 5.8 GHz over all bias voltages. The phase shift is $440^\circ$ at 5.6 GHz with an associated insertion loss of only 2.1 dB and a reflection coefficient better than 13 dB. At 5.9 GHz, the phase shift reduces to $315^\circ$ which is equivalent to a 3-bit design with an insertion loss of still $< 2.0$ dB. The phase shifter results in state-of-the-art performance and is suitable for WLAN
smart antennas at the 5.5-6.0 GHz.

Appendix B presents the fabrication steps for the fabrication of the RF MEMS switched capacitor used as the tuning devices in Chapter 5.
Chapter 2

A Two-Pole Two-Zero Tunable Filter With Improved Linearity

2.1 Introduction

Microwave tunable bandpass filters have the potential to replace switched-filter banks in multi-band communication systems, and are based on different technologies: (a) Yttrium-Iron-Garnet (YIG) based resonators (b) semiconductor (silicon, GaAs) varactor diodes (c) P-I-N diodes (d) ferroelectric varactors and (e) RF-MEMS devices [6]-[16]. Varactor diodes are used due to their fast tuning speed (ns) and low cost. They have a moderate $Q$ ($Q = 50-150$ at 1-2 GHz) but suffer from poor linearity characteristics. From a system level prospective, the non-linear characteristics of tunable filters have a severe impact on the the RF-front end performance since the tunable filter is placed between the antenna and the LNA. In previous varactor-tuned filters, the main focus was on the tunability of the filter topology with improved insertion loss. Hunter et al. [8] reported a 2-pole varactor-tuned filter at 3500-4500 MHz utilizing a comb-line filter with a 3-5 dB insertion loss and a 5.7-4.4% fractional-bandwidth. Brown et al. [17] realized a 4-pole varactor-tuned filter at 700-1330 MHz using an interdigital filter with an insertion loss of 2-5 dB and a fractional-bandwidth of 10-16%, respectively. Park et al. [12] has recently demonstrated 2-pole tunable filters with predefined bandwidth
characteristics at 850-1300 MHz with an insertion loss of 1-3 dB and a fractional bandwidth of 4-5%. However, none of the above work addressed improvements in the filter linearity. As is well known, most varactor-tuned filters result in an $IIP_3$ of 6-25 dBm depending on the filter bandwidth and the varactor bias voltage.

The intermodulation distortion introduced by different varactor diode configurations was first derived in closed-form by Meyer et al. [18]. The analysis showed that a back-to-back (sometimes known as anti-series) varactor diode can result in a theoretically distortionless varactor diode. However, this derivation assumed an infinite biasing resistance for all the frequency components which is not necessarily a valid assumption. Buisman et al. [19] has shown that by properly choosing the back-to-back diode junction areas, cancelation for the $IM_3$ can occur even for $n \neq 0.5$ given that the biasing circuit is again ideal (infinite impedance at all frequencies). A conventional anti-parallel diode pair was added to the biasing network to reduce the effect of the non-ideal biasing effect. However, this technique resulted in a limited improvement in the $IIP_3$ due to the off-state capacitance of the anti-parallel diode pair. Huang et al. [20] proposed low-distortion varactor diodes using back-to-back configuration with an optimized doping profile given that the biasing network behaves as a low-impedance at baseband frequencies and a high impedance at RF-frequencies. However, this approach resulted an improvement over the conventional design only for small difference frequencies and was worse for moderate-to-large difference frequencies.

This paper presents two different but related topics in tunable filters: First, a varactor-tuned two-pole filter based on a miniaturized shorted folded-resonator is presented. Two transmission zeros are added to the filter response using a source-load coupling technique [21]. The zeros move as the center frequency tune and this improves the attenuation characteristics and results in a sharp attenuation skirt for all states. Two tunable filters with single diode and back-to-back varactor diode are implemented and the measured small-signal and large-signal characteristics are presented for both topologies. It is seen that with the proper design of the varactor biasing network, the back-to-back diode tunable filter tuner results in 13-15 dB improvement over a single-diode tunable filter in the measured $IIP_3$ for
all bias voltages. This paper also presents an exact analysis done using Volterra series [22] for the back-to-back varactor nonlinearity including biasing network. The effects of the bias network impedance, difference frequency ($\Delta f$), and diode mismatches on the intermodulation products ($IM_3$), as well as the effect of the RF voltage amplitude on the resonator frequency response are presented together with a detailed comparison between measurements and simulations.

2.2 Filter Design

2.2.1 Admittance Matrix of the Filter

The proposed filter is composed of two folded short-ended microstrip-line resonators loaded with varactor diodes (Fig. 2.1) and the external coupling is established by the tapping position and $C_m$. $C_{z1}$ introduces a source-load coupling for added transmission zeros in the $S_{21}$ response. $C_{z2}$ is attached to a transmission line of admittance $Y_{z2}$ and electrical length $\phi_{z2}$ and adds a far transmission zero. The even and odd-mode admittances of the filter seen from port A and port B are

Figure 2.1: Electrical circuit model of the tunable filter.
defined by

\[ Y_{re} = \frac{Y_{ie}Y_3 + jY_3^2\tan \phi_3}{Y_3 + jY_{ie}\tan \phi_3}, \quad Y_{ro} = \frac{Y_{io}Y_3 + jY_3^2\tan \phi_3}{Y_3 + jY_{io}\tan \phi_3} \]  (2.1)

where

\[ Y_{ie} = \frac{-jY_1Y_2e\cot \phi_2e + jY_1^2\tan \phi_1}{Y_1 + Y_2e\cot \phi_2e \tan \phi_1} + \frac{j\omega C_m(Y_0 + Y_{me})}{Y_{me} + Y_0 + j\omega C_m} \]  (2.2)

\[ Y_{io} = \frac{-jY_1Y_2o\cot \phi_2o + jY_1^2\tan \phi_1}{Y_1 + Y_2o\cot \phi_2o \tan \phi_1} + \frac{j\omega C_m(Y_0 + Y_{mo})}{Y_0 + Y_{mo} + j\omega C_m} \]  (2.3)

\[ Y_{me} = \frac{j\omega Y_{z2}C_{z2} + jY_{z2}^2\tan \phi_{z2}}{Y_{z2} - \omega C_{z2} \tan \phi_{z2}} + jY_{z1} \tan \phi_{z1} \]  (2.4)

\[ Y_{mo} = \frac{j\omega Y_{z2}C_{z2} + jY_{z2}^2\tan \phi_{z2}}{Y_{z2} - \omega C_{z2} \tan \phi_{z2}} + \frac{j2\omega Y_{z1}C_{z1} + jY_{z1}^2\tan \phi_{z1}}{Y_{z1} - 2\omega C_{z1} \tan \phi_{z1}} \]  (2.5)

The overall admittance matrix can then be written as

\[ Y = \begin{bmatrix} \frac{Y_{re} + Y_{ro} + j\omega C_L}{2} & \frac{Y_{re} - Y_{ro}}{2} \\ \frac{Y_{re} - Y_{ro}}{2} & \frac{Y_{re} + Y_{ro} + j\omega C_L}{2} \end{bmatrix} \]  (2.6)

### 2.2.2 Design Procedure

The Y-matrix shown in (5.9) represents a filter with a passband centered at \(\omega_0\) and a fractional bandwidth \(\Delta\) provided that [15]

\[ Im[Y_{11}(\omega_0)] = 0, \quad \frac{Im[Y_{12}(\omega_0)]}{b} = \frac{\Delta}{\sqrt{g_1 g_2}} = k_2 \]  (2.7)

\[ Q_{ext} = \frac{b}{Re[Y_{r11}(\omega_0)]} = \frac{g_0 g_1}{\Delta} \]  (2.8)

where

\[ b = Im[\frac{\omega_0}{2} \frac{\partial Y_{r11}(\omega_0)}{\partial \omega} - \frac{Y_{r11}(\omega_0)}{2}], \quad Y_{r11} = \frac{Y_{re} + Y_{ro}}{2} \]  (2.9)
Figure 2.2: Electrical circuit model for calculating $Q_{ext}$.

The design procedure starts with arbitrarily choosing $Y_1, \phi_1, Y_2, \phi_2, Y_3, \phi_3, Y_{z1}, \phi_{z1}, Y_{z2}, \phi_{z2}$ and the rest of the design parameters, $C_L, C_m, C_{z1}, C_{z2}$ and $s$ should then be determined. $C_{z2}$ adds a transmission zero at $\omega_{z2}$ where $\omega_{z2} > \omega_0$. $C_{z2}$ is chosen to the first order by $[Z_{nz2}(\omega_{z2})] = 0$ where

$$Z_{nz2} = Y_{z2} - \omega_{z2}C_{z2}\tan\phi_{z2}$$

(2.10)

The next step is to calculate the input matching capacitor $C_m$ using $Q_{ext}$ (5.11). The spacing $s$ can be decoupled by approximating the slope parameter $b$ such that the uncoupled slope parameter is used and therefore $Y_{2e}$ and $Y_{2o}$ are replaced with $Y_2$ in (2.2) and (2.3). In addition, $C_{z1}$ presents a high impedance at $\omega_0$ and can be ignored in the first-order analysis at passband. The circuit model for calculating $Q_{ext}$ and therefore $C_m$ is shown in Fig. 2.2.

In addition, the spacing, $s$, is calculated to satisfy the coupling coefficient $(k_{21})$ as per (4.5) and again $C_{z1}$ is neglected in the calculation. $C_L$ is calculated to satisfy the resonance condition such that $Im[Y_{11}] = 0$ where $Y_{11}$ is obtained using (5.9). Notice that the Y-matrix is calculated at the physical position of $C_L$ which
makes it easy to uncouple $C_L$ from the slope parameter $b$.

Finally, $C_{z1}$ is added to the circuit so that transmission zeros can be synthesized to enhance the rejection close to the passband. The filter is inductive away from the passband frequencies and the source-load coupling path is capacitive. Therefore, two zeros will be present in the transmission response ($S_{21}$) and the exact locations of these zeros are found by solving $\text{Im}[Y_{ze} - Y_{zo}] = 0$ where

$$Y_{z(e,o)} = Y_{m(e,o)} + \frac{j\omega C_m Y_{p(e,o)}}{Y_{p(e,o)} + j\omega C_m}$$  \hspace{1cm} (2.11)

$$Y_{p(e,o)} = Y_d + \frac{-jY_1 Y_{2(e,o)} \cot \phi_{2(e,o)} + jY_1^2 \tan \phi_1}{Y_1 + Y_{2(e,o)} \cot \phi_{2(e,o)} \tan \phi_1}$$  \hspace{1cm} (2.12)

$$Y_d = \frac{j\omega Y_3 C_L + jY_3^2 \tan \phi_3}{Y_3 - \omega C_L \tan \phi_3}, \quad Y_{m(e,o)} \text{ given by (2.4, 2.5)}$$  \hspace{1cm} (2.13)

Notice that the zeros move with $C_L$ (and $f_0$) and results in a sharp response for all tunable states.

### 2.3 Back-to-back Varactor Diode Non-Linearity with Biasing Circuit Effect

The capacitance-voltage relationship of $D_1$ and $D_2$ are given by a Taylor expansion

$$C_{D1}(v_1, V_{dc}) = \frac{C_{jLo} \phi_{1}^{n_1}}{(V_{dc} - v_1 - \phi_1)^{n_1}} = L_0 + 2L_1 v_1 + 3L_2 v_1^2 + ....$$  \hspace{1cm} (2.14)

$$C_{D2}(v_2, V_{dc}) = \frac{C_{jMo} \phi_{2}^{n_2}}{(V_{dc} + v_2 + \phi_2)^{n_2}} = M_0 + 2M_1 v_1 + 3M_2 v_1^2 + ....$$  \hspace{1cm} (2.15)

where $C_{jLo}$ and $C_{jMo}$ are the zero-bias junction capacitance of $D_1$ and $D_2$, respectively, $v_1$ and $v_2$ are the applied ac voltages on the diodes, $V_{dc}$ is the dc reverse bias.
Figure 2.3: A back-to-back diode parallel-resonance circuit including biasing circuit effects.

voltage, $\phi_1$ and $\phi_2$ are the built-in potential voltages, $n_1$ and $n_2$ are the power-law exponent of the diodes. $L_n$ and $M_n$ are the Taylor expansion coefficients around $V_{dc}$ given by $\frac{\partial^n C_D(v, V_{dc})}{\partial v^n n!}\bigg|_{v=0}$.

For a back-to-back varactor diode in a resonant circuit with a transmission line characteristic admittance $Y_0$, an electrical length $\Phi_0$ at $f$, and an equivalent parallel resistance $R_p$, the impedance transfer function between the input ac-current, $i_{ac}$, and the output ac-voltage, $v_{out}$, including the effect of the non-ideal biasing circuit is derived using Volterra series analysis and is given by

$$v_{out} = H_1(s)i_{ac} + H_2(s_1, s_2)i_{ac}^2 + H_3(s_1, s_2, s_3)i_{ac}^3$$  \hspace{1cm} (2.16)

where

$$H_1(s) = \frac{L_0 + M_{01}}{L_0 M_{01}s + (L_0 + M_{01})y_L(s)}$$  \hspace{1cm} (2.17)

$$H_2(s_1, s_2) = -\frac{H_1(s_1)H_1(s_2)(L_1 M_{01}(s_1)M_{01}(s_2)M_{02} + M_1 L_0^2)}{(L_0 + M_{01}(s_1))(L_0 + M_{01}(s_2))(L_0 + M_{02})} \left[ \frac{L_0 M_{02}}{L_0 + M_{02}} + \frac{y_L(s_1, s_2)}{(s_1 + s_2)} \right]$$  \hspace{1cm} (2.18)

$$H_3(s_1, s_2, s_3) = -\frac{(M_{03} H_{n13} + L_0 H_{n23})(L_0 M_{03})}{(L_0 + M_{03})} \left[ \frac{L_0 M_{03}}{L_0 + M_{03}} + \frac{y_L(s_1, s_2, s_3)}{(s_1 + s_2 + s_3)} \right]$$  \hspace{1cm} (2.19)
and

\[ y_L(s) = \frac{1}{R_p} - jY_0 \cot\left(\frac{s}{j2\pi f}\Phi_0\right) \]  

(2.20)

\[ y_L(s_1, s_2) = y_L(s_1 + s_2), \quad y_L(s_1, s_2, s_3) = y_L(s_1 + s_2 + s_3) \]  

(2.21)

\[ M_{01}(s) = M_0 + \frac{G_{bias}}{s}, \quad M_{02} = M_0 + \frac{G_{bias}}{(s_1 + s_2)} \]  

(2.22)

\[ M_{03} = M_0 + \frac{G_{bias}}{(s_1 + s_2 + s_3)} \]  

(2.23)

\[ H_{n13} = L_2 H_{L1}(s_1) H_{L1}(s_2) H_{L1}(s_3) + \frac{2}{3} L_1 H_a \]  

(2.24)

\[ H_{n23} = L_2 H_{M1}(s_1) H_{M1}(s_2) H_{M1}(s_3) + \frac{2}{3} M_1 H_b \]  

(2.25)

\[ H_a = H_{L1}(s_1) H_{L2}(s_2, s_3) + H_{L1}(s_2) H_{L2}(s_1, s_3) + H_{L1}(s_3) H_{L2}(s_1, s_2) \]  

(2.26)

\[ H_b = H_{M1}(s_1) H_{M2}(s_2, s_3) + H_{M1}(s_2) H_{M2}(s_1, s_3) + H_{M1}(s_3) H_{M2}(s_1, s_2) \]  

(2.27)

\[ H_{L1}(s) = H_1(s) \frac{M_{01}}{(L_0 + M_{01})}, \quad H_{M1}(s) = H_1(s) \frac{L_0}{(L_0 + M_{01})} \]  

(2.28)

\[ H_{L2}(s_1, s_2) = -\frac{H_2(s_1, s_2) y_L(s_1, s_2)}{(s_1 + s_2)} + L_1 H_{L1}(s_1) H_{L1}(s_2) \]  

(2.29)

\[ H_{M2}(s_1, s_2) = -\frac{H_2(s_1, s_2) y_L(s_1, s_2)}{(s_1 + s_2)} + M_1 H_{M1}(s_1) H_{M1}(s_2) \]  

(2.30)
With the Volterra series coefficients determined, the $IM_2(\omega_1-\omega_2)$ and $IM_3(2\omega_1-\omega_2)$ components normalized to the output signal at $\omega_1$ can be written as

$$v_{out}(\omega_1) = I_{ac}H_1(j\omega_1)$$  \hspace{1cm} (2.31)

$$IM_2 = I_{ac}\left|\frac{H_2(j\omega_1,-j\omega_2)}{H_1(j\omega_1)}\right|$$  \hspace{1cm} (2.32)

$$IM_3 = \frac{3I_{ac}^2}{4}\left|\frac{H_3(j\omega_1,j\omega_1,-j\omega_2)}{H_1(j\omega_1)}\right|$$  \hspace{1cm} (2.33)

where $IM_2$ and $IM_3$ are the normalized output voltages (unitless), and $I_{ac}$ is the magnitude of the input current.

Note that $IM_2$ simplifies to zero when the two back-to-back diode are identical and biased using an infinite impedance network ($H_2(j\omega_1,j\omega_2) = 0$). However, once a finite biasing resistor is used, it modifies the $M_{01}$ coefficient of $D_1$ in (2.22) by an amount of $\frac{1}{jR_{bias}(\omega_1-\omega_2)}$ for the second-order intermodulation product. $M_{01}$ is effectively the $M_0$ coefficient of $D_1$ with a bias resistor. This additional value in $M_{01}$ is comparable to $M_0$ and results in a finite $IM_2$ output due to the mismatches in the diode coefficients. The modification in $M_0$ is frequency dependent and is more severe if a small difference frequency $(\omega_1 - \omega_2)$ is chosen.

In addition, for two matched diodes with $n = 0.5$ and an infinite impedance biasing network, $H_3(j\omega_1,j\omega_1,-j\omega_2)$ is also zero. The condition for an infinite bias impedance is a theoretical requirement to obtain a zero $IM_3$ and $IM_2$ for matched diodes with $n = 0.5$. This theoretical value is not practically possible. However, significant improvement in $IM_2$ and $IM_3$ can be obtained by using resistor values tending to infinite. This is true as long as the C-V relationship is given by (2.14) and (2.15) and is because any capacitance increase or decrease in $D_2$ is compensated by a decrease or increase of the $D_1$ capacitance. This results in a constant capacitance vs. applied ac-voltage for $v < \phi + V_{dc}$. At the $IM_3$ frequency and with the biasing network effect included, the $M_{03}$ coefficient is modified according to (2.23), and the effect is negligible since $s_1+s_2+s_3 \approx j\omega_1$. However, $H_2(j\omega_1,-j\omega_2)$ is also used in the calculation of $H_3(j\omega_1,j\omega_1,-j\omega_2)$ and has an effect on (2.26) and (2.27), and therefore the biasing network will have a significant effect on the $IM_3$ values. The current in the bias network has a low-pass response with a 3-dB corner frequency given by $f_{3dB} = 1/(2\pi R_{bias}M_0)$ and the effect will be more
pronounced for $\Delta f < f_{3dB}$ [19].

For $\Delta f < f_{3dB}$ and with two matched diodes, the $IM_3$ component of the circuit shown in Fig. 2.3 can be written as

$$IM_3 \simeq \frac{I_{ac}^2}{32} | H_1(j\omega_0) |^3 | 3j\omega_0L_2 + \frac{2\omega_0^2L_1}{j\omega_0L_0} |$$

$$= \frac{L_0n\omega_0I_{ac}^2}{64(\phi + V_{Bias})^2} | H_1(j\omega_0) |^3$$

(2.34)

To make a full comparison, the $IM_3$ component of the same circuit using a single diode with a capacitance value equivalent to the back-to-back-diode capacitance ($C_{j0\text{-single}}$ equals to $C_{j0\text{-back}}/2$) is given by

$$IM_3 \simeq \frac{I_{ac}^2}{8} | H_1(j\omega_0) |^3 | 3j\omega_0L_2 + \frac{2\omega_0^2L_1}{j\omega_0L_0 + y(j2\omega_0)} |$$

(2.35)

where $L_0$, $L_1$, $L_2$ are the Taylor coefficients of the back-to-back diode. It should be noted that unlike the back-to-back-diode case, the $IM_3$ value is not a function of the difference frequency, $\Delta(f)$. In addition, the $IM_3$ value is independent of the biasing impedance as long as the biasing impedance is much greater than the diode impedance at RF frequencies. From (2.34) and (2.35) it is seen that even when $\Delta f < f_{3dB}$, the $IM_3$ component for the single diode circuit is $\sim 12$ dB higher than the back-to-back circuit and corresponds to $\sim 6$ dB degradation in the $IIP_3$ value. For $\Delta f > f_{3dB}$, the back-to-back diode $IM_3$ value falls at a $-20$ dB/decade since the current in the bias network drops vs. $\Delta f$ and the difference between the diode coefficients $L_0$ and $M_{01}$ is much less. In this case, the diode mismatches ($n_1 \neq n_2$, $\phi_1 \neq \phi_2$, ... etc) will determine the $IM_3$ level.

Fig. 2.5 presents the IM3 component normalized to the fundamental tone voltage for a back-to-back varactor diode each with ($C_{j0} = 5.2$ pF, $n = 0.5$ and $\phi = 0.7$ V), and placed in a resonator with $Y_0 = 1/50$ S., $\Phi = 53^\circ$, $R_p = 1$ kΩ, ($Q = 12$ at 2 GHz). The two-tone frequency excitations are placed at the resonance frequency for each bias voltage. It can be seen that the $IM_3$ improves as the bias voltage increases which is due to the decrease in the C-V slope vs. voltage (Fig. 2.4(b)). In addition, as shown in (2.34), the $IM_3$ value is independent of the biasing resistor and is determined by the diode parameters for $\Delta f < f_{3dB}$,
Figure 2.4: (a) capacitance C-V curve, (b) Simulated third-order intermodulation product vs. different biasing voltage, $Y_0 = 1/50 \ S$, $\Phi = 53^\circ$, $R_p = 1 \ k\Omega$ at 2 GHz, $V_{RFswing} = \pm 0.25 \ V$ across each diode.

and then decreases at 20 dB/decade for $\Delta f > f_{3dB}$. Also, the $IM_3$ levels-off at different values for high $\Delta f$ depending on the diode mismatches (Fig. 2.5(b)).

For a single tone frequency excitation, the biasing condition for a distortionless diode is more severe since it can be considered as two tones with a frequency difference ($\Delta f = 0$) and therefore only an infinite biasing resistor can result in a significant improvement. Therefore, the effective diode capacitance at the fundamental frequency will be a function of the voltage amplitude ($V_0$) and this will cause a drift in the fundamental resonance frequency. The diode self-biasing effect
Figure 2.5: Simulated third-order intermodulation product for $Y_0 = 1/50 \, S$, $\Phi = 53^\circ$, $R_p = 1 \, k\Omega$ at 2 GHz, $V_{RF\,swing} = \pm 0.25 \, V$ across each diode. (a) vs. difference frequency at $V_b = 4 \, V$, (b) effect of diodes doping mismatches at $V_b = 4 \, V$. 
is approximated using a truncated Volterra-series to the third-order transfer function and the impedance of the resonant circuit (with two matched diodes) is given by

\[ Z(\omega, V_0) \simeq Z(\omega) - \frac{V_0^2}{32} [Z(\omega)]^2 [j3\omega L_2 + \frac{2\omega^2 L_1}{j\omega L_0}] \]  

(2.36)

and for a single diode is given by:

\[ Z(\omega, V_0) \simeq Z(\omega) - \frac{V_0^2}{8} [Z(\omega)]^2 [j3\omega L_2 + \frac{2\omega^2 L_1}{j\omega L_0 + y(j2\omega)}] \]  

(2.37)

where \( Z(\omega) \) is the resonance circuit linear input impedance and \( V_0 \) is the amplitude of the linear fundamental ac-voltage. Again (2.36) and (2.37) show that the change in the impedance due to the nonlinearity is \( \sim 4 \) times less in back-to-back diode than for a single diode for the same resonator voltage magnitude. In addition, the resonance frequency \( (f_0) \) decreases since the diode effective capacitance increases vs. the output voltage swing. Fig. 2.6 presents the simulated \( \Delta f_0 \) for a resonator with \( L_p = 8 \) nH, \( Cj_0 = 5.2 \) pF, and \( V_b = 4 \) V and 12 V . A harmonic-balance simulation in ADS is also done so as to obtain more accurate results for high voltage swings (in this case, the Volterra series requires more terms than the third-order transfer function).
2.4 Implementation of the Tunable Filter

The Y-matrix developed in Section II does not include the resonator bend, via-holes inductance, and coupling between adjacent folded resonator transmission lines. Therefore, a full-wave simulation for the filter structure without any of the capacitors was done in Sonnet [23] and the 14-ports Y-matrix is extracted (Fig. 2.1). This matrix is then transferred into a 2-port matrix relative to ports A and port B by terminating the 14 ports Y-matrix with the lumped capacitors and varactor diodes. The elements of the loaded Y-matrix ($Y_{14 \times 14}^m$) are given by

$$y_{ii}^m = y_{ii} + j\omega C_i, \quad y_{ij}^m = y_{ij} - j\omega C_{ij}, \quad i \neq j,$$

where $C_i$ is the lumped element capacitance between port $i$ and other ports in the circuit, and $C_{ij}$ is the lumped element capacitance between ports $i$ and $j$, $i, j = 1, 2, 3, ..., 14$.

The 2-port Y-matrix is then defined as:

$$Y_{2 \times 2} = \frac{1}{(z_{11}z_{22} - z_{12}z_{21})} \begin{bmatrix} z_{22} & -z_{21} \\ -z_{12} & z_{11} \end{bmatrix} \quad (2.39)$$

where

$$z_{ij}$$

are the elements of the matrix $[Z_{14 \times 14}] = [Y_{14 \times 14}^m]^{-1}$ \quad (2.40)

With the full-wave simulation-based $Y_{2 \times 2}$ calculated, the same design procedure outlined in Section II can be used. Table 2.2 presents the filter dimensions for both the single diode and the back-to-back diode tunable filter designs for operation at 1.4-1.9 GHz.

2.5 Fabrication and Measurement

The filters are fabricated on a 0.625 mm Duroid substrate ($\epsilon_r = 6.15$, Roger RT/Duroid 6006) using a copper etching process [24]. The S-parameters of both filters were measured with an Agilent E5071B PNA. An SOLT calibration was
Table 2.1: Dimensions for single diode and back-to-back diode Filters (Dimensions are in mm, and Capacitances are in Picofarad, $\varepsilon_r = 6.15$, 20 mils Microstrip Substrate is Assumed. $w_1 = w_2 = w_3, w_{z1} = w_{z2}$)

<table>
<thead>
<tr>
<th></th>
<th>$w_1/w_{z1}/s$</th>
<th>$l_1/l_2/l_3$</th>
<th>$l_{z1}/l_{z2}$</th>
<th>$C_M/C_{z1}/C_{z2}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>Single diode</td>
<td>0.63/0.16/0.62</td>
<td>4.4/3.4/1.85</td>
<td>6.7/1.8</td>
<td>1.82/0.2/1.6</td>
</tr>
<tr>
<td>Back-to-back</td>
<td>0.81/0.18/0.44</td>
<td>4.25/3/3</td>
<td>6.5/1.9</td>
<td>1.85/0.2/1.55</td>
</tr>
</tbody>
</table>

Figure 2.7: Fabricated single-diode tunable filter on a Duroid substrate ($\varepsilon_r = 6.15$, $t = 25$ mils).

performed using an Agilent E-cal kit. The reference planes are at the SMA connectors. The chip capacitors $C_m$, and $C_{z2}$ are ATC 600S [25] and $C_{z1}$ is an AVX Accu-P [26] and all of them have a $Q > 200$ at 2 GHz.

2.5.1 Tunable Filter with Single Varactor Diode

The fabricated single-diode tunable filter is shown in Fig. 2.7 using GaAs varactors MA46H071-1056 [27] ($C_{j0} = 2.75$ pF, $n = 0.74$, $\phi = 1.2$ V) and $R_s = 1 \pm 0.1$ $\Omega$. The diode results in $C_{\text{total}} = 0.5 - 2$ pF for $V_b = 1 - 20$ V, and a $Q = 57 - 170$ at 1.4-1.8 GHz. A 10 pF DC-blocking chip capacitor (ATC 600S,
\( R_s = 0.12 \, \Omega \) is connected in series with each GaAs diode to isolate the anode from the ground, (Fig. 2.7). The dc biasing is done using two 10 kΩ resistors connected in series to reduce the RF-signal leakage through the bias network.

The measured frequency response is shown in Fig. 5.10 with frequency coverage of 1.39-1.81 GHz. The measured insertion loss is 2.5 dB with a 4.55% (65 MHz) 1-dB bandwidth and a center frequency of 1.39 GHz at a bias voltage of 1 V. The measured insertion loss improves to 1.80 dB with a 5.37% (97 MHz) 1-dB bandwidth and a center frequency of 1.81 GHz at 20 V. The measured return loss is better than 15 dB for all states at both ports. The improvement in the insertion loss is because the varactor diode has \( \sim 4 \) times higher \( Q \) at \( (V_b = 20 \, \text{V}) \) and also due to the slight increase in the filter fractional bandwidth. Two far zeros are present in the response due to slight mismatches in the values of \( C_{z2} \) at the input and the output ports. The simulated and measured results show excellent agreement with a rejection better than -30 dB up to 3 GHz with a spurious passband occurs at 4.0 GHz (Fig. 2.9). The diodes are pre-measured for different bias voltages using Agilent E4991A impedance analyzer, and the measured circuit models are used in simulations. The discrepancy in the upper stop band attenuation is due to the tolerance in \( C_{z2} \) (± 0.1 pF). The summary of the filter performance is shown in Fig. 3.14. The fitted resonator \( Q \) is 72-95 at \( V_b = 1 - 20 \, \text{V} \).

### 2.5.2 Tunable Filter with Back-to-Back Varactor Diode

The fabricated filter with back-to-back diode is shown in Fig. 2.11. The tuning is implemented using uniformly doped silicon tuning varactors (Metelics MSV34,064, 2 diode per package) [28]. Each varactor diode has \( C_{j0} = 5.2 \, \text{pF} \), \( n = 0.47, \phi = 0.6 \, \text{V} \) and an equivalent series resistance of \( \sim 0.7 \, \Omega \) at 1.4-2 GHz. The diode results in \( C_{\text{total}} = 3.4 - 0.9 \, \text{pF} \) for \( V_b = 1 - 30 \, \text{V} \) and a \( Q = 46 - 125 \) at 1.4-1.9 GHz. The dc biasing was done using two 10 kΩ resistors connected in series with a 1000 kΩ resistor. As indicated in Section II, the purpose of this additional resistor is to reduce any signal leakage through the biasing network in the \( H_2(jw_1, -jw_2) \) Volterra series transfer function which will then improve the \( IIP_3 \) of the whole filter response.
Figure 2.8: Measured S-parameters of the single diode tunable filter. The measured center frequency is 1.39-1.8 GHz for a bias voltage of 1-20 V.
Figure 2.9: Measured S-parameters vs. simulation for the single diode tunable filter. The bias voltage is 1 V ($f_0 = 1.39$ GHz) and 20 V ($f_0 = 1.8$ GHz).
Figure 2.10: Performance summary of the single diode tunable filter.

The measured frequency response is shown in Fig. 4.10 with the frequency coverage of 1.52-1.95 GHz. The measured insertion loss is 2.93 dB with a 4.39% (67 MHz) 1-dB bandwidth and a center frequency of 1.52 GHz at a bias voltage of 1.8 V. The measured insertion loss improves to 1.25 dB with a 5.45% (105 MHz) 1-dB bandwidth and a center frequency of 1.933 GHz at a bias voltage of 30 V. The measured return loss is better than 15 dB for all states at both ports. Again, the improvement in the insertion loss is due to the varactor diode improved $Q$ ($\sim 4$ times higher) at $V_b = 30$ V and also due to the increase in the filter fractional bandwidth. The far transmission zero $\omega_z$ is located at 2.75-3 GHz. The simulated and measured results show excellent agreement with a spurious response at 4 GHz (Fig. 4.11). The summary of the filter performance is shown in (Fig. 4.12). The fitted resonator $Q$ is 56-125 at $V_b = 2 - 30$ V.

### 2.6 Non-linear Measurements

The single diode ($n = 0.74$, $\phi = 1.2$ V) and back-to-back diodes ($n = 0.47$, $\phi = 0.6$ V) have different $n$ and $\phi$ values, but result in the same non-linear effects.
This can be explained by writing Eq. (14) as
\[ C = \frac{C_{jo}}{(1 + (V_{dc} \pm v)/\phi)^n} \]
and noticing that if both \( n \) and \( \phi \) are higher as in the case of the single diode, then any non-linearity increase due to a higher \( n \) is mitigated by a non-linearity decrease due to a lower \((V_{dc} \pm v)/\phi\). In effect, the simulated \( IIP_3 \) in the tunable filter for a single diode with \( C_{jo} = 2.75 \) pF, \( n = 0.74 \), and \( \phi = 1.2 \) V or \( C_{jo} = 2.75 \) pF, \( n = 0.47 \), \( \phi = 0.6 \) V are within 1.5 dB of each other for a bias voltage of 2-20 V. Therefore, we feel that using these two different diodes in the two filters presents a fair comparison in the non-linearity performance of single and back-to-back topologies.

The measured \( IIP_3 \) for the single and back-to-back diode tunable filters are shown in Fig. 3.16. The measured \( IIP_3 \) for \( \Delta f = 1 \) MHz of the back-to-back diode and the single diode filters are 27.5 dBm and 13.5 dBm at 4 V, and improves to 41.5 dBm and 26.5 dBm at 20 V, respectively. It is clear that the back-to-back diode design has significantly increased performance (13-15 dB improvement) over the single diode design. Still, the finite \( IIP_3 \) in the back-to-back diode design is due to \( n_1 = n_2 = 0.47 \) (independently measured on the diodes), the effect of the finite
Figure 2.12: Measured S-parameters of the back-to-back diode tunable filter. The center frequency is 1.52-1.95 GHz for a bias voltage of 1.8-30 V.
Figure 2.13: Measured S-parameters vs. simulation for the back-to-back diode tunable filter. The bias voltage is 1.8 V ($f_0 = 1.52$ GHz) and 30 V ($f_0 = 1.95$ GHz).
biasing resistor and slight diode mismatches. Fig. 2.15(b) shows the measured $IIP_3$ for the back-to-back tunable filter vs. the difference frequency. As expected from the analysis in Section III, the $IIP_3$ is constant for $\Delta f < f_{3dB}$ with an $IIP_3 = 21$ dBm and 34 dBm at 4 V and 12 V, respectively, with an improvement of 7-8 dB over a single diode design. In addition, the $IIP_3$ improves for $\Delta f > f_{3dB}$ and levels-off ($n_1$ and $n_2 \neq 0.5$) at 27 dBm and 36 dBm at 4 V and 12 V, respectively, with an improvement of 13-15 dB over a single diode design.

The 1-dB compression point (the input power that results in 1 dB of $S_{21}$ compression) of the tunable filters have been measured at the center passband frequency for different biasing conditions (Fig. 2.17). It is seen that the back-to-back diode tunable filter results in 6 – 7 dB improvement in the 1 dB compression point (in comparison to the single diode design. This is due to the voltage swing being nearly equally divided for the back-to-back diode. Fig. 2.17 also presents the voltage swing across each individual diode at the 1-dB compression point at the center frequency of each biasing condition. The power handling of the back-to-back diode filter is limited by the forward biasing condition ($V_{dc} + \phi$) whereas for the single diode case, the filter shifts in frequency and compresses before reaching the forward biasing condition.

Figure 2.14: Performance summary of the back-to-back diode tunable filter.
The 1 dB compression point at $f_0$ does not truly represent the large signal performance of the filter response. The full filter response is dependent on the pole locations (where the highest voltage swing occurs). Also, the resonators result in different voltage swings across the different varactor diodes (Fig. 2.17) and this results in un-equal loading capacitance which in turn results in a distorted filter response. The large signal $S_{21}$ has been measured with the test setup shown in Fig. 2.16(b). The measurement results shows a power handling improvement of $\sim 8$ dB for the back-to-back diode design (Fig. 16b,c). Also, as shown in Section III, the tunable filter center frequency lowers vs. the applied input power and the frequency shift is $\simeq 25$ MHz for $V_b = 4$ V at the $P_{1dB}$ compression point for the back to-back tunable filter. For a single diode tunable filter, the frequency shift is $\simeq 24$ MHz and 30 MHz for $V_b = 4$ V and $V_b = 20$ V, respectively.

## 2.7 Summary

This chapter shows that back-to-back diode tuners result in a 13-15 dB improvement in $IIP_3$ over a single tuner for the same filter specifications. This $IIP_3$ improvement occurs for $\Delta f > f_{3dB}$ and is 6-7 dB for $\Delta f < f_{3dB}$. The improvement is limited by practical considerations such as diode mismatches and $n \neq 0.5$. As expected, the back-to-back diode can handle 6-7 dB more power than the single diode design, but the $P_{1dB}$ is not necessarily the correct measure for power handling. The paper also shows that a considerable frequency shift occurs at the $P_{1dB}$ level at virtually all bias voltages, and this may be the limiting criteria for the power handling of the tunable filters.

This chapter is mostly a reprint of the material as it appears in IEEE Microwave Theory and Techniques, 2009. Mohammed A. El-Tanani; G. M. Rebeiz. The dissertation author was the primary author of this material.
Figure 2.15: (a) Measured and simulated $IIP_3$ vs. bias voltage, $\Delta f = 1$ MHz.
(b) Measured $IIP_3$ for different $\Delta f$ for $R_b = 1000$ kΩ.
Figure 2.16: (a) Experimental setup for intermodulation measurements, (b) Measurement system for large-signal $S_{21}$.

Figure 2.17: Measured 1 dB compression point (P1-dB) vs. bias voltage, and simulated voltage swing across each diode in resonators 1 and 2 at the respective P1-dB.
Figure 2.18: (a) measured back-to-back diode filter response, (b) measured single diode filter response.
Chapter 3

Corrugated Microstrip Coupled Lines for Constant Absolute Bandwidth Tunable Filters

3.1 Introduction

RF tunable filter have received a recent attention due to their potential to significantly reduce system size and complexity for multi-band communication systems. Different planar technologies for the tuning have been reported: (a) semiconductor (silicon, GaAs) varactor diodes, (b) P-I-N diodes, (c) ferroelectric varactors, and (d) RF-MEMS devices. Frequency agility has been the main focus in research on tunable filters with little attention given to preserve the absolute bandwidth characteristics across the tuning range. Hunter et al. [8] demonstrated 2-pole strip-line tunable comb-line filter at 3500-4500 MHz with a 3-5 dB insertion loss and a 200 ± 20 MHz absolute-bandwidth. The analysis showed that constant absolute bandwidth filters can be achieved for resonators having 53° electrical length at the mid-band frequency. However, the analysis is based on strip-line technology, and this is not applicable to microstrip-line case with high dielectric constant substrates, due to the even and odd-mode phase velocity mismatches. In addition, the 53° electrical length requirement has the drawback of requiring high
capacitance ratio to achieve wide band tuning range.

Park et al. [12] recently demonstrated 2-pole tunable filters with predefined bandwidth characteristics at 850-1300 MHz with an insertion loss of 3-1 dB and an absolute bandwidth of $43 \pm 3$ MHz. However, this work cannot be extended to higher order tunable filter in a planar technology. Sanchez et al. [11] demonstrated bandwidth control of comb-line filters by inserting a coupling reducer between the combline resonators. This however increases the complexity and size of the filter. Jen-Tasi et al. [29] used corrugated coupled-lines to suppress the harmonic response in parallel coupled filter.

In this chapter, a mixed coupling scheme is introduced with the corrugated coupled-line concept. A full study of the coupling characteristics is done and results in synthesis of constant absolute bandwidth tunable filters. The proposed filter has two additional transmission zeroes using source-load coupling which result in improved attenuation characteristics for all tuning states. In addition, this chapter utilizes the corrugated coupled-lines principle to demonstrate a fixed miniaturized comb-line filter. The corrugations introduce distributed electric coupling which is in anti-phase with the conventional magnetic coupling and results in reduced resonator spacing for moderate to narrow-bandwidth combline filters.

### 3.2 Corrugated Microstrip Lines

Fig. 3.1 presents a corrugated coupled-lines structure with a unit cell $l_p$. For $l_p$ and $l_d << \lambda$, the coupling impedance is approximated by a periodic coupling capacitance. The associated even and odd ABCD matrix for a unit cell without taking into account any transmission-line losses is

$$A_{e,o} = D_{e,o} = \cos(\Phi_{e,o}) - \frac{\omega C_{fe,fo}}{2Y_{e,o}} \sin(\Phi_{e,o})$$

$$B_{e,o} = j \left[ \frac{\sin(\Phi_{e,o})}{Y_{e,o}} - \frac{\omega C_{fe,fo}}{Y_{e,o}^2} \sin^2 \left( \frac{\Phi_{e,o}}{2} \right) \right]$$

$$C_{e,o} = j \left[ Y_{e,o} \sin(\Phi_{e,o}) + \frac{\omega C_{fe,fo}}{2} \cos^2 \left( \frac{\Phi_{e,o}}{2} \right) \right]$$
where \( Y_{e,o} \) and \( \Phi_{e,o} \) are the corresponding even and odd-mode characteristic admittances and electrical lengths of the uncorrugated coupled lines, and \( C_{fe} \) and \( C_{fo} \) are the even and odd-mode capacitance per finger for the corrugated lines. \( C_{fe} \) and \( C_{fo} \) are approximated to the first order when \( l_d << \lambda \) as \( C_{fe,fo} = C'_{fe,fo} l_d \) where \( C'_{fe,fo} \) are the static even and mode capacitance per unit length of a periodic array of coupled lines [30]. The unit cell even and odd-mode admittance and electrical length can then be written as

\[
Y'_{e,o} = \sqrt{\frac{C_{e,o}}{B_{e,o}}}, \quad \Phi'_{e,o} = \cos^{-1}(A_{e,o})
\]

Fig. 3.3 shows the fitted and calculated even and odd-mode impedances and electrical lengths for a unit cell with \( l_p = 0.764 \) mm, \( l_d = 0.6 \) mm, \( g = 60 \) \( \mu \)m,
Figure 3.2: Corrugated coupled-lines with a loading capacitor $C_L$.

Figure 3.3: Full-wave and calculated corrugated coupled lines even and odd mode characteristic impedances and electrical lengths.

$w_d = 0.25 \text{ mm}$, $w = 1 \text{ mm}$, and $s = 0.75 \text{ mm}$ on a substrate with $\epsilon_r = 6.15$ and thickness of 0.625 mm. The full-wave results are obtained by simulating a line of 7 unit cells in Sonnet [23] and then fitting the corresponding even and odd mode characteristics. $C_{fe}$ and $C_{fo}$ calculated using [30] as well as simulations extracted from Sonnet [23] are also presented. The calculated $Z'_e$, $Z'_o$, $\Phi'_e$, $\Phi'_o$ from [30] are all within 4% of the full-wave simulated values.

The $Y$-matrix of two coupled resonators having $N$ cascaded unit cells loaded with a tuning capacitor $C_L$ is (Fig. 4.1)
\[
Y = \begin{bmatrix}
\frac{Y_{re} + Y_{ro}}{2} + j\omega C_L & \frac{Y_{re} + Y_{ro}}{2} \\
\frac{Y_{re} + Y_{ro}}{2} & \frac{Y_{re} + Y_{ro}}{2} + j\omega C_L
\end{bmatrix}
\]

(3.5)

and

\[
Y_{re} = -jY_{ne} \cot(N\Phi_{ne}), \quad Y_{ro} = -jY_{no} \cot(N\Phi_{no})
\]

(3.7)

The coupling coefficient, \(k_{21}\), of the resonators is

\[
k_{21} = \frac{\text{Im}[Y_{12}(\omega_0)]}{b} = \frac{BW}{f_0\sqrt{g_1g_2}}
\]

(3.8)

where

\[
b = \text{Im}\left[\frac{\omega_0}{2} \frac{\partial Y_{11}(\omega_0)}{\partial \omega} - \frac{Y_{11}(\omega_0)}{2}\right], \quad Y_{11} = \frac{Y_{re} + Y_{ro}}{2}
\]

(3.9)

The coupling coefficient \(k_{21}\) is not only a function of the resonators spacing, \(s\), but also a function of \(C_{fo}\). This property of corrugated coupled lines can be used to reduce the resonators spacing. For miniaturized filters, high dielectric constant substrates are used to reduce the resonators size and also thick substrates are used to reduce the conductive losses. However, thick substrates results in an increase in the resonator spacing for narrow and moderate bandwidth filters. Fig. 3.4a shows the dependence of \(k_{21}\) on the spacing for conventional comb-line coupled resonators on \(\epsilon_r = 10.2\) substrates (\(Z_o = 55 \Omega, C_L = 1.18\) pF, and \(f_o = 2\) GHz). For a 5\% filter with 0.05 dB Chebeychev prototype, a spacing of 4 mm and 2 mm is required on a 1.27 and 0.6 mm thick substrate, respectively. Using corrugated-coupled lines with \(C_{fo} = 200\) fF, the same coupling coefficient can be achieved with a spacing of 1.0 and 0.5 mm for a substrate thickness of 1.27 and 0.63 mm, respectively (Fig. 3.4b), resulting in substantial size improvement. It is also seen also that \(k_{21}\) changes from magnetic to electric coupling for increasing values of \(C_{fo}\).

In addition, the corrugated coupled-line structure can achieve constant absolute bandwidth filters, where \(k_{21}\) is inversely proportional to the center frequency. For a given electrical length, \(k_{21}\) is synthesized by controlling the even and odd-mode finger capacitance and choosing the width, length and gap between the
Figure 3.4: Coupling coefficient $k_{21}$ variation: (a) conventional resonator vs. spacing $s$, (b) corrugated coupled vs. $C_{f_0}$ ($\epsilon_r = 10.2$, $Z_0 = 55\ \Omega$, $C_L = 1.18\ \text{pF}$, and $f_o = 2\ \text{GHz}$)

corrugations. The $k_{21}$ variation versus center frequency for different corrugations capacitance $C_{f_0}$ is shown in Fig. 4.3a for $\Phi_0 = 40^\circ$, $Z_0 = 48\ \Omega$. Fig. 4.3b presents the percentage change of the filter bandwidth normalized to the minimum bandwidth across the tuning range. It is clear that for the strip-line case, an optimum length of $53^\circ$ results in the lowest bandwidth change [8].

However, for a microstrip line on a high $\epsilon_r$ substrate ($\epsilon_r > 3$), it is not possible to get constant absolute bandwidth characteristics for an octave tuning even at longer electrical lengths. A corrugated coupled-line with 9 unit cells ($\theta_0 = 40^\circ$) and having $C_{fe} = 15\ fF$, $C_{f_0} = 45\ fF$ results in $< 20\%$ bandwidth change
an octave tuning, and is the same as the 53° stripline resonators (note that for conventional lines with 40° electrical length, the corresponding change in bandwidth is 80%). With $C_{fe} = 15$ fF, $C_{fo} = 45$ fF, the $C_L$ for a microstrip line with $\Phi_o = 40^\circ$ at mid-band results in a capacitance ratio of 5.2 for octave tuning Fig. 4.3c. The corresponding $C_L$ for the 53° stripline case is 0.36-2.9 pF which is a capacitance ratio of 8.0.

### 3.2.1 3-Pole Fixed Filter Design

The proposed miniaturized 3-pole fixed filter is shown Fig. 3.6a. The method introduced by [31] together with full-wave simulations is used to for the filter design. Also, source-load coupling is introduced for improved rejection characteristics. The external coupling is done by choosing the tapping position and the matching capacitors $C_m$. The response of a 6%, 0.05 dB ripple 3-pole Chebeychev conventional combline filter (shown in Fig. 3.6b) and the corresponding miniaturized filters are compared in Fig. 3.7. In this case, $\epsilon_r = 10.2$, substrate thickness $h = 1.27$ mm, with a base resonator width of 1.2 mm ($Z_o = 55$ Ω) and a simulated $Q = 170$ at 2 GHz. The conventional combline filter results in $s = 3$ mm and the two miniaturized filters are simulated with $s = 1$ mm and $s = 1.5$ mm. The transmission zero on the upper frequency side is pushed closer to the passband when a high miniaturization ratio is achieved due to the increased capacitive coupling so as to achieve the required $k_{21}$ of 6%.

It is seen that the miniaturized filter is $\sim$ 50% smaller in size as compared to the conventional design (Fig. 3.6). A more compact filter can be achieved using direct tapping and removing $C_m$. The simulated insertion loss is 1.4 dB and 1.0 dB for the conventional and miniaturized designs, respectively. The insertion loss for the miniaturized filter is 0.4 dB better for the same return loss level and resonator lengths and widths due to the corrugations which effectively synthesize a wider resonator.
Figure 3.5: (a) $k_{21}$ versus frequency with different $C_{f0}$, (b) percentage change of the bandwidth normalized to $BW_{\text{min}}$, and (c) $f_{0}$ versus the loading capacitance $C_L$. $C_{fe} = 15fF$ in all simulations.
Figure 3.6: 3-pole combline filter: (a) corrugated $s = 1$ mm, (b) conventional $s = 3$ mm. Figures are to scale.
Figure 3.7: Simulated $S_{21}$ for conventional and miniaturized combline filters, $S_{11}$ is $\pm 20$ dB in the passband.

3.3 Tunable Filter Design

Fig. 3.8 shows the proposed miniature 2-pole tunable filter. The even and odd-mode admittances seen from port A and port B are defined by

\[
Y_{re} = y_{11} + \frac{y_{31}^2 (y_{41} - y_{33} - y_{ime})}{(y_{33} + y_{ke})(y_{44} + y_{ime}) - y_{34}^2} + Y_{Le} \quad (3.10)
\]

\[
Y_{Le} = \frac{y_{41}(y_{34}y_{31} - y_{41}(y_{33} + y_{ke}))}{(y_{33} + y_{ke})(y_{44} + y_{ime}) - y_{34}^2} \quad (3.11)
\]

\[
Y_{ro} = y_{11} + \frac{y_{31}^2 (y_{41} - y_{33} - y_{imo})}{(y_{33} + y_{ko})(y_{44} + y_{imo}) - y_{34}^2} + Y_{Lo} \quad (3.12)
\]

\[
Y_{Lo} = \frac{y_{41}(y_{34}y_{31} - y_{41}(y_{33} + y_{ko}))}{(y_{33} + y_{ko})(y_{44} + y_{imo}) - y_{34}^2} \quad (3.13)
\]

\[
y_{ke} = -jY_{ne} \cot(N \phi_{ne}), \quad y_{ko} = -jY_{no} \cot(N \phi_{no}) \quad (3.14)
\]

\[
y_{ime} = Y_0 + jY_{z2} \cot \phi_{z2} \quad (3.15)
\]

\[
y_{imo} = Y_0 + j2\omega C_{z1} + jY_{z2} \cot \phi_{z2} \quad (3.16)
\]
Figure 3.8: Electrical circuit model of the miniaturized 2-poles filter.

\[
y_{33} = -\frac{j}{2} (Y_{1e} \cot \phi_{1e} + Y_{1o} \cot \phi_{1o}) \\
y_{34} = -\frac{j}{2} (Y_{1e} \cot \phi_{1e} - Y_{1o} \cot \phi_{1o}) \\
y_{41} = \frac{j}{2} (Y_{1e} \csc \phi_{1e} + Y_{1o} \csc \phi_{1o}) \\
y_{41} = \frac{j}{2} (Y_{1e} \csc \phi_{1e} - Y_{1o} \csc \phi_{1o})
\]

where \( Y_{ne,no}, \phi_{ne,no} \), are respectively the even and odd-mode characteristic impedances and electrical lengths of the corrugated coupled lines unit cell calculated as outlined in Section I. \( N \) is the number of the unit cells constituting the corrugated transmission line.

The overall admittance matrix can then be written as

\[
Y = \begin{bmatrix}
\frac{Y_{re} + Y_{ro}}{2} + j\omega C_L & \frac{Y_{re} + Y_{ro}}{2} \\
\frac{Y_{re} + Y_{ro}}{2} & \frac{Y_{re} + Y_{ro}}{2} + j\omega C_L
\end{bmatrix}
\]

(3.21)

The Y-matrix (5.9) represents a filter with a passband centered at \( \omega_0 \) and a fractional bandwidth \( \Delta \) provided that

\[
\text{Im}[Y_{11}(\omega_0)] = 0, \quad \frac{\text{Im}[Y_{12}(\omega_0)]}{b} = \frac{\Delta}{\sqrt{g_1g_2}} = k_{21}
\]

(3.22)
\[ Q_{\text{ext}} = \frac{b}{\text{Re}[Y_{r11}(\omega_0) : \omega_0]} = \frac{g_0 g_1}{\Delta} \]  

(3.23)

where

\[ b = \text{Im}\left[ \frac{\omega_0}{2} \frac{\partial Y_{r11}(\omega_0)}{\partial \omega} \right] \cdot \frac{Y_{r11}(\omega_0)}{2}, \quad Y_{r11} = \frac{Y_{re} + Y_{ro}}{2} \]  

(3.24)

A similar design procedure outlined in [32] can be used to design the tunable filter. Initially, a choice of the design parameters \( Y_1, \phi_1, \phi_2, Y_{z2}, \) and \( \phi_{z2} \) is taken. The resonator admittance and electrical length, \( Y_1 \) and \( (\phi_1 + \phi_2) \), trade off between the resonator \( Q \) and the required tuning capacitance ratio. \( Y_{z2} \) is typically chosen to be a high impedance line so that it has minimal effect on the filter passband and its electrical length \( \phi_{z2} \) is chosen to introduce a far transmission zero at \( \omega_{z2} \) such that \( \cot(\phi_{z2}) = 0 \).

The rest of the design parameters, \( C_L, s_1, s_2, C_o, C_e \) are then determined. An initial value for \( s_1 \) is chosen such that the \( k_{21} \) of the coupled resonators satisfies the bandwidth requirement according to (3.22) at the lowest frequency. Initially, \( C_{fe} \) and \( C_{fo} \) are assumed to be zero and the resonators are uncoupled to the external transformer circuit (replacing \( \Phi_{1e} \) and \( \Phi_{1o} \) by \( \Phi_1 \) value in (5.9)). Next, the \( C_{fe} = 28fF \) and \( C_{fo} = 150fF \) are added so that the \( k_{21} \) is inversely proportional with the center frequency. \( s_2 \) is then chosen to satisfy the \( Q_{\text{ext}} \) according to (5.11). It should be noted that for a narrow bandwidth filter, a small gap ’\( s_2 \)’ is required if the transformer line width is kept the same as the resonators. Therefore a narrower line with a higher characteristic impedance is chosen and the analysis of unsymmetrical coupled-line mode impedance and electrical length is used [33]. With the transformer circuit parameters determined, a more exact value for \( s_1, C_{fe}, C_{fo} \) are obtained using (3.22) with the transformation circuit included. \( C_L \) is determined by the \( Y_{11} \) resonance condition in (3.22). Finally, a weak source-load coupling is introduced to present two transmission zeroes close to the filter passband such that \( Y_{21}(\omega_{z2}) = 0 \). Typically, this coupling capacitance has a high impedance value and has a minimal effect on the passband characteristics. The physical implementation is a small value of interdigital capacitance.
Table 3.1: Dimensions for the fabricated tunable filter (Dimensions are in mm, \( \varepsilon_r = 6.15, 0.62 \) mm. \( w' = w_1, l_t = l_1 \)

<table>
<thead>
<tr>
<th>( w_1/w_{z2}/w_t )</th>
<th>( 1/l_{z2}/l' )</th>
<th>( s_1/s_2 )</th>
<th>( w_d/l_d/g )</th>
</tr>
</thead>
<tbody>
<tr>
<td>1/0.12/0.1</td>
<td>7/11.5/6.4</td>
<td>0.72/0.1</td>
<td>0.25/0.6/0.1</td>
</tr>
</tbody>
</table>

Figure 3.9: Simulated \( k_{21} \), \( Q_{\text{ext}} \) and normalized bandwidth percentage change of the tunable filter.

Fig. 4.8 presents \( k_{21} \), \( Q_{\text{ext}} \) and the normalized bandwidth variation \( (k_{21}f_0 - \min(k_{21}f_0))/\min(k_{21}f_0) \times 100\% \) vs. the resonance frequency. These parameters are calculated using the full-wave simulated Y-matrix per the design method outlined above and includes the effects of resonator bend, open-end fringing, via-holes effects, coupling between adjacent folded resonator transmission lines. Dimensions for the tunable filter are presented in Table I for \( \varepsilon_r = 6.15 \) and \( h = 0.62 \) mm.

### 3.4 Measurements

The S-parameters of both filters were measured with an Agilent E5071B PNA. An SOLT calibration was performed using an Agilent E-cal kit. The reference planes are at the SMA connectors.
3.4.1 Miniaturized 3-Pole Fixed Filter

The filter is shown in Fig. 3.10 and is fabricated on a 1.27 mm Duroid substrate ($\varepsilon_r = 10.2$, Roger RT/Duroid 6010) using a copper etching process [24]. The loading capacitors are AVX Accu-P [25] with a $Q > 200$ at 2 GHz. Dimensions for the filter are presented in Table II. The measured insertion loss is 1.1 dB with a 4.7% (92 MHz) 1-dB bandwidth and a center frequency of 1.94 GHz. The measured return loss is better than 20 dB at both ports. The zero close to the passband is due to the cancelation of the distributed magnetic coupling by the electrical coupling from the corrugations (see Section II). Two additional zeroes appear in the response at 1.4 and 2.5 GHz due to the introduced source-load coupling. The filter passband group delay is shown in (Fig. 3.11a) and is $5 \pm 1$ ns at the 1-dB bandwidth. The simulated and measured results show good agreement (Fig. 3.11a) and the filter has a second passband at 5.5 GHz.

3.4.2 Miniaturized 2-Poles Tunable Filter

The tunable filter is shown in Fig. 3.12 and is fabricated on a 0.62 mm Duroid substrate ($\varepsilon_r = 6.15$, Roger RT/Duroid 6006) [24]. The varactor diode
Figure 3.11: Measured S-parameters vs. simulation for the miniaturized fixed filter.
Figure 3.12: Fabricated constant absolute bandwidth tunable filter on a Duroid substrate ($\epsilon_r = 6.15$, $t = 0.62$ mm).

is GaAs MA46H071-1056 [27] ($C_{j0} = 2.75$ pF, $n = 0.74$, $\phi = 1.2$ V) and $R_s = 1 \pm 0.1$ $\Omega$. The diode results in $C_{\text{total}} = 0.5 - 2$ pF for $V_b = 1 - 20$ V, and a $Q = 57 - 170$ at 1.3-1.9 GHz. A 10 pF DC-blocking chip capacitor (ATC 600S, $R_s = 0.12$ $\Omega$) is connected in series with each GaAs diode to isolate the anode from the ground, (Fig. 3.12). The dc biasing is done using two 10 k$\Omega$ resistors connected in series to reduce the RF-signal leakage through the bias network.

The measured frequency tuning is 1.45-1.89 GHz with an insertion loss of 2.50-2.92 dB (Fig. 5.10). The absolute bandwidth of the filter is $70 \pm 4$ MHz across the tuning range. As expected from Section I, the bandwidth slightly increases till the mid-band frequency and then decreases to maintain the constant absolute bandwidth characteristics (Fig. 3.14). The fitted resonator $Q$ is $60 - 85$ at $V_b = 1 - 20$ V. The measured return loss is better than 17 dB for all states at both ports. The change in the $S_{11}$ shape is due to the change in relationship between $k_{21}$ and $Q_{ex}$ shown in Fig. 4.8 according to [5]

$$k_{21} < \frac{1}{Q_{ex}} + \frac{1}{Q_u} \quad (3.25)$$

The simulated and measured results show good agreement over wide frequency range (Fig. 5.11). The measured third-order intercept point, $IIP_3$ varies from 6-26 dB for a biasing voltage of 1-20 V (Fig. 3.16a). The 1-dB compression point, does not truly represent the large signal S-parameters in filters since the $S_{21}$ response shifts in frequency at lower power levels [32]. Therefore the large
Figure 3.13: Measured S-parameters of the single diode tunable filter. The measured center frequency is 1.45-1.89 GHz for a bias voltage of 1-20 V.
signal $S_{21}$ is measured and the filter can handle 6-20 dBm for a biasing voltage of 4-20 V before a considerable change in $S_{21}$ is observed (Fig. 3.16b). Substantial improvement in the nonlinear tunable filter characteristics can be obtained using back-to-back varactor diodes [32] or RF-MEMS devices [16]-[15].

3.5 Summary

This chapter demonstrates that corrugated microstrip coupled-lines result in miniaturized fixed combline filters for narrow and moderate bandwidths. The corrugated lines can also be used to control the coupling coefficient and result in constant absolute bandwidth filters. This approach can be applied to arbitrary resonator electrical lengths which results in the freedom to choose between the required tuning capacitance ratio and the achieved loaded resonator $Q$.

This chapter is mostly a reprint of the material that is submitted for publication in IEEE Microwave Theory and Techniques, 2009. Mohammed A. El-Tanani; G. M. Rebeiz. The dissertation author was the primary author of this material.
Figure 3.15: Measured S-parameters vs. simulation for the constant bandwidth tunable filter. The bias voltage is 1 V ($f_0 = 1.45$ GHz) and 20 V ($f_0 = 1.98$ GHz).
Figure 3.16: Measured tunable filter nonlinear characteristics.
Chapter 4

Capacitively Compensated 1.4-2.2 GHz Combline Tunable Filters

4.1 Introduction

Combline-filter are based on loaded $< \lambda/4$ resonator which gives it the advantage of size reduction at 1.5-2.5 GHz. A 2-pole suspended strip-line varactor-tuned filter at 3500-4500 MHz with a 3-5 dB insertion loss and a $200 \pm 20$ absolute-bandwidth was analyzed in [8]. The analysis showed that constant absolute bandwidth filter can be achieved for resonators having $53^\circ$ electrical length at the mid-band frequency. However, the analysis is based on strip-line technology and is not applicable to microstrip-line case with due to the even and odd-mode phase velocity mismatches. Kim et al. proposed a stepped impedance resonator to overcome the bandwidth increase in the microstrip case, however this resulted in a very wide resonators and the technique is demonstrated only for narrow tuning range (1.9-2.15 GHz). Sanchez et al. [11] demonstrated a bandwidth control of comb-line filter by inserting a coupling reducer between the combline resonators. This however increase the complexity and size of the filter. In the previous chapter, corrugated-coupled concept was used to achieve constant absolute bandwidth characteristics for comb-line topology. The corrugations are adding distributed capacitive coupling to the resonator magnetic coupling. In this chapter, the capaci-
itive coupling is realized using a localized capacitor between the resonators and its effect on bandwidth characteristics is studied in detail.

4.2 Compensated Microstrip Lines

The proposed topology consists of comb-line coupled resonators with a compensation capacitor added in the coupled section at a distance \( l_1 \) from the short-circuited end (Fig. 4.1). Dishal [31] has demonstrated that narrow bandwidth filters can be described by three fundamental variables: the resonance frequency, \( f_0 \), the coupling coefficient, \( k_{21} \), and the external \( Q, Q_{ext} \). In the analysis below, these parameters will be calculated based on the \( Y \)-matrix of distributed coupled resonators. The \( Y \)-matrix of the compensated coupled resonators loaded with a variable capacitance \( C_L \) is (Fig. 4.1)

\[
Y = \begin{bmatrix}
\frac{Y_{re} + Y_{ro}}{2} + j\omega C_L & \frac{Y_{re} - Y_{r0}}{2} \\
\frac{Y_{re} - Y_{r0}}{2} & \frac{Y_{re} + Y_{r0}}{2} + j\omega C_L
\end{bmatrix}
\] (4.1)

where

\[
Y_{re} = -jY_e \cot(\Phi_{re}), \quad Y_{ko} = -jY_o \cot(\Phi_{1o}) + j2\omega C_c
\] (4.3)

\[
Y_{ro} = \frac{Y_{ko}Y_o + jY_o^2 \tan(\Phi_{ro} - \Phi_{1o})}{Y_o + jY_{ko} \tan(\Phi_{ro} - \Phi_{1o})}
\] (4.4)

The coupling coefficient, \( k_{21} \), of the resonators is

\[
k_{21} = \frac{Im[Y_{12}(\omega_0)]}{b} = \frac{BW}{f_0\sqrt{g_1g_2}}
\] (4.5)

where

\[
b = Im[\frac{\omega_0}{2} \frac{\partial Y_{11}(\omega_0)}{\partial \omega} - \frac{Y_{r11}(\omega_0)}{2}], \quad Y_{r11} = \frac{Y_{re} + Y_{ro}}{2}
\] (4.6)
Figure 4.1: Corrugated coupled lines with a loading capacitor $C_L$.

Figure 4.2: Normalized bandwidth change and the required capacitance ratio for octave tuning vs. resonator electrical length.
Fig. 4.2 presents the maximum change of normalized bandwidth ($\Delta B$) using conventional comb-line microstrip resonators ($C_c = 0$). It is seen that with high dielectric constant substrates, the change in the normalized bandwidth is more severe due to the difference in the even and odd-mode phase velocities. In addition, the 53° electrical length proposed by Hunter [8] for constant absolute bandwidth strip-line resonators is not generally valid for microstrip case for octave tuning. In addition, $k_{21}$ is nearly constant with frequency which results in a nearly constant fractional bandwidth (increasing absolute bandwidth) characteristics. The change in bandwidth is less severe in low dielectric constant substrates since the even and odd mode phase velocities mismatch is smaller. A bandwidth change of < 30% can be achieved for microstrip-line case with $\epsilon_r = 2.92$ and a 60° electrical length, however, the required capacitance ratio for an octave tuning is unpractically high.

By introducing the compensation capacitance, $C_c$, which only affects the odd-mode line characteristics, $k_{21}$ is now a function of the spacing as well as the value and location of $C_c$. The slope of the coupling coefficient, $k_{21}$, can now be synthesized to be inversely proportional with frequency to result in a constant-absolute-bandwidth tunable filter (4.5). Fig. 4.3 shows the $k_{21}$ variation versus center frequency for different $C_c$ values placed in the middle of the coupled resonators and $C_c = 100$ fF results in a constant-absolute-bandwidth case. The required coupling capacitance to achieve the constant absolute bandwidth for different resonators lengths is shown in Fig. 4.4a. The position of the coupling capacitor is at the resonator center. Fig. 4.4b shows the dependence of the capacitance value on the position of the compensation capacitor for a resonator electrical length of 40°. The compensation capacitor value increases as the distance to the short circuit ends is smaller due to the increased magnetic coupling component closer to the short-circuited ends.

The change in the bandwidth for resonators compensated with the optimum capacitance at different positions is shown in Fig. 4.5a. The optimum position for minimal bandwidth change is at the open edge where the magnetic coupling is minimum and the electric coupling is maximum. However, the edge compensated resonators have a higher sensitivity to the value of the compensation capacitance
Figure 4.3: (a) $f_o$ versus the loading capacitance $C_L$ (b) $k_{21}$ versus frequency with different $C_{f_o}$.

(Fig. 4.5b). It is therefore a reasonable compromise to choose the middle of the resonators for the placement of the compensation capacitance. This results in $\Delta B < 18\%$ and a sensitivity of $< 10\%$ to the compensation capacitance for an octave tuning case.
Figure 4.4: (a) $f_o$ versus the loading capacitance $C_L$ (b) $k_{21}$ versus frequency with different $C_{f_o}$.

### 4.3 Tunable Filter Design

A 3-pole comb-line filter based on compensated coupled-lines is shown in Fig. 4.6. The method presented in [31] combined with analytical solution is used in the filter design. Since the compensation capacitors are implemented with
Figure 4.5: (a) $f_o$ versus the loading capacitance $C_L$ (b) sensitivity to compensation capacitor placed at the edge (c) sensitivity to compensation capacitor placed at the middle.
interdigital capacitors, a more accurate Y-matrix is defined as

\[
Y = \begin{bmatrix}
\frac{Y_{re} + Y_{r2}}{2} + j\omega C_L & \frac{Y_{re} - Y_{r0}}{2} \\
\frac{Y_{re} - Y_{r0}}{2} & \frac{Y_{re} + Y_{r0}}{2} + j\omega C_L
\end{bmatrix}
\] (4.7)

where

\[
Y_{(re,ro)} = \frac{Y_{(1e,1o)}Y_{(Ae,Ao)} + jY_{(1e,1o)}^2\tan\Phi_{(1e,1o)}}{Y_{(1e,1o)} + jY_{(Ae,Ao)}\tan\Phi_{(1e,1o)}}
\] (4.8)

\[
Y_{Ae,Ao} = \frac{Y_{(e,o)y\,(se,so)} + jY_{(e,o)}^2\tan\Phi'_{(e,o)}}{Y_{(e,o)} + jy_{(se,so)}\tan\Phi'_{(e,o)}}
\] (4.9)

\[
y_{se} = -jY_{1e}\cot\Phi_{1e}, \; y_{so} = -jY_{1o}\cot\Phi_{1o}
\] (4.10)

and \(Y'_{e,o}\) and \(\Phi'_{e,o}\) are defined in [34] and \(Y_{1e,1o}, \Phi_{1e,1o}\) are the even and odd-mode characteristic admittances and electrical lengths of the un-compensated coupled lines.

The coupling coefficient, \(k_{21}\), is calculated using (4.5). The compensation capacitance has a minimal effect on \(Q_{ext}\) and Fig. 4.7b shows the approximate circuit model to get \(Q_{ext}\),

\[
Q_{ext} = \frac{b}{R_{e}[Y_L(\omega_0)]} = \frac{g_0g_1}{\Delta}
\] (4.11)

where

\[
Y_L = y_{11} + j\omega C_L - \frac{y_{21}^2}{(y_{22} + y_L)}, \; y_L = \frac{j\omega C_m(Y_0)}{Y_0 + j\omega C_m}
\] (4.12)

and \(y_{11}, y_{11}\) and \(y_{21}\) are the Y-parameters of the un-symmetrical coupled lines defined in [33]. When the transformer has the same characteristics impedance as the resonator, \(y_{11}\) and \(y_{21}\) simplify to

\[
y_{11} = y_{22} = \frac{-j}{2}(Y_{1e}\cot\Phi_{1e} + Y_{1o}\cot\Phi_{1o})
\] (4.13)

\[
y_{21} = \frac{j}{2}(Y_{1e}\csc\Phi_{1e} - Y_{1o}\csc\Phi_{1o})
\] (4.14)

The design procedure starts with initial choice for the design values for the resonators parameters \(Y_1, \Phi_1, Y_n, \Phi_n\) and the transformer parameters \(Y_t, \Phi_t\) is
Figure 4.6: Electrical circuit model of the modified combline filter.

Figure 4.7: Electrical circuit model of circuits to calculate filter parameters. (a) coupling coefficient (b) external $Q$
taken. The external coupling circuit is determined by the spacing $s_2$ and $C_m$ and the resonators spacing $s$ and $C_e = C_o = 0$ are chosen to satisfy $k_{21}$ (4.5). Firstly, $s$ is chosen with $C_e = C_o = 0$ to satisfy the coupling condition at the lower frequency and then $C_e = C_o = 0$ are added so that $k_{21}$ has an inversely proportional relationship with the center frequency.

With the initial design parameters determined, full-wave simulation is used to get accurate design parameters. The full-wave simulation is done for the filter (Fig. 4.6) without the lumped components $C_L, C_m, C_{dc}$. The simulated 16-ports matrix is reduced to 3-ports Y-matrix referred to $P_1$, $P_2$, and $P_3$ (Fig. 4.6).

The elements of the loaded Y-matrix ($Y_{16 \times 16}^m$) are given by

$$y_{ii}^m = y_{ii} + j\omega C_i, \quad y_{ij}^m = y_{ij} - j\omega C_{ij}, \quad i \neq j,$$  

where $C_i$ is the lumped-element capacitance at port $i$, and $C_{ij}$ is the lumped element capacitance between ports $i$ and $j$, $i, j = 1, 2, 3, ..., 16$.

The 3-port Y-matrix is then defined as

$$Y_{3 \times 3} = \begin{bmatrix} z_{11} & z_{12} & z_{13} \\ z_{21} & z_{22} & z_{23} \\ z_{31} & z_{32} & z_{33} \end{bmatrix}^{-1}$$  

and $z_{ij}$ are the elements of the matrix $[Z_{16 \times 16}] = [Y_{16 \times 16}^m]^{-1}$.

The $Y_{3 \times 3}$ matrix represents a filter network provided that

$$\text{Im}[Y_{11} (\omega_0)] = \text{Im}[Y_{22} (\omega_0)] = \text{Im}[Y_{33} (\omega_0)] = 0,$$  

$$k_{21} = k_{32} = \frac{\text{Im}[Y_{12}(\omega_0)]}{b} = \frac{\Delta}{\sqrt{g_1 g_2}}$$  

$$Q_{ext} = \frac{b}{\text{Re}[Y_{11}(\omega_0)]} = \frac{g_0 g_1}{\Delta}$$  

where

$$b = \text{Im}\left[\frac{\omega_0}{2} \frac{\partial Y_{11}(\omega)}{\partial \omega} - \frac{Y_{11}(\omega_0)}{2}\right]$$  

The optimized filter dimensions are presented in Table I and the corresponding filter parameters based on (4.17)-(5.11) are shown in Fig. 4.8. It is seen that filter can be tuned from $1.4 - 2.2$ GHz with $\sim 10\%$ change in the filter bandwidth.
Table 4.1: Dimensions for single diode and back-to-back diode Filters (Dimensions are in \( mm \), and Capacitances are in Picofarad, \( \varepsilon_r = 2.92, 0.75 \) \( mm \) Microstrip Substrate is Assumed. \( w_1 = w_2 = w_3, l_1 = l_t \)

<table>
<thead>
<tr>
<th>( w_1/w_t )</th>
<th>( l_1/l_d )</th>
<th>( w_d/g )</th>
<th>( s_1/s_2 )</th>
<th>( C_M/C_{dc} )</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.1/0.5</td>
<td>12/1</td>
<td>0.28/0.15</td>
<td>1.2/0.3</td>
<td>2.5/10</td>
</tr>
</tbody>
</table>

Figure 4.8: \( k_{21}, Q_{ex} \) and normalized bandwidth percentage change of the tunable filter.
4.4 Fabrication and Measurement

The filter is fabricated on a 0.75 mm Duroid substrate ($\epsilon_r = 2.92$, Roger RT/Duroid 6006) using a copper etching process [24]. The varactor diode used is GaAs MA46H071-1056 [27] ($C_{j0} = 2.75$ pF, $n = 0.74$, $\Phi = 1.2$ V) and $R_s = 1 \pm 0.1$ Ω. The diode results in $C_{\text{total}} = 0.5 - 2$ pF for $V_b = 1 - 20$ V, and a $Q = 60 - 170$ at 1.4-1.9 GHz. A 10 pF DC-blocking chip capacitor (ATC 600S, $R_s = 0.12$ Ω) is connected in series with each GaAs diode to isolate the anode from the ground. The dc biasing is done using two 10 kΩ resistors connected in series to reduce the RF-signal leakage through the bias network. The S-parameters of both filters were measured with an Agilent E5071B PNA. The reference planes are at the SMA connectors.

The fabricated 3-pole tunable filter is shown in Fig. 4.9 and the measured frequency coverage is 1.4-2.2 GHz (Fig. 4.10). The measured return loss is better than 13 dB for all states at both ports. The absolute bandwidth of the filter is $157 \pm 7$ MHz across the tuning range with an insertion loss of $2.4 \pm 0.2$ dB (Fig. 4.12). The insertion loss at the highest biasing voltage could be further improved if larger bias resistors are used (> 30 kΩ). The simulated and measured results show excellent agreement (Fig. 4.11). The large signal $S_{21}$ shows that the tunable filter handles 9-12 dBm of input power before a change of frequency response is observed (Fig. 4.11).

4.5 Summary

Constant absolute bandwidth filter has been demonstrated using the compensated coupled-lines technique. Middle compensation position was shown to give good compromise between the bandwidth sensitivity to capacitance tolerance and maximum change in constant absolute bandwidth.

This chapter is mostly a reprint of the material that will be submitted for publication in IEEE Microwave Theory and Techniques, 2009. Mohammed A. El-Tanani; G. M. Rebeiz. The dissertation author was the primary author of this
Figure 4.9: Fabricated 3-poles capacitively compensated tunable filter on a Duroid substrate ($\epsilon_r = 6.15$, $t = 25$ mils.)

material.
Figure 4.10: Measured S-parameters of the 3-poles partially corrugated tunable filter. The center frequency is 1.52-1.95 GHz for a bias voltage of 1.8-30 V.
Figure 4.11: Measurement vs. simulation for the 3-poles capacitively compensated tunable filter. The bias voltage is 1.4 V ($f_0 = 1.52$ GHz) and 20 V ($f_0 = 2.1$ GHz)
Figure 4.12: Performance summary of the 3-poles capacitively compensated tunable filter.

Figure 4.13: Large signal $S_{21}$ at different input power levels. The bias voltage is 2 V ($f_0 = 1.50$ GHz) and 7 V ($f_0 = 1.9$ GHz).
Chapter 5

High Performance 1.5-2.5 GHz RF-MEMS Tunable Filters for Wireless Applications

5.1 Introduction

RF MEMS tunable filters have recently demonstrated high-$Q$, wide tuning range and very high linearity designs in the 0.1 to 10 GHz range [1-8], especially with capacitive-based switch networks. This is due to the very low loss seen in capacitive RF MEMS devices, their large capacitance ratio ($C_r = 3 - 10$), and their inherent mechanical response which does not allow the generation of intermodulation products [10]. In fact, in most of the filters presented in literature, it is the planar resonator $Q$ which limits the overall filter $Q$, and not the inherent RF MEMS device loss. Suspended resonators or cavity-based designs are currently emerging which result in a substantially higher performance, but at the expense of a relatively large volume, which is not suitable for compact and low-cost wireless applications [6,8,10-11].

This chapter presents two planar RF MEMS tunable filters designed specifically as a demonstration of this technology for the wireless bands. The filters are integrated on a ceramic substrate ($h = 0.74$ mm, $\epsilon_r = 9.9$) in order to result
in a small size, while still keeping a high resonator $Q$. Furthermore, the design employs a distributed capacitive coupling between the resonators which results in constant absolute bandwidth over the tuning range while still using a short electrical resonator length [12]. The distributed capacitive coupling introduces electric coupling which is in anti-phase with the conventional magnetic coupling and results in reduced resonator spacing for moderate to narrow-bandwidth combline filters. Furthermore, a wideband transformer circuit is used to achieve excellent impedance matching across the 1.5-2.5 GHz band without the need for tuning element in the transformer. The RF MEMS devices are built directly on the ceramic substrate together with the resonators using a thick electroplated metal process so as to result in a high $Q$ at 2.5 – 3.5 GHz, and provide both digital and analog tuning capabilities [35]. This tuning agility is important in order to get the same loading capacitance at each resonator and an excellent frequency response, especially for the narrowband design.

5.2 Design

5.2.1 Admittance Matrix

Fig. 5.1a shows the miniature 2-pole tunable filter with wide-band tuning range. The filter is based on corrugated coupled-lines inverter [34] with an improved input impedance transformer. The even and odd-mode admittances seen from port A and port B are defined by

$$Y_{re} = y_{11} + \frac{2y_{41}(y_{11} - y_{33} - y_{ime})}{y_{33} + y_{ke})(y_{44} + y_{ime}) - y_{34}^2} + Y_{Le}$$  \hspace{1cm} (5.1)$$

$$Y_{Le} = \frac{y_{41}(y_{34}y_{31} - y_{41}(y_{33} + y_{ke}))}{y_{33} + y_{ke})(y_{44} + y_{ime}) - y_{34}^2}$$  \hspace{1cm} (5.2)$$

$$Y_{ro} = y_{11} + \frac{y_{33}^2(y_{11} - y_{33} - y_{imo})}{y_{33} + y_{ko})(y_{44} + y_{imo}) - y_{34}^2} + Y_{Lo}$$  \hspace{1cm} (5.3)$$

$$Y_{Lo} = \frac{y_{41}(y_{34}y_{31} - y_{41}(y_{33} + y_{ko}))}{y_{33} + y_{ko})(y_{44} + y_{imo}) - y_{34}^2}$$  \hspace{1cm} (5.4)$$
Figure 5.1: Electrical model of the 2-pole tunable filters: (a) wide-band design (b) narrow-band design.
\[ y_{ke} = -jY_e' \cot(N\phi'_e), \quad y_{ce} = jY_z \cot \phi_z + y_f \]  
\[ y_{ko} = -jY_o' \cot(N\phi'_o), \quad y_{co} = y_a + y_f \]  
\[ y_{im(e,o)} = \frac{j\omega y_{c(e,o)}C_{m1}}{y_{c(e,o)} + j\omega C_{m1}}, \quad y_p = \frac{j\omega Y_0C_m}{Y_0 + j\omega C_m} \]  
\[ y_f = \frac{y_fY_m + jY_m^2\tan \phi_m}{Y_m + jy_p \tan \phi_m}, \quad y_a = \frac{j\omega C_zY_z - \omega C_zY_m^2 \tan \phi_z}{Y_z - \omega C_z \tan \phi_z} \]  

and \( y_{33}, y_{11}, y_{44}, y_{31}, y_{41}, y_{33} \) are the unsymmetrical coupled-lines Y-parameters found in [33]. \( Y_e', Y_o', \phi'_e, \phi'_o \) are respectively the even and odd-mode characteristic impedances and electrical lengths of the corrugated coupled lines unit cell [34], and \( N \) is the number of the unit cells.

The overall admittance matrix can then be written as

\[
Y = \begin{bmatrix}
\frac{Y_{re} + Y_{ro}}{2} + j\omega C_L & \frac{Y_{re} + Y_{ro}}{2} \\
\frac{Y_{re} + Y_{ro}}{2} & \frac{Y_{re} + Y_{ro}}{2} + j\omega C_L
\end{bmatrix}
\]  

(5.9)

The Y-matrix for the 1.5 – 2.0 GHz tunable filter shown in Fig. 5.1a is the same as (5.9) with the change of \( y_{ime} \) and \( y_{imo} \) definitions according to

\[ y_{ime} = y_{imo} = \frac{y_fY_{m2} + jY_{m2}^2 \tan \phi_{m2}}{Y_{m2} + jy_f \tan \phi_{m2}} \]  

(5.10)

The external coupling circuits presented in Fig. 5.1 are synthesized to achieve impedance matching across the tuning range without the need of tunable components in the input network. \( Q_{ext} \) is weakly dependent on the enter-resonator coupling, \( k_{21} \), for narrow to moderate bandwidth filters [31], and Fig. 5.2 shows the first-order model for \( Q_{ext} \) calculations. The reference port for \( Q_{ext} \) is chosen at the loading capacitance position to uncouple \( C_L \)

\[
Q_{ext} = \frac{b}{\text{Re}[Y_{re}(\omega_0)]} = \frac{g_0g_1}{\Delta}, \quad b = \text{Im} \left[ \frac{\omega_0 \partial Y_{re}(\omega_0)}{2} - \frac{Y_{re}(\omega_0)}{2} \right]
\]  

(5.11)

where \( \omega_0 \) is the passband center frequency and \( \Delta \) is the filter fractional bandwidth and \( Y_e', Y_o' \) are replaced by the uncoupled transmission-line parameters in (5.5).

The wide-band transformer circuit presented in Fig. 5.2a can be used to synthesize the same \( Q_{ext} \) value at a specific frequency but with different slopes.
Figure 5.2: (a) Approximate model of the wide-tuning range transformer, (b) simulated resonator $Q_{ex}$ with different transformer parameters, $\epsilon_r = 9.9$ (alumina), $w_1 = 0.85$ mm, $l_1 = 4.5$ mm, $l_t = 5.5$ mm, $w_t = 0.15$ mm, and $s_1 = 0.12$ mm.
The $Q_{ext}$ for different matching capacitors is presented in Fig. 5.3 and one can synthesize a $Q_{ext}$ for tunable filters with constant absolute bandwidth or constant fractional bandwidth with standard $C_m$ values. The same technique can be applied for the input matching of Fig. 5.1b.

### 5.2.2 Implementation

The narrow bandwidth and wide bandwidth tunable filters are designed with constant absolute bandwidth of 70 MHz and 110 MHz and an associated tuning range of 1.5-2.0 GHz and 1.5-2.5 GHz, respectively. The design procedure is based on (5.9) as outlined in [34]. However, to take into account the physical layout parasitics (bends, via-hole inductance, parasitic coupling, etc) the final design parameters are based on a full-wave Y-matrix. A full-wave simulation for the filter structure without any of the capacitors was done in Sonnet [23] and the 12-ports Y-matrix is extracted. This matrix is then transferred into a 2-port matrix relative to the tunable capacitors positions by terminating the 12 ports Y-matrix with the tunable and matching capacitors. The elements of the loaded Y-matrix ($Y_{12 \times 12}^m$) are given by

$$y_{ii}^m = y_{ii} + j\omega C_i, \ y_{ij}^m = y_{ij} - j\omega C_{ij}, \ i \neq j,$$

where: $C_i$ is the lumped-element capacitance at port $i$, and $C_{ij}$ is the lumped element capacitance between ports $i$ and $j$, $i, j = 1, 2, 3, ..., 12$.

The 2-port Y-matrix is then defined as:

$$Y_{2 \times 2} = \frac{1}{(z_{11}z_{22} - z_{12}z_{21})} \begin{bmatrix} z_{22} & -z_{21} \\ -z_{12} & z_{11} \end{bmatrix}$$ (5.13)

and $z_{ij}$ are the elements of the matrix $[Z_{12 \times 12}]=[Y_{12 \times 12}^m]^{-1}$.

Fig. 5.3 shows the extracted coupling coefficient $k_{21}$ and $Q_{ext}$ for both filters, and Table I shows the tunable filters dimensions. The matching capacitors used are $C_m = 2.85 \text{ pF}$ for the narrow-bandwidth filter and $C_m = 2.85 \text{ pF}$, $C_{m1} = 3.1 \text{ pF}$ for the wide-bandwidth filter.
Table 5.1: Dimensions for the fabricated wide-bandwidth tunable filter (Dimensions are in mm, $\varepsilon_r = 9.9$, h=0.76 mm). For the NBW filter: $w_{m2} = 0.72$ mm, $l_{m2} = 1.5$ mm.

<table>
<thead>
<tr>
<th>$w_1/w'$</th>
<th>$w_t/w_m/w_z$</th>
<th>$l_1/l_m/l'$</th>
<th>$s_1/s_2$</th>
<th>$w_d/l_d/g$</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.8/0.9</td>
<td>0.15/0.13/0.17</td>
<td>4.6/7.6/4</td>
<td>0.4/0.2</td>
<td>0.17/0.37/0.025</td>
</tr>
<tr>
<td>1/1</td>
<td>0.27/0.72/−</td>
<td>6.2/2.4/5</td>
<td>0.9/0.12</td>
<td>0.37/0.75/0.12</td>
</tr>
</tbody>
</table>

Figure 5.3: Simulated $k_{21}$, $Q_{ex}$ and normalized bandwidth percentage change of the tunable filter.
The simulated capacitance value for the 1.5-2.0 GHz (1-dB bandwidth 70 MHz, \(C_L = 0.5 - 2.2\) pF) and the 1.5-2.5 GHz (1-dB bandwidth 110 MHz, \(C_L = 0.5 - 2.7\) pF) are shown in Fig. 5.4 for a 4-bit implementation. The required capacitance ratio is 4.5-5.5, and this can be achieved using RF-MEMS switched capacitors [?].

### 5.2.3 RF-MEMS Tunable Capacitive Network

**RF-MEMS device**

A cantilever-switch with digital and analog tuning capabilities is used in this work [35]. The switch is based on 3.5-4 \(\mu m\) thick gold beam and results in \(C_u = 50 - 70\) fF and \(C_d = 200 - 300\) fF depending on the design (Fig. 5.5c). The RF-MEMS switch utilizes a zipping effect (Fig. 5.5a) with a hold-down bias voltage \(V_h\) for analog tuning which makes it ideal for continuous frequency coverage between the digital states. Alternatively, the analog tuning can be achieved using the pull-down voltage \(V_p\), by applying a higher \(V_p\) once the switch is pulled-down. This eliminates the need of the large MIM capacitor connected in series with the devices (Fig. 5.5b).

This device has been tested without failures to > 65 billion cycles (at 16 kHz under partial vacuum, with \(V_p = 65\) V), under hot switching conditions (\(f_0 = 10\) GHz, \(P_{in} = 1\) W). Such large cycle counts are obtainable because there is always a 0.4 – 0.5 \(\mu m\) air-gap between the cantilever and pull-down electrode which results in a low electric field and no substrate charging.

**Tuning Network**

The 3-bit tunable network is shown in Fig. 5.6. Due to the large required capacitance, several MEMS devices are placed in a parallel configuration for bits 1 and 2 and results in a very low loss network. A fixed series MAM capacitor is not used in this network since the analog tunability of the device removes the need of fine capacitance control. The main mechanisms of loss in RF-MEMS networks are the conductive losses and the bias-line effects. To ensure a low-loss network, the
Figure 5.4: Simulated tunable filters center frequency versus loading capacitance $C_L$.

Length of the thin metal in the RF-MEMS device is as short as possible and is 65 $\mu m$ (see Fig. 5.5).

The SiCr bias-lines are placed orthogonal to the high electric field in the resonator gap to reduce the coupled RF-current to the bias lines [15]. The bias lines width is 10 $\mu m$ close to the resonators and 20 $\mu m$ away from the resonators to further reduce the loss. The bias lines are not directly attached to the device but coupled through the small capacitance between the beam and pull-down electrode ($C_p = 70 \, \text{fF}, X_p = -j1.2 \, \text{k}\Omega \text{ at } 2 \, \text{GHz}$) which further reduces the RF-energy leakage. The total bias-line length is 2.7 mm and chosen to result in a bias resistance of $< 500 \, \text{k}\Omega$ for switching speed purposes.

5.3 Fabrication Process

The filters are fabricated on an alumina 99.6% substrate ($\epsilon_r = 9.9$). Via-holes with 350 $\mu m$ diameter are laser drilled on a 1 mm thick substrate and the substrate is lapped and fine polished to a final thickness of 0.76 mm. Next the via-holes are filled with a gold electroplating process and again fine polished. A
Figure 5.5: (a) Zipping effect in the high-Q tunable capacitive cantilever, (b) the fabricated high-Q tunable capacitive cantilever, (c) capacitive cantilever capacitance versus the bias voltage $V_p$. 
Figure 5.6: (a) The high-Q RF-MEMS cantilever based capacitive network, (b) electrical circuit model.

Figure 5.7: Fabrication process of the tunable filters.
layer of TiW/Au (0.1/2 µm) is first sputtered on both sides of the substrate [7]. The front side metal is patterned and etched to form pads around the via-holes while the metal on the back-side is protected to make the microstrip ground plane (Fig. 5.7(b)). Second, a SiCR layer (1700 Å) is sputtered and patterned to form the high resistance bias lines. A 600/3300 TiW/Au layer is sputtered and patterned to form the RF-MEMS bottom electrode and the filter (Fig. 5.7(c)). Next, a 1500 dielectric (Si₃N₄) layer is deposited using plasma enhanced chemical vapor deposition (PECVD) and patterned with reactive ion etching (RIE) to form the dielectric layer (Fig. 5.7(d)).

Next, a sacrificial layer (PMMA) is used with a thickness of 1.5 µm, and patterned using an (RIE) machine with evaporated Ti (800 Å) as a mask layer. Next, a seed Ti/Au/Ti layer (200/3000/200 Å) is sputtered and selectively electroplated to 3.5 µm to form the cantilevers and the filter metal (Fig. 5.7(f)). The filter transmission lines are then selectively electroplated for an additional 4 µm to reduce the RF losses (5.7(g)). The total filter thickness is 8 – 8.5 µm which is three times the skin depth at 1.5 GHz. The seed-layer is then etched in the areas that were non electroplated. The final step consists of removing the sacrificial layer in a solvent and in drying the device using a super-critical point drier (Fig. 5.7(h)).

The measured pull-down voltage of a MEMS switched capacitor on the same wafer is ≈ 42 V which corresponds to a spring constant of ≈ 34 N/m. The optical profilimeter shows that the beam is curled-down by about 0.2 µm due to vertical stress gradient across the beam (average of 3 MPa/µm). The measured C-V curve is shown in Fig. 5.5 with upstate capacitance \( C_u = 65 \) fF, and a down-state capacitance \( C_d = 185 – 300 \) fF, for a \( V_p \) between 40 – 80 V. The bias line resistance is ≈ 2 kΩ/□ for this fabrication run.

### 5.4 Measurements

The S-parameters of both filters were measured with an Agilent E5071B PNA, and the reference planes are at the SMA connectors. The filters are measured
Figure 5.8: Measurement test fixture for the RF-MEMS tunable filters.

Figure 5.9: Fabricated narrow-bandwidth tunable filter.
in a shielded box with teflon pushers on the the top cover to assure a good electrical contact between the filter ground plane and the box (no solder used on the ground plane). The box has also an opening on one side for DC-probing (Fig. 5.8). The RF MEMS capacitive switches were actuated using a 1 kHz bipolar waveform to reduce the effects of substrate charging. The matching capacitors are implemented with surface mount high-$Q$ capacitors (0201 size) [25].

Figure 5.10: Measured S-parameters of the narrow-bandwidth tunable filter. The measured center frequency is 1.55-2.05 GHz.
5.4.1 Narrow-Bandwidth Miniaturized RF-MEMS Tunable Filter

A photograph of the fabricated tunable filter is shown in Fig. 5.9. The measured filter response covers a tuning range of 1.55-2.04 GHz, with an insertion loss and 1-dB absolute bandwidth of 1.9 – 2 dB and 72±3 MHz, respectively (Fig. 5.10 and Table II). The return loss is better than 20 dB at all states at both ports. The fitted resonator $Q$ is 125 – 165 at 1.55 – 2.04 GHz tuning range. The insertion loss is also measured with the top box cover removed and showed no improvement. This is due the negligible filter radiation loss due to the substrate thickness (0.76 mm) and high dielectric constant used ($\epsilon_r = 9.9$). The measured insertion loss of a similar filter fabricated without the bias line to bit 1 switches (see Fig. 5.6) showed an improvement of only 0.1 dB. The exact capacitance value of the switches varies across the wafer and therefore simulation results with fitted capacitance value is obtained and shows good agreement with the measured filter response (Fig. 5.11)

Table 5.2: Summary of the Measured RF-MEMS Narrow Bandwidth Tunable Filter, $f_o$ in GHz

<table>
<thead>
<tr>
<th>$f_o$ (GHz)</th>
<th>$BW$ (MHz)</th>
<th>$IL$ (dB)</th>
<th>$f_o$ (GHz)</th>
<th>$BW$ (MHz)</th>
<th>$IL$ (dB)</th>
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<tbody>
<tr>
<td>1.55</td>
<td>69</td>
<td>1.93</td>
<td>1.81</td>
<td>75</td>
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<td>69</td>
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<td>1.62</td>
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<td>1.64</td>
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<td>1.91</td>
<td>73</td>
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<td>73</td>
<td>1.92</td>
<td>1.96</td>
<td>73</td>
<td>1.98</td>
</tr>
<tr>
<td>1.72</td>
<td>69</td>
<td>1.96</td>
<td>2.01</td>
<td>73</td>
<td>1.98</td>
</tr>
<tr>
<td>1.78</td>
<td>75</td>
<td>1.92</td>
<td>2.04</td>
<td>72</td>
<td>1.99</td>
</tr>
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</table>
Figure 5.11: Measured vs. simulated S-parameters for the narrow-bandwidth tunable filter ($f_o=1.55$ GHz $C_L=1.85$ pF, $f_o=1.78$ GHz $C_L=1.87$ pF, $f_o=2.05$ GHz $C_L=0.52$ pF).
5.4.2 Wide-Bandwidth Miniaturized RF-MEMS Tunable Filter

A photograph of the fabricated tunable filter is shown in Fig. 5.12. The measured filter response covers a tuning range of $1.56 - 2.48$ GHz with an insertion loss and 1-dB absolute bandwidth of $1.9 - 2.2$ dB and $115 \pm 10$ MHz, respectively (Fig. 5.13 and Table III). The return loss is better than 14 dB at all states at both ports. The fitted resonator $Q$ is 86-116 at $1.6 - 2.5$ GHz tuning range.

The insertion loss is also measured with the top box cover removed and showed no improvement. Again, simulation results with fitted capacitance values show good agreement with the measured filter response (Fig. 5.14). The rejection at the high frequency side is limited by the source-load coupling path. Simulations show that the rejection improves by additional 10 dB at 4 GHz with the source-load coupling removed.

5.4.3 Non-linear Measurements

The RF-signal across the RF-MEMS capacitance generates a mechanical force proportional to $V_{rms}^2$ that is acting on the tip of cantilever. This RF-voltage
Figure 5.13: Measured S-parameters of the wide-tuning tunable filter. The measured center frequency is 1.56-2.48 GHz.
Figure 5.14: Measured vs. simulated S-parameters for the wide-bandwidth RF-MEMS tunable filter. ($f_o=1.56$ GHz $C_L=2.74$ pF, $f_o=1.77$ GHz $C_L=1.87$ pF, $f_o=2.2$ GHz $C_L=1$ pF, $f_o=2.48$ GHz $C_L=0.5$ pF)
Table 5.3: Summary of the Measured RF-MEMS Wide Bandwidth Tunable Filter, $f_0$ in GHz

<table>
<thead>
<tr>
<th>$f_0$</th>
<th>$BW$ (MHz)</th>
<th>$IL$ (dB)</th>
<th>$f_0$</th>
<th>$BW$ (MHz)</th>
<th>$IL$ (dB)</th>
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<td>1.56</td>
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<td>1.60</td>
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<td>2.10</td>
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<td>114</td>
<td>2.00</td>
<td>2.22</td>
<td>126</td>
<td>2.04</td>
</tr>
<tr>
<td>1.77</td>
<td>112</td>
<td>1.97</td>
<td>2.27</td>
<td>125</td>
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<td>1.82</td>
<td>117</td>
<td>1.94</td>
<td>2.34</td>
<td>124</td>
<td>2.00</td>
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<td>2.39</td>
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<td>120</td>
<td>1.92</td>
<td>2.44</td>
<td>119</td>
<td>2.04</td>
</tr>
<tr>
<td>1.94</td>
<td>123</td>
<td>1.92</td>
<td>2.48</td>
<td>115</td>
<td>2.03</td>
</tr>
</tbody>
</table>

swing causes a non-linear capacitance behavior which results in small-signal distortion. With large-signal voltage, this also results in self-biasing of the RF-MEMS cantilevers and non-optimal filter response. The small-signal and large signal measurements setup are shown in Fig. 5.15. All the nonlinear measurements are done in the up-state position since this results in the maximum RF-voltage swing across the RF-MEMS cantilevers and therefore the worst nonlinear characteristics. The measured input $P_{1dB}$ show that both tunable filters can handle $\sim 25$ dBm of input power before self-biasing occurs (Fig. 5.15c). This corresponds to a simulated $V_{rms}$ of 16 V across the RF-MEMS capacitance. The switch has a lower pull-in voltage in this case because the spring constant defined at the cantilever tip is lower than the spring constant defined above the pull-down electrode. Using a thicker beam results in a higher spring constant (at the tip of the cantilever) which increases the power handling capability of the filter at the expense of a higher control voltage.

The $IIP_3$ of the tunable filters is measured vs. the difference frequency, $\Delta f$, and results in $IIP_3 > 35$ dBm for $\Delta f > 100$ kHz. For the RF-MEMS switches, the intermodulation component follows the mechanical response of the bridge, and the $IIP_3$ level increases by 20 dB/decade for $\Delta f > f_m$, where $f_m$ is
Figure 5.15: (a) $P_{1dB}$ measurement setup, (b) $IIP_3$ measurement setup (c) Measured $P_{1dB}$, (d) Measured $IIP_3$. 
the bridge mechanical resonance frequency [10]. The $IIP_3$ measurement shows a mechanical resonance frequency around 30 kHz which is same as expected for a single device [35].

A W-CDMA signal with quadrature phase shift keying (QPSK) modulation and chip rate of 3.84 Mcps is also applied to the input of the RF-MEMS tunable filters at large-signal level. The output spectrum shows no distortion or signal growth occurred as long as the signal power is below the 1dB compression point (Fig. 5.16). This was predicted theoretically by [36] and shows the excellent linearity and power handling of RF-MEMS tunable filters.

5.5 Summary

This chapter demonstrated that RF MEMS tunable filters is a suitable technology for wireless systems in the 1.5—2.5 GHz, and can result in a narrowband filter response (72 MHz) and low insertion loss (< 2 dB). Also, the filters can handle at least 300 mW of RF power with very low distortion when characterized using a two-tone technique or using a W-CDMA signal (ACPR, etc.). A smaller filter can be implemented in the future with the use of high dielectric constant ceramic substrates. These may require higher capacitance loading, which can also be achieved using RF MEMS devices.

This chapter is mostly a reprint of the material that is submitted for publication in IEEE Microwave Theory and Techniques, 2009. Mohammed A. El-Tanani; G. M. Rebeiz. The dissertation author was the primary author of this material.
Figure 5.16: Measured filter output spectrum for WCDMA input at different input power levels, (a) narrow-bandwidth filter, (b) wide-bandwidth filter.
Chapter 6

Conclusion and Future Work

6.1 Conclusion

The tunable filters presented in this dissertation demonstrated substantially improved linearity and frequency tunability while maintaining constant absolute bandwidth across the tuning range. The improved linearity is due to the back-to-back diode configuration together with the biasing circuit which was supported by detailed Volterra series analysis. The measured results for tunable filters built of 1.55-1.90 GHz and showed an IIP3 improvement of $>13$ dB for $\Delta f = 1$ MHz.

Detailed modeling of the novel corrugated-coupled lines resonators showed that the coupling coefficient can be synthesized to be inversely proportional to the center frequency. This technique was used to design a 1.45-1.90 GHz tunable filter with $70 \pm 4$ MHz constant absolute bandwidth over this tuning range. This technique also demonstrated 3-poles fixed filter which is $\sim 2x$ smaller than the conventional design. The fixed filter is designed at 1.94 GHz with a bandwidth of 94 MHz and an insertion loss of 1 dB.

Detailed analysis of the conventional coupled-lines showed that the 53° proposed by Hunter et al. [8] is only valid for the strip-line case. For microstrip lines, the compensated coupled-lines scheme is proposed and fully studied. This technique is used to design a 1.40-2.10 GHz 3-poles tunable filter with a bandwidth of $150 \pm 10$ MHz across the tuning range.

High Q RF MEMS switched capacitor was used to design high performance
RF MEMS tunable filters with constant absolute bandwidth for the 1.5 − 2.0 and 1.5 − 2.5 GHz wireless band with an associated bandwidth of 70 MHz and 110 Mhz respectively. Ceramic substrate was used for size miniaturization. The filters showed an $IIP_3 \gg 33$ dBm and also showed no distortion when tested under wideband CDMA waveforms up to 24.8 dBm. The insertion loss of both filters are $< 2$ dB which shows that RF MEMS results in high performance in term of linearity, tunability and loss.
6.2 Future Work

In cognitive radio systems, the radios themselves sense the available spectrum and decide on the communications channel (frequency, bandwidth and modulation scheme) to use [3]. It is therefore, important to design a tunable filter with changing center frequency and bandwidth. The compensated capacitively compensated comb-line filter proposed in chapter 3 can be further extended to have bandwidth tunability (Fig. 6.1). To get maximum sensitivity to the tuning capacitance and therefore highest bandwidth tuning capability, the location of the coupling capacitance should be at the open end of the resonator. This however results in small capacitance values and therefore the position will be adjusted based on the used technology and the tunable capacitance values.

The source-load coupling introduce in Chapter 2 can be further extended to result in a tunable filter with tunable zero characteristics. This gives the agility to not only tune the center frequency but also the rejection level for strong out-band interference signals. The proposed filter topology is shown in Fig. 6.2. The required capacitance values are shown in Fig. 6.3 and Table I. The simulated response assumed a capacitance $Q = 200$. The simulated S-parameters are shown
in Fig. 6.2 and the filter performance is summarized in Table II.

Table 6.1: Capacitance values for the tunable zeroes filter

<table>
<thead>
<tr>
<th>Zero state</th>
<th>$C_z$ (pF)</th>
<th>$C_{z2}$ (pF)</th>
<th>$C_m$ (pF)</th>
</tr>
</thead>
<tbody>
<tr>
<td>State 1</td>
<td>0.01</td>
<td>0.9</td>
<td>0.85</td>
</tr>
<tr>
<td>State 2</td>
<td>0.2</td>
<td>0.9</td>
<td>0.85</td>
</tr>
</tbody>
</table>

Figure 6.2: Tunable filter with tunable zeroes.

Figure 6.3: Required loading capacitance.
Figure 6.4: Simulated $S_{21}$ (a), and $S_{11}$ (b).

Table 6.2: Simulated tunable filter with tunable zeroes

<table>
<thead>
<tr>
<th>$f_o$ (GHz)</th>
<th>1.65</th>
<th>1.70</th>
<th>1.77</th>
<th>1.84</th>
<th>1.92</th>
<th>2.0</th>
<th>2.1</th>
<th>2.2</th>
</tr>
</thead>
<tbody>
<tr>
<td>$IL$ (dB)</td>
<td>2.3</td>
<td>2.2</td>
<td>2.05</td>
<td>1.91</td>
<td>1.83</td>
<td>1.73</td>
<td>1.6</td>
<td>1.5</td>
</tr>
<tr>
<td>$FBW%$ (dB)</td>
<td>3.7</td>
<td>3.77</td>
<td>3.78</td>
<td>3.83</td>
<td>3.94</td>
<td>4.04</td>
<td>4.11</td>
<td>4.2</td>
</tr>
</tbody>
</table>
Appendix A

C-Band Low-Loss Phase Shifter

$> 360^\circ$ for WLAN Applications

A.1 Introduction

Wireless systems in the 5.6-6.0 GHz range are currently employing two different antennas for propagation diversity, and a single-pole double-throw switch is needed to select between these antennas. The insertion loss of the switch and associated t-lines is 1.5 dB at 5.8 GHz which affect the receiver noise figure and the data rate. A better design would be to use a 2-4 element phased array where each antenna is followed by a phase shifter and the total power is combined in a 1:2 or 1:4 power combiner. If the phase shifter loss is kept at $<2$ dB, this system would result in a better performance since the phase shifter/power combiner loss is mitigated by the increase in the antenna gain. Furthermore, the phased array allows nulls in the receive pattern which can attenuate an offending interferer by 20 dB. A literature review of 5-6 GHz phase shifters show many different designs, but none with very low insertion loss. F. Ellinger et al. presents a reflective-type phase shifter MMIC at C-band with $360^\circ$ phase-control range for smart antenna combining [37], F. Ellinger et al also presents Varactor-loaded transmission-line phase shifter at C-band using lumped elements [38]. The literature even shows some Duroid based phase shifters at lower frequency and with higher loss. A.
Keerti, et al. presents high power linearized RF phase shifter using Anti-Series diodes [39]. This work presents a bi-directional reflection-type phase shifter based on a complex load design and Schottky varactor diodes with very low insertion loss, excellent match, and a > 360° phase shift at 5.8 GHz.

### A.2 Design

A reflection-type phase shifter based on a quadrature coupler is shown in Fig. A.1a. In this classic design, with a varactor used as the capacitive load (L = 0 nH), the maximum phase shift is 74° at 6 GHz with a capacitance change of 4.0 (0.25-1 pF). The phase shift can be increased to 154° by adding a 1.75 nH inductor in series with the varactor. The maximum phase shift can be increased to 360° by using two different series resonating loads in a parallel configuration (Fig. A.1b), typically called a "complex load" [40]. In this design, $L_1$ is chosen such that it series-resonates with $C_{min}$, $L_2$ is chosen such that it series-resonates with $C_{max}$ such that:

$$L_{12} = \frac{1}{\omega_0^2 C_{min,max}} \quad (A.1)$$

The phase of each series resonance is 0° and therefore, this design guarantees a 360° phase shift when the varactors are biased from $C_{min}$ to $C_{max}$.
It is important to look at the loss of the complex load at the parallel resonance point since the load will have a higher loss when it is totally resistive (no reactive component). At the series resonance points and with a varactor resistance of $R_s < 3\, \Omega$ at 6 GHz, the loss is about 1 dB. However, at the parallel resonance, the equivalent impedance ($Z_p = R_{eq}$) is:

$$R_{eq} = \frac{R_s}{2} + \frac{X_p^2}{2R_s} \approx \frac{X_p^2}{2R_s} \quad \text{(A.2)}$$

where $X_p$ is the equivalent reactance of the complex load and $R_s$ is the series resistance of each diode.

$$X_p = \pm \frac{\omega_o}{2} (L_1 - L_2) = \pm \frac{1}{2\omega_o} \left[ \frac{1}{C_{min}} - \frac{1}{C_{max}} \right] \quad \text{(A.3)}$$

and for $C_r = 4$ (0.25-1 pF), $R_s = 3\, \Omega$, this results in $R_{eq} = 285\, \Omega$ and a reflection loss of 3 dB. It is seen that choosing a varactor with a high capacitance ratio ($C_{max}/C_{min}$) will result in a high $X_p$ and increase the parallel resonance resistance by $X_p^2$, which effectively increases the $Q$ of the parallel resonance and reduces the reflection loss. In order to further increase $R_p$ and reduce the reflection loss, a step-up matching network is typically used (Fig. A.1c). However, the matching network ($L_m$, $C_m$) itself has a finite $Q$ and will increase the loss at the series resonance points. With $L_m = 0.86\, \text{nH}$ and $C_m = 0.55\, \text{pF}$, the equivalent input impedance at the parallel resonance point is increased to 570 $\Omega$ and the reflection loss is reduced to 1.5 dB. The circuit model of the GaAs M/A-COM MA46H200-1056 surface-mount varactor diode is shown in Fig. A.2. The diode resistance varies between 0.93 $\Omega$ (VR=15 V) and 4 $\Omega$ (VR=2 V). The usable capacitance ratio is 4 when $C_p$ is included in the total diode capacitance ($C_{max} = 1\, \text{pF}$, $C_{min} = 0.25\, \text{pF}$).
The quadrature coupler was designed and full-wave EM simulation (Sonnet [4]) is used to model the tee-junction effects on a 0.5 mm-thick $\epsilon_r = 2.9$ dielectric substrate. The effect was compensated by increasing the impedance and changing the transmission lines length of the coupler (while keeping the symmetry). The via-hole is simulated in Sonnet [7] and fitted to an inductance value of 0.165 nH using Agilent-ADS (Advanced Design System [41]). $L_1$, $L_2$, $L_m$, and $C_m$ values were chosen to be 1.16 nH, 0.4 nH, 0.86 nH and 0.55 pF, respectively, as per the description above and were implemented in a distributed fashion using a full-wave EM simulator (Sonnet [23]) to model and compensate for the interconnects parasitic. The characteristic impedances and lengths of the distributed model are presented on the layout shown in Fig. A.3.

### A.3 Fabrication and Measurements

The phase shifter was fabricated on 0.5 mm-thick Duroid substrate ($\epsilon_r = 2.9$, Roger RT/Duroid 6002) using a copper etching process (Fig. A.4). The M/A-COM varactor diode was epoxied with solder paste (Indium corporation) on the Duroid substrate, and the via-holes were done using a 10 mils bit (0.100 Stub Endmill, T-Tech Inc.). A thin copper wire is used to fill the hole through the substrate and connect to the ground plan. The varactors are biased using the network analyzer bias-tee from 0 to -20 V.

The phase shifter measurements show a center frequency of 5.8 GHz in both the reflection coefficient and the phase measurements. The measured reflection coefficient remains $<-10$ dB for all bias points from 5.5 to 6.2 GHz (Fig. A.5). The measured phase shift is $>360^\circ$ at 5.8 GHz and much higher at 5.5-5.7 GHz ($492^\circ-400^\circ$) and is shown in Fig. A.6. This is due to the complex load design, and at lower frequencies, the two series resonance points occur at $V_b > 2$ V and $V_b < 17$ V, and therefore, the phase shift is $>360^\circ$ over the entire bias range. On the other hand, at 6 GHz, the maximum measured phase shift is $280^\circ$ which is equivalent to a 2-bit phase shifter. The phase shifter can be easily used from about 5.6 to 5.9 GHz with good phase-shift performance ($>315^\circ$, equivalent to $>3$-bit). The measured phase shift and insertion loss as a function of the bias voltage at different
Figure A.3: Layout of the reflection-type coupler on $\epsilon_r = 2.9$ with a complex load.

Figure A.4: The fabricated complex load phase shifter. The ruler units are in inches (2.5 cm).
frequencies are shown in Figs. A.8 and A.9. The average insertion loss, calculated by averaging the loss at 0, -45, -90, etc., up to 315°, is only 2.0-1.7 dB at 5.6-5.8 GHz. A comparison with other designs is shown in table 1. To our knowledge, this represents the lowest-loss phase shifter to-date at C-band. The non-linear phase vs. voltage measurement (Fig. A.8) is due to the fast impedance (and therefore fast phase) change of the load around the parallel resonance point. The simulated IIP3 at 5.8 GHz is >20 dBm for all bias voltages (2-18 V) and phase states. This makes this phase shifter design excellent for wireless applications since it is placed before the amplifiers and therefore must have very low intermodulation products.

A.4 Conclusion

This appendix presents a very low-loss phase shifter based on a complex-load design and a 3-dB quadrature coupler. The measured performance covers 5.5-6.0 GHz and can be used for WLAN smart-antenna applications. In the future, the 3-dB coupler can be replaced by a lumped-element design resulting in a much smaller phase shifter (albeit at an increase of about 0.5 dB in insertion loss).
Figure A.6: The measured and simulated maximum measured phase shift vs. frequency for the phase shifter at 5.8 GHz.

Figure A.7: The measured S21 vs. bias voltage @ 5.8 GHz.
Figure A.8: The measured and simulated phase shift ($S_{21}$) vs. bias voltage from 5.4-6.0 GHz.

Figure A.9: The measured insertion loss vs. bias voltage from 5.4-6.0 GHz.
This appendix is mostly a reprint of the material as it appears in IEEE European Microwave Conference, 2009. Mohammed A. El-Tanani; G. M. Rebeiz. The dissertation author was the primary author of this material.
Appendix B

RF MEMS Cantilever Fabrication Process

B.1 Introduction

This appendix presents the fabrication procedure for RF MEMS switched capacitors, which are the building blocks of both 1.55-2.05 and 1.55-2.5 GHz tunable filters discussed in detail in chapters 5. The fabrication process is the result of a joint effort with other researchers in Prof. Rebeiz’s group, mainly Alex Grichner and Isak Reines. The ceramic wafers are laser drilled with AccuTek Laser Processing Inc, CA USA, polished at centerline technologies, MA USA and gold filled at Vishay EFI Inc. Vishay EFI Inc. also sputtered 2 um of gold on the front and back side to assure good step coverage with the via-hole.

B.2 Fabrication Steps

B.2.1 Wafer Clean

1. Rinse wafer in Acetone, Methanol, IPA followed by a DI water rinse and N2 dry
2. Clean fluoroare with Acetone, Methanol, IPA, and N2 dry thoroughly
B.2.2 Layer 1: Via-holes Pads

3. Dehydrate wafer for 2 minutes at 120C
4. Load wafer into spinner bowl and blow off any particles on wafer with N2 gun
5. Spin 1805 photoresist at 4Krpm for 50 seconds with acceleration set to 0.03
6. Align wafer on Karl Suss MA6 and expose pattern for 20 seconds at 9mW/cm² intensity
7. Develop in MF319 for 40 seconds (watch pattern clear and then add 10 seconds)
8. Wafer inspect to make sure that photoresist pattern looks acceptable
9. Remove exposed top TiW with H2O2 (heated to 30° C) on test sample from sputter deposition and note time (should be 3-5 minutes)
10. Etch top TiW on device wafer with same H2O2 (heated to 30° C) solution for 3-5 seconds then DI rinse in bath and N2 dry
11. Etch same glass slide sample in KII gold etch to calibrate etch time for device sample. Note (time should be 1 minute for 3000A of Au)
12. Etch device sample in KII (watch for the gold to clear then add 2-3 seconds before removing) then DI rinse in bath and N2 dry
13. Remove photoresist by rinsing in Acetone, Methanol, IPA

B.2.3 Layer 2: SiCrNx Bias Lines

14. Dehydrate wafer for 2 minutes at 120C
15. Load wafer into spinner bowl and blow off any particles on wafer with N2 gun
16. Spin NR9 negative photoresist at 4Krpm for 50 seconds with acceleration set to 0.03
17. Bake at 150C for 1 minute (Use temperature probe to verify temperature setting)
18. Align wafer on Karl Suss MA6 and expose pattern for 10 seconds at 9mW/cm² intensity
19. Post expose bake at 100C for 1 minute (Use temperature probe to verify temperature setting)
20. Develop in straight RD6 for 7 seconds (Time may vary to up to 10 seconds)
21. Wafer inspect (look for undercut of the PR showing the negative sloped sidewall)

22. Load wafer into Denton discovery 18 system with 2 glass slides and deposit SiCrNx with the following deposition conditions to achieve a 1500A thick layer with a sheet resistance between 10-50KOhm/sq

RF Power: 300W (50W/30second ramp up and ramp down)
Argon: 35sccm, Nitrogen: 4sccm
Chamber Pressure: 4.1-4.3mT
Rotation: 65rpm
Time: 6 minutes with pressure of 5 mT and 15 minutes of pressure of 4.1 mT with a 5-10 minute target burn in prior to deposition

23. Remove wafer from sputter chamber and soak in Acetone for 30minutes-1hour
24. Use ultrasonic bath for 1-2 minutes in Acetone to further aid liftoff
25. Rinse wafer in Acetone, Methanol, IPA, DI rinse and then N2 dry
26. Wafer inspect to verify complete liftoff
27. Measure SiCr thickness in the following locations:
28. 02 plasma descum wafer in old asher at 150W, 250mT for 2 minutes
29. Clean fluroware with Acetone, Methanol, IPA, and N2 dry thoroughly

B.2.4 Layer 3: Bottom Contact

30. Load wafer into Denton discovery 18 system with 2 glass slides and deposit TiW/Au/TiW (500/3000/500A) with the following deposition conditions:

DC Power: 250W
Argon: 38sccm
Chamber Pressure: 4.1-4.3mT
Rotation: 65rpm
Time: 120 seconds for the top and bottom TiW and 6 minutes for the Au
31. Dehydrate wafer at 120C for 2 minutes
32. Load wafer into spinner bowl and blow off any particles on wafer with N2 gun
33. Spin 1805 positive photoresist at 3 Krpm for 35 seconds with the acceleration set to 255
34. Bake at 105C for 90 seconds
35. Align wafer on Karl Suss MA6 and expose pattern for 20 seconds at $9\text{mW/cm}^2$ intensity
36. Develop in MF319 for 40 seconds (watch pattern clear and then add 10 seconds)
37. Wafer inspect to make sure that photoresist pattern looks acceptable
38. Remove exposed top TiW with H2o2 (heated to 30° C) on test sample from sputter deposition and note time (should be 3-5 minutes)
39. Etch top TiW on device wafer with same H2o2 (heated to 30° C) solution for 3-5 seconds then DI rinse in bath and N2 dry
40. Etch same glass slide sample in KII gold etch to calibrate etch time for device sample. Note (time should be 1 minute for 3000A of Au)
41. Etch device sample in KII (watch for the gold to clear then add 2-3 seconds before removing) then DI rinse in bath and N2 dry
42. Remove photoresist by rinsing in Acetone, Methanol, IPA
43. Soak sample in NMP (1165) remover at 80C for 30 minutes then thoroughly rinse in DI and N2 dry
44. Wafer inspect to verify that all 1805 photoresist has been removed
45. Etch top and bottom TiW using H2o2 (heated to 30° C) for 3-5 seconds (clearing is obvious)
46. Wafer inspect to check metal etch step
47. Measure Bottom contact thickness in the following locations:
48. 02 plasma descum wafer in old asher at 150W, 250mT for 2 minutes
49. Clean fluoroware with Acetone, Methanol, IPA, and N2 dry thoroughly

B.2.5 Layer 4: SiN Dielectric

50. Run 5 minute condition run in the Oxford PECVD system using the following the SiN HF/LF recipe with the following parameters:

**Temperature:** 350C

**Gases:** 5% SiH4 (silane) / 95% N2: 400sccm NH3 (ammonia): 20sccm
**Pressure:** 650mT

HF RF power (13.56MHz): 20W for 13 seconds

LF RF power (100-300KHz): 20W for 7 seconds

51. Load silicon test sample and deposit SiN for 12 minutes

52. Turn on ellipsometer and check system using calibration piece on program 5

53. Measure SiN thickness on silicon test piece

54. Measure same sample using the filimetrics system

55. If thickness is between 1500A +/- 100A run device for 12 minutes. Note: Make sure wafer pre-heat time is changed from 1 minute to 15 minutes in process recipe. Also include another silicon test sample for dielectric etch calibration

56. Measure SiN thickness using both the ellipsometer and filimetrics systems

57. Dehydrate wafer at 120C for 2 minutes on hotplate

58. Load wafer into spinner bowl and blow off any particles on wafer with N2 gun

59. Spin 1827 at 3Krpm for 35 seconds with the acceleration set to 255

60. Bake on hotplate at 105C for 90 seconds

61. Align wafer on Karl Suss MA6 and expose pattern for 20 seconds at 9mW/cm² intensity

62. Develop in MF319 for 40 seconds (watch pattern clear and then add 10 seconds)

63. Wafer inspect to make sure that photoresist pattern looks acceptable

64. Run a 5 minute condition run in the Oxford 80+ RIE using the standard SiN etch process with the following parameters:

**Temperature:** Room Temp

**CF4:** 20sccm, **O2:** 3sccm

**Pressure:** 75mT

**RF power:** 100W

65. Load device sample and silicon test piece with SiN into RIE chamber using capton tape to keep wafers centered in chamber

66. Etch SiN for 2 minutes (Typical etch rate of SiN with this recipe is 1000A/min). Also note to avoid over etching as quartz substrate will be etched

67. O2 plasma descum in old asher at 150W, 250mT for 2 minutes to breakdown
PR scum that forms on photoresist during etch
68. Rinse wafer thoroughly in Acetone, Methanol, IPA, N2 dry
69. Wafer inspect to check that wafer is clean
70. If wafer is still not clean soak in 1165 remover at 80C for 30 minutes
71. Measure SiN dielectric thickness in 5 locations using Dektak making sure to measure the test structures that take into account any substrate loss
72. O2 plasma descum in old asher at 100W, 250mT for 2
73. Clean flouroware with Acetone, Methanol, IPA, and N2 dry thoroughly
74. Dehydrate wafer at 120C for 2 minutes
75. Load wafer into spinner bowl and blow off any particles on wafer with N2 gun

B.2.6 Layer5: PMMA Sacrificial Layer

A. PMMA Layer:
93. Spin HMDS adhesion layer at 3000 rpm for 30 sec full ramp.
94. Spin PMMA 950 K, A9 at 1900 rpm for 45 sec full ramp. This results in 1.5 \( \mu \text{m} \) PMMA thickness.
95. Hard-bake at 130\(^\circ\)C using the hot plate for 10 min to avoid degassing of the PMMA layer.
97. Bake at 170\(^\circ\)C in oven for 30 min and let it cool down for 10 min.

B. Ti Mask:
98. Evaporate or sputter 2000 \( \AA \) of Ti.
99. Spin photoresist 1827 at 3000 rpm for 30 sec full ramp.
100. Soft-bake at 105\(^\circ\)C for 2 min.
102. Flood expose 1 min and develop in 351:DI(1:5). Note: Do not hard bake and put wafer in plasma O\(_2\) etcher since it etches the PMMA sacrificial layer too.

C. PMMA RIE Etching and Mask Removal:
103. Etch PMMA in RIE with the following parameters: O\(_2\) = 20 sccm, Pressure = 20 mT, Power = 50 W, Time = 30 min for 1.5 \( \mu \text{m} \) PMMA layer removal.

**B.2.7 Layer 5: Cantiliver Metal and Electroplating**

105. Deposit sputtered Au/Ti (8000Å/200Å) using the following parameters.
Note: Also include at least 1 glass slide for metal etch calibration:

**DC Power:** 300W for Au and 200W for Ti

**Substrate heating:** 150°C

**Argon:** 45sccm for Au and 38sccm for Ti

**Chamber Pressure:** 5.1-5.2mT for Au, and 4.1-4.3mT for Ti

**Rotation:** 65rpm

**Time:** 10 minutes for Au and 55 seconds Ti

106. Dehydrate wafer at 120°C for 2 minutes on hotplate

107. Load wafer into spinner bowl and blow off any particles on wafer with N₂ gun

108. Spin 1805 positive photoresist at 3 Krpm for 35 seconds with the acceleration set to 255

109. Bake at 105°C on hotplate for 2 minutes

110. Align and expose pattern on Karl Suss MA6 aligner for 20 seconds with an intensity of 9mW/cm²

111. Develop photoresist in MF-319 for 40 seconds, DI rinse and N₂ dry. Note: Once pattern clears add 10 seconds.

112. Wafer inspect to verify that plating mold is acceptable

113. Measure the plating mold thickness in 3 locations

114. Turn on hotplate for the plating bath and set temperature to 55°C and stir speed to 200rpm. Note: Let temperature stabilize before beginning electroplating 45 minutes

115. Just before electroplating strip top layer of Ti with 10:1 Di:HF for 3-5 seconds followed by a DI rinse and N₂ dry. Note: Run glass slide test piece first to check etch time
116. Load wafer into the plating bath and make sure that plating clip is not exposed to solution
117. Given plating area calculate total current assuming a current density of 2mA/cm². Note: Typical plating rate at this current density is 0.133um/minute or 4um’s on 30minutes
118. Electroplate sample for calculated time. If necessary take out 5 minutes before sample should be finished to check metal thickness
119. Take sample out of bath and rinse with copious amounts of DI water and N2 dry
120. Measure depth from photoresist down to the plated metal to verify the metal thickness
121. Strip plating mold using Acetone, Methanol, IPA followed by N2 dry
122. Clean fluoware with Acetone, Methanol, IPA, and N2 dry thoroughly
123. Measure plated metal thickness in 5 locations using Dektak:

**B.2.8 Layer 6: Filter Metal Electroplating**

124. Load wafer into spinner bowl and blow off any particles on wafer with N2 gun
125. Spin 1805 positive photoresist at 3 Krpm for 35 seconds with the acceleration set to 255
126. Bake at 105C on hotplate for 2 minutes
127. Align and expose pattern on Karl Suss MA6 aligner for 20 seconds with an intensity of 9mW/cm²
128. Develop photoresist in MF-319 for 40 seconds, DI rinse and N2 dry. Note: Once pattern clears add 10 seconds.
129. Wafer inspect to verify that plating mold is acceptable
130. Measure the plating mold thickness in 3 locations
131. Turn on hotplate for the plating bath and set temperature to 55C and stir speed to 200rpm. Note: Let temperature stabilize before beginning electroplating 45 minutes
132. Load wafer into the plating bath and make sure that plating clip is not exposed to solution
133. Given plating area calculate total current assuming a current density of 2mA/cm². Note: Typical plating rate at this current density is 0.133um/minute or 4um’s on 30minutes
134. Electroplate sample for calculated time. If necessary take out 5 minutes before sample should be finished to check metal thickness
135. Take sample out of bath and rinse with copious amounts of DI water and N2 dry
136. Measure depth from photoresist down to the plated metal to verify the metal thickness
137. Strip plating mold using Acetone, Methanol, IPA followed by N2 dry
138. Clean fluoware with Acetone, Methanol, IPA, and N2 dry thoroughly
139. Measure plated metal thickness in 5 locations using Dektak:

B.2.9 Layer 6: Metal Etch

140. Dehydrate wafer at 120C for 2 minutes
141. Load wafer into spinner bowl and blow off any particles on wafer with N2 gun
142. Spin 1818 positive photoresist at 4Krpm for 35seconds with the acceleration set to 255
143. Bake at 105C for 90 seconds
144. Align wafer on Karl Suss MA6 and expose pattern for 20 seconds at 9mW/cm² intensity
145. Develop in MF319 for 40 seconds (watch pattern clear and then add 10 seconds)
146. Wafer inspect to make sure that photoresist pattern looks acceptable
147. Remove exposed top Ti with 10:1 DI:HF on test sample from sputter deposition and note time (should be 3 – 5 seconds)
148. Etch top Ti on device wafer with same 10:1 DI:HF solution for 3-5 seconds then DI rinse in bath and N2 dry
149. Etch same glass slide sample in KII gold etch to calibrate etch time for device sample. Note: Time should be 3 minutes for 8000A of Au
150. Etch device sample in KII (watch for the gold to clear then add 2-3 seconds before removing) then DI rinse in bath and N2 dry
151. Remove 1818 photoresist with Acetone rinse, N2 dry
152. Wafer inspect to verify that the photoresist is removed
153. Remove Ti layer from the top of the MEMS bridge using 10:1 HF:DI for 3-5 seconds then DI rinse and N2 dry
154. Wafer inspect to verify Ti layer is properly etched
155. Clean flooware with Acetone, Methanol, IPA, and N2 dry thoroughly

**B.2.10 Wafer Dicing and Release**

152. If the wafer requires dicing follow process below or if not skip to step 120
153. Load wafer into spinner bowl and blow off any particles on wafer with N2 gun
154. Spin 1818 positive photoresist at 4Krpm for 35 seconds with the acceleration set to 255
155. Bake at 105C for 90 seconds
156. Ship wafer out for dicing
157. Carefully remove die from dicing tape
158. Remove bulk of the photoresist with Acetone rinse then N2 dry
159. Carefully transfer die into 1165 remover at 80C. Note: This bath should have a glass slide at 20-45 degrees depending on the size of the glass beaker and a stir bar underneath set at 50-100rpm. Soak sample for 2-3 hours
160. Carefully remove sample from the 1165 remover and place into DI water for 30 seconds keeping meniscus on sample at all times. Repeat this step 2 more times with fresh DI water
161. Carefully remove sample from DI water and place into Methanol for 30 seconds keeping meniscus on sample at all times. Repeat this step 2 more times with fresh Methanol
162. CPD release with chamber inserts to reduce volume and then set the purge time 15 minutes

163. Wafer inspect using VEECO profilimeter to verify that the MEMS are correctly released

164. Place wafer in flouroware and ESD bag before vacuum sealing bag for safe transfer to the RF test lab
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