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Design, Characterization, and Modeling of GaN based HFETs for Millimeter Wave and Microwave Power Amplifier Applications

A dissertation submitted in partial satisfaction of the requirements for a Doctor of Philosophy in Electrical Engineering (Applied Physics)

by

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2006
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Chair

University of California, San Diego
2006
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ABSTRACT OF THE DISSERTATION

Design, Characterization, and Modeling of GaN based HFETs for Millimeter Wave and Microwave Power Amplifier Applications

by

Adam M. Conway

Doctor of Philosophy in Electrical Engineering (Applied Physics)

University of California, San Diego 2006

Professor Peter M. Asbeck, Chair

GaN Heterostructure Field Effect Transistors (HFETs) have been the subject of intense research over the last decade, and provide exciting opportunities for high power microwave and millimeter wave power amplifiers. While extremely high power densities and efficiencies have been achieved at relatively low microwave frequencies, there are still material and device challenges which prevent the GaN HFETs from being used commercially at higher frequencies.

The work discussed herein attempts to improve transistor power performance at microwave and millimeter wave frequency range by gaining a physical understanding of anomalous device behavior. The work demonstrates that by comparing nominal device
characteristics measured using standard techniques (DC, s-parameters) with to pulsed I-V measurements taken at judiciously chosen quiescent bias points, device performance under large single conditions can be inferred.

Physical simulations of GaN HFETs which exhibit good agreement with measurements are described. The effects of layer structure and geometry on device performance are calculated and measured. It is shown that the anomalous transient phenomena collectively known at “current slump” can be accurately simulated by taking into account nonlinear transport of charge along the surface at the drain edge of the gate.

A novel measurement of FET thermal resistance is presented. Using three dimensional heat flow simulations which incorporate temperature dependent thermal conductivities, the thermal characteristics of various GaN HFET layer structures are compared.

Compact-models of GaN HFETs were developed which phenomena logically include anomalous transient behavior. The models accurately reproduced device performance under large signal conditions.
Chapter 1. Introduction and Background

1.1 Historical Context

The history of heterojunction based transistors for amplification of radio frequency (RF) signals began with a patent by William Shockley in 1948 in the context of bipolar transistors. These ideas were extended Herbert Kroemer in 1957, who proposed that by using a wider bandgap material for the emitter than the base of a bipolar transistor, the emitter injection efficiency could be improved [1]. It took another 20 years of material growth improvements before these devices could be realized. The first modulation doped heterostructure was implemented in 1978 by Dingle et al [2] using an AlGaAs/GaAs heterostructure to form a two dimensional electron gas (2DEG) in the undoped GaAs. In 1980, Mimura et al first reported a three terminal FET structure using modulation doping in an AlGaAs/GaAs structure to form the channel of the FET [3]. In the modulation doped structure, the donor atoms are spatially separated from the electrons in the 2DEG, which increases the mobility compared to bulk material leading to these new FET structures being named “High Electron Mobility Transistors” or HEMTs. This type of device structure is also known as a Heterostructure Field Effect Transistor or HFET. Other materials were investigated throughout the 1980s and 1990s to improve the performance HFETs. The first published report of a GaN based HFET was by Asif-Khan in 1994 [4]. Since then extensive work has been performed on GaN based HFETs due to their tremendous potential for power amplifier applications.
1.2 High Frequency Power Amplifiers

To compare the intrinsic potential of GaN based transistors to transistors fabricated in other material systems, the characteristics required for power transistors must be discussed. The amount of power that can be delivered to a load by a transistor can be described by the equation:

\[ P_{out\,\text{max}} = \frac{(V_{bk} - V_{knee}) \cdot (I_{knee} - I_{min})}{8} \]  

(1.1)

Where \( V_{bk} \) is the breakdown voltage, \( V_{knee} \) is the knee voltage, \( I_{knee} \) is the knee current and \( I_{min} \) is the leakage current between the drain and source, figure 1-1.

![Figure 1-1. Schematic diagram of Ids versus Vds curves for field effect transistors.](image-url)
Figure 1-2. Bandgap energy versus lattice constants for common semiconductors including nitrides.

Because of its wide bandgap of 3.4eV, GaN has a breakdown field of $5 \times 10^6$ V/cm which is ten times that of GaAs, whose bandgap is only 1.42eV, and 17 times that of Si (at a bandgap of 1.1eV), figure 1-2.

Figure 1-3. Velocity versus electric field for common semiconductors.
The knee current is also significantly higher than other technologies. The maximum knee current density can be calculated from:

\[ J_{knee} = qv_{sat}N_s \]  

(1.2)

Where \( q \) is the electron charge, \( v_{sat} \) is the saturation velocity and \( N_s \) is the number of electrons in the channel. The saturated velocity for electrons in GaN is calculated to be higher than that of more traditional material systems such as Si and GaAs as shown in figure 1-3. In the GaN HFETs, the density of electrons in the channel is also extremely high. The nitrides can be grown with either a Zinc Blende or wurtzite crystal structure. The wurtzite structure is typically used, resulting in a highly polarized unit cell, figure 1-4a, which cause a large spontaneous polarization change in the material. By growing dissimilar materials epitaxially, layers with high strain can be formed. The conventional GaN HFET structure is shown in figure 1-4b. The AlGaN layer can be under large amounts of tensile strain that is dependent on the Al mol fraction. This high strain translates into large stresses within the device structure and because of large piezoelectric constants of these materials, which are over ten times that of GaAs, a high piezoelectric polarization is present in the AlGaN/GaN HFET. The combination of spontaneous and piezoelectric charge densities gives rise to a large positive bound polarization sheet charge (>1x10^{13}/cm^2) that arises at the interface between the AlGaN and GaN which induces a two dimensional electron gas (2DEG) without any intentional doping. Because of the large differences in band gaps of the binary nitride materials, large band offsets can be achieved. This helps support the high density 2DEG formed in the channel. The 2DEG in GaN HFETs is typically an order of magnitude higher than in other material systems partly because of these large conduction band offsets.
Figure 1-4. a) Unit cell of GaN crystal. b) Schematic diagram of strain and polarization charge in conventional AlGaN/GaN HFET structure.

The energy band diagram for the structure in figure 1-5a is shown in figure 1-6. This polarization charge adds a new degree of freedom in device design not previously available in other III-V material systems, paving the way for new and exciting device structures.

Figure 1-5. Energy band diagram of conventional Al$_{0.25}$Ga$_{0.75}$N-GaN HFET structure underneath the Schottky barrier gate contact.
Knowing $I_{d_{knee}}$, the knee voltage can be estimated from:

$$V_{knee} = R_{ds} I_{d_{knee}}$$  \hspace{1cm} (1.3)

Where $R_{ds}$ is the drain to source resistance, which is given by:

$$R_{ds} = \frac{1}{q \mu_n N_s W t_{ch}}$$  \hspace{1cm} (1.4)

Where $\mu_n$ is the low field mobility, $L$ is source to drain spacing, $W$ is the device width, and $t_{ch}$ is the channel thickness. To compare the potential for power handling capability for each material system, the maximum power was estimated from highly idealized DC parameters. A summary of the values used for estimation for common semiconductors given in table 1-1 with the normalized results for $P_{out_{max}}$ given in the final row. GaN devices show potential for greater than 400 times improvement in power density over conventional semiconductor materials for a given device geometry.

<table>
<thead>
<tr>
<th>Material</th>
<th>Band Gap (eV)</th>
<th>Mobility (cm$^2$/Vs)</th>
<th>$N_s$ (/cm$^2$)</th>
<th>$V_{sat}$ (cm/s)</th>
<th>Breakdown Field (V/cm)</th>
<th>$P_{out_{max}}$ (normalized)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Si</td>
<td>1.12</td>
<td>1400</td>
<td>$1 \times 10^{12}$</td>
<td>$1 \times 10^7$</td>
<td>$3 \times 10^7$</td>
<td>1</td>
</tr>
<tr>
<td>GaAs</td>
<td>1.424</td>
<td>8500</td>
<td>$1 \times 10^{12}$</td>
<td>$1 \times 10^7$</td>
<td>$5 \times 10^7$</td>
<td>1.33</td>
</tr>
<tr>
<td>InP</td>
<td>1.344</td>
<td>5400</td>
<td>$1 \times 10^{12}$</td>
<td>$2 \times 10^7$</td>
<td>$4 \times 10^7$</td>
<td>3.33</td>
</tr>
<tr>
<td>SiC</td>
<td>3.23</td>
<td>900</td>
<td>$1 \times 10^{12}$</td>
<td>$1.8 \times 10^7$</td>
<td>$5 \times 10^6$</td>
<td>24</td>
</tr>
<tr>
<td>GaN</td>
<td>3.4</td>
<td>1500</td>
<td>$1 \times 10^{13}$</td>
<td>$2.5 \times 10^7$</td>
<td>$5 \times 10^6$</td>
<td>417</td>
</tr>
</tbody>
</table>

This improved power performance lends itself to a wide range of commercial and military applications, including amplifiers for: wireless basestations, wireless LAN, RADAR, satellite up and down links, and intra-satellite communications.

### 1.3 Issues with GaN HFETs

Unfortunately, the extremely high power densities estimated from material parameters have not been achieved in practice. The causes of this discrepancy are two
fold. First, anomalous transients are observed under pulsed conditions. These transients are characterized by an increase in on-resistance, leading to increased knee voltage and reduced Idmax as shown in figure 1-7. The measured saturated output power has been shown to correlate with pulsed Id-Vds curves and therefore much lower than predicted from DC Id-Vds parameters [6].

![Figure 1-6. Representative comparison of DC and pulsed Ids versus Vds curves for AlGaN-GaN HFET, normalized to Idmax of the DC curve, demonstrating effect of anomalous transients on device characteristics. Quiescent bias for pulsed I-V, QVd=20 QVg=--3 with pulse width of 200nS and a pulse separation of 1mS.](image)

Secondly, delivery of RF power to the load is not performed with 100% efficiency. Thus, much DC power must be dissipated as heat within the device. As the temperature within the device increases the device mobility and saturated velocity decreases, which reduces output power. Due to reduced gain, efficiency decreases as the operating frequency increases, making this effect even more important at mm-W frequencies. The nitride material system lacks a commercially available lattice matched substrate upon which to be grown. Historically, sapphire was used as the substrate because it is chemically inert and relatively inexpensive. However, a large mismatch in lattice constants, figure 1-2, led to poor crystal quality with a large numbers of
dislocations. SiC substrates provide a much closer lattice constant match and result in much higher quality epi material however are much more expensive. Another benefit of SiC substrates is its 20X larger thermal conductivity. As will be shown in detail in chapter four, this enhanced substrate thermal conductivity dramatically lowers the total thermal resistance of the layer structure.

![Figure 1-7. Comparison of representative DC Ids versus Vds curves of conventional AlGaN-GaN HFET on SiC substrate for various base plate temperatures.](image)

1.4 Scope of dissertation

The work contained in the dissertation is divided into four categories focused around the central goal of improving GaN based HFETs for microwave and millimeter-wave power amplifier applications. These categories correspond to the next four chapters.

In chapter two, the optimization of layer structure and geometry is discussed. Through iterations of comparing simulation to measurements, accurate physical modeling can be performed. With models in hand, exploration of device design can be carried out in simulation. Effects of geometry and layer structure are characterized by trade-offs
between DC, small signal and power performance. These trade offs are analyzed in simulation and then measurements on fabricated devices using the simulation results as a guide to device design illustrate the effect of geometrical and layer structure parameters on power performance.

Chapter three delves deeper in the physics of AlGaN/GaN HFETs by exploring anomalous transient phenomena. Characterization of the transients is performed using pulsed current versus voltage measurements. Two dimensional physical modeling was performed to explain the observed phenomena.

Chapter four explores heat flow within GaN based transistors. Three dimensional modeling of the entire device structure as a function of temperature and power dissipation for various device layer structures was performed to determine thermal resistance of various layer structures. A novel, all electrical technique based was developed to measure the thermal resistance of the layer structure. High resolution infrared microscopy was used to corroborate electrical based measurements and simulations.

Chapter five, compact circuit models the devices were created that represent the unique phenomena present in GaN HFETs that can be used for design of monolithic microwave integrated circuits. The models were also used to design a linearization technique for power amplifiers which achieves enhanced linearity while simultaneous maintaining high efficiency.

Finally in chapter six, a summary of the dissertation will be given followed by suggestions for future work.
References for Chapter 1


Chapter 2. Optimization of GaN HFETs for Microwave and Millimeter-wave Power Amplifier Applications

2.1 Introduction

In this chapter, two dimensional numerical simulations of GaN based HFETs are used to guide the optimization of transistor performance for microwave and millimeter-wave power amplifier applications. Both simulated and measured results for optimization of epitaxial layer structure, device geometry and layout are discussed.

2.2 Simulation Setup

Two dimensional numerical simulators solve a set of discretized equations that govern behavior of electrons and holes within a given device structure under the influence of applied voltages. The commercially available simulator package used in this work was ISE TCAD v. 10.0 [1]. A variety of built in models are available to the user to represent the many physical phenomena that are present in semiconductor devices. This simulation suite is also capable of performing three dimensional simulations. In the work that follows a conventional AlGaN/GaN heterostructure field effect transistor on a SiC substrate was the baseline device for comparison. Physical effects that were included in the simulations for device optimization include: velocity saturation, self-heating, channel quantization, impact ionization and piezoelectric effects.

2.2.1 Material Parameters

A prerequisite for accurate physical modeling of any semiconductor device is knowledge of the primary material parameters. For the nitrides these material parameters include: bandgap, electron affinity, dielectric constant, carrier mass, density of states in
the conduction and valence bands, carrier mobility, carrier velocity dependence on electric field, ionization coefficients, piezoelectric constants and spontaneous polarization. The fundamental material parameters used in the simulations for this chapter are shown in table 2-1. The values for electron mobility and saturated velocity listed in table 2-1 differ slightly from the maximum reported values listed in table 1-1 because they were extracted from measurements performed on the epi-layers used to fabricate the devices measured in this work, which will be discussed in section 2.2.4. Because the devices of interest employ ternary compounds the material parameters must either be known for both of the binary constituents of the ternary material or measured for the compositions used in simulations. When measured data for the ternary does not exist in literature, the parameters for the ternary material were linearly interpolated between the binary material values. See appendix A for exact material files used in simulations. The baseplate temperature for all of the simulations in this chapter was 300K.

<table>
<thead>
<tr>
<th>Material Parameter (300K)</th>
<th>GaN</th>
<th>AlN</th>
</tr>
</thead>
<tbody>
<tr>
<td>Band Gap (eV)</td>
<td>3.4</td>
<td>6.2</td>
</tr>
<tr>
<td>Dielectric Constant</td>
<td>9.5</td>
<td>8.5</td>
</tr>
<tr>
<td>Electron Affinity (eV)</td>
<td>4.1</td>
<td>0.6</td>
</tr>
<tr>
<td>Nc</td>
<td>2.3x10^{18}</td>
<td>6.24x10^{18}</td>
</tr>
<tr>
<td>Nv</td>
<td>4.62x10^{19}</td>
<td>4.88x10^{20}</td>
</tr>
<tr>
<td>(\mu_{\text{low}}) (cm/Vs)</td>
<td>1200</td>
<td>300</td>
</tr>
<tr>
<td>(V_{\text{sat}}) (cm/s)</td>
<td>2x10^{7}</td>
<td>1x10^{7}</td>
</tr>
</tbody>
</table>

### 2.2.2 Piezo-electric Polarization Charge

As discussed in chapter 1, the nitride material system has a highly polar wurtzite crystalline structure (figure 1-3). The values of piezo-electric constants are up to ten
times larger than for those in GaAs based crystals. High spontaneous polarization (polarization at zero strain) is also present in nitride crystals. Furthermore, using epitaxial growth techniques such as MBE or MOCVD, large amounts of strain can be built into heterostructures due to the difference in lattice constants between the materials. In the conventional AlGaN/GaN HFET structure, the AlGaN layer is under tensile strain. By knowing the piezo-electric constants of the materials, the piezo-electric polarization field can be related to the stress and strain by:

\[
P_{pz,i} = d_{\nu k} \sigma_{ij} = e_{\nu k} \epsilon_{ij}, \sigma_{ij} = C_{ijkl} \epsilon_{ij}
\]  

(2.1)

Due to symmetries in the wurtzite crystal structure (2.1) can be reduced to:

\[
P_{pz,z} = 2d_{31} \left( c_{11} + c_{12} - \frac{c_{13}^2}{c_{33}} \right) \epsilon_1
\]  

(2.2)

Where \( c_{ij} \) are the elastic constants in contracted notation and \( \epsilon_1 \) is the strain in the AlGaN layer, which is given by the ratio of the difference in unstrained lattice constants of the two materials to the unstrained lattice constant of the AlGaN layer:

\[
\epsilon_1 = \frac{a_{GaN} - a_{AlGaN}}{a_{AlGaN}}
\]  

(2.3)

At the abrupt interface between the AlGaN and GaN a sheet charge will be induced which is associated with the gradient of the polarization:

\[
\nabla \cdot P = \nabla \cdot (P_{SP} + P_{PE}) = -\rho_{pol} = P_{PZ}(AlGaN) + P_{SP}(AlGaN) - P_{PS}(GaN)
\]  

(2.4)

The spontaneous polarization in the nitride materials has been calculated using ab initio pseudo potential methods and found to be non-linear as a function of Al percentage [2]. Using the calculated spontaneous polarization, the induced sheet charge as a function of Al composition for an AlGaN/GaN heterostructure is shown in figure 2-1.
Figure 2-1. Calculated bound charge induced at an AlGaN/GaN heterojunction as a function of Al mol fraction, from [2].

For AlGaN/GaN HFET structures it is most advantageous to grow Ga face material in the (0001) orientation, so the bound charge at the AlGaN/GaN interface is positive, inducing a two dimension electron gas.

2.2.3 Channel Quantization Effects

To accurately represent the distribution of electrons in the channel, the quantum nature of electrons must be accounted for. By simply solving the Poisson equation for the conventional layer structure, the electron distribution is sharply peaked at the AlGaN/GaN interface, figure 2-2. By self-consistently solving the Poisson and Schrödinger equations, the wave nature of the electron is included in the calculation, which results in an electron distribution shown by the dashed line in figure 2-2. Under current flow conditions, the implementation of the Schrödinger solver in the simulation tool is not numerically robust. When electron flow must be included in a simulation, an alternate model, the density gradient model, was used. The density gradient model approximates the quantum nature of the electron distribution by adding a potential-like factor to the equation for electron density given by:
\[ n = N_c F_{1/2} \left( \frac{E_f - E_C - \Lambda}{k_b T} \right) \]  \hspace{1cm} (2.1)

Where \( F_{1/2} \) is the Fermi integral of order \( 1/2 \) and \( \Lambda \) is given by:

\[ \Lambda = -\frac{\gamma \hbar^2}{12m} \left( \nabla^2 \log n + \frac{1}{2} (\nabla \log n)^2 \right) = -\frac{\gamma \hbar^2 \nabla^2 \sqrt{n}}{6m \sqrt{n}} \]  \hspace{1cm} (2.2)

and \( \gamma \) is a fit factor. Using \( \gamma = 0.45 \), the electron distribution using the density gradient model can be fit reasonably well to the distribution calculated from the coupled solution of Poisson and Schrödinger equations as shown by the diamond markers in figure 2-2.

![Figure 2-2. Comparison of electron distribution in channel with and without quantization. Excellent agreement between the density gradient model and Schrödinger solution can be achieved.](image)

Fermi statistics were used in all simulations as the density of electrons in the channel is degenerate.

### 2.2.4 Carrier Transport

Field effect transistors are majority carrier devices. Therefore to simulate device behavior, one must be primarily concerned with the physics of transport for the majority charge carrier, which in GaN HFETs is the electron.
2.2.4.1 Mobility

In GaN HFET devices, electrons in the 2DEG experience scattering from interface roughness, dislocations, phonons, and electron-electron interaction [3]. At room temperature, scattering is dominated by optical phonons as shown in figure 2-2.

![Hall Mobility vs Temperature](image)

**Figure 2-3. 2DEG hall mobility versus temperature for AlGaN/ GaN heterostructure [3].**

At room temperature and low electric fields, mobility can vary between 900 cm²/Vs and 2000 cm²/Vs depending on Al composition and thus 2DEG charge density. When the charge density is greater than 1x10¹³/cm², interface roughness becomes the dominant scattering mechanism because the wave function of electrons in the channel penetrates further into the AlGaN barrier layer. The interface roughness is highly dependent on material quality, layer structure and percentage of aluminum in the barrier layer. For this work, the measured hall mobility at room temperature varied between 1200 and 1400 cm²/Vs.

2.2.4.2 Velocity Saturation
The velocity-field relation in GaN devices is heavily debated in the literature [4,5,6], as measurements and basic theory exhibit different behavior. As in many other III-V semiconducting materials, a region of velocity overshoot is predicted by Monte Carlo simulations [5] as shown in figure 2-3.

Figure 2-4. Velocity versus electric field as a function of Aluminum composition [5].

However, in practice, this region of velocity overshoot is not realized and the measured saturated velocity is lower than predicted from simulations. It is theorized that a build up of optical phonons in the high electric field region scatters the electrons before they can reach the theoretical values predicted by traditional Monte Carlo simulations [5]. Monte Carlo simulations including hot-phonon and degeneracy effects in the 2DEG agree well with measured data [6].

To model the electron velocity’s dependence on electric field the Caughey-Tomas mobility model [7] was used in this work. This model assumes a Si-like curve with no velocity overshoot (which approximately corresponds to the phonon limited transport case) given by:
\[ \mu(F) = \frac{\mu_{\text{low}}}{1 + \left( \frac{\mu_{\text{low}} F}{v_{\text{sat}}} \right)^{\beta}} \]  \hspace{1cm} (2.5)

Where \( \mu_{\text{low}} \) is the low field electron mobility, \( F \) is the electric field, \( v_{\text{sat}} \) is the saturated velocity and \( \beta \) is a fitting parameter. The model parameters used in this work (Table 2-1) were extracted from pulsed I-V measurements performed on an ungated device structure at various base plate temperatures. Using a very short pulse width and low duty cycle the effect of self heating can be negated. The measured and modeled velocity versus electric field curves which were used in the simulations are shown in figure 2-4.

![Graph showing measured and modeled drift velocity as a function of electric field for baseplate temperatures of 50°C (blue squares), 100°C (red circles), and 150°C (green diamonds) using the Caughey-Thomas mobility model.](image)

**Figure 2-5.** Measured and modeled drift velocity as a function of electric field for baseplate temperatures of 50°C (blue squares), 100°C (red circles), and 150°C (green diamonds) using the Caughey-Thomas mobility model.

### 2.3 Layer Structure Optimization

Two basic device structures were simulated in this work: a standard single heterostructure field effect transistor (SHFET) [8] and a double heterostructure field effect transistor (DHFET) [9]. The SHFET device structure employed 140Å of
Al$_{0.25}$Ga$_{0.75}$N on a 4000Å of GaN buffer. A 400um semi-insulating SiC substrate was included in the simulations. A positive bound sheet charge density of $1.1 \times 10^{13}$ charges/cm$^2$ was placed at the interface between the Al$_{0.25}$Ga$_{0.75}$N and GaN to correspond to the bound piezoelectric charge at the interface. A fixed negative charge of $1 \times 10^{12}$ charges/cm$^2$ was placed at the surface of the AlGaN representing surface traps to achieve the appropriate source and drain access resistances. A Pt Schottky barrier gate contact was placed on top of the AlGaN with a barrier height of 1.7eV for 25% Al. For the DHFET structure there is surface layer of 140Å of Al$_{0.29}$Ga$_{0.75}$N, under which there is a 200Å GaN channel followed by 4000Å Al$_{0.04}$Ga$_{0.96}$N. Additional negative bound charge of density $1.5 \times 10^{12}$ charges/cm$^2$ is placed at the bottom heterojunction in the channel to represent piezoelectric charge in the simulations. A schematic diagram of the layer structure is shown in figure 2-5.

![Figure 2-6. Schematic diagram of transistor layer structure for simulations. Parameters such as field plate length ($L_{FP}$), SiN$_x$ thickness and source to drain spacing were varied to optimize device performance.](image)

### 2.3.1 Energy band diagrams
The energy band diagram for the SHFET is shown in figure 2-6. The positive bound charge at the interface between the AlGaN and GaN pulls the energy bands down and electrons gather to form the 2DEG channel. During normal operation, the electrons are free to move laterally along the channel and blocked from moving in the AlGaN barrier by the band offset at the heterointerface and by the electric field from the gate which forces the electrons toward the channel. Electrons can also move into the GaN buffer, which can reduce the control of the channel electron density by the gate. As can be seen in figure 2-7, there are a significant number of electrons in the GaN buffer in the SHFET. Figure 2-8 shows the energy band diagram of the SHFET structure with the normalized electron wave for the first four energy bands superimposed. The upper three subbands extend deep into the GaN buffer. When the channel length is sufficiently small, any loss of channel control by the gate gives way to increased control of the potential in the channel by the drain, also known as the short channel effect. This leads to high output conductance, poor pinchoff characteristics and low device isolation.

![Figure 2-7. Thermal equilibrium energy band diagrams for SHFET (blue) and DHFET (red) layer structure.](image-url)
To help confine electrons in the channel, a second heterostructure at the backside of the channel was implemented using AlGaN with low mol fraction Al. This backside barrier utilizes the piezoelectric nature of the nitrides, as opposed to conduction band offsets, and thus only a small percentage of Al is required. For 4% Al in the buffer, a 1.1eV barrier is formed on the backside of the channel as seen in figure 2-7. In other III-V material systems DHFET structures are often used for the same purpose, however, they require higher percentage ternary materials to create the conduction band offset necessary for confinement. In the AlGaNDaN material system, to achieve a 1.1eV conduction band offset, an Al % of greater than 50% would be required. Using high Al content in the buffer layer would lead to reliability issues due to critical thickness limits and reduced thermal conductivity. At the back side of the channel the bands are pulled up by the negative bound piezoelectric charge which leads to better confinement of electrons in the channel. The electron concentration in the buffer was reduced by five orders of magnitude. The Al composition in the barrier layer was increased relative to the SHFET
(25% to 29%) in an effort to maintain the $1.1 \times 10^{13}$ charges/cm$^2$ bound piezoelectric charge at the AlGaN barrier – GaN channel interface. The bound positive polarization charge at the AlGaN barrier – GaN channel interface becomes reduced because GaN channel is grown pseudomorphically on the AlGaN buffer layer which reduces the strain in the AlGaN barrier layer compared to AlGaN grown on fully relaxed GaN. However, even by increasing the Al in the barrier layer to 29%, the total channel charge in the DHFET was still reduced by 40% compared to the SHFET. Further increase in Al content is not advisable due to critical thickness issues during growth. To understand the reduction in 2DEG charge density, the energy band diagram and electron wave function of a DHFET layer structure with 29% Al in the barrier layer and 4% in the buffer layer is shown in figure 2-9. Only two subbands are populated in this structure and the wave functions are confined to the channel.

![Energy band diagram of SHFET structure including electron wave functions.](image)

To increase the number of electrons in the channel and maintain the backside barrier to electrons, an n-type doping spike was placed in the channel near the back heterojunction. The simulated energy band diagram and electron density for this
structure are compared to the SHFET structure in figure 2-10. With a Si-doping spike of $1 \times 10^{12} \text{ /cm}^2$ placed 150Å from the top AlGaN barrier, the density of electrons in the channel can be increased by 5% over the SHFET layer structure and the backside barrier is 0.5eV without reduced mobility due to ionized impurity scattering. The density of electrons in the channel is increased by two mechanisms. The first is that the donor spike widens the effective channel which reduces the electric field normal to the channel and allows the wave function of the electrons to spread out, as shown in figure 2-11. Secondly, the n-type doping spike serves as modulation doping. This structure will be referred to as a doped channel double heterostructure FET or DC-DHFET.

Figure 2-10. Thermal equilibrium energy band diagram for SHFET and DC-DHFET.
2.3.2 DC Characteristics

The DC characteristics of the three layer structures were compared using 2D simulations. The velocity versus electric field relation was the same for all simulations. Simulated $I_d$ versus $V_{ds}$ characteristics at $V_{gs}=1V$ are shown in figure 2-12. Due to reduced electron concentration in the channel, the drain current is much lower for the DHFET than the other two structures.

Figure 2-11. Energy band diagram of DC-DHFET including electron wave functions.

Figure 2-12. Simulated $I_d$ versus $V_{ds}$ at $V_g=1$ for SHFET, DHFET and DC-DHFET layer structures.
The threshold voltage is also reduced in the DHFET structure due to lower channel charge as seen in figure 2-13. The pinch-off characteristics for the DHFET and DC-DHFET are much sharper than the SHFET due to confinement of electrons in the channel. In figure 2-14, the subthreshold characteristics can be seen. The subthreshold current is reduced by three orders of magnitude in the DHFET compared to the SHFET.

Figure 2-13. Simulated $I_d$ versus $V_{gs}$ curve at $V_{ds} = 10V$ for SHFET, DHFET and DC-DHFET layer structures.

Figure 2-14. Simulated Log $I_d$ versus $V_{gs}$ at $V_{ds}=10$ for SHFET, DHFET and DC-DHFET layer structures.
The simulated transconductance (gm) versus Vgs at Vds=10V is shown in figure 2-15. The peak gm for the SHFET and DC-DHFET are the same while the DC-DHFET exhibits a broader gm curve which could improve device linearity.

![Simulated gm versus Vgs at Vd=10V for SHFET, DHFET and DC-DHFET layer structures.](image)

**Figure 2-15.** Simulated gm versus Vgs at Vd=10V for SHFET, DHFET and DC-DHFET layer structures.

### 2.3.3 Experimental results

Using the simulation results as a guide, SHFET, DHFET and DC-DHFET devices were fabricated. Figure 2-16 shows the measured Id versus Vds curves. As seen in simulation, the DHFET exhibits lower maximum drain current than the SHFET structure. The DC-DHFET has larger maximum drain current than the SHFET. This can be attributed to the reasons enumerated in the last section and also to a thicker AlGaN buffer layer.
Figure 2-16. Measurement of Id vs. Vds curves for SHFET, DHFET and DC-DHFET layer structures.

Even with the delta doping in the channel, the pinch off characteristics remain sharp. However, drain leakage current (Ids for Vgs values below Vt) has increased compared to the DHFET structure as seen in figure 2-17. The measured Ids versus Vgs curves are shown in figure 2-17. The DHFET displays superior subthreshold characteristics. The threshold voltage of the DC-DHFET is more negative than the SHFET which can be attributed to the thicker AlGaN barrier layer which increases the charge in the channel and reduces Gm.
Figure 2-17. Log Id versus Vgs for SHFET, DHFET and DC-DHFET layer structures at Vds = 10 V. A comparison of Gm versus Vgs at Vds=10V for the three structures is shown in figure 2-17. The Gm curve for the DC-DHFET is broader than the SHFET and DHFET. This is due to a combination of two effects. First, a slightly thicker AlGaN barrier layer decreases the gate control over channel. Second, the distribution of carriers in the channel is more spread out which moves the centroid of the distribution away from the AlGaN barrier-GaN channel interface thus reducing Gm. As mentioned previously, a broader gm curve is expected to improve small signal linearity performance. Simulation results agree well with measurements.
2.3.4 Power measurements results

Load pull measurements were performed using a Maury Automated Tuner system. The tuners are capable of operating from 8 to 50 GHz making X band (nominally 10GHz) and Ka band (nominally 30GHz) measurements possible on the same system. The measurement procedure is as follows: the device is biased at the desired drain voltage, drain current and input drive level, then the source impedance is matched for optimum gain and the drain impedance is tuned either for optimum output power or optimum PAE at input high drive levels. Iteration is often necessary to achieve optimization of matching conditions due to the bilateral nature of the device under test. Next the Pin versus Pout measurement is performed. Generally the drain bias is then increased and the matching procedure is repeated, although often in an effort to reduce measurement time, the source impedance is held constant once tuned at the first drain bias (inasmuch as the improvement in device performance with subsequent source tuning is usually negligible). Also at large drain biases retuning of the output impedance at high drive levels often leads to catastrophic device failure; beyond 75% of the maximum drain
bias the output match is not retuned. The actual drain voltage value where this becomes appropriate is dependent on the device geometry, specifically gate to drain spacing, gate length, and gate type (field plate or t-gate).

Single tone large signal measurements were also performed in a load and source pull environment on 2x100um SHFETs, DHFET and DC-DHFET field plate devices. The device geometry used in these measurement included: a nominal gate foot length of 0.15um, field plate length of 0.2um, source to drain spacing of 2.5um and SiN thickness of 500A. The measured output power density as a function of Vds, matched for optimum power, for devices fabricated on the three different layer structures is shown in figure 2-19.

![Figure 2-19. Measured saturated output power versus Vds for SHFET, DHFET and DC-DHFET at 10GHz.](image)

The DC-DHFET structure shows a larger increase in output power density with increased drain voltage due to the larger knee current. While the SHFET and DC-DHFET show linear increase in output power with increased drain voltage, the DHFET shows a sublinear dependence. This could be caused by two physical phenomena: self-heating or
knee voltage walkout. As the drain voltage increases, the power dissipated as heat in the device also increases. Increased operating temperature decreases mobility which in turn, increases the on resistance and the knee voltage. With a large knee voltage, the RF voltage swing is reduced which, as illustrated in equation 1.1, also reduces the power delivered to the load. The DHFET layer structure has a higher thermal resistance and thus higher junction temperature than the SHFET structure, but should have the same thermal resistance as the DC-HFET, therefore the relative power reduction cannot be wholly attributed to thermal effects.

An increase in knee voltage along with a decrease in knee current can also be caused by surface charge between the gate and drain, as will be discussed in more detail in chapter three and mentioned in briefly section 1.3. Pulsed I-V measurements are a technique often used to measure the amount of knee voltage walkout under transient conditions. Figures 2-20, 2-21 and 2-22 compare the DC I-V curves to pulsed I-V curves measured at a quiescent bias of $V_d=25$ and $V_g=-5$ for the SHFET, DHFET and DC-DHFET devices respectively. The SHFET and DC-DHFET exhibit much less knee walkout than the DHFET device.

Surface state phenomena can be highly dependent on device geometry, device processing, and material quality. The device geometry was nominally the same for all three structures. Each of these wafers was processed individually so it is possible that the DHFET structure experienced slightly harsher processing conditions, namely a slightly longer recess etch which would create more surface damage and therefore potentially enhancing the anomalous transients. Another possible explanation for the larger amount
of knee walkout could be slight variations in surface passivation, or even a combination of a larger surface state density with poorer surface passivation.

Figure 2-20. Comparison of DC and pulsed I-V curves measured at a quiescent bias point of \( V_{ds}=25\text{V} \), and \( V_{gs}=-5\text{V} \) for a 2x100um Wg field plate gate SHFET.

Figure 2-21. Comparison of DC and pulsed I-V curves measured at a quiescent bias point of \( V_{ds}=25\text{V} \), and \( V_{gs}=-5\text{V} \) for a 2x100um Wg field plate gate DHFET.
Figure 2-22. Comparison of DC and pulsed I-V curves measured at a quiescent bias point of $V_{ds}=25\text{V}$, and $V_{gs}=-5\text{V}$ for a 2x100um Wg field plate gate DC-DHFET.

It is likely that the reduction in output power is a combination of the two effects. If the power delivered by the load is reduced due to surface charge induced knee voltage walkout, the power added efficiency also decreases. Reduced efficiency means that more of the DC power is being dissipated as heat and thus the device junction temperature is increased relative to the case were the efficiency is not reduced.

The measured PAE as a function of $V_{ds}$, matched for optimum efficiency, for devices fabricated on the three different layer structures is shown in figure 2-23. The DC-DHFET structure maintains a high PAE with increased drain bias, while the DHFET and SHFET roll off more rapidly. The reduction in efficiency as a function of drain bias can be correlated with output power and the differences between the layer structures can be explained by the same phenomena causing the differences in saturated output power.
Figure 2-23. Measured peak PAE versus Vds for SHFET, DHFET and DC-DHFET at 10GHz.

The DC-DHFET combines the benefits of sharp pinch off characteristics, low drain to source leakage current and good isolation from the DHFET and high Idmax and low on resistance of the SHFET to achieve superior DC and power performance compared to either of the two parent structures.

2.4 Device Layout Optimization

T-gate and field plate devices were fabricated on SHFET and DHFET layer structures. DC and S-parameter measurements were performed on the fabricated devices. Figure 2-10 shows a comparison between simulated and measured Idmax. Simulations were performed with slightly different Al composition than the fabricated devices so to compare simulation and measurement the Idmax values were normalized to the Idmax of the SHFET with T-gate. There is good agreement between simulation and measurement as depicted in figure 2-24.
AC simulations were also performed and compared with measured data. As summarized in table 2-2 there is excellent agreement between measurement and simulation for $F_t$.

<table>
<thead>
<tr>
<th></th>
<th>SHFET T-Gate</th>
<th>SHFET FP</th>
<th>DHFET FP</th>
</tr>
</thead>
<tbody>
<tr>
<td>Simulated</td>
<td>1.384</td>
<td>1.343</td>
<td>1.187</td>
</tr>
<tr>
<td>Measured</td>
<td>1.276</td>
<td>1.25</td>
<td>1.1</td>
</tr>
<tr>
<td>$I_{D_{max}}$ (A/mm)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$F_t$ (GHz)</td>
<td>81</td>
<td>53.5</td>
<td>50</td>
</tr>
<tr>
<td></td>
<td>80.5</td>
<td>50.6</td>
<td>50</td>
</tr>
</tbody>
</table>

With good agreement between simulations and measurement in hand, two dimensional hydrodynamic simulations were performed to investigate HFET structure variations which could further improve device performance under large signal conditions. The geometrical parameters explored in this work were: the field plate length, Si$\text{N}_x$ thickness and source to drain spacing, as shown schematically in figure 2-5. Device metrics of interest are $I_{D_{max}}$, peak $G_m$ and breakdown voltage. Simulations were
performed on SHFET and DHFET layer structures for both T-gate and field plate gate types.

2.4.1 DC characteristics

A comparison of Idmax (drain current at Vds=10, Vgs=1) versus SiN\textsubscript{x} thickness for various gate geometries is shown in figure 2-25. The addition of the field plate reduces Idmax because the field plate reduces the number of electrons in the access regions of the device between the gate and source and gate and drain. Increasing the field plate length decreases Idmax as more of the access region is controlled by the gate electric field. Increasing the SiN\textsubscript{x} thickness for field plate gates increases the Idmax until it saturates when the thickness reaches 1000\text potential, after which the field plate loses its effect on the electric field in the channel.

![Graph showing Idmax versus SiN_x thickness for various gate geometries and layer structures at Vgs=1V and Vds=10V.](image)

Similar trends were also seen for Gm as a function of SiN\textsubscript{x} thickness, figure 2-26. For longer field plates the increase in Gm with increased SiN\textsubscript{x} thickness was more pronounced.
2.4.2 Breakdown voltage

One benefit of using a field plate gate is the reduction of the peak electric field in the channel, which occurs at the drain edge of the gate under normal operating conditions, figure 2-13. As the field plate length is increased, the electric field in the channel is spread out, reducing the peak field. To simulate on-state breakdown voltage, hydrodynamic simulations were performed for an SHFET structure with 500Å of SiN$_x$ for various field plate lengths ($L_{FP}$=0 corresponds to T-gate). The simulator uses the general equation:

$$G_{avalanche} = \alpha_n n v_n + \beta_p p v_p$$  \hspace{1cm} (2.6)

Where $G_{avalanche}$ is the generation of electron hole pairs due to avalanche multiplication, and $\alpha_n$ and $\beta_p$ are the ionization coefficients for electrons and holes respectively. The
ionization coefficients are function of electric field in the channel parallel to current flow and given by:

$$\alpha(F) = \gamma a e^{\frac{b}{F}}$$  \hspace{1cm} (2.7)

Where $a$ and $b$ are fitting coefficients and $\gamma$ expresses the temperature dependence of the phonon gas against which the carriers are accelerated [1]:

$$\gamma = \frac{\tanh\left(\frac{\hbar \omega_{op}}{k T_0}\right)}{\tanh\left(\frac{\hbar \omega_{op}}{k T}\right)}$$  \hspace{1cm} (2.8)

Coefficients were extracted from monte-carlo simulations performed and reported by Oguzman et al [10]. Results of the on-state breakdown simulations are shown in figure 2-27. As the field plate length is increased the peak electric field in the channel is decreased, leading to increased breakdown voltage, figure 2-28.

![Figure 2-27. Simulated Ids versus Vds at Vg=0 including avalanche generation for various field plate lengths with 500A SiNx on SHFET layer structure. The gate foot length is 0.1um.](image)
Figure 2-28. Channel electric field as a function of position for various field plate lengths. Subset shows decrease in peak electric field.

Figure 2-29. Simulated on-state breakdown voltage for various field plate lengths for an SHFET device structure with 500A of SiN. The source to drain spacing was 2um.

After a field plate length of 0.5um, the breakdown voltage was only slightly enhanced by increasing the field plate length, figure 2-29. Only simulations of on-state break down were completed as simulations of off state breakdown led to convergence issues.

2.4.3 AC Characteristics
While field plates help increase breakdown voltage and reduce anomalous transients due to surface charge, as will be extensively discussed in chapter 3, they also increase the gate capacitance which degrades the transistor’s high frequency performance. To understand the effects of device geometry on AC characteristics, AC simulations were performed.

Shown in figure 2-30 is the simulated gate to source capacitance. The bias condition was at $V_{ds}=10\text{V}$ and $V_{gs}=-2\text{V}$. Because the field plate extends symmetrically towards both the source and drain, larger field plate length increases $C_{gs}$. As the SiN$_x$ thickness is increased the $C_{gs}$ is reduced because the distance between the field plate and the channel is increased.

![Figure 2-30. $C_{gs}$ versus SiN$_x$ thickness for various gate geometries and layer structures at $V_{gs}$ for peak $G_m$ and $V_{ds}=10$.](image)

However, the gate to drain capacitance increases as the SiN$_x$ thickness increases, figure 2-31. Unlike in the source access region, the channel is depleted underneath the field plate and thus the capacitance between the metallization dominates. Because the relative
dielectric constant of SiN$_x$ is 7.5 in these simulations, increasing its thickness effectively replaces air in the parallel plate capacitor between the gate and drain metallization. For the 0.4um field plate case, the entire gate to drain access region under the field plate is not depleted, thus Cgd does decrease once the SiN$_x$ is made thick enough to reduce the gate to channel component of Cgd, highlighting the importance of accurately modeling the depletion region in the gate to drain access region for AC simulations.

![Figure 2-31. Cgd versus SiN$_x$ thickness for various gate geometries and layer structures at Vgs for peak Gm and Vds=10.](image)

$F_T$ and $F_{MAX}$ were also extracted from AC simulations to explore the effect of device geometry on the high frequency current gain and power gain capability.

$$F_T = \frac{G_m}{2 \pi \cdot C_{GS}} \quad (2.9)$$

$$F_{MAX} = \frac{F_T}{2 \sqrt{\frac{R_G + R_I + R_S}{R_{DS}} + 2 \pi \cdot F_T \cdot R_G \cdot C_{GD}}} \quad (2.10)$$
As shown in figure 2-32, minimizing the field plate length along with maximizing SiN$_x$ thickness provide the highest values of Ft for field plate devices, as expected from trends in Gm and Cgs.

![Graph showing Ft versus SiN$_x$ thickness for various gate geometries and layer structures at Vgs for peak Gm and Vds=10.](image)

**Figure 2-32.** Ft versus SiN$_x$ thickness for various gate geometries and layer structures at Vgs for peak Gm and Vds=10.

Fmax plots show similar trends for field plate length and SiN$_x$ thickness as Cgd, implying that Cgd is the dominant parameter in small signal power gain, figure 2-33. While a larger field plate increases Cgd, the increased metallization lowers the gate resistance which improves Fmax. For the 0.4um field plate device, the gate resistance is very low due to the additional gate metal. As a consequence, the stability factor, k, is not greater than one for the frequency range of the simulations at low drain bias. Fmax is extracted from the maximum stable gain, which requires a stability factor greater than one (which explains the missing data points for the 0.4um field plate curve.)
Figure 2-33. $F_t$ versus SiN$_x$ thickness for various gate geometries and layer structures at Vgs for peak Gm and Vds=10.

Figure 2-34 plots $F_t$, $F_{max}$ and small signal gain at 30GHz as function of source to drain spacing for an 0.25um field plate SHFET with 500A of SiN$_x$. Increasing the source to drain spacing increases the access resistances and decreases the parasitic gate capacitance. Increased access resistance decreases the extrinsic Gm causing $F_t$ and $F_{max}$ to decrease with increased source to drain spacing. However there is a trade off between access resistance and breakdown voltage. As the source to drain region is increased the breakdown voltage correspondingly increases also due to reduced electric field in the channel.
Figure 2-34. Effect of source to drain spacing on $F_t$, small signal gain and $F_{max}$, 0.25um FP SHFET with 500A SiN$_x$.

T-gate devices exhibit superior small signal high frequency performance compared to field plate devices due the combination of low gate resistance and low parasitic gate capacitance. With speed comes reduced breakdown voltage, which reduces the large signal power handling capability of the transistors.

### 2.4.4 Measured Power Performance

Single tone large signal measurements were performed in a load and source pull environment on 2x100um SHFETs. Using the simulation results as a guide, the SHFETs were field plate devices with nominal gate foot length of 0.15um, field plate length of 0.2um, source to drain spacing of 1.5um and SiN$_x$ thicknesses of 500A and 750A. This device geometry was expected based on DC and small signal simulation results to deliver the maximum output power and efficiency. The saturated output power measured at 30 GHz as a function of drain bias is shown in figure 2-35 for the two SiN$_x$ thicknesses. Because a short source to drain spacing was used to reduce access resistances, the breakdown voltage was also reduced, thus limiting the maximum quiescent drain bias to 25 V.
The device with the thicker nitride shows better power performance for all Vds values because increased SiNₓ reduces gate capacitance as shown in simulation, thus improving gain.

![Comparison of measured saturated output power versus Vds for SHFETs with 1um SD spacing at 30GHz with 500A or 750A of SiNₓ.](image)

Measured PAE versus drain bias is shown in figure 2-36, for devices with either 500A or 750A of SiNₓ. At low drain bias the thicker nitride device shows slightly improved efficiency however at 25V the efficiency of the two devices is the same. The measured performance at 30 GHz was reduced compared to devices measured at 10Ghz because of reduced gain at the higher measurement frequency. There were also measurement limitations at 30GHz. Due to loss in the system between the tuner and DUT, the optimal matching conditions cannot be achieved.
2.5 Conclusion

Two dimensional hydrodynamic simulations have been performed and compared to measured data. There is excellent agreement between measurement and simulation. Layer structure enhancement with the use of the doped channel DHFET structure improves both DC and large signal power performance. Trade offs between device metrics of Ft, Fmax and breakdown voltage have been shown in simulation.

2.6 Acknowledgments

Some of the material in chapter 2 is as it appears in “Design and Fabrication of GaN based Doped Channel Double Heterostructure FETs,” submitted to IEEE Transactions on Electron Devices. The contributions from co-authors P.M. Asbeck, M. Micovic and J.S. Moon are appreciated. The author was the primary investigator for this work.
### 2.7 References for Chapter 2


Chapter 3. Transient measurements and modeling of GaN-based HFETs

3.1 Introduction

In the last chapter, simulations were used to optimize the GaN HFET layer structure and device geometry to achieve maximum power and efficiency. However, as discussed briefly in chapter 1, the potential for very high output power per unit width and high efficiency of these devices has often not been realized in practice as a result of anomalous transients in the I-V characteristics, particularly "knee voltage walkout" and "current slump", which manifest themselves as an increase in parasitic resistance when the device is operated at high drain voltage for a sufficient period of time [1,2]. To reduce the effect of these anomalous transients and thus increase power density, two major breakthroughs in device design have been achieved over the past six years: the addition of surface passivation, and the use of field plate technology. In this chapter simulations will be carried a step further to model the anomalous transients present within GaN HFETs as characterized in pulsed I-V measurements.

2D numerical simulations of transients effects in GaN HFETs have been previously reported [3-6] to explain the transient phenomena measured under pulsed I-V conditions. While the basic effect of knee voltage walkout has been captured, key elements of the observed behavior have been neglected. Meneghesso et al [3] demonstrated the time dependent nature of current collapse using transient simulations, at a low drain bias (<6V Vds). Tirada et al [4] performed simulations of AlGaN/GaN HFETs and GaN MESFETs including a fixed surface charge density, however, the bias dependence as well as the position dependent nature of the filled surface states was omitted. Other authors [5,6] have shown how buffer traps can play a role in knee voltage
walkout, but excluded the contribution of surface states to the phenomena. None of the previous reports included field plates in their analysis of the anomalous transients.

In this chapter, experimental measurements of the anomalous transients by pulsed I-V measurements at various bias conditions for T-gate and field plate geometries are presented. Our measurements show that the knee voltage walkout is strongly dependent on the bias conditions, depth of the recessed region, and gate geometry. The results strongly support the model that current slump is due to surface traps. To explain these measurements, 2D numerical device simulations of HFET characteristics were performed. For the first time accurate bias dependence of the knee voltage walkout was captured in a numerical model by including a Poole-Frenkel based electric field dependent surface conduction model. Also for the first time, simulations show how the addition of field plates mitigate “current slump” by reducing the density of surface charges within the framework of an electric field dependent surface conductivity model. With this accurate surface charging model in place, a comparison of various field plate geometries affect on knee voltage walkout was also performed in simulation.

3.2 Anomalous Current Transients

3.2.1 Knee voltage walkout

Knee voltage walkout is the phenomenon characterized by increased knee voltage, and often decreased knee current (also known as “current collapse”) under pulsed I-V measurement conditions in comparison with corresponding values in DC I–V measurements, shown in figure 3-1. The anomalous transients are evaluated in this work by measuring the I-V characteristics during short pulses of gate and drain voltage, with low duty cycle (of order 0.001 or below). It is theorized that carriers become trapped within the device structure under quiescent conditions. In the DC case, the trapped electrons can react to the changes in bias. For pulse widths shorter than the time it takes
for trapped electron density to respond to the pulsed voltage, however, the resultant pulsed I-V curve is significantly different. The quiescent bias sets the state of the traps within the structure for a particular pulsed I-V measurement. In general, these trap states could be located in the GaN buffer, within the AlGaN barrier layer or at the surface of the AlGaN in the ohmic access regions between the source and gate or between the gate and drain. The main cause of this effect has been attributed to charging of surface states between the gate and drain. Surface charging has been experimentally observed through Kelvin probe measurements on unpassivated devices [7] and determined to be highly voltage dependent [7,8]. Surface passivation has been shown to significantly reduce the current slump phenomena [2,7] however the surface charge is still measurable after passivation using an MIS test electrode [12].

![Figure 3-1](image.png)

**Figure 3-1.** Representative DC and pulsed I-V curves for T-gate device with 0.2us pulses separated by 1ms.

In previous experiments, it has been shown that surface treatments such as SiNx passivation [2,7,11], nitrogen anneal [12], doped cap layers [14,15] and distance between
the channel and the surface [16,17] greatly reduce the effect of knee voltage walkout and current collapse, which points to surface charge as the dominant mechanism for these phenomena. Various mechanisms for surface state charging have been proposed including gate tunneling at the edge of the gate, hopping conduction, and Frenkel-Poole conduction [9,10]. Negatively charged surface states deplete carriers in the channel leading to bias dependent drain and source access resistances. This negative charge is the result of donor-like states becoming neutralized by electrons which effectively uncovers bound negative polarization charge. This picture has become known as the virtual gate model [18].

### 3.2.2 Pulsed I-V Measurements

In previous work [1], it has been shown that the amount of RF power available from a device in class A or class AB bias is less than is predicted from DC I-V curve load line calculations. This phenomenon is known as RF power slump. The actual RF power available from a device instead correlates with the power calculated from pulsed I-V curves where quiescent drain and gate voltages are taken to be the DC values of the corresponding voltages during microwave power measurements. According to:

$$P_{out_{\text{max}}} = \frac{(V_{\text{max}} - V_{\text{knee}}) \cdot (I_{\text{knee}} - I_{\text{min}})}{8}$$

(3.1)

the increase of $V_{\text{knee}}$ and the decrease of $I_{\text{knee}}$ observed in figure 3-1 lead to reduced $P_{out_{\text{max}}}$.

Pulsed I-V measurements were performed on these devices using Accent Optical’s DiVA system. This system allows for simultaneous pulsing of the gate and drain with pulse widths of 200nS to 1mS. The quiescent bias point of the gate and drain is held constant throughout the measurement while the pulsed through a family of $I_d$ versus $V_{ds}$ curves, figure 3-1. A schematic of the pulse train is shown in figure 3-2.
Figure 3-2. Timing schematic of gate and drain voltages during pulsed I-V measurement.

Figure 3-3. Pulsed Ids vs Vds at various quiescent drain voltages with the quiescent gate voltage held at 1 V for a 2x100um T-gate device with 150A of Al_{0.25}Ga_{0.75}N.

3.2.2.1 T-Gate

AlGaN/GaN HFET’s were fabricated using a process that includes gate recess etch to move the gate closer to the channel thus improving modulation efficiency. 0.15 um T-shaped gates were defined by e-beam lithography. PECVD SiNx was deposited to
passivate the surface. Devices were processed with differing recess depths to study the effect of surface to channel separation on device performance. In the nominal case the entire 2 \, \mu m source to drain region was etched resulting in a gate to channel separation of 230A. For comparison, devices with a deeper recess, AlGaN thickness of 150A, were also fabricated. Representative DC and pulsed I-V characteristics are shown in figure 3-3 with a pulse width of 0.2\mu S and pulse separation of 1mS, for a conventional 2x100um T-gate device with 150A of Al\textsubscript{0.25}Ga\textsubscript{0.75}N at a quiescent gate bias of -5V (device pinched off) and increasing quiescent drain biases. Strongly pinching off the channel is commonly the most severe gate bias condition for knee voltage walkout. For simplicity, only curves pulsed to V\textsub{g}=1V are shown. With increasing quiescent drain bias, the R\textsub{ds} in the linear region is increased and Id\textsub{ss} is decreased causing the knee voltage to increase or “walkout.” The magnitude of the knee voltage walkout has a nonlinear gate and drain bias dependence. During these experiments there is no power dissipated in the quiescent state thus the contribution of thermal effects to the I-V changes is likely to be small.
In figure 3-4, the quiescent gate bias is changed to 1V. The drain bias dependence of the knee voltage walkout is readily observed, although it is substantially less than that measured at QVg=-5. Also, since the device is conducting current during the quiescent state of the measurement, significant power is dissipated during the measurement which causes an increase in the on resistance of the device due to thermal effects.
Figure 3-5. Pulsed $I_{ds}$ vs $V_{ds}$ at various quiescent drain voltages with varied quiescent gate voltages for a 2x100um T-gate device with 230A of Al$_{0.25}$Ga$_{0.75}$N.

Similar measurements were performed on a device with 230A of AlGaN. The results are shown in figure 3-5 for the case where $V_{g}$ is held both 1V and -5V during the quiescent period while the quiescent drain voltage is varied. The resulting increase in $R_{ds}$ and $I_{dss}$ is much less severe than for the deeper gate recess case. This difference in knee voltage walkout between the two AlGaN thicknesses can be explained by assuming that the surface Fermi level becomes pinned at the energy level of the surface states for both AlGaN thicknesses. When the states become filled during the quiescent portion of the measurement, they continue to pinch off the channel during the pulse. The quiescent bias condition dictates the density and spatial distribution of the trapped charges. The AlGaN thickness determines the amount of band bending for a given density and spatial distribution of charge. For the 150A AlGaN case, the band bending will be more severe than the 230A AlGaN structure, resulting in a larger electric field and thus greater depletion of electrons in the channel.
### 3.2.2.2 Field Plate Gate

Figure 3-6 shows the comparison of DC and pulsed I-V curves for various bias conditions for a field plate gate with a 0.2um field plate extension towards the drain and 500A of SiN$_x$. For this gate geometry significant improvement in knee voltage walkout is observed. Even for the most severe bias condition resulting in the greatest knee voltage walkout for the T-gate, only minimal walkout occurs in the field plate device. Differences in the magnitude of the current density between the T-gate and the field plate device are due to the differences in the thickness and Al composition of the AlGaN barrier layer. Further discussion of physical mechanisms leading to this improvement will be discussed in the following section.

![Figure 3-6](image-url)

**Figure 3-6.** Pulsed Ids vs Vds at various quiescent drain voltages with the quiescent gate voltage held at -5 V for a field plate device with 0.2 um field plate over 500A SiNx.

### 3.3 Simulations

#### 3.3.1 Setup

To model these phenomena, two-dimensional numerical simulations were performed using a commercial simulator software package (ISE-Synopsis, DESSIS). An
AlGaN/GaN HFET device structure was implemented as follows: a 2μm undoped GaN buffer layer, followed by a 200Å of Al$_{0.25}$Ga$_{0.75}$N barrier layer, a variable thickness SiN$_x$ passivation layer, an 0.2μm length gate with 1μm source to gate and gate to drain spacings. A fixed charge density of 1.1 x 10$^{13}$/cm$^2$ was placed at the AlGaN/GaN interface to represent piezoelectric and spontaneous polarization charges [19]. Within the GaN channel the low field electron mobility is set to 1200 cm$^2$/Vs with a saturated velocity of 1x10$^7$ cm/s. Drift diffusion transport models were employed for electron transport within the device. Thermal effects were not included in these simulations.

Several mechanisms were studied in simulation to model the trap-filling mechanism. First, acceptor like traps of various depths and densities were placed at the surface and distribution of filled states for various bias conditions were analyzed, namely under pinch-off conditions with increasing drain biases. Including acceptor-like traps is numerically identical to donor-like traps which uncover bound negative charge when filled with an electron; both result in a net negative charge at the surface when filled with electrons. One would expect more surface states to be filled when the device is pinched off than when the channel is open. The same result is expected with increased drain bias. These spatial distributions should qualitatively be able to reproduce quiescent bias dependence of the pulsed I-V measurements described in the previous section. Using drift diffusion transport models, it was not possible to achieve the correct bias dependence of the filled trap spatial distribution as there was no conduction path for electrons to get to the surface state. Next hydro-dynamic transport models were used in an attempt to model real space transfer of electrons from the channel to the surface. This model was unable to recreate the effect seen in measurement that when the quiescent gate bias is made more negative than the pinch-off voltage, the effect is more pronounced. In the real-space transfer model, the filled surface state density peaks just before pinch-off and then decreases as the gate voltage lowered below pinch-off. From the observed
quiescent gate bias dependence of the knee voltage walkout, on can infer that the gate to drain voltage is the driving force behind this effect and also that the dependence on said voltage is very non-linear.

One non-linear transport mechanism that has been reported in conjunction with GaN HFETs and pulsed experiments is Frenkel-Poole emission [9,10]. A schematic diagram of the Frenkel-Poole emission is shown in figure 3-7.

![Schematic diagram of Frenkel-Poole emission at AlGaN surface.](image)

When an electric field is applied to a filled trap, the coulomb potential of the charged trap pulls down the barrier increasing the probability of emission. To model the trap-filling mechanism, an electric field dependent conductivity model based on Frenkel-Poole transport theory [20] was coded into the simulator using the built in physical model interface [21] for electron mobility. This mechanism yields an effective mobility versus electric field relationship given by:

\[
\mu_{\text{PF}} = \exp \left[ \frac{-q\left(\phi_b - \frac{qE}{\pi\epsilon}\right)}{kT} \right]
\]  

(3.2)
where $E$ is the electric field and $\Phi_b$ is the trap depth. The model was applied to a 25Å thick AlGaN layer at interface between the Si$_3$N$_4$ and the AlGaN barrier layer which represents a conductive surface layer and could be physically due to the combination of dangling bonds, surface damage due to processing and/or surface contamination due to foreign species. Acceptor-like traps, which become negatively charged when electrons are captured, were placed at the interface between the field dependent conductivity region and AlGaN barrier layer between the gate and drain and gate and source at an energy level 0.5 eV below the conduction band. The density was varied between $1 \times 10^{12}$ / cm$^2$ and $1.1 \times 10^{13}$ / cm$^2$. 
3.3.2 T-gate devices

The T-gate or mushroom gate geometry (figure 3-8a) is commonly used in high frequency FETs to reduce gate resistance in short gate length devices. The gate head is far removed from the surface, approximately 4000Å, and thus has almost no effect on the electric field at the surface or in the channel of the device. The lateral surface electric field as function of position for a t-gate geometry is shown in figure 3-9.
Figure 3-9. Surface electric field as a function of position for various bias conditions for t-gate.

As the drain bias is increased, the peak electric field increases and the field spreads out farther towards the drain. When the gate bias is made more negative, the peak field at the drain edge of the gate is increased substantially and decreases rapidly farther from the gate edge only to rise in a second peak further from the gate. This double peak is characteristic of a field plate geometry, however in this case the effective field plate is actually the trapped negative surface charge. The increased electric field gives rise to enhanced surface layer conductivity as shown in figure 3-10.

Figure 3-10. Surface conductivity as a function of position with varied biases for t-gate geometry.

Using the simulated conductivity, a charging delay can be calculated from:

$$\tau = RC = \frac{\varepsilon LA}{\sigma d}$$  \tag{3.3}
This gives a charging time on the order of $1 \times 10^{-4}$ to $1 \times 10^{-2}$ s. At low bias and thus low electric fields, the conductivity decreases significantly yielding discharging time of the order 100s. These time constants are consistent with measured results and show how asymmetric the capture and emission process can be using this model. An alternative discharging process could be one where the electrons tunnel out of trap states to the channel. In this tunneling based model, it becomes increasingly more difficult for the electrons to tunnel out the state to channel as the population decreases. As the number of trapped electron at the surface is reduced, the conduction band at the surface is lowered thus widening the effective tunneling barrier as shown in figure 3-11.

![Band diagrams of electrons tunneling from surface states to channel. As electrons tunnel from surface states to channel, the effective tunneling barrier increases.](image)

The resulting surface charge profile is shown in figure 3-12 for the same set of bias conditions as the previous two figures. The distance over which the surface charge
extends towards the drain correlates with region of high electric field and enhanced surface conductivity.

![Surface Charge Density vs Distance from Gate Edge](image)

**Figure 3-12.** T-gate surface charge density as a function of position for various gate and drain biases.

Inclusion of the electric field dependent surface mobility model is essential for accurate voltage dependence of surface charge density. This negative surface charge causes the channel region between the gate and drain to be partially depleted, leading to increased resistance. To simulate pulsed I-V characteristics, the negative surface charge density is calculated from steady state simulations. This charge density is then placed at the device surface as fixed charge (assuming that during the short measurement pulse the trap occupancy does not change), and the steady state I-V curves are then resimulated using this new device structure [4,16]. This simulation does not model the transient nature of the phenomenon; it attempts to recreate the measurement in which the pulse width is very short compared with the duration of the transient. Equivalent pulsed I-V curves at different quiescent biases can thus be obtained (figure 3-13).

Reductions in Id are simulated to be of similar magnitude as found in the experimental results, and ID regains its full value after VDS is increased to the level measured in the experiments.
The model shows that the current slump effect is exacerbated by increasing \( QV_d \), and is dramatically increased by reducing \( QV_g \) to below pinchoff. While the simulated pulsed I-V curves for the T-gate structure match qualitatively, there are quantitative differences particularly in the maximum current density. The simulated structure was set up to match the field plate geometry in AlGaN thickness and composition leading to the discrepancies.

However, if the power density is calculated using (3.1) from the DC and pulsed I-V curves there is very good agreement between measurement and simulation, figure 3-15. Also differences in the knee region for the DC curve are due to the use of drift diffusion transport equations. A hydrodynamic based temperature dependent transport model would remove this discrepancy. It was not included in these simulations to reduce simulation time and improve convergence.
Figure 3-14. Reconstructed pulsed I-V curves for t-gate as a function of surface state density for QVd=10 V and QVg=-5 V.

Figure 3-15. Comparison of power density extracted from measured and simulated pulsed I-V curves normalized to DC theoretical limit for T-gate device structure.

3.3.3 Field Plate Effects

To improve the power performance of AlGaN/GaN HFETs, field plate technology has been implemented. Field plates of two main types have been used: 1) extensions of the gate metallization towards the drain (and sometimes source) [22,23], figure 3-8b; 2) a separate metallization in between the gate and drain, electrically connected to the gate or
source either directly via an airbridge over the gate metal [24] or outside of the active area of the device, figure 3-8c. The result is a dramatic increase the power density of AlGaN/ GaN HFETs, with record power densities of 30 W/mm measured at 4 GHz [24]. Field plates improve device performance in two ways: by increasing the breakdown voltage through a reduction in the peak parallel electric field in the channel as discussed in chapter 2, and by reducing the electric field at the surface, resulting in less negative trapped charge and thus less knee voltage walkout. They also reduce the maximum operating frequency by increasing gate to source and/or gate to drain capacitance depending on the type of field plate used as shown in chapter 2.

Simulations were also carried out for the two field-plate geometries most commonly used in GaN based HFET power devices, figure 3-8b. Simulation based experiments were performed for the structure in figure 3-8b by varying the field plate length ($L_{FP}$) as well as the thickness of the SiNx ($T_{SiNx}$). The effect of the field plate geometry on the electric field in the channel, and the surface state density were examined.

### 3.3.3.1 Effect on Breakdown in Channel

The primary use of field plates in power transistor technology is to reduce the peak electric field within the device and thus increase the breakdown voltage. Increased breakdown voltage allows for larger quiescent drain biases which from (1) should give rise to larger maximum RF output power that is linearly dependent on the drain quiescent bias. As discussed in chapter 2, for GaN based HFETs, the dominant breakdown mechanism is impact ionization of electrons in the channel of the transistor [25]. Figure 3-16 shows the electric field in the channel parallel to flow of electrons for field plate geometries as a function of field plate length for $T_{SiNx}$ of 500A. The characteristic double peak corresponding to the edge of the gate foot and the edge of the field plate is readily observed.
The field effectively spreads out the electric field over the region between gate foot and field plate edge resulting in a lower peak electric field. As the field plate length is increased, the peak electric is reduced thus increasing breakdown voltage. As discussed in chapter 2, metallization extending towards the drain will increase parasitic gate to drain capacitance which decreases the $F_{\text{max}}$ of the transistor leading to a design trade off between breakdown voltage and gate to drain capacitance [26].

Even for the case where no field plate metallization is included in the simulation, some spreading of the lateral electric field in the channel is observed. The trapped charge itself has some “field plate” effect by shielding the underlying regions from high electric fields caused by the gate. Figure 3-17 shows the electric field in the channel for various field plate geometries as a function of SiN$_x$ thickness. Our model predicts that for thicknesses above 500A the field plate loses its effectiveness due to screening of the field plate from the channel by surface charge and thus the peak electric field is unchanged. The amount of reduced field plate effect is dependent on the density of available surface states.
Figures 3-16 and 3-17 show the most severe cases, where the density of surface states is equal to the density of bound charges at the AlGaN/ GaN interface. A 2D
contour plot of the structure with 1000A of SiNx and a 0.2um field plate is shown in figure 3-18. The field lines are shielded by the surface charge. Figure 3-19 shows the channel electric field as function of position in the channel for various SiNx thicknesses with no surface states and thus no shielding of the electric field in the channel from the field plate. The field plate reduces the electric field in the channel even for SiNx thicknesses as large as 2000A. The difference between figures 3-17 and 3-19 illustrate the importance of including surface charge when simulating breakdown in GaN HFETs.

![Graph showing channel electric field with different SiNx thicknesses](image)

**Figure 3-19.** Channel electric field with no surface states at Vd=20, Vg=-3.

### 3.3.3.2 Effect on surface charge density

Another benefit of including field plates in GaN HFET design is the reduction of power slump. This is accomplished by decreasing the electric field at the surface thus decreasing the amount of surface charge. Surface electric profiles as a function of the distance from the gate edge are shown in figure 3-20 for various field plate lengths. The amount of electric field reduction at the gate edge increases with increasing field plate length, and varies inversely with the distance between the field plate and the AlGaN surface. The amount of trapped charge is also reduced significantly, as shown in figure...
There is a notable difference however between the field plate electrically connected to the source and field plate connected to the gate for comparable dimensions.

![Figure 3-20. Surface electric field parallel to channel for different field plate lengths with 500A SiNx and 1.1x10^{13}/cm² surface states at Vd=20, Vg=-3 (Class AB bias point).](image)

![Figure 3-21. Surface state density for different field plate geometries.](image)

While both show similar effect on the channel electric field, the field plate connected to the gate significantly reduces the amount of surface charge when negative bias is applied to the gate. The simulated pulsed I-V curves are shown in figure 3-22 for different field plate gate configurations. The lower surface charge density of the field
plate electrically connected to the gate results in a lower access resistance. It is clear from these simulation results that longer field plates with thin SiN$_x$ electrically connected to the gate will provide for maximum breakdown voltage and greatest reduction in knee voltage walkout. Simulated pulsed I-V curves as a function of quiescent bias are shown in figure 3-23 for a 0.2um field plate with 500A of SiN$_x$. These results agree well with measurements of the same structure (figure 3-6.)

![Figure 3-22: Reconstructed pulsed I-V curves for different gate geometries with 1.1x10$^{13}$/cm$^2$ surface states at QVd=20, QVg=-3 (Class AB bias point).](image)

### 3.4 Conclusion

This work has shown simulation results of AlGaN/GaN HFETs including surface electron traps and electric field dependent surface conductivity which reproduce the measured phenomena known as knee voltage walkout and current collapse. Also simulations show the effect of different field plate geometries on reducing electric fields at the surface, which in turn decreases the amount of trapped negative charge and knee voltage walkout and in the channel while also increasing breakdown voltage. The simulations point the way to detailed optimization procedures for field-plate structures.
Figure 3-23. Reconstructed pulsed I-V curves for field plate as a function of quiescent bias for 0.2um field plate connected to the gate with 500Å SiN, and $1.1 \times 10^{13}/\text{cm}^2$ surface states.

3.5 Acknowledgment

The author would like to thank David Root for guidance in linearization of the Frenkel-Poole equation for computational efficiency. This work was supported by ONR, monitored by Dr. Harry Dietrich and Dr. Paul Maki. Some of the material in chapter 3 is as it appears in “Simulation and Measurement of AlGaN/GaN HFET Pulsed I-V Curves,” submitted to IEEE Transactions on Electron Devices in 2006. The contributions from co-authors P.M. Asbeck, M. Micovic and J.S. Moon are appreciated. The author was the primary investigator for this work.
3.6 References for Chapter 3


Chapter 4. Accurate Thermal Analysis of GaN HFETs

4.1 Introduction

AlGaN-GaN Heterostructure field effect transistors (HFETs) have been under intense investigation over the last decade [1]. Due to the large breakdown strength and high polarization charge of this material system, extremely high power densities can be achieved. While the devices are suited for many types of power amplifiers, they are most commonly used in Class AB mode of operation. Discrete devices in a load- and source-pull environment have been reported to achieve power densities up to 30W/mm and, on the same device type but at lower Vds, Power Added Efficiency (PAE) of 65% at 4GHz [2]. Typically, however, once the device is fabricated in a MMIC and packaged, these high values are not achieved. At higher frequencies, the highest reported efficiency numbers are much lower. For example, at Ka band, PAEs between 32% and 43%, depending on bias level, have been reported [3,4]. This means the majority of the DC power used in these devices is dissipated as heat. For high power applications it is imperative for reliability concerns to have a firm understanding of the channel temperature in these devices. Understanding the temperature and power dissipation dependence of the thermal resistance of GaN HFETs is also important for accelerated life testing, where accurate knowledge of the channel temperature is essential for failure analysis.

4.2 Thermal Resistance Measurements

There are numerous methods for measurement of FET channel temperature (and thus thermal resistance of FETs) and many of them have been applied to GaN FETs. The
most common of them are: infrared camera technique, the liquid crystal technique [5], micro-Raman [6,7], photoluminescence [8], and pulsed I-V [9, 10]. The resolution of infrared cameras is limited to the wavelength of black body radiation from the surface of the device which is approximately 5μm [11]. The photoluminescence technique has a resolution of 2-3μm which is not small enough to resolve a heat source on the order of 0.2μm. The same is true of the liquid crystal technique which has a spatial resolution of 1μm and a temperature resolution of +/-1°C. In this technique, it is also assumed that the surface is the same temperature as the junction; however, for MMICs with substantial amounts of topside dielectric and metal layers, this may not be the case. Micro-raman spectroscopy also has a resolution of approximately 1μm however only a 10°C temperature resolution. An all electrical measurement is desirable to remove the spatial and temperature accuracy concerns imposed by the aforementioned techniques.

One such technique employs pulsed I-V measurements at elevated temperature, which are compared to DC measurements of the transistor structure at room temperature to extract the channel temperature [9, 10]. As a DC I-V curve is measured, power dissipated during the measurement causes localized heating which reduces the saturated velocity of electrons in the channel and thus the amount of current at a given bias voltage. Self heating can cause negative output conductance often measured on GaN HFETs grown on low thermal conductivity substrates or at high levels of power dissipation. Under proper pulsed I-V conditions the effect of self-heating and traps is negated. This occurs when the pulse duty cycle is low enough to not allow self heating to occur and when the quiescent bias is such that there is no power being dissipated and no external electric fields to cause traps states to charge or discharge. Pulsed I-V measurements at
elevated baseplate temperatures can be used as a thermometer to determine the
temperature increase in the channel due to self heating. This technique is applicable to
transistors where the source-to-gate access region is much smaller than the heat source
region as shown in figure 4-1a. This is not the case for deep sub micron power GaN
HFETs, for which the heat source region is smaller than the source access region, figure
4-1b.

\[ Gm_{\text{ext}} = \frac{Gm_{\text{int}}}{1 - Rs \cdot Gm_{\text{int}}} \]  \hspace{1cm} (4.1)

Using the pulsed I-V technique in its standard way [9, 10] the junction temperature is
underestimated by not taking into account the decrease in extrinsic Gm as a function of
temperature for submicron devices.
To overcome the limitations of previous techniques, a new technique is demonstrated here. For the short gate length transistors, the heat source is defined as the region where the electric field is high and thus the electrons in the channel are moving at their saturated velocity. Under DC conditions this region heats up and the saturated velocity is reduced. However, if an ungated structure is used the temperature dependence of velocity saturation within the channel can be measured [12], as the current in an ungated structure is given by:

\[ J_{D-\text{ungated}}(T) = qnv_{\text{sat}}(T) \]  

(4.2)

Using the difference in measured drain current between DC and pulsed I-V conditions along with the dependence of the saturated velocity on temperature, one can determine very accurately the temperature in the channel at a given amount of power dissipation.

![Figure 4-2. Ids vs. Vds curves for an un-gated FET structure with 2um source to drain spacing.](image)

4.2.1 Velocity versus temperature

The Id versus Vds curves for the ungated structure with 2um source to drain separation are shown in figure 4-2. By taking the ratio of the current at elevated
temperature to current at room temperature, and then plotting that ratio as a function of the change in temperature, the relationship between change in current and change in temperature can be calculated. For this work, the drain current at $V_{ds}=15\text{V}$ was used. The resulting curve is show in figure 4-3.

![Figure 4-3. Percent change in $I_{ds}$ as a function of change in temperature.](image)

Using a least mean square linear fit to the data, the following relation between the ratio of currents and change in temperature is extracted:

$$\frac{I_{d_{\text{pulsed}}}}{I_{d_{\text{DC}}}} = 9.26 \cdot 10^{-4} \cdot \Delta T$$

(4.3)

Using a ratioed measurement also reduces uncertainty in device dimensions or number of charges in the channel. It assumes that the number of electrons in the channel is constant over temperature, which has been shown to be an accurate assumption [10]. This allows one ungated structure to be used to extract the thermal resistance for devices of many sizes.
4.2.2 Thermal Resistance of HFET

The device used in this work was a Double Heterostructure FET [13] which had the following layer structure as shown in figure 4-4: 200Å Al$_{0.29}$Ga$_{0.71}$N, 500Å GaN, 4000Å Al$_{0.04}$Ga$_{0.96}$N, 400um of SiC, 5um of gold, 50um of Au$_{80}$Sn$_{20}$ eutectic die attach and a 2000um Cu fixture. The device employed a 2 finger, 100um wide field plate gate which has a 0.2um gate foot and 0.2um field plate. The layer structure also included 500Å of SiN$_x$ for surface passivation.

Figure 4-4. Nominal layer structure used for measurements and simulations.

To deduce the junction temperature in a gated FET structure, pulsed I-V and DC measurements were performed. By setting the quiescent bias of the pulsed I-V measurement at $V_d=0$ and $V_g=0$, no current was flowing and thus no power was dissipated within the device during the off state of the measurement. For these measurements, a pulse length of 0.2μS and a pulse separation of 10mS were used. A quiescent bias of $V_d=0$ and $V_g=0$ also ensures that the state of the traps within the device
is in thermal equilibrium at the beginning of the pulses, and expected to remain near that for the short pulses used. These conditions also effectively negate self heating within the device. DC current versus voltage measurements were performed for comparison. The effect of self heating is most significant in the high current saturation region of the curves where the most power is dissipated. When heat is generated the output conductance of the devices often becomes negative. It is in this region that the ratio between the pulsed I-V and the DC I-V curves was used to determine channel temperature. Using this ratio and (4.2) the change in temperature required to cause the amount of current reduction measured in the DC I-V curves can be calculated. The thermal resistance is then given by:

\[ R_{TH} = \frac{\Delta T}{P_{Diss}} \]  

(4.4)

where \( P_{Diss} \) is calculated from DC I-V measurement. The channel temperature is calculated by adding the baseplate temperature of the measurement to the calculated \( \Delta T \). This sequence can be repeated at multiple baseplate temperatures to extract the temperature dependence of the thermal resistance of the DUT. A representative set of DC and pulsed Id versus Vds with Vgs=1V curves at various base plate temperatures is shown in figure 4-5 for a 2x100 DHFET structure grown on 400um SiC substrate. The extracted thermal resistance as a function of dissipated power is shown in figure 4-6, along with the simulated data which will be discussed in the follow section. The extracted thermal resistance as a function of base plate temperature is shown in figure 4-7.
Figure 4-5. DC and pulsed $I_d$ vs. $V_d$, $V_{gs}$=1 curves at various baseplate temperatures for 2x100um device.

Figure 4-6. Comparison of measurement and simulation of thermal resistance for a 2x100um DHFET on SiC.
Figure 4-7. Simulated and measured thermal resistance for 2x100um DHFET on full thickness SiC substrate dissipating 1 W.

The measurement was repeated for a 10x100um DHFET structure on a 50um SiC substrate with through-substrate source vias. The DC and pulsed IV curves are shown in figure 4-8 along with the extracted thermal resistance as a function of dissipated power in figure 4-9. While the larger gate periphery device has a lower thermal resistance in units of deg C/W, if one instead compares thermal resistance per gate width (in units of deg C/W/mm) to corresponding values of reference devices for different gate peripheries, the multi fingered device was found to be hotter. As will be shown in simulation, there was thermal crosstalk between fingers as well as a reduction in heat spreading due to the thermally insulating vias.
4.2.3 IR Camera

Although IR detectors are limited in resolution, they give an accurate measurement of the surface temperature in the region between the source and drain. Shown in figure 4-10 is an image of a 2x100um DHFET on 400um of SiC dissipating 1
W. The peak temperature measured by the IR microscope is 133°C at baseplate temperature of 60°C. This is slightly lower than the channel temperature of 142°C inferred from the electrical measurement which is to be expected as the optically measured result is an average of the region between the source and drain.

Figure 4-10. IR camera image 2x100um DHFET with 400um SiC substrate.

4.3 Simulation Setup

To calculate the thermal resistance and thus the junction temperature of HFET layer structures, 3D finite element heat flow simulations were performed using a commercially available simulation tool (Synopsis-ISE TCAD). The device used as a reference for comparison is a Double Heterostructure FET [13] and has the following layer structure as shown in figure 4-4: 200Å Al\textsubscript{0.29}Ga\textsubscript{0.71}N, 500Å GaN, 4000Å...
Al\textsubscript{0.04}Ga\textsubscript{0.96}N, 400um of SiC for the full thickness wafer, 5um of gold, 50um of Au80Sn20 eutectic die attach and 2000um of Cu representing the package. Also included in the simulation are a 500A passivation layer of SiN\textsubscript{x}, the source, gate, field plate and drain contact metal. The effect of substrate material (Sapphire, Si, GaN, SiC, or Diamond), substrate thickness, and through substrate vias is investigated. Comparison to the conventional SHFET structure (where the AlGaN buffer layer is replaced with GaN) is also performed.

### Table 4-1. Table of room temperature thermal conductivities used in simulations.

<table>
<thead>
<tr>
<th>Material</th>
<th>Room temperature $\kappa$ (W/cm K)</th>
</tr>
</thead>
<tbody>
<tr>
<td>GaN</td>
<td>2.25</td>
</tr>
<tr>
<td>Al\textsubscript{0.29}Ga\textsubscript{0.71}N</td>
<td>0.33</td>
</tr>
<tr>
<td>Al\textsubscript{0.25}Ga\textsubscript{0.75}N</td>
<td>0.38</td>
</tr>
<tr>
<td>Al\textsubscript{0.04}Ga\textsubscript{0.96}N</td>
<td>1.25</td>
</tr>
<tr>
<td>SiC</td>
<td>3.5</td>
</tr>
<tr>
<td>SiN\textsubscript{x}</td>
<td>0.18</td>
</tr>
<tr>
<td>Cu</td>
<td>3.4</td>
</tr>
<tr>
<td>Au</td>
<td>3.1</td>
</tr>
<tr>
<td>Au80Sn20</td>
<td>0.57</td>
</tr>
<tr>
<td>Si</td>
<td>1.55</td>
</tr>
<tr>
<td>Sapphire</td>
<td>0.34</td>
</tr>
<tr>
<td>CVD Diamond</td>
<td>17.5</td>
</tr>
</tbody>
</table>

#### 4.3.1 Material Parameters

An important factor in thermal simulation of semiconductor devices is accurate material parameters. Room temperature thermal conductivities used in the simulations are shown in table 4-1. It has been widely reported that ternary compounds have significantly reduced thermal conductivities compared to their binary constituents due to alloy scattering. This is also the case with AlGaN. The dependence of the thermal conductivity of AlGaN on Al mol fraction was studied by Liu et al [14] and the extracted data is shown in figure 4-11. While many device thermal simulations use a $T^{-1}$
temperature dependence of thermal conductivity to represent phonon-phonon scattering, the reported temperature dependence of the thermal conductivity is a more complex function of temperature. Specifically detailed characterization of Si, AlGaN, GaN, SiC, sapphire and diamond [14-20] has been performed and is shown in figures 4-12 and 4-13. The thermal conductivities for the other materials (Au, Cu, SiNx and AuSn) used in the simulations are temperature independent. The symmetry of the simulated structure is taken advantage of by only simulating one half of the total structure. This allows for the use of more mesh points within the heat source area and reduces computational load. Reflecting boundary conditions are employed at the all boundaries except the bottom of the structure which is taken to be a perfect heat sink.

![Graph](image)

Figure 4-11. Thermal conductivity of AlGaN as a function of Al mol fraction.
Figure 4-12. Temperature dependence of thermal conductivity of materials used in simulations.

Figure 4-13. Thermal conductivity of SiC [11] and CVD Diamond [12] versus temperature.

The position of the heat source within the model is a key element in achieving an accurate model. To determine the position of the heat source within the channel, two dimensional electrostatic simulations of the device structure were performed. The resulting electric field profile for a 0.2um gate length gate with a 0.2um field plate is shown in figure 4-14. The majority of the high electric field region (which corresponds
to the heat source region in the thermal simulation) is next to gate on the drain side. The dual peak nature of the electric field profile in the channel is characteristic of FET devices with a field plate [21]. It is important to consider the positioning of the heat source region relative to the gate as the gate metal acts as a heat spreader. For short gate lengths this effect is reduced because the heat source region is offset from the center of the gate towards the drain.

Figure 4-14. Electric field profile in the channel for DHFET field plate device with 500A of SiNx.

4.4 Simulation Results

4.4.1 2x100um Gate Width Device

The temperature distribution in a 2x100um DHFET with a 400um SiC substrate dissipating 1 W at a base plate temperature of 23 C (296K) is shown in three dimensions in figure 4-15. This structure will be used for a baseline comparison with other layer structures and device geometries.
Figure 4-15. Three dimensional temperature distribution in DHFET.

Figure 4-16 is a two dimensional cut through the center of the gate; notice the heat source is offset from the gate foot towards the drain. For 1 W of dissipated power, the peak temperature within the device was 99.6 C, while the spatially averaged temperature in the high electric field region was 94.8 C which gives a thermal resistance of 74.4 C/W. For comparison with measurements the spatially averaged temperature will be used to describe the device geometries and layer structures.
Figure 4-16. Two dimensional cross section of gate head in DHFET. Note heat source offset from gate foot.

Figure 4-17. Spatial temperature distribution across channel (y-direction) for standard structure.

One dimensional temperature profiles are shown in figures 4-17, 4-18 and 4-19.

Figure 4-17 shows the temperature distribution through the center of the gate along the
channel from drain to source. In the region on the left side of the graph which represents
the drain between gate fingers, the temperature does not reach the lattice temperature.
This shows there is some interaction between gate fingers. The temperature profile along
the gate in the center of the heat source is shown in figure 4-18. There is a 10 C
difference between the center of the gate and the edge.

![Temperature Profile](image)

**Figure 4-18.** Simulated spatial temperature distribution along gate finger (x-direction).

The temperature profile into the substrate through the heat source is shown in
figure 4-19. The temperature drops off rapidly: 60% of the temperature rise is recovered
in the first 25um and slowly reaches thermal equilibrium at the bottom of the sample.
Figure 4-20 shows a close up of the active region of the device. The resulting thermal
conductivities are plotted in grey on the right Y axis. The Al$_{0.04}$Ga$_{0.96}$N buffer layer acts
as a thermal barrier to heat generated in the channel.
The effect of power dissipation and lattice temperature on the thermal resistance and peak channel temperature is shown in figures 4-21 and 4-22 respectively. Because thermal conductivity of the materials used in the structure is varies roughly inversely with
temperature, the thermal resistance of the entire device increases when the baseplate temperature or the power dissipation increases. Figures 4-21 and 4-22 also illustrate how the choice in buffer materials affects the thermal resistance of the device. The SHFET exhibits approximately 10% lower thermal resistance across the temperature range shown.

Figure 4-21. Rth and maximum channel temperature as a function of power dissipation for DHFET and SHFET structures with 300um SiC substrates at 23C baseplate temperature.

Figure 4-22. Rth and maximum channel temperature as a function of baseplate temperature for DHFET and SHFET structures with 300um SiC substrates dissipating 1W.
Figure 4-23 shows the effect of substrate thinning for through substrate source via fabrication on the thermal resistance of a standard DHFET structure as a function of temperature. At room temperature the thermal resistances with and without thinning were comparable. However, as the temperature was increased, the thinned substrate device structure exhibits significantly lower thermal resistance than the full substrate structure due to the reduction in SiC thermal conductivity as a function of temperature. The vias themselves show almost no impact on the overall thermal resistance.

![Graph showing thermal resistance as a function of temperature for different substrate thicknesses](image)

**Figure 4-23.** Thermal resistance as a function of temperature for the standard 2x100um structure (DHFET on SiC) for different substrate thicknesses: full thickness (300um) and 2mil (50um) substrate. Through substrate source vias are shown to have almost no effect on the 2x100um device thermal resistance.

The choice of substrate material is another variable to be considered in the design of a GaN HFET layer structure. Traditionally, HFETs were grown on sapphire substrates due to its low cost and relatively close match of lattice constant and coefficient of thermal expansion to GaN. The main drawback, however, is its very low thermal conductivity compared to the alternatives (Si, free standing GaN or SiC substrates). At room temperature, sapphire is 6.6 times less thermally conductive than GaN, 10 times less
thermally conductive than SiC and 50 times less thermally conductive than Diamond, table 4-1. Figure 4-24 shows the effect of substrate material on the overall device thermal resistance for a 2x100um DHFET dissipating 1W on a 50um substrate with source vias. The device on the sapphire substrate has a 334% greater temperature rise than the device on SiC. By replacing the SiC with CVD diamond, which could be accomplished by removing the active device from the original substrate and bonding it to the CVD diamond, the room temperature thermal resistance is decreased by 30%.

![Figure 4-24. Effect of substrate material on 2x100 um DHFET dissipating 1W. Substrate thickness is 50um; through substrate vias are included.](image)

Further reduction of the thermal resistance can be achieved by the use of CVD diamond on the topside of the device. The effect of adding diamond layers to the top side of the device with a range of thicknesses is shown for various substrate materials in figure 4-25. The device on SiC will be discussed. By replacing the SiNx passivation with CVD diamond, the overall thermal resistance drops by 13%. Adding an additional 0.5um layer decreases the thermal resistance by another 6%. If the entire region between
the plated source and drain contact metal is filled in with diamond the thermal resistance is reduced by total of 35% from the standard device.

![Bar chart showing thermal resistance (Rth) for different substrate materials with varying topside diamond layers.](image)

**Figure 4-25.** Effect of topside diamond layers on thermal resistance of 2x100 GaN DHFET dissipating 1W at 23C baseplate temperature with varied substrate materials.

By simply filling in the region between the plated source and drain contact metal without replacing the SiNx passivation, the overall thermal resistance is reduced by 25%. This illustrates to the effectiveness of the field plate’s heat shunting ability. In standard structure with no topside diamond layers, there is not enough gate metal to shunt the heat from the channel to cooler regions of the chip. With the addition of a few microns of diamond, heat shunt becomes possible and has a dramatic effect on the device thermal resistance.

### 4.4.2 10x100um Gate Width Device

Thermal characteristics of 1mm gate periphery DHFET on 50um SiC substrate with source vias were also investigated. The device has 10x100um gate fingers separated
by 50um. A one dimensional temperature profile perpendicular to the center of the gate is shown in figure 4-26. There is significant cross talk between fingers which is demonstrated by the 10 C difference between the center finger and the outermost finger.

![Temperature profile](image)

**Figure 4-26.** Temperature profile perpendicular to center of the gate for 10x100 DHFET dissipating 5W.

In figure 4-27 the power dissipation and channel temperature are plotted as a function of drain efficiency for a constant RF output power of 5W. As the efficiency is reduced the power dissipated within the device increases causing the channel temperature to increase rapidly. For a decrease in efficiency from 60% to 33.3% the channel temperature rise increases by a factor of 3. This demonstrates the importance of operating GaN based high power amplifiers in high efficiency modes.
4.5 Conclusion

The thermal resistance of GaN HFETs has been analyzed. A new electrical method of measuring thermal resistance has been used to determine the thermal resistance of a 2x100 um DHFET on 400um SiC substrate and a 10x100um DHFET on a 50um SiC substrate with source vias. Three dimensional finite element thermal simulations have also been performed to compare various device designs. Simulations agree well with measurements over power dissipation and baseplate temperature. The effect of device layer structure and growth substrate has been shown. Simulations also point the way to ultra low thermal resistance device structures using CVD diamond either by replacing the growth substrate during backside processing or by depositing diamond layers on the fabricated device.
4.6 Acknowledgement

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4.7 References for Chapter 4


5.1 Introduction

To harness the many benefits of GaN based transistors, they must be implemented in circuits. For high frequency power amplifier circuit design as well as mixed signal circuit design, it is essential that an accurate large signal model be used. Models should describe as many of the physical phenomena present in these devices as possible including: breakdown; short channel effects; and self-heating behavior (since with the high power density of GaN, thermal management is an important issue.) Also, models should include the trapping effects present in many GaN HFETs, to alert the designer about the possible consequences of anomalous transients for circuit behavior. Compact circuit modeling of AlGaN/GaN HFETs including self-heating and trapping effects is the subject of this chapter.

5.2 Overview of important physical mechanisms

As discussed extensively in previous chapters, AlGaN/GaN HFETs exhibit behavior which under normal operating conditions, can deviate from current - voltage relationships predicted from the conventional gradual channel approximation. The most significant of these are short channel effects, self heating effects, and anomalous transient effects.

5.2.1 Short Channel Effects

The transistors discussed in this work have been designed to deliver high power densities at radio frequencies between X and Ka band. As discussed in chapter 2, the optimum device configuration to achieve simultaneous high efficiency and power density
in these frequency bands is a very short gate length DHFET with a field plate. SHFET devices with T-gates were also modeled. The gate length of the transistors discussed herein is varied between 0.12\(\mu\)m and 0.25\(\mu\)m. Due to the small nature of this dimension the gradual channel approximation commonly used to derive I-V relationships for FETs is not applicable. Many physical mechanisms must be taken into account for accurate representation of the characteristics of transistors of this scale including drain induced barrier lowering, velocity saturation and channel length modulation, which are generally referred to as short channel effects [1].

![Schematic diagram of drain induced barrier lowering (DIBL).](image)

**Figure 5-1.** Schematic diagram of drain induced barrier lowering (DIBL).

### 5.2.1.1 Drain Induced Barrier Lowering (DIBL)

Under off state conditions for a long channel device, there is a potential barrier to electron flow in the channel which is controlled strictly by the gate voltage, figure 5-1. When the channel length is scaled down to submicron dimensions, the drain voltage also plays a role in controlling the magnitude of the potential barrier to electron flow in the channel. In this short channel case, as the drain bias is increased the potential barrier is
decreased resulting in a decrease in the effective threshold voltage of the device. This leads to increased subthreshold source to drain current at a given gate bias for increasing drain bias. To model this effect, the threshold voltage must have a drain voltage dependence.

![Schematic diagram of Ids vs. Vds curves comparing long and short channel behavior.](image)

**Figure 5-2.** Schematic diagram of Ids vs. Vds curves comparing long and short channel behavior.

### 5.2.1.2 Velocity Saturation

Another effect relating to short gate length devices is that of velocity saturation. As the gate length is decreased, the electric field in the channel parallel to current flow increases. When the electric field reaches a critical value, the electrons in the channel typically attain a maximum steady state velocity obtainable in a given material, called the saturated velocity. For very short gate channels, higher velocities are often attainable through the velocity overshoot phenomenon. When the velocity becomes saturated, the drain current also saturates. The voltage at which the current saturates is commonly referred to as the knee voltage or \( V_{dsat} \). In short gate length devices, velocity saturation of electrons in the channel causes a knee voltage to be at drain voltages lower than
predicted by the gradual channel approximation (figure 5-2) which must be adequately reflected in the I-V relationships of the model.

5.2.1.3 Channel Length Modulation

According to the gradual channel approximation, in principle, the output conductance, $dI_{ds}/dV_{ds}$, of the device in the saturation region is zero. In practice, for short gate length devices when the device is biased beyond saturation, the output conductance is a positive non-zero quantity. This is due in part to DIBL, since as the drain voltage is increased beyond saturation, the threshold voltage decreases and thus the drain current increases. Another effect that must be considered for accurate modeling of short channel length FETs is channel length modulation.

As the drain voltage reaches $V_{dsat}$, the electric field at the drain edge of the gate along the channel becomes comparable to vertical field. As the drain voltage is increased further the drain voltage effectively depletes the channel at the drain edge of the gate causing the effective channel length to decrease. This effect is shown schematically in figure 5-3. The device reacts as though its channel length has decreased thus increasing the drain current by a factor related to the length of the depleted region underneath the gate, $\Delta L$.

$$I_{ds} = \frac{I_{dsat}}{1 - (\Delta L / L)}$$  \hspace{1cm} (5.1)

Because $\Delta L$ increases as the drain bias is increased, the drain current continues to increase beyond $V_{dsat}$, causing positive output conductance.
Figure 5-3. Schematic diagram showing channel length modulation for an HFET biased beyond the saturation point. The channel is depleted in the region $\Delta L$ where the carriers reach saturation velocity.

5.2.2 Self heating

Self heating occurs when power is dissipated within a device in the form of heat. When the lattice temperature is increased electrons in the channel are subjected to increased scattering by phonons, thus reducing the mobility and saturated velocity. Reduced mobility and saturated velocity in turn cause the current to decrease. This effect can readily be observed in DC $I_d$ vs $V_d$ curves as negative output conductance in high power dissipation regions, figure 4-20. The magnitude of the localized temperature rise is given by equation 4.2. Detailed thermal analysis of GaN HFETs is given in chapter 4. This negative output conductance associated with self heating counteracts the positive output conductance associated with short channel effects. In regions of the $I_d$ versus $V_d$ curve with high drain voltage and low current, short channel effects dominate and in regions of high current and high drain voltage self heating can dominate, although the magnitude of self heating is dependent on the layer structure and the device geometry. Thus accurate thermal resistance modeling is essential for precise DC modeling.
5.2.3 Anomalous transients

To model the large signal characteristics of GaN HFETs, the device must be characterized in such a way that behavior under large current and voltage swings is captured. As discussed extensively in chapter three, pulsed I-V measurements are an appropriate way to extract this information. Under pulsed conditions the I-V curve corresponding to the quiescent bias point of the large signal measurement can be measured. In general, as the quiescent drain bias is increased, the on resistance and the knee voltage also increase. Also, for increasingly negative quiescent gate bias, the knee current is reduced, figure 3-1.

5.2.4 S-parameters

To capture the transistor’s switching and amplifying capability, careful attention must be paid to extraction of both DC and RF model parameters. The metrics \( F_T \) and \( F_{MAX} \) are used describe the frequency dependence of a transistor’s current gain and power gain respectively.

\[
F_{MAX} = \frac{F_T}{2 \sqrt{\frac{R_G + R_I + R_S}{R_{DS}}} + 2\pi \cdot F_T \cdot R_G \cdot C_{GD}}
\]

(5.2)

Where \( R_G \) is the gate resistance, \( R_I \) is the intrinsic resistance, \( R_S \) is the source resistance and \( R_{DS} \) is the total source-drain resistance. \( F_T \) the frequency of unity current gate is given by:

\[
F_T = \frac{G_m}{2\pi \cdot C_{GS}}
\]

(5.3)

Where \( Gm \) is the transconductance and \( C_{GS} \) is the gate to source capacitance. As seen in equations 5.3 and 5.4, \( F_T \) and \( F_{MAX} \) contain both DC and AC components. The final set
of characteristics that must be properly modeled for accurate design of power amplifier circuits are the scattering parameters. The s-parameters are a useful way to measure the transistors AC characteristics as function of bias at high frequencies. By assuming the appropriate equivalent circuit model, figure 5-4, the s-parameters can be converted to Y or Z parameters, from which, the device capacitances and AC conductances can be derived [3].

![Equivalent circuit model of FET structure used for small signal model extraction](image)

**Figure 5-4.** Equivalent circuit model of FET structure used for small signal model extraction [3].

### 5.2.4.1 Field plate effect on bias dependence of Cgd

One must pay particular attention when modeling the capacitance between the gate and drain, Cgd, for field plated transistors. This is because Cgd has a strong drain bias dependence. The capacitance between the field plate and channel is reduced as the access region between the gate and drain becomes depleted as the drain bias is increased. Cgd plays an important role in device performance, as captured by the figure of merit, $F_{\text{MAX}}$.

### 5.3 BSIM3 Based Model
A compact circuit model for GaN HFETs based on the BSIM3v3.3 MOSFET model with subcircuit elements added to represent the effects not captured in the intrinsic BSIM model was developed. BSIM3 was chosen as the base model for this work because it is physically based, scalable, and includes short channel effects and velocity saturation. The BSIM3 model, however, contains a multitude of parameters, many of which do not have physical significance in an HFET. Parameters related to the body effect are not used since the body effect does not occur in the GaN HFETs used in this work, because they were fabricated on a semi-insulating substrate. Accordingly, the parameter set was reduced from 128 to 24 parameters.

![Schematic of BSIM3 based compact model for GaN devices including self heating and transient effects.](image)

Figure 5-5. Schematic of BSIM3 based compact model for GaN devices including self heating and transient effects.

Of the remaining model parameters most correspond to physical components of the device. A spreadsheet was developed to estimate the model parameters, including the parasitics, from device geometry and layer structure. This allows designer to have some
predictive ability as well as flexibility by using transistor geometrical parameters for
circuit optimization and design. Additional elements and subcircuits are also included to
model the Schottky gate forward conduction, gate resistance, parasitic inductances and
capacitances, self-heating and transient phenomena, figure 5-5.

5.3.1 Device Layer Structure

The transistors modeled are AlGaN/GaN SHFETs grown and fabricated at HRL
Laboratories, LLC [4]. The devices were grown by plasma assisted MBE on semi-
insulating SiC substrates. The layer structure is as follows: 20 nm thick nucleation layer,
2 μm thick GaN buffer layer, and 30 nm thick Al_{0.3}Ga_{0.7}N Schottky barrier layer. The
transistors measured have a T-gate with a gate foot length of 0.15 μm and gate width of
100μm. The process includes surface passivation with SiNx.

5.3.2 Model Structure

With the extraneous model parameters set to zero, the basic I-V relationship is
given by:

\[
I_D = \frac{W}{L} \mu_n C_{ox} \left[ (V_{GS} - V_T) V_{DS,eff} - \frac{V_{DS,eff}^2}{2} \right] \left( 1 + \frac{V_{DS} - V_{DS,sat}}{V_A} \right) 
\]

(5.4)

Where \( W \) is the gate width, \( L \) is the gate length, \( \mu_n \) is the electron mobility \( C_{ox} \) is the
effective oxide capacitance, and \( V_T \) is the threshold voltage. \( V_{DS,eff} \) is the effective drain-
source voltage which contains a smoothing function to allow one equation to represent
the device in both the linear and saturation regions while simultaneously be infinitely
differentiable in \( V_{DS} \):

\[
V_{DS,eff} = V_{DS,sat} - \frac{1}{2} \left( V_{DS,sat} - V_{DS} - \Delta + \sqrt{(V_{DS,sat} - V_{DS} - \Delta)^2 + 4 \Delta V_{DS,sat}} \right) 
\]

(5.5)
The \(\left(1 + \frac{V_{DS} - V_{DS, sat}}{V_A}\right)\) portion of the equation incorporates the short channel effects into the calculation of output conductance at drain voltages greater than \(V_{DS, sat}\). The equations for \(V_T\) and \(\mu_n\) incorporate DIBL and velocity saturation respectively.

### 5.3.2.1 Subcircuits

To include the effects of self-heating on the I-V characteristics, a subcircuit was added that calculates the power dissipated in the device and the corresponding temperature increase at a given bias condition. The rise in temperature causes the drain current to decrease due to mobility degradation from increased phonon scattering. This is represented in the model as a dependent current source opposing the drain source current.

To model the temperature rise caused by power dissipation and thus the drop in drain current, the thermal resistance of the layer structure must be determined. The approach taken in this work was to use a three-dimensional thermal simulator to model the device and also to measure the thermal resistance using a novel electrical technique as discussed in chapter 4.

Transient effects including gate lag and drain lag was also qualitatively represented using subcircuits, figure 5-5. Gate lag was modeled as voltage source between the gate terminal of the internal BSIM3 model and external gate voltage which represents a threshold voltage shift dependent on the history of the transistor bias. An RC circuit was used to couple the applied gate voltage signal to the voltage source. Under DC conditions, this voltage source provides no gate voltage shift. Under pulsed gate voltage conditions, the applied voltage passes through the RC network, which reacts with a time constant of 1us reproducing the gate lag phenomenon, figure 5-6. Drain lag was
represented by voltage dependent drain resistance [7]. To implement the voltage dependence of the resistor, a current source was placed in parallel with the external drain resistance, whose current level depended exponentially on the applied drain bias. The applied drain bias was coupled through an RC network so that under DC conditions, the value of the drain resistance remains constant.

![Simulated Id vs. Vds under DC and pulsed conditions at a Vgs= 1V. Only the gate voltage was pulsed, from -5V to 1V with a 1us pulse width.](image)

**5.3.3 DC and RF fits**

The model was extracted from a suite of DC and s-parameter measurements on HFETs. Figures 5-6 and 5-7 show representative comparisons of measured versus modeled DC and RF characteristics.
Figure 5-7. Comparison of measurement and BSIM3 based model for DC I-V curves of a 100um T-gate SHFET on a SiC substrate.

Figure 5-8. Measured and model s-parameters from 1-40GHz for a 100um Wg T-gate SHFET on SiC at Vds=10V, Vgs=-3V.

Shown in figure 5-8 are model versus measurement comparisons of $F_T$ and $F_{MAX}$ extractions at a single bias point and in figure 5-9, $F_T$ versus drain bias for model and measurement is shown. The comparisons confirm the accuracy of both the DC and RF components of the model.
Figure 5-9. Comparison of measured and modeled $|H_{21}|$ and maximum available gain from 1-40GHz for $F_T$ and $F_{MAX}$ extraction of a 100um Wg T-gate SHFET on SiC at $V_{ds}=10V$ $V_{gs}=-3V$.

Figure 5-10. $F_T$ versus bias for a 100um Wg T-gate SHFET on SiC at $V_{ds}=10V$ $V_{gs}=-3V$.

5.3.4 Model drawbacks

While the BSIM based GaN HFET model adequately fits of DC and s-parameter data, discontinuities in the intrinsic BSIM3 equations lead to model convergence problems under large signal conditions. Also, while the subcircuits shown in figure 5.5 could qualitatively represent anomalous transients, exact fitting of pulsed I-V curves over a range of quiescent bias conditions was not possible with this model and the time
dependence of the current transients was more complex than the simple exponential relationship afforded by a single RC network.

5.4 EEHEMT

5.4.1 Model Description

The Agilent EEHEMT model [8] is an empirical analytical model specifically developed to fit the electrical behavior of HEMTs. It has an accurate isothermal drain current model that is capable of fitting a variety of processes. An advantage of this model is its flexible transconductance formulation which permits accurate fitting of transconductance compression found in GaN HFETs. The model includes a correction for self heating as well as a flexible charge model capable of fitting capacitance values over most bias ranges. Gate to drain breakdown and Gm dispersion [9,10] are also contained in the model. Another benefit of the EEHEMT model over other HFET models (such as the CFET model) is that the model expressions are not polynomials and formulated to be well behaved outside the region of extraction.

5.4.2 Devices Used for Model Extraction

The devices tested were AlGaN/GaN/AlGaN DHFETs grown and fabricated at HRL Laboratories. The devices were grown by plasma assisted MBE on semi-insulating SiC substrates [5]. The layer structure is as follows: 20 nm thick nucleation layer, 500 nm thick Al$_{0.04}$Ga$_{0.96}$N buffer layer, 40 nm thick pseudomorphically grown GaN channel layer, 20 nm thick Al$_{0.3}$Ga$_{0.7}$N Schottky barrier layer, and n+ cap layer consisting of 10 nm thick Al$_{0.3}$Ga$_{0.7}$N layer capped by a 10 nm thick GaN layer. The transistors measured have a recessed field plate gate with a gate foot length of 0.15 um and gate width of 200um. The process includes surface passivation with SiN$_x$. 

5.4.3 Model Equations

The drain current model in EEHEMT is comprised of various analytic expressions that were developed through examination of $g_m$ versus bias plots on a wide class of devices from various manufacturers [8]. The model assumes the device is symmetrical. The $g_m$, $g_{ds}$ and $I_{ds}$ equations take on four different forms depending on the value of $V_{gs}$ relative to some of the model parameters. The $I_{ds}$ expression is continuous through at least the second derivative everywhere. To model negative conductance effects due to self-heating, the thermal model of Canfield was incorporated [9].

$$I_{ds} = I_{ds}'(1 + Kapa \cdot V_{ds}) \cdot \tanh\left(\frac{3 \cdot V_{ds}}{V_{sat}}\right)$$  \hspace{1cm} (5.6)

$$I_{ds}' = Gmm(x) \cdot (V_{gs} - V_{ch})(1 + \Gammaamma(V_{dso} - V_{ds})) - \frac{V_{go} + V_{to}}{2} + V_{ch}$$  \hspace{1cm} (5.7)

This formulation of the drain current’s gate and drain voltage dependence allows for accurate fitting of all GaN HFET DC characteristics. Transient characteristics of the
transistor were captured using pulsed I-V measurements at the desired bias point for the PA design, figure 5-16.

![Figure 5-12. Schematic of EEHEMT model parameters for Gm versus Vgs representation [8].](image)

![Figure 5-13. Pulsed Ids versus Vds curves for a 6x100um Wg field plate DHFET on SiC, comparison of EEHEMT model and measurement. QVds=28V and QVgs=-3.2V with a pulsed width of 200ns and a pulsed separation of 1mS.](image)

5.4.4 Pad De-embedding

The transistors modeled in this section are of various gate widths from 300um to 1mm. Representative fits for a 6x100um device were used for demonstration purposes. When the devices are used in circuit applications, they are laid out differently than when configured for on wafer characterization of individual devices, specifically the probe pads
are not present in circuit applications. For accurate design of input and output matching networks for power amplifier circuits, parasitic inductance, capacitance and resistance due the contact pads must be de-embedded from the measured s-parameters of the device.

5.4.4.1 Cold FET Technique

To extract pad parasitics, the cold-fet method [3] was used. This method assumes that the equivalent circuit of the transistor can be portioned into intrinsic parameters which are dependent on bias conditions and extrinsic parameters which are bias independent, figure 5-3. To determine the extrinsic elements, s-parameter measurements at zero drain bias (causing no drain current to flow thus rendering the device “cold”) are performed. With the gate sufficiently forward biased and the drain voltage at zero, the gate capacitance is short circuited reducing the circuit to the series combination of resistances and parasitic inductances. S-parameters measured with the gate biased below pinch-off allow the parasitic pad capacitances to be determined. These to measurements combined with measurement of the source resistance using the end resistance technique [11] allow for all the parasitic elements to be determined [3].

5.4.4.2 De-embedded s-parameters

After the parasitics are de-embedded from the measured s-parameters the EEHMT model parameters are extracted. Comparison of the model with measurement is shown in figure 5-13.
Also, an important parameter to accurately model is the gate to drain capacitance particularly for precise representation of transistor gain as a function of drain bias, figure 5-14.

The magnitude of the incremental current gain, H21, and the maximum available gain, MAG, as a function of frequency for various bias conditions are shown in figure 5-15. There is very good agreement between measurement and model.
Figure 5-16. $|H21|$ and MAG/MSG versus frequency for various gate and drain biases for a 6x100um Wg field plate DHFET on SiC, comparison of EEHEMT model and measurement.

Figure 5-17. Simulation of load pull characteristics of a 6x100 um field plate DHFET at 10 GHz with $P_{in}=21$dBm, $V_{ds}=28$V and $V_{gs}=-3.2$V.

5.4.5 Large Signal Model Validation

After the model was extracted, load pull simulations were performed, figure 5-16.

The impedances predicted by the simulations for maximum power delivered to the load...
and for maximum PAE were compared to on wafer load pull measurements performed on the same devices. They were found to be within 5% of the measured values. Using the output match for maximum PAE, power sweep simulations were performed. A comparison of simulations and measurement is shown in figure 5-17. There is excellent agreement between simulation and measurement.

![Graph showing comparison between measured and modeled gain, output power (Pout), and power added efficiency (PAE) vs. input power (Pin) for a 6x100 um field plate DHFET at 10 GHz, Vds=28V and Vgs=-3.2V.](image)

Figure 5-18. Measured (solid) and modeled (circle) Gain, Pout and PAE vs. Pin for 6x100 um field plate DHFET at 10 GHz, Vds=28V and Vgs=-3.2V.

### 5.4.6 Conclusions

Modeling of GaN HFETs using the Agilent EEHEMT model has been performed on device of gate widths of 300um, 600um, 800um and 1mm. Pad parasitics were de-embedded from measured s-parameters using the cold-FET method. Load pull simulations and power sweep measurements using the extracted model show excellent agreement between measurements and model. However, one drawback of this model is that it is only accurate under large signal conditions for the quiescent bias point for the pulsed I-V curves were measured.
5.5 Virtual Gate Compact Model

The use of a model extracted from the pulsed I-V measurements at one particular quiescent bias point, such as the EEHEMT model just described, is a considerable limitation for circuit design. To effectively capture the large signal characteristics of GaN HFETs over a range of quiescent bias conditions and yet still be useful in circuit design, a compact model must be sufficiently complex to contain all pertinent information yet not overly so that parameter extraction and model fitting requires extensive effort and time. As discussed throughout this work and extensively in chapter 3, the anomalous transients observed in GaN HFETs caused by surface effects can be described as resulting from a virtual gate at the surface of the nitride layer. As seen in the simulations of chapter three, this virtual gate exists on the drain side of the gate and depletes the underlying channel to various extents depending on the quiescent bias. In an attempt to achieve to model the device characteristics, as well as maintain a connection to the physical mechanism of the underlying phenomena, a virtual gate based compact model was investigated under the assumption that the transient effects exhibited in GaN HFETs could be captured most simply by having two transistors in series; one to represent the standard device in the absence of surface effects and a second, which captures the anomalous transient behavior, represents the channel pinch-off by the virtual gate. For the remainder of this section, the individual transistor models for these to components of the overall model will be referred to as the main transistor and parasitic transistor. The entire model, including the two transistor models and the subcircuits to capture the time and voltage dependence will be referred as the virtual gate model. A proof of concept implementation of the model is the subject of this section.
The base transistor model used in this work was the EEHEMT model. Model parameters for the main transistor model and the parasitic transistor were fit to DC and pulsed I-V data taken using various quiescent bias points and pulse widths. A t-gate device with a gate length of 0.15um and gate width of 4x75um was measured. The following was observed about the measured pulsed I-V data relative to the DC data. At high quiescent Vds, the pulsed I-V data shows a large output conductance and high on resistance. This was implemented by using a shorter effective gate length and larger output conductance for the parasitic transistor model than that of the main transistor model. The drain resistance of the main transistor model was set to zero ohms and then accounted for in the parasitic model. The other model parameters for both device models used to fit the data. A circuit schematic of the model is shown in figure 5-19. On the left, the two transistors in series represent the parasitic (top) and main (bottom) components of the device. The virtual gate transistor captures the anomalous transients observed under pulsed conditions and the nominal transistor captures the DC characteristics. The right hand side of the figure shows the circuit which couples the applied drain bias to the gate of the virtual transistor and the drain of the nominal transistor.
**5.5.1 Quiescent Bias Dependence**

The quiescent bias dependence of the model was implemented by connecting the applied drain bias to the gate of the top transistor in the circuit, (which represents the virtual gate,) through an RC network and nonlinear, equation-based circuit element which translates the applied drain voltage to the appropriate sign and magnitude for a gate voltage. As the applied drain voltage is increased, the virtual gate voltage is made more negative, thus lowering the drain current and increasing the effective drain resistance. This represents the physical effect of an increased density of filled surface states with increased quiescent drain bias, which depletes the underlying channel thus increasing the drain resistance. A representative set of simulated $I_d$ versus $V_d$ curves for various quiescent drain biases is shown in figure 5-20. As discussed in chapter 3, the amount of knee voltage walk out exhibited by a device at a particular quiescent bias condition is
heavily dependent on device geometry. Because of its inherent flexibility, this model could be used to fit any set of pulsed I-V curves.

Figure 5-20. Measured (symbol) and simulated (line) pulsed Ids vs. Vds curves at Vgs=1V showing the quiescent drain bias dependence for a pulse width of $2 \times 10^{-7}$ s.

While not included in this model, the effect quiescent gate bias is another important factor to consider. It could be included in the same manner as shown here for the drain quiescent bias, by appropriate changes to the equation for the parasitic gate voltage.

### 5.5.2 Time Dependence

To incorporate the transient nature of these phenomena, the applied drain bias is capacitively coupled to the gate of the virtual transistor. Therefore, under DC conditions, the gate is biased at 1V, fully turning on the channel, and the voltage drop across the parasitic transistor represents the DC drain resistance. Similarly, in the measured data, under DC conditions charges populating surface states have time to react to changes bias and thus do not affect the transistor’s characteristics. In the model, the time dependence was represented by four RC networks in parallel to achieve the measured drain dependence on pulse width. The RC networks had time constants of 1us, 10us, 100us and 1mS. When added in parallel, the resultant voltage as logarithmic dependence on
time over the range of $2 \times 10^{-7}$ s to $1 \times 10^{-3}$ s as shown in figure 5-21. The measured and simulated response to a drain voltage pulse from 20V to the knee voltage (2V) divided by the DC drain current at 2V as a function of time is shown in figure 5-22.

For short pulse widths ($\leq 1$us), the resulting curve has a significant amount of current reduction at the knee voltage. As the pulse width increases the current returns to the DC level.
The simulated power performance as a function of quiescent drain bias with and without the virtual gate is compared to measured power data and is shown in figure 5-23. In the case where the device performance is predicted only from dc I-V (no virtual gate) measurements the power is linearly dependent on the drain voltage. When the virtual gate is included the simulated saturated output power agrees well with the measurements.

![Graph showing simulated and measured power as a function of Vds](image)

**Figure 5-23.** Saturated output power as a function of quiescent drain bias.

### 5.5.3 Summary

This section has demonstrated a proof of concept compact model based on the virtual gate physical model for describing the anomalous transients observed in GaN HFETs. Both the effects of quiescent drain bias and pulse width have been qualitatively implemented in this model. The power performance of the virtual gate model matches the trend seen in measured devices. Used in combination with an accurate large signal model, such as those described in previous sections, the virtual gate model would be better equipped accurately design advanced power amplifiers where the time and
quiescent bias dependence of these effects can have a significant impact in the large signal operation of the circuit.

5.6 Conclusion

The use of compact models to fit DC, pulsed I-V, small signal and large signal characteristic has been shown in this chapter. Both the physically based BSIM3 model combined with spice element subcircuits and the empirical EEHEMT model extracted from pulsed I-V curves have been shown to fit various GaN device sizes and gate geometries. A proof of concept virtual gate based compact circuit model has been demonstrated to implement the quiescent bias and time dependence of pulsed I-V curves.
5.7 References for Chapter 5


Chapter 6. Summary and Future Work

6.1 Summary

The primary motivation for the work contained in this dissertation was to design GaN based heterostructure field effect transistors (HFETs) with improved large signal performance at microwave and millimeter wave frequencies. The main obstacle to improved device performance was overcoming anomalous transients and thermal limitations occurring in conventional devices. Characterizing and modeling these effects was the first step towards the design of an improved device.

In this dissertation, characterization and modeling of various GaN based HFETs has been performed. Standard DC and RF characterization was used to calibrate TCAD simulation tools. Excellent agreement was achieved between simulations and measurement by including quantum and self-heating effects in the simulations. 2D simulations were then performed to optimize layer device structure and geometry for high frequency power amplifier applications. The effect of AlGaN barrier thickness, backside barriers, and field plate technologies were investigated. Fabricated devices show improved power performance over the conventional device structure.

Anomalous transients in these devices were characterized using pulsed I-V measurements on both T-gate and field plated devices. A new Frenkel-Poole surface conduction based model was implemented in 2D simulations which recreates the measured phenomena on a quasi-static basis. For the first time, a model accurately predicts the quiescent bias dependence of the anomalous transients as well as field plate affect on pulsed I-V curves.
A novel thermal resistance measurement technique was employed on GaN HFETs. 3D heat flow simulations using temperature dependent thermal conductivities were performed which agree very well with measurements as both a function of dissipated power and ambient temperature. The effect of device layer structure on thermal resistance was investigated.

Finally, compact circuit models were developed which accurately represent large signal device behavior. Device behavior under transient conditions was implemented using a virtual gate model structure giving the model the appropriate dependence on quiescent gate and drain biases.

**6.2 Suggestions for future work**

While much work was performed on optimization of device layer structure, the flexibility provided by the addition of polarization engineering to the already important bandgap engineering gives rise to almost endless possibilities for device design with the use of indium containing materials. Tailoring devices with optimum performance for a given application, whether the metric be switching speed, power density, efficiency or linearity will be possible in this material system. The use of quaternaries and indium containing ternaries for device design are already being incorporated by various groups. [1,2] Fabrication of devices with diamond deposited on the surface or back side also remains to be done. As presented in chapter four, significant reduction in overall thermal resistance (leading improved reliability and device performance) is expected by incorporating diamond [3].

Another benefit of using GaN devices is the extremely high breakdown field. While many conventional devices have exploited this property by applying very high
drain voltages to achieve extremely high power densities, an alternative approach could be to design ultra scaled devices that can operate at very high frequencies at more modest drain voltages and still deliver record power densities compared to other material systems.

Characterization of the linearity of GaN devices is still an area of research with very few reported results. The use of polarization effects for the design of composite channel devices for improved linearity should be investigated.

More work to characterize the transients in GaN devices is possible. There is evidence that capture and emission rates within these devices are very different. Using time domain measurements with various pulse trains could be used to characterize these differences. Extending 2D models to contain these asymmetric capture and emission rates could also be undertaken.

Also, the temperature dependence of the anomalous transients will provide insight into the energy levels of the surface and bulk states. If the energy levels associated with each mechanism are significantly different, it could provide a method for determining the origin of various transients. The addition of bulk states to the 2D model would be appropriate if their contribution to observed anomalous transients could be accurately extracted from measurements.

Much work still remains to be done in the compact modeling arena. Developing models flexible enough to accurately represent device characteristics in the presence of complex modulated input waveforms and with various gate geometries is an ongoing challenge.
6.3 References for Chapter 6


Appendix: ISE Dessis files

Boundary File for Mesh

#0.2um gate length device with 2um S-D spacing
GaN "gan" {rectangle[(-0.01,0.52) (2.21,0.6)]}
GaN "gan_buf" {rectangle[(-0.01,0.6) (2.21,2)]}
AlGaN "algan" {rectangle[(0,0.500) (2.2,0.52)]}
AlGaN "algan_sg" {rectangle[(0,0.4998) (1.0,0.500)]}
AlGaN "algan_gd" {rectangle[(1.2,0.4998) (2.2,0.5)]}
AlGaN "algan_edges1" {rectangle[(-0.01,0.495) (0.0,0.52)]}
AlGaN "algan_edges1" {rectangle[(2.2,0.495) (2.21,0.52)]}
AlGaN "condsin_sg" {rectangle[(0.0,0.495) (1.0,0.4995)]}
AlGaN "condsin_gd" {rectangle[(1.2,0.495) (2.2,0.4998)]}
Si3N4 "condsin" {rectangle[(1.0,0.45) (1.2,0.5)]}
Si3N4 "sin_gd" {rectangle[(1.2,0.45) (2.2,0.495)]}
Si3N4 "sin_sg" {rectangle[(-0.01,0.45) (1.2,0.495)]}
Contact "gate_ohm" {line[(1.0,0.495)(1.0,0.4997)]}
Contact "gate_ohm" {line[(1.2,0.495)(1.2,0.4997)]}
Contact "gate" {line[(1.001,0.5)(1.199,0.5)]}
Contact "source" {line[(-0.01,0.5203)(0.05,0.5203)]}
Contact "drain" {line[(2.15,0.5203)(2.21,0.5203)]}
Contact "source_condsin" {line[(0.0,0.495)(0.0,0.4996)]}
Contact "drain_condsin" {line[(2.2,0.495)(2.2,0.4996)]}
Command File for Mesh

Title "hydro dd gan hfet"
Controls {
}
Definitions {
  AnalyticalProfile "AnalyticalProfileDefinition_1"
  {
    Species = "BoronActiveConcentration"
    Function = Erf(SymPos = 0, MaxVal=1e15, Length = 0.1)
    LateralFunction = Erf(Factor = 0)
  }
  AnalyticalProfile "AnalyticalProfileDefinition_2"
  {
    Species = "PhosphorusActiveConcentration"
    Function = Erf(SymPos = 0, MaxVal=1e18, Length = 0.05)
    LateralFunction = Erf(Factor = 0)
  }
  Constant"ConstantProfileDefinition_1"
  {
    Species = "PhosphorusActiveConcentration"
    Value=5e19
  }
  Constant"ConstantProfileDefinition_2"
  {
    Species = "PhosphorusActiveConcentration"
    Value=1e15
  }
  Constant"ConstantProfileDefinition_3"
  {
    Species = "PhosphorusActiveConcentration"
    Value=1e19
  }
  Multibox "ganbuf2.mb"
  {
    MaxElementSize = ( 0.2 0.8 )
    MinElementSize = ( 0.2 0.3 )
    Ratio = ( 1 1.3 )
  }
  Multibox "ganbuf1.mb"
  {
    MaxElementSize = ( 0.1 0.2 )
    MinElementSize = ( 0.1 0.1 )
    Ratio = ( 1 1.2 )
  }
  Multibox "gan.mb"
  {
    MaxElementSize = ( 0.1 0.1 )
    MinElementSize = ( 0.1 0.01 )
    Ratio = ( 1 1.2 )
  }
  Multibox "gan_chan2.mb"
  {
    MaxElementSize = ( 0.1 0.01 )
  }
MinElementSize = ( 0.1 0.001 )
Ratio = ( 1 1.2 )
}
Multibox "algan.mb"
{
    MaxElementSize = ( 0.1 0.0025 )
    MinElementSize = ( 0.1 0.0025 )
    Ratio = ( 1 1 )
}
Multibox "sin.mb"
{
    MaxElementSize = ( 0.2 0.2 )
    MinElementSize = ( 0.2 0.005 )
    Ratio = ( 1 -1.2 )
}
Multibox "condsin.mb"
{
    MaxElementSize = ( 0.1 0.1 )
    MinElementSize = ( 0.1 0.005 )
    Ratio = ( 1 1 )
}
Multibox "channel.mb"
{
    MaxElementSize = ( 0.1 0.0002 )
    MinElementSize = ( 0.1 0.0002 )
    Ratio = ( 1 1 )
}
Multibox "algan_gate_drain.mb"
{
    MaxElementSize = ( 0.05 0.005 )
    MinElementSize = ( 0.05 0.005 )
    Ratio = ( 1 1 )
}
Multibox "gate_edge.mb"
{
    MaxElementSize = ( 0.02 0.1 )
    MinElementSize = ( 0.02 0.1 )
    Ratio = ( 1 1 )
}
Multibox "gate_edge2.mb"
{
    MaxElementSize = ( 0.005 0.1 )
    MinElementSize = ( 0.005 0.1 )
    Ratio = ( 1 1 )
}
Multibox "gate_edge3.mb"
{
    MaxElementSize = ( 0.0025 0.0005 )
    MinElementSize = ( 0.0025 0.0005 )
    Ratio = ( 1 1 )
}
Multibox "surftrap.mb"
{ MaxElementSize = ( 0.1 0.0001 )
MinElementSize = ( 0.1 0.0001 )
Ratio = ( 1 1 )
}

Multibox "contact.mb"
{
MaxElementSize = ( 0.02 0.0002 )
MinElementSize = ( 0.02 0.0002 )
Ratio = ( 1 1 )
}

Placements {
Constant "source_dop"
{
Reference = "ConstantProfileDefinition_1"
EvaluateWindow{
Element=Rectangle [( -0.01 0.5202 ) , ( 0.1 0.521 )]
DecayLength=0.0
}
}

Constant "drain_dop"
{
Reference = "ConstantProfileDefinition_1"
EvaluateWindow{
Element=Rectangle [( 2.1 0.5202 ) , ( 2.21 0.521 )]
DecayLength=0.00
}
}

Constant "draincondsin_dop"
{
Reference = "ConstantProfileDefinition_3"
EvaluateWindow{
Element=Rectangle [( 2.2 0.49 ) , ( 2.21 0.4998 )]
DecayLength=0.0
}
}

Constant "sourcecondsin_dop"
{
Reference = "ConstantProfileDefinition_3"
EvaluateWindow{
Element=Rectangle [( -0.01 0.49 ) , ( 0.0 0.4998 )]
DecayLength=0.0
}
}

Constant "condsin_dop"
{
Reference = "ConstantProfileDefinition_2"
EvaluateWindow{
Element=Rectangle [( 0.0 0.49 ) , ( 2.2 0.4997 )]
DecayLength=0.0
}
}

Multibox "ganbuf2.pl"
{
Reference = "ganbuf2.mb"
RefineWindow = Rectangle [( -0.01 1 ) , ( 2.21 2)]
}

Multibox "ganbuf1.pl"
{
Reference = "ganbuf1.mb"
}
RefineWindow = Rectangle [(-0.01 0.6), (2.21 1)]

Multibox "gan.pl" {
    Reference = "gan.mb"
    RefineWindow = Rectangle [(-0.01 0.55), (2.21 0.6)]
}

Multibox "gan_chan.pl" {
    Reference = "gan_chan2.mb"
    RefineWindow = Rectangle [(-0.01 0.52), (2.21 0.55)]
}

Multibox "algan.pl" {
    Reference = "algan.mb"
    RefineWindow = Rectangle [(-0.01 0.5), (2.21 0.52)]
}

Multibox "sin.pl" {
    Reference = "sin.mb"
    RefineWindow = Rectangle [(-0.01 0.45), (2.21 0.5)]
}

Multibox "surftrap.pl" {
    Reference = "surftrap.mb"
    RefineWindow = Rectangle [(-0.01 0.4997), (2.21 0.5001)]
}

Multibox "channel.pl" {
    Reference = "channel.mb"
    RefineWindow = Rectangle [(-0.01 0.5195), (2.21 0.521)]
}

Multibox "source.pl" {
    Reference = "contact.mb"
    RefineWindow = Rectangle [(-0.01 0.52), (0.05 0.5215)]
}

Multibox "drain.pl" {
    Reference = "contact.mb"
    RefineWindow = Rectangle [(2.15 0.52), (2.21 0.5215)]
}

Multibox "gate_edges.pl" {
    Reference = "gate_edge.mb"
    RefineWindow = Rectangle [(0.96 0.4995), (1.4 0.505)]
}

Multibox "gate_edged2.pl" {
    Reference = "gate_edge2.mb"
    RefineWindow = Rectangle [(1.19 0.4995), (1.25 0.521)]
}

Multibox "gate_edged3.pl" {
    Reference = "gate_edge3.mb"
    RefineWindow = Rectangle [(1.199 0.495), (1.23 0.5001)]
}

Offsetting {
    maxangle=180
    usebox=0
    triangulate=0
}
maxconnect=1000000
background=""
options=""
recoverholes=1

noffset {
    hlocal=0
    factor=1.3
    maxlevel=200
    terminateline=3
    maxedgelength=1000000
    subdivide=0
}

boundary {
    hglobal=1000000
}

}
Dessis Command file for Surface Conduction Simulations

File {

* input files:
  Grid = "nofp_p15_3_msh.grd"
  Doping = "nofp_p15_3_msh.dat"
  Parameters = "des_fp_3.par"
  PMIPath="."

* output files:
  Plot = "nofp_1p1e13_phibp3_m1_p15_3.dat"
  Current = "nofp_1p1e13_phibp3_m1_p15_3.plt"
  Output = "out_nofp_1p1e13_phibp3_m1_p15_3"
}

Electrode {
  {Name="source" Voltage=0.0 }
  {Name="source_condsin" Voltage=0}
  {Name="drain" Voltage=0.0 }
  {Name="drain_condsin" Voltage=0 }
  {Name="gate_ohm" Voltage=0.0 }
  {Name="gate" Voltage=0.0 Schottky Workfunction=5}
}

Physics {
  AreaFactor=1000
  Temperature=300
  Fermi
  EffectiveIntrinsicDensity(NoBandgapnarrowing)
  Thermionic
}

Physics (Material="AlGaN")
  {MoleFraction (xfraction=0.25)}

Physics (Region="condsin_sg")
  {Mobility (eHighfieldsaturation(pmi_PF_phibp3_m1 GradQuasiFermi))}

Physics (Region="condsin_gd")
  {Mobility (eHighfieldsaturation(pmi_PF_phibp3_m1 GradQuasiFermi))}

Physics (Region="algan_gd2")
  {Mobility (eHighfieldsaturation(pmi_PF_phibp3_m1 GradQuasiFermi))}

Physics (Region="algan_gd3")
  {Mobility (eHighfieldsaturation(pmi_PF_phibp3_m1 GradQuasiFermi))}

Physics (Region="algan_sg2")

Mobility \( (\text{eHighfieldsaturation}(\text{pmi}\_\text{PF}\_\text{phibp3}\_m1\ \text{GradQuasiFermi})) \)

Physics (Region="algan\_sg3")
{
  Mobility \( (\text{eHighfieldsaturation}(\text{pmi}\_\text{PF}\_\text{phibp3}\_m1\ \text{GradQuasiFermi})) \)
}

Physics (Region="algan\_sg")
{
  Mobility \( (\text{eHighfieldsaturation}(\text{pmi}\_\text{PF}\_\text{phibp3}\_m1\ \text{GradQuasiFermi})) \)
  Traps (acceptor level conc=5.5e20 fromCondBand EnergyMid=0.5 eXsection=1e-10
           hXsection=1e-15)
}

Physics (Region="algan\_gd")
{
  Mobility \( (\text{eHighfieldsaturation}(\text{pmi}\_\text{PF}\_\text{phibp3}\_m1\ \text{GradQuasiFermi})) \)
  Traps (acceptor level conc=5.5e20 fromCondBand EnergyMid=0.5 eXsection=1e-10
           hXsection=1e-15)
}

Physics (Material="GaN")
{
  Mobility \( (\text{eHighfieldsaturation}(\text{GradQuasiFermi})) \)
}

Physics (RegionInterface="algan/gan")
{
  HeteroInterface
  Charge(Uniform Conc=1.1e13)
}

Plot {
  eDensity hDensity eCurrent/Vector hCurrent/Vector
  ConductionCurrent/Vector Current/Vector DisplacementCurrent/Vector
  Potential/Vector SpaceCharge ElectricField/Vector eEnormal eEparallel
  eMobility hMobility eVelocity/Vector hVelocity/Vector
  Doping DonorConcentration AcceptorConcentration
  eJouleHeat eTemperature hJouleHeat hTemperature
  Bandgap ElectronAffinity
  ConductionBandEnergy eQuasiFermi
  ValenceBandEnergy hQuasiFermi
  xMoleFraction eTrappedCharge hTrappedCharge
}

Math {
  -\text{CheckUndefinedModels}
  Extrapolate
  DirectCurrentComputationAtContact
  Derivatives
  \text{RelErrControl}
  \text{Digits}=5
  \text{RhsFactor}=1e40
  \text{NewDiscretization}
}

Math {
  -\text{CheckUndefinedModels}
  Extrapolate
  DirectCurrentComputationAtContact
  Derivatives
  \text{RelErrControl}
  \text{Digits}=5
  \text{RhsFactor}=1e40
  \text{NewDiscretization}
}
ExitOnFailure
Iterations=10000
Cnormprint

##### Id vs Vds ###########################

Solve{
#-initial solution:
  Poisson
  Coupled {Poisson electron}
  Coupled {poisson electron hole}
  Plot (FilePrefix="I_nofp_1p1e13_phibp3_m1_p15_3")
save(FilePrefix="vg0vd0_nofp_1p1e13_phibp3_m1_p15_3")
NewCurrent="vg0_idvds_
  Quasistationary
    (MaxStep=0.5 MinStep=1e-5 initialstep=1e-3
     Increment=2 Decrement=1.5
     Goal{ Name="drain" Voltage=10 }
     Goal{ Name="drain_condsin" Voltage=10 }
   )
   {coupled(iterations=5) {poisson electron hole}}
  }
  Plot (FilePrefix="g0d10_nofp_1p1e13_phibp3_m1_p15_3")
  Quasistationary
    (MaxStep=0.5 MinStep=1e-4 initialstep=1e-2
     Increment=1.4 Decrement=1.5
     Goal{ Name="drain" Voltage=20 }
     Goal{ Name="drain_condsin" Voltage=20 }
   )
   {coupled(iterations=5) {poisson electron hole}}
  }
  Plot (FilePrefix="g0d20_nofp_1p1e13_phibp3_m1_p15_3")
NewCurrent="vd20_idvgs_
  Quasistationary
    (MaxStep=0.5 MinStep=1e-4 initialstep=1e-3
     Increment=2 Decrement=1.5
     Goal{ Name="gate" Voltage=-1 }
     Goal{ Name="gate_ohm" Voltage=-1 }
   )
   {coupled(iterations=5) {poisson electron hole}}
  }
  Plot (FilePrefix="g-1d20_nofp_1p1e13_phibp3_m1_p15_3")
  Quasistationary
    (MaxStep=0.5 MinStep=1e-4 initialstep=1e-3
     Increment=2 Decrement=1.5
Goal{ Name="gate" Voltage=-2 }
Goal{ Name="gate_ohm" Voltage=-2 }
}
coupled(iterations=5) {poisson electron hole}

Plot ( FilePrefix="g-2d20_nofp_1p1e13_phibp3_m1_p15_3"
Quasistationary
               MaxStep=0.5 MinStep=1e-4 initialstep=1e-3
Increment=2 Decrement=1.5
Goal{ Name="gate" Voltage=-3 }
Goal{ Name="gate_ohm" Voltage=-3 }
}
coupled(iterations=5) {poisson electron hole}

Plot ( FilePrefix="g-3d20_nofp_1p1e13_phibp3_m1_p15_3"
Quasistationary
               MaxStep=0.5 MinStep=1e-4 initialstep=1e-3
Increment=2 Decrement=1.5
Goal{ Name="gate" Voltage=-4 }
Goal{ Name="gate_ohm" Voltage=-4 }
}
coupled(iterations=5) {poisson electron hole}

Plot ( FilePrefix="g-4d20_nofp_1p1e13_phibp3_m1_p15_3"
load(FilePrefix="vg0vd0_nofp_1p1e13_phibp3_m1_p15_3"
Quasistationary
               MaxStep=0.5 MinStep=1e-4 initialstep=1e-3
Increment=2 Decrement=1.5
Goal{ Name="gate" Voltage=-5 }
Goal{ Name="gate_ohm" Voltage=-5 }
}
coupled(iterations=5) {poisson electron hole}

Plot ( FilePrefix="g-5d0_nofp_1p1e13_phibp3_m1_p15_3"
### Ramp drain
Quasistationary
               MaxStep=0.5 MinStep=1e-4 initialstep=1e-2
Increment=1.4 Decrement=1.5
Goal{ Name="drain" Voltage=10 }
Goal{ Name="drain_condsin" Voltage=10 }
}
coupled(iterations=5) {poisson electron hole}

Plot ( FilePrefix="g-5d10_nofp_1p1e13_phibp3_m1_p15_3"
Quasistationary

MaxStep=0.5 MinStep=1e-4 initialstep=1e-2
Increment=1.4 Decrement=1.5
Goal{ Name="drain" Voltage=20 }
Goal{ Name="drain_condsin" Voltage=20 }
)
{coupled(iterations=5 ) {poisson electron hole}

Plot ( FilePrefix="g-5d20_nofp_1p1e13_phibp3_m1_p15_3" )

Quasistationary

MaxStep=0.5 MinStep=1e-4 initialstep=1e-2
Increment=1.4 Decrement=1.5
Goal{ Name="drain" Voltage=30 }
Goal{ Name="drain_condsin" Voltage=30 }
)
{coupled(iterations=5 ) {poisson electron hole}}
Plot ( FilePrefix="g-5d30_nofp_1p1e13_phibp3_m1_p15_3" )

Quasistationary

MaxStep=0.5 MinStep=1e-5 initialstep=1e-2
Increment=1.4 Decrement=1.5
Goal{ Name="drain" Voltage=40 }
Goal{ Name="drain_condsin" Voltage=40 }
)
{coupled(iterations=5 ) {poisson electron hole}}
Plot ( FilePrefix="g-5d40_nofp_1p1e13_phibp3_m1_p15_3" )

Quasistationary

MaxStep=0.5 MinStep=1e-5 initialstep=1e-2
Increment=1.4 Decrement=1.5
Goal{ Name="drain" Voltage=50 }
Goal{ Name="drain_condsin" Voltage=50 }
)
{coupled(iterations=5 ) {poisson electron hole}}
Plot ( FilePrefix="g-5d50_nofp_1p1e13_phibp3_m1_p15_3" )

}
Dessis Command file Including Quantum and Temperature dependent effects

******************************************************************************
# GaN HFET Simulation Deck       #
# Id vs Vds, Id vs Vgs         #
# Models Turned On:           #
# Drift-Diffusion Transport   #
# Temperature Dependent       #
# Fermi Statistics            #
# Density Gradient Model      #
# # #
# Adam Conway                   #
# 10-9-2006                    #
******************************************************************************

File {

* input files:
   Grid = "D14_fp_tdep_msh.grd"
   Doping = "D14_fp_tdep_msh.dat"
   Parameters = "des_D14_Tdep.par"
   #PMIPath="."
* output files:
   Plot = "Q_Tdep_dd_D14_fp.dat"
   Current = "Q_fp_mup1p2k_v2p2_B1p3_D14_Tdep_dd.plt"
   Output = "out_Q_Tdep_dd_D14_fp"
}

Electrode {
   {Name="source" Voltage=0.0}
   {Name="drain" Voltage=0.0}
   {Name="gate" Voltage=0.0 Schottky Barrier=1.76 }
}

Thermode {
   {Name="bottom" Temperature=300}
}

Physics {
   AreaFactor=1000
   Temperature=300
   # Hydrodynamic(etemperature)
   Mobility ( eHighfieldsaturation(GradQuasiFermi) )
   eQuantumPotential
   Fermi
   Thermodynamic
}

############### SHFET Physics Section #####################

Physics (Material="AlGaN")
   {
      MoleFraction (xfraction=0.25)
   }

Physics (MaterialInterface="AlGaN/GaN")
{ 
HeteroInterface 
Charge(Uniform Conc=1.12e13) 
} 

Physics (RegionInterface="sin_sg/algan") 
{ 
 Charge (Uniform Conc=-1e12) 
} 

Physics (RegionInterface="sin_gd/algan") 
{ 
 Charge (Uniform Conc=-1e12) 
} 

Physics (Material="Si3N4") 
{ 
  -eQuantumPotential 
} 

Plot 
{ 
  eDensity hDensity eCurrent/Vector hCurrent/Vector 
  ConductionCurrent/Vector Current/Vector DisplacementCurrent/Vector 
  Potential/Vector SpaceCharge ElectricField/Vector eNormal eParallel 
  eMobility hMobility eVelocity/Vector hVelocity/Vector 
  Doping DonorConcentration AcceptorConcentration 
  eJouleHeat eTemperature hJouleHeat hTemperature 
  Temperature TotalHeat LatticeTemperature ThermalConductivity 
  Bandgap ElectronAffinity ConductionBandEnergy eQuasiFermi 
  ValenceBandEnergy hQuasiFermi xMoleFraction eTrappedCharge hTrappedCharge 
  eQuantumPotential 
} 

Math 
{ 
  -CheckUndefinedModels 
  Extrapolate 
  DirectCurrentComputationAtContact 
  Derivatives 
  RelErrControl 
  NewDiscretization 
  ExitOnFailure 
  Iterations=1000 
  Cnормprint 
} 

#### Id vs Vds #################### 

Solve 
{ 
#-initial solution: 
  Poisson 
  Coupled {Poisson eQuantumPotential} 
  Coupled {poisson electron eQuantumPotential} 
  Coupled {poisson electron hole eQuantumPotential} 
  Coupled {poisson electron hole eQuantumPotential temperature} 
  Plot (FilePrefix="I_Q_fp_mu1p2k_v2p2_B1p3_D14_Tdep_dd") 
} 

Quasistationary
### Ramp drain voltage

Quasistationary

\[
\begin{align*}
\text{MaxStep} &= 1 \times 10^{-1} \\
\text{MinStep} &= 1 \times 10^{-5} \\
\text{initialstep} &= 1 \times 10^{-2} \\
\text{Increment} &= 1.4 \\
\text{Decrement} &= 1.5 \\
\text{Goal} &= \{ \text{Name} = \text{gate}, \text{Voltage} = -3 \} \\
\end{align*}
\]

\{ coupled(iterations=5) \} \{ poisson electron hole temperature eQuantumPotential \} }

NewCurrent="Idvds_vg-3"

### Ramp gate voltage

Quasistationary

\[
\begin{align*}
\text{MaxStep} &= 1 \times 10^{-1} \\
\text{MinStep} &= 1 \times 10^{-5} \\
\text{initialstep} &= 5 \times 10^{-4} \\
\text{Increment} &= 1.3 \\
\text{Decrement} &= 1.4 \\
\text{Goal} &= \{ \text{Name} = \text{drain}, \text{Voltage} = 10 \} \\
\end{align*}
\]

\{ coupled(iterations=5) \} \{ poisson electron hole temperature eQuantumPotential \} }

NewCurrent="temp"

### Ramp drain voltage

Quasistationary

\[
\begin{align*}
\text{MaxStep} &= 1 \times 10^{-1} \\
\text{MinStep} &= 1 \times 10^{-5} \\
\text{initialstep} &= 1 \times 10^{-3} \\
\text{Increment} &= 1.4 \\
\text{Decrement} &= 1.5 \\
\text{Goal} &= \{ \text{Name} = \text{gate}, \text{Voltage} = -1 \} \\
\end{align*}
\]

\{ coupled(iterations=5) \} \{ poisson electron hole temperature eQuantumPotential \} }

NewCurrent="Idvds_vg-2"

### Ramp gate voltage

Quasistationary

\[
\begin{align*}
\text{MaxStep} &= 1 \times 10^{-1} \\
\text{MinStep} &= 1 \times 10^{-5} \\
\text{initialstep} &= 5 \times 10^{-4} \\
\text{Increment} &= 1.3 \\
\text{Decrement} &= 1.4 \\
\text{Goal} &= \{ \text{Name} = \text{drain}, \text{Voltage} = 0 \} \\
\end{align*}
\]

\{ coupled(iterations=5) \} \{ poisson electron hole temperature eQuantumPotential \} }

NewCurrent="temp"

### Ramp drain voltage

Quasistationary

\[
\begin{align*}
\text{MaxStep} &= 1 \times 10^{-1} \\
\text{MinStep} &= 1 \times 10^{-5} \\
\text{initialstep} &= 1 \times 10^{-3} \\
\text{Increment} &= 1.4 \\
\text{Decrement} &= 1.5 \\
\text{Goal} &= \{ \text{Name} = \text{gate}, \text{Voltage} = -2 \} \\
\end{align*}
\]

\{ coupled(iterations=5) \} \{ poisson electron hole temperature eQuantumPotential \} }

NewCurrent="Idvds_vg-2"

### Ramp drain voltage
Quasistationary

(  
MaxStep=1e-1 MinStep=1e-5 initialstep=5e-4  
Increment=1.3 Decrement=1.4  
Goal{ Name="drain" Voltage=10 }  
)  
{coupled(iterations=5) {poisson electron hole temperature eQuantumPotential}}

NewCurrent="temp"

### Ramp gate voltage
Quasistationary

(  
MaxStep=1e-1 MinStep=1e-5 initialstep=1e-3  
Increment=1.4 Decrement=1.5  
Goal{ Name="gate" Voltage=-3 }  
)  
{coupled(iterations=5) {poisson electron hole temperature eQuantumPotential}}

NewCurrent="Idvds_vg-3"

### Ramp drain voltage
Quasistationary

(  
MaxStep=1e-1 MinStep=1e-5 initialstep=5e-4  
Increment=1.3 Decrement=1.4  
Goal{ Name="drain" Voltage=0 }  
)  
{coupled(iterations=5) {poisson electron hole temperature eQuantumPotential}}

}
Parameter files
GaN

* Matched Madelung p89 for E perpendicular to c
* Epsilon
  * Ratio of the permittivities of material and vacuum
    * epsilon() = epsilon
      epsilon  = 9.5

* Values for 2DEG at AlGaN/GaN interface
* Values from http://www.ioffe.rssi.ru/SVA/NSM/Semicond/GaN

ConstantMobility:
  * mu_const = mumax (T/T0)^(-Exponent)
    mumax  = 1.2e+03 , 1.00e+01  # [cm^2/(Vs)]
    Exponent  = 1.50 , 0.00    # [Conway 9-27-06]

QuantumPotentialParameters
  * gamma: weighting factor for quantum potential
  * theta: weight for quadratic term
  * xi: weight for quasi Fermi potential
  * eta: weight for electrostatic potential
    gamma = 3.6 , 5.6 # [1]
    gamma = 0.45 , 5.6 # [1]
    theta = 0.5 , 0.5 # [1]
    xi    = 1 , 1  # [1]
    eta   = 1 , 1  # [1]

* Values from http://www.ioffe.rssi.ru/SVA/NSM/Semicond/GaN
* Used Chin et al experimental data assuming theta = 0.75
* This leads to a ~1E17cm-3 concentration for constant mu model
* Curve fitting yielded horrible results
* Doping dependence turned off, set to constant mobility parameters

DopingDependence:
  * For doping dependent mobility model three formulas can be used. Formula1 is based on Masetti et al. approximation.
  * Formula2 uses approximation, suggested by Arora.
  * Changing Masetti to equal Thomas-Caughey
  * Formula2 uses approximation, suggested by Arora.
  * formula = 2 , 2 # [1]
    formula = 1 , 1  # Mnatsakanov et al.
* If formula=1, model suggested by Masetti et al. is used:
* mu_dop = mumin1 exp(-Pc/N) + (mu_const - mumin2)/(1+(N/Cr)^alpha)
*   - mu1/(1+(Cs/N)\^beta)
* with mu_const from ConstantMobility
  mumin1 = 55 , 3  # [cm^2/Vs]
  mumin2 = 55 , 3  # [cm^2/Vs]
  mu1    = 0 , 0  # [cm^2/Vs]
  Pc      = 0.0000e+00 , 0 # [cm^3]
\[
\begin{align*}
Cr &= 2e17, 3e17 \quad \text{[cm}^3]\text{]} \\
Cs &= 0.0, 0.000e+0 \quad \text{[cm}^3]\text{]} \\
\text{alpha} &= 1, 2 \quad \text{[#1]} \\
\text{beta} &= 1, 1 \quad \text{[#1]} \\
\text{If formula} &= 2, \text{model suggested by Arora is used:} \\
* \mu_dop &= \text{mumin}_A + \text{mud}_A/(1+(N/N00)^A A), \\
* \text{where mumin}_A &= \text{Ar}_mumin(T/T0)^\text{Ar}_alm; \text{mud}_A = \text{Ar}_mud(T/T0)^\text{Ar}_ald \\
* N &= \text{net doping} \\
* N00 &= \text{Ar}_N0(T/T0)^\text{Ar}_alN; AA &= \text{Ar}_a(T/T0)^\text{Ar}_ala \\
* \text{Ar}_mumin &= +3.00e+02, +1.50e+02 \quad \text{[cm}^2/\text{Vs}] \\
* \text{Ar}_alm &= -1.75e+00, -6.60e+00 \quad \text{[#1]} \\
* \text{Ar}_mumin &= +5.50e+02, +1.00e+01 \quad \text{[cm}^2/\text{Vs}] \\
* \text{Ar}_alm &= +0.00e+00, +0.00e+00 \quad \text{[#1]} \\
* \text{Ar}_mud &= +0.00e+00, +0.00e+00 \quad \text{[#1]} \\
* \text{Ar}_ald &= +1.00e+00, +1.00e+00 \quad \text{[#1]} \\
* \text{Ar}_N0 &= +0.00e+00, +0.00e+00 \quad \text{[#cm}^3(-3)] \\
* \text{Ar}_alN &= +1.00e+00, +1.00e+00 \quad \text{[#1]} \\
* \text{Ar}_a &= +0.00e+00, +0.00e+00 \quad \text{[#1]} \\
* \text{Ar}_ala &= +1.00e+00, +1.00e+00 \quad \text{[#1]} \\
\end{align*}
\]

* Values from GaAs (needs update)
* Only velocity saturation and field at peak velocity value updated
* Holes and electrons are equal
* Temperature dependence of vsat removed

\text{HighFieldDependence:}
{ * Caughey-Thomas model: \\
* \mu_{highfield} = \mu_{lowfield} / ( 1 + (\mu_{lowfield} E / vsat)^\beta)^\beta \text{betaexp.} \\
\begin{align*}
\text{beta0} &= 1.3, 1.7 \quad \text{[#1]} \\
\text{betaexp} &= 0.0000e+00, 0.0000e+00 \quad \text{[#1]} \\
\end{align*}

* Smoothing parameter for HydroHighField Caughey-Thomas model: \\
* if T_1 < T_c < (1+K_dT)*T_1, then smoothing between low field mobility \\
* and HydroHighField mobility is used.
\begin{align*}
K_{dT} &= 0.2, 0.2 \quad \text{[#1]} \\
\end{align*}

* Transferred-Electron Effect: \\
* \mu_{highfield} = (\mu_{lowfield}+(vsat/E)\text*(E/E0_{TrEf})^4)/(1+(E/E0_{TrEf})^4) \\
\begin{align*}
E0_{TrEf} &= 1.2500e+05, 1.2500e+05 \quad \text{[#1]} \\
K_{smooth_{TrEf}} &= 1, 1 \quad \text{[#1]} \\
\end{align*}

* For vsat either Formula1 or Formula2 can be used.
\begin{align*}
Vsat_{Formula} &= 2, 2 \quad \text{[#1]} \\
\end{align*}

* Formula2 for saturation velocity: \\
* \text{vsat} = A_{vsat} - B_{vsat}(T/T0) \\
* (Parameter Vsat_{Formula} has to be equal to 2): \\
\begin{align*}
A_{vsat} &= 1.32e+07, 1.00e+07 \quad \text{# Adam 9-27-06} \\
A_{vsat} &= 2.2e+07, 1.00e+07 \quad \text{# Adam 9-27-06} \\
B_{vsat} &= 0.0000e+00, 0.0000e+00 \quad \text{[#1]} \\
vsat_{min} &= 1.000e+06, 1.000e+06 \quad \text{# Adam 1-23-06} \\
\end{align*}
* Value from Madelung p88
RefractiveIndex
{ * Optical Refractive Index

* refractiveindex() = refractiveindex * (1 + aplha * (T-Tpar))
  refractiveindex  = 2.29
  alpha  = 1.6000e-05
  Tpar  = 3.0000e+02
}

* Value from http://www.ioffe.rssi.ru/SVA/NSM/Semicond/GaN
LatticeHeatCapacity
{ * lumped electron-hole-lattice heat capacity

* cv() = cv + cv_b * T + cv_c * T^2 + cv_d * T^3
  cv  = 5.63  # [J/(K cm^3)]
  cv_b  = 1.3200e-03  # [J/(K^2 cm^3)]
  cv_c  = 0.0000e+00  # [J/(K^3 cm^3)]
  cv_d  = 0.0000e+00  # [J/(K^4 cm^3)]
}

* Value from Madelung p88 (temperature invariant)
Kappa
{ * Lattice thermal conductivity

  Formula = 1:
  * kappa() = kappa + kappa_b * T + kappa_c * T^2
    kappa  = 4.0912  # [W/(K cm)]
    kappa_b  = -7.62e-03  # [W/(K^2 cm)]
    kappa_c  = 5e-06  # [W/(K^3 cm)]
}

* Value from GaAs (needs update)
EnergyRelaxationTime
{ * Energy relaxation times in picoseconds
  (tau_w)_ele  = 0.1  # [ps]
  (tau_w)_hol  = 0.1  # [ps]
}

* Impact ionization factors at http://www.ioffe.rssi.ru/SVA/NSM/Semicond/GaN
AvalancheFactors
{ * Coefficients for avalanche generation with hydro
  * Factors n_1_f, p_1_f for energy relaxation length in the expressions
  * for effective electric field for avalanche generation
  * eEeff = eEeff / n_1_f ( or b = b*n_1_f )
  * hEeff = hEeff / p_1_f ( or b = b*p_1_f )
  * Additional coefficients n_gamma, p_gamma, n_delta, p_delta
    n_1_f  = 0.8  # [1]
    p_1_f  = 0.8  # [1]
    n_gamma  = 0.0000e+00  # [1]
    p_gamma  = 0.0000e+00  # [1]
    n_delta  = 0.0000e+00  # [1]
    p_delta  = 0.0000e+00  # [1]
Eg = Eg0 + alpha Tpar^2 / (beta + Tpar) - alpha T^2 / (beta + T)

- Parameter 'Tpar' specifies the value of lattice temperature, at which parameters below are defined
- Chi0 is electron affinity.

Chi0 = 4.10 # [eV]
Bgn2Chi = 0.5 # [1]
Eg0 = 3.427 # [eV]
alpha = 9.3900e-04 # [eV K^-1]
beta = 7.7200e+02 # [K]
Tpar = 0.0000e+00 # [K]

For effective mass specification Formula1 (me approximation):

* For effective mass specification Formula1 (me approximation):
* or Formula2 (Nc300) can be used:

Formula = 2 # [1]

Formula2:
* me/m0 = (Nc300/2.540e19)^2/3
* Nc(T) = Nc300 * (T/300)^3/2
  Nc300 = 2.300e+18 # [cm-3]

For effective mass specification Formula1 (mh approximation):

* For effective mass specification Formula1 (mh approximation):
* or Formula2 (Nv300) can be used:

Formula = 2 # [1]

Formula2:
* mh/m0 = (Nv300/2.540e19)^2/3
* Nv(T) = Nv300 * (T/300)^3/2
  Nv300 = 4.6200e+19 # [cm-3]

For the hole masses for Schroedinger equation you can use different formulas.

- formula=1 (for materials with Si-like hole band structure)
- m(k)/m0=1/(A+-sqrt(B+C*((xy)^2+(yz)^2+(zx)^2)))
- where k=(x,y,z) is unit normal vector in reziprocal space. '+' for light hole band, '-' for heavy hole band

* formula=2: Heavy hole mass mh and light hole mass ml are specified explicitly.

* formula=3: A is the relative effective mass. This formula must only be used for metal and will be used in tunnelling current computation only.

* formula<0 means no default model and no default parameters
* are available, so you have to provide values for
* 'formula' and the respective parameters in order to use
* this parameter set.

    formula = 2  # [1]

* Formula 2 parameters:

    ml  = 0.259  # [1]
    mh  = 1.400  # [1]

}  

* Impact ionization factors at http://www.ioffe.rssi.ru/SVA/NSM/Semicond/GaN
vanOverstraetendeMan * Impact Ionization:

    * G_impact = alpha_n n v_drift_n + alpha_p p v_drift_p
* with alpha = gamma a \exp(-b gamma/E) for E<E0 (low) and E>E0 (high)
* with gamma = tanh(hbarOmega/(2kT0)) / tanh(hbarOmega/(2kT))

    a(low)  = 4.0000e+08 , 1.3400e+08  # [1/cm]
    a(high) = 4.0000e+08 , 1.3400e+08  # [1/cm]
    b(low)  = 2.3000e+08 , 2.0300e+08  # [V/cm]
    b(high) = 2.3000e+08 , 2.0300e+08  # [V/cm]
    E0      = 4.0000e+08 , 4.0000e+08  # [V/cm]
    hbarOmega = 0.035 , 0.035  # [eV]
AlGaN

* All values taken from Asbeck's 1DPS material file
* Remaining unknowns filled in from Ioffe website

Epsilon

* Ratio of the permittivities of material and vacuum

* epsilon() = epsilon
  epsilon = 9.50  # [1]
* Mole fraction dependent model.
* If just above parameters are specified, then its values will be
* used for any mole fraction instead of an interpolation below.
* The linear interpolation is used on interval [0,1].
  epsilon(1) = 8.5  # [1]

QuantumPotentialParameters

* gamma: weighting factor for quantum potential
* theta: weight for quadratic term
* xi: weight for quasi Fermi potential
* eta: weight for electrostatic potential
* gamma = 3.6 , 5.6  # [1]
  gamma = 0.45 , 5.6  # [1]
  theta = 0.5 , 0.5  # [1]
  xi = 1 , 1  # [1]
  eta = 1 , 1  # [1]

RefractiveIndex

* Optical Refractive Index

* refractiveindex() = refractiveindex * (1 + alpha * (T-Tpar))
  refractiveindex = 2.2900# [1]
  alpha = 1.6000e-05  # [1/K]
  Tpar = 3.0000e+02  # [K]
* Mole fraction dependent model.
* If just above parameters are specified, then its values will be
* used for any mole fraction instead of an interpolation below.
* The linear interpolation is used on interval [0,1].
  refractiveindex(1) = 2.15000  # [1]
  alpha(1) = 1.6000e-05  # [1/K]

LatticeHeatCapacity

* AlN specific heat needs a second order term of T^-2 order

* cv() = cv + cv_b * T + cv_c * T^2 + cv_d * T^3
  cv = 5.63  # [J/(K cm^3)]
  cv_b = 1.3200e-03  # [J/(K^2 cm^3)]
  cv_c = 0.0000e+00  # [J/(K^3 cm^3)]
  cv_d = 0.0000e+00  # [J/(K^4 cm^3)]
* Mole fraction dependent model.
* If just above parameters are specified, then its values will be
* used for any mole fraction instead of an interpolation below.
* The linear interpolation is used on interval [0,1].
  \[ cv(1) = 6.79 \] \[ J/(K\text{cm}^3) \]
  \[ cv_b(1) = 4.9500e-04 \] \[ J/(K^2\text{cm}^3) \]
  \[ cv_c(1) = 0.0000e+00 \] \[ J/(K^3\text{cm}^3) \]
  \[ cv_d(1) = 0.0000e+00 \] \[ J/(K^4\text{cm}^3) \]
}

* Temperature dependence turned off
* Ioffe website has T dependent data
Kappa
{ *
* Lattice thermal conductivity

Formula = 1
  \[ \kappa() = \kappa + \kappa_b * T + \kappa_c * T^2 \]
  \[ \kappa = 1.30 \] \[ W/(K \text{ cm}) \]
  \[ \kappa_b = 0.0000e+00 \] \[ W/(K^2 \text{ cm}) \]
  \[ \kappa_c = 0.0000e+00 \] \[ W/(K^3 \text{ cm}) \]
* Mole fraction dependent model.
* If just above parameters are specified, then its values will be
* used for any mole fraction instead of an interpolation below.
* The following interpolation polynomial can be used on interval [Xmin(I),Xmax(I)]:
  \[ F(X) = F(I-1)+A(I)*(X-Xmin(I))+B(I)*(X-Xmin(I))^2+C(I)*(X-Xmin(I))^3, \]
  * where Xmax(I), F(I), B(I), C(I) are defined below for each interval.
  * A(I) is calculated for a boundary condition F(Xmax(I)) = F(I).
  * Above parameters define values at the following mole fraction:
    \[ Xmax(0) = 0.0000e+00 \] \[ 1 \]
* Definition of mole fraction intervals, parameters, and coefficients:
  \[ Xmax(1) = 1 \] \[ 1 \]
  \[ \kappa(1) = 2.85 \] \[ W/(K \text{ cm}) \]
  \[ B(\kappa(1)) = 0.0000e+00 \] \[ W/(K \text{ cm}) \]
  \[ C(\kappa(1)) = 0.0000e+00 \] \[ W/(K \text{ cm}) \]
  \[ \kappa_b(1) = 0.0000e+00 \] \[ W/(K^2 \text{ cm}) \]
  \[ B(\kappa_b(1)) = 0.0000e+00 \] \[ W/(K^2 \text{ cm}) \]
  \[ C(\kappa_b(1)) = 0.0000e+00 \] \[ W/(K^2 \text{ cm}) \]
  \[ \kappa_c(1) = 0.0000e+00 \] \[ W/(K^3 \text{ cm}) \]
  \[ B(\kappa_c(1)) = 0.0000e+00 \] \[ W/(K^3 \text{ cm}) \]
  \[ C(\kappa_c(1)) = 0.0000e+00 \] \[ W/(K^3 \text{ cm}) \]
}

EnergyRelaxationTime
{ *
* Energy relaxation times in picoseconds
  \[ (\tau_w)_{\text{ele}} = .1 \] \[ \text{ps} \] conway 5-6-04
  \[ (\tau_w)_{\text{hol}} = 0.4 \] \[ \text{ps} \] conway 5-6-04
}

* Values from AlGaAs (needs update)
AvalancheFactors
{ *
* Coefficient for avalanche generation with hydro
* Factors n_1_f, p_1_f for energy relaxation length in the expressions
* for effective electric field for avalanche generation
  \[ eE_{\text{eff}} = eE_{\text{eff}}/n_1_f \] ( or \( b = b*n_1_f \)
  \[ hE_{\text{eff}} = hE_{\text{eff}}/p_1_f \] ( or \( b = b*p_1_f \)
* Additional coefficients n_gamma, p_gamma, n_delta, p_delta
n_l_f = 0.8 # [1]
p_l_f = 0.8 # [1]
n_gamma = 0.0000e+00 # [1]
p_gamma = 0.0000e+00 # [1]
n_delta = 0.0000e+00 # [1]
p_delta = 0.0000e+00 # [1]

} Values from Ioffe, Asbeck's 1DPS, and guesses
* Modified AlN Chi and EG from Martin et al paper

Bandgap
{ * Eg = Eg0 + alpha Tpar^2 / (beta + Tpar) - alpha T^2 / (beta + T)
* Parameter 'Tpar' specifies the value of lattice
* temperature, at which parameters below are defined
* Chi0 is electron affinity.
  Chi0 = 4.10000 # [eV]
  Bgn2Chi = 0.5
  Eg0 = 3.427 # [eV]
  alpha = 9.3900e-04 # [eV K^-1]
  beta = 7.7200e+02 # [K]
  Tpar = 0.0000e+00 # [K]

* Mole fraction dependent model.
* If just above parameters are specified, then its values will be
* used for any mole fraction instead of an interpolation below.
* The following interpolation polynomial can be used on interval [Xmin(I),Xmax(I)]:
  \[ F(X) = F(I-1) + A(I) (X-Xmin(I)) + B(I) (X-Xmin(I))^2 + C(I) (X-Xmin(I))^3, \]
* where Xmax(I), F(I), B(I), C(I) are defined below for each interval.
* A(I) is calculated for a boundary condition F(Xmax(I)) = F(I).
* Above parameters define values at the following mole fraction:
  Xmax(0) = 0.0000e+00 # [1]

* Definition of mole fraction intervals, parameters, and coefficients:
  Xmax(1) = 1.00 # [1]
  Eg0(1) = 6.20000 # [eV]
  B(Eg0(1)) = 0.0000e+00 # [eV]
  C(Eg0(1)) = 0.0000e+00 # [eV]
  alpha(1) = 1.7990e-03 # [eV K^-1]
  B(alpha(1)) = 0.0000e+00 # [eV K^-1]
  C(alpha(1)) = 0.0000e+00 # [eV K^-1]
  beta(1) = 1.4620e+03 # [K]
  B(beta(1)) = 0.0000e+00 # [K]
  C(beta(1)) = 0.0000e+00 # [K]
  Chi0(1) = 2.027 # [eV]

* Chi0(1) = 0.6 # [eV]
  B(Chi0(1)) = 0.0000e+00 # [eV]
  C(Chi0(1)) = 0.0000e+00 # [eV]

}

* Values from Ioffe
eDOSMass
{
* For effective mass specification Formula1 (me approximation):
* or Formula2 (Nc300) can be used :
  Formula = 2 # [1]
* Formula2:
  me/m0 = (Nc300/2.540e19)^2/3
\[ N_c(T) = N_{c300} \times (T/300)^{3/2} \]
\[ N_{c300} = 2.2300e+18 \quad \text{[cm}^{-3}\text{]} \]

* Mole fraction dependent model.
* If just above parameters are specified, then its values will be
  used for any mole fraction instead of an interpolation below.
* The linear interpolation is used on interval \([0,1]\).

\[ N_{c300}(1) = 6.2400e+18 \quad \text{[cm}^{-3}\text{]} \]

* Values from Ioffe

\text{hDOSMass}

\{ 
  * For effective mass specification Formula1 (mh approximation):
  * or Formula2 (Nv300) can be used:
    \[ \text{Formula} = 2 \quad \text{# [1]} \]
  * Formula2:
    \[ mh/m_0 = (Nv300/2.540e19)^{2/3} \]
    \[ N_v(T) = N_{v300} \times (T/300)^{3/2} \]
    \[ N_{v300} = 4.6200e+19 \quad \text{[cm}^{-3}\text{]} \]
  * Mole fraction dependent model.
  * If just above parameters are specified, then its values will be
    used for any mole fraction instead of an interpolation below.
  * The linear interpolation is used on interval \([0,1]\).
    \[ N_{v300}(1) = 4.8800e+20 \quad \text{[cm}^{-3}\text{]} \]
\}

* Values from Ioffe

\text{SchroedingerParameters}

\{ 
  * For the hole masses for Schroedinger equation you can
  use different formulas.
  * formula=1 (for materials with Si-like hole band structure)
    \[ m(k)/m_0 = 1/(A+\sqrt{B+C^*((xy)^2+(yz)^2+(zx)^2)}) \]
  * where \( k = (x,y,z) \) is unit normal vector in reziprocal
    space. '+' for light hole band, '-' for heavy hole band
  * formula=2: Heavy hole mass mh and light hole mass ml are
    specified explicitly.
  * formula=3: \( A \) is the relative effective mass. This
    formula must only be used for metal and will be used in
    tunnelling current computation only.
  * formula<0 means no default model and no default parameters
    are available, so you have to provide values for
    'formula' and the respective parameters in order to use
    this parameter set.
    \[ \text{formula} = 2 \quad \text{# [1]} \]
  * Formula 2 parameters:
    \[ ml = 0.259 \quad \text{# [1]} \]
    \[ mh = 1.400 \quad \text{# [1]} \]
  * Mole fraction dependent model.
  * If just above parameters are specified, then its values will be
    used for any mole fraction instead of an interpolation below.
  * The linear interpolation is used on interval \([0,1]\).
    \[ ml(1) = 0.24 \quad \text{# [1]} \]
    \[ mh(1) = 3.53 \quad \text{# [1]} \]
\}
* Values from Ioffe

**ConstantMobility:**

\{
  * \( \mu_{\text{const}} = \mu_{\text{max}} \left( \frac{T}{T_0} \right)^{-\text{Exponent}} \)
  * \( \mu_{\text{max}} = 5.50 \times 10^2 \), \( 1.00 \times 10^1 \) \([\text{cm}^2/(\text{Vs})]\)
  * \( \text{Exponent} = 0.00 \), \( 0.00 \) \([\text{1}]\)
  * \( \mu_{\text{max}} = 5.5 \times 10^2 \), \( 1.00 \times 10^{-5} \) \([\text{cm}^2/(\text{Vs})]\)
  * \( \text{Exponent} = 1.50 \), \( 0.00 \) \([\text{1}]\)
\}

* Mole fraction dependent model.
  * If just above parameters are specified, then its values will be
    * used for any mole fraction instead of an interpolation below.
  * The linear interpolation is used on interval \([0,1]\).
  * \( \mu_{\text{max}}(1) = 3.00 \times 10^2 \), \( 1.00 \times 10^1 \) \([\text{cm}^2/(\text{Vs})]\)
  * \( \text{Exponent}(1) = 0.00 \), \( 0.00 \) \([\text{1}]\)
  * \( \mu_{\text{max}}(1) = 3.0 \times 10^2 \), \( 1.00 \times 10^{-5} \) \([\text{cm}^2/(\text{Vs})]\)
  * \( \text{Exponent}(1) = 1.50 \), \( 0.00 \) \([\text{1}]\)

* Eventually populate this matrix

**DopingDependence\{\ldots\}**

* By default, for mole fraction dependency of parameters
  * of the model, the following linear interpolation is applied
  * between two materials: \( P = x \times P(\text{AlAs}) + (1-x) \times P(\text{GaAs}) \)
    * where \( P(m) \) is a parameter of material \( m \).
  * If the parameters are specified, then its values
    * will be used instead of the interpolation.

**HighFieldDependence:**

* Caughey-Thomas model:
  * \( \mu_{\text{highfield}} = \mu_{\text{lowfield}} / (1 + (\mu_{\text{lowfield}} E / v_{\text{sat}})^{\beta})^{1/\beta} \)
  * \( \beta = \beta_0 \left( \frac{T}{T_0} \right)^{\beta_{\text{exp}}} \)
    * \( \beta_0 = 1.0 \), \( 1.7 \) \([\text{1}]\)
    * \( \beta_{\text{exp}} = 0.0000 \times 10^0 \), \( 0.0000 \times 10^0 \) \([\text{1}]\)
* Smoothing parameter for HydroHighField Caughey-Thomas model:
  * if \( T_1 < T_c < (1 + K_{dT}) T_1 \), then smoothing between low field mobility
  * and HydroHighField mobility is used.
    * \( K_{dT} = 0.2 \), \( 0.2 \) \([\text{1}]\)
* Transferred-Electron Effect:
  * \( \mu_{\text{highfield}} = (\mu_{\text{lowfield}} + (v_{\text{sat}} E / E_{0\_TrEf})^4)/(1 + (E / E_{0\_TrEf})^4) \)
    * \( E_{0\_TrEf} = 1.2500 \times 10^5 \), \( 1.2500 \times 10^5 \) \([\text{1}]\)
    * \( K_{\text{smooth\_TrEf}} = 1 \), \( 1 \) \([\text{1}]\)
* For \( v_{\text{sat}} \) either Formula1 or Formula2 can be used.
  * \( v_{\text{sat\_Formula}} = 2 \), \( 2 \) \([\text{1}]\)
* Formula2 for saturation velocity:
  * \( v_{\text{sat}} = A_{\text{vsat}} - B_{\text{vsat}} (T/T_0) \)
    * \( A_{\text{vsat}} = 8.0000 \times 10^6 \), \( 1.00e+06 \) \([\text{1}]\)
    * \( B_{\text{vsat}} = 0.0000 \times 10^0 \), \( 0.0000 \times 10^0 \) \([\text{1}]\)
    * \( v_{\text{sat\_min}} = 1.0000 \times 10^6 \), \( 5.0000 \times 10^5 \) \([\text{1}]\)

* Mole fraction dependent model.
  * If just above parameters are specified, then its values will be
    * used for any mole fraction instead of an interpolation below.
  * The linear interpolation is used on interval \([0,1]\).
    * \( \beta_0(1) = 1.0 \), \( 1.7 \) \([\text{1}]\)
\[
\begin{align*}
\text{betaexp}(1) & = 0.0000e+00, \quad 0.0000e+00 \quad \#[1] \\
A_{vSat}(1) & = 3.00e+06, \quad 1.00e+06 \quad \#[\text{cm/s}] \\
B_{vSat}(1) & = 0.0000e+00, \quad 0.0000e+00 \quad \#[\text{cm/s}] \\
vSat_{min}(1) & = 1.0000e+05, \quad 1.0000e+06 \quad \#[\text{cm/s}] \\
\text{* Values from GaN} \\
\text{Scharfetter * relation and trap level for SRH recombination:} \\
\{ \text{ * tau} = \text{taumin} + ( \text{taumax} - \text{taumin}) / (1 + (N/Nref)^\gamma) \} \\
\text{* tau(T) = tau * ((T/300)^\alpha) (TempDep)} \\
\text{taumin} & = 0.0000e+00, \quad 0.0000e+00 \quad \# [\text{s}] \\
\text{taumax} & = 5.0000e-10, \quad 5.0000e-10 \quad \# [\text{s}] \\
\text{Nref} & = 1.0000e+16, \quad 1.0000e+16 \quad \# [\text{cm}^{-3}] \\
\gamma & = 1, \quad 1 \quad \# [1] \\
\text{talp} & = 0.0000e+00, \quad 0.0000e+00 \quad \# [1] \\
Tcoeff & = 0.0000e+00, \quad 0.0000e+00 \quad \# [1] \\
\text{Etrap} & = 0.0000e+00 \quad \# [\text{eV}] \\
\text{\text{* Values from AlGaAs (needs update)} \\
\text{Auger * coefficients:} \\
\{ \text{ * R}_\text{Auger} = (C_n n + C_p p) (n p - n_i^2) \} \\
\text{with C_n,p = (A + B (T/T_0) + C (T/T_0)^2) (1 + H \exp(-{n,p}/N_0))} \\
A & = 1.0000e-30, \quad 1.0000e-30 \quad \# [\text{cm}^6/\text{s}] \\
B & = 0.0000e+00, \quad 0.0000e+00 \quad \# [\text{cm}^6/\text{s}] \\
C & = 0.0000e+00, \quad 0.0000e+00 \quad \# [\text{cm}^6/\text{s}] \\
H & = 0.0000e+00, \quad 0.0000e+00 \quad \# [1] \\
N_0 & = 1.0000e+18, \quad 1.0000e+18 \quad \# [\text{cm}^{-3}] \\
\text{\text{* Values from AlGaAs (needs update)} \\
\text{vanOverstraetendeMan * Impact Ionization:} \\
\{ \text{ * G}_\text{impact} = \alpha_n n v_{\text{drift}_n} + \alpha_p p v_{\text{drift}_p} \} \\
\text{with } \alpha = \gamma a \exp(-b \gamma/E) \text{ for } E<E_0 \text{ (low) and } E>E_0 \text{ (high)} \\
\text{with } \gamma = \tanh(h \Omega/(2kT_0)) / \tanh(h \Omega/(2kT)) \\
a(\text{low}) & = 4.0000e+06, \quad 1.3400e+06 \quad \# [1/\text{cm}] \\
a(\text{high}) & = 4.0000e+06, \quad 1.3400e+06 \quad \# [1/\text{cm}] \\
b(\text{low}) & = 2.3000e+06, \quad 2.0300e+06 \quad \# [\text{V/cm}] \\
b(\text{high}) & = 2.3000e+06, \quad 2.0300e+06 \quad \# [\text{V/cm}] \\
E_0 & = 4.0000e+05, \quad 4.0000e+05 \quad \# [\text{V/cm}] \\
h \Omega & = 0.035, \quad 0.035 \quad \# [\text{eV}] \\
\text{\text{* Mole fraction dependent model.} \\
\text{The linear interpolation is used on interval [0,1].} \\
a(\text{low})(1) & = 4.0000e+06, \quad 1.3400e+06 \quad \# [1/\text{cm}] \\
a(\text{high})(1) & = 4.0000e+06, \quad 1.3400e+06 \quad \# [1/\text{cm}] \\
b(\text{low})(1) & = 2.3000e+06, \quad 2.0300e+06 \quad \# [\text{V/cm}] \\
b(\text{high})(1) & = 2.3000e+06, \quad 2.0300e+06 \quad \# [\text{V/cm}] \\
E_0(1) & = 4.0000e+05, \quad 4.0000e+05 \quad \# [\text{V/cm}] \\
h \Omega(1) & = 0.035, \quad 0.035 \quad \# [\text{V/cm}] \\
\text{Value taken from http://www.ioffe.rssi.ru/SVA/NSM/Semicond/GaN} \\
\text{RadiativeRecombination * coefficients:} \\
\{ \text{ * R}_\text{Radiative} = C (n p - n_i^2) \} \\
C & = 0.4000e-10 \quad \# [\text{cm}^3/\text{s}] \\
\}
// implementation of the Poole-Frenkel mobility model using the PMI interface
class PF_HighFieldMobility : public PMI_HighFieldMobility {

private:

// container for temporary data used in parallel mobility calculations
class TempData {
public:
    double Fabs,q0,eps0,epsR,k0,x1,x2,phiB,our_sqrt,arg,A,B,m,our_sqrt2,arg2,ec,dmudF;
};

void Compute_internal (TempData& data,
                       const double t, const double mulow, const double F);

protected:

const double T0;
double phi0, beta_PF, gamma_PF;

class:

PF_HighFieldMobility (const PMI_Environment& env,
                      const PMI_HighFieldDrivingForce force,
                      const PMI_AnisotropyType anisotype);

~PF_HighFieldMobility ();

void Compute_mu
    (const double pot,       // electrostatic potential
     const double n,        // electron density
     const double p,        // hole density
     const double t,        // lattice temperature
     const double ct,       // carrier temperature
     const double mulow,    // low field mobility
     const double F,        // driving force
double& mu);            // mobility

void Compute_dmudpot
    (const double pot,       // electrostatic potential
     const double n,        // electron density
     const double p,        // hole density
     const double t,        // lattice temperature
     const double ct,       // carrier temperature
     const double mulow,    // low field mobility
     const double F,        // driving force
double& dmudpot);       // derivative of mobility
                         // with respect to electrostatic potential

void Compute_dmudn
(const double pot, // electrostatic potential
c   const double n, // electron density
c   const double p, // hole density
c   const double t, // lattice temperature
c   const double ct, // carrier temperature
c   const double mulow, // low field mobility
c   const double F, // driving force
double& dmudn); // derivative of mobility
   // with respect to electron density

void Compute_dmudp
   (const double pot, // electrostatic potential
c   const double n, // electron density
c   const double p, // hole density
c   const double t, // lattice temperature
c   const double ct, // carrier temperature
c   const double mulow, // low field mobility
c   const double F, // driving force
double& dmudp); // derivative of mobility
   // with respect to hole density

void Compute_dmudt
   (const double pot, // electrostatic potential
c   const double n, // electron density
c   const double p, // hole density
c   const double t, // lattice temperature
c   const double ct, // carrier temperature
c   const double mulow, // low field mobility
c   const double F, // driving force
double& dmudt); // derivative of mobility
   // with respect to lattice temperature

void Compute_dmudct
   (const double pot, // electrostatic potential
c   const double n, // electron density
c   const double p, // hole density
c   const double t, // lattice temperature
c   const double ct, // carrier temperature
c   const double mulow, // low field mobility
c   const double F, // driving force
double& dmudct); // derivative of mobility
   // with respect to carrier temperature

void Compute_dmudmulow
   (const double pot, // electrostatic potential
c   const double n, // electron density
c   const double p, // hole density
c   const double t, // lattice temperature
c   const double ct, // carrier temperature
c   const double mulow, // low field mobility
c   const double F, // driving force
double& dmudmulow); // derivative of mobility
   // with respect to low field mobility
```c
void Compute_dmudF
(const double pot, // electrostatic potential
 const double n, // electron density
 const double p, // hole density
 const double t, // lattice temperature
 const double ct, // carrier temperature
 const double mulow, // low field mobility
 const double F, // driving force
 double& dmudF); // derivative of mobility
    // with respect to driving force
};

void PF_HighFieldMobility::
Compute_internal (TempData& data,
    const double t, const double mulow, const double F)
{
    data.Fabs = fabs (F);
    data.phiB=0.7;
    data.q0=1.6e-19;
    data.epsi0=8.85e-14;
    data.epsiR=10;
    data.k0=1.38e-23;
    data.x1=1;
    data.x2=1;
    data.m = 1.7;
    data.ec=3e6;
    data.A = -data.q0/data.k0/T0*data.phiB;
    data.B = data.m*data.q0/data.k0/T0*pow(data.q0/3.1415/data.epsi0/data.epsiR,0.5);
    data.our_sqrt = pow(pow(F,2)+data.x1,0.25)-data.x2;
    data.our_sqrt2 =pow(pow(data.ec,2)+data.x1,0.25)-data.x2;
    data.arg= data.A+data.B*data.our_sqrt;
    data.arg2=data.A+data.B*data.our_sqrt2;
    data.dmudF=0.5*data.B*data.ec*exp(data.arg2)/pow(data.ec*data.ec+data.x1*data.x1,0.75);
}

PF_HighFieldMobility::
PF_HighFieldMobility (const PMI_Environment& env,
    const PMI_HighFieldDrivingForce force,
    const PMI_AnisotropyType anisotype) :
    PMI_HighFieldMobility (env, force, anisotype),
    T0 (300.0)
{}

PF_HighFieldMobility::
~PF_HighFieldMobility ()
{}

void PF_HighFieldMobility::
Compute_mu (const double pot, const double n,
    const double p, const double t, const double ct,
    const double mulow, const double F, double& mu)
{
    TempData data;
    Compute_internal (data, t, mulow, F);
    if (data.Fabs<data.ec){
        // code for low field mobility
    } else {
        // code for high field mobility
    }
}
```
mu = mulow+exp(data.arg);
}
else{mu = mulow+data.Fabs*data.dmudF+exp(data.arg2)-data.dmudF*data.ec;}
}
void PF_HighFieldMobility::
Compute_dmudpot (const double pot, const double n,
    const double p, const double t, const double ct,
    const double mulow, const double F, double& dmudpot)
{ dmudpot = 0.0;
}
void PF_HighFieldMobility::
Compute_dmudn (const double pot, const double n,
    const double p, const double t, const double ct,
    const double mulow, const double F, double& dmudn)
{ dmudn = 0.0;
}
void PF_HighFieldMobility::
Compute_dmudp (const double pot, const double n,
    const double p, const double t, const double ct,
    const double mulow, const double F, double& dmudp)
{ dmudp = 0.0;
}
void PF_HighFieldMobility::
Compute_dmudt (const double pot, const double n,
    const double p, const double t, const double ct,
    const double mulow, const double F, double& dmudt)
{ TempData data;
    dmudt=0;
}
void PF_HighFieldMobility::
Compute_dmudct (const double pot, const double n,
    const double p, const double t, const double ct,
    const double mulow, const double F, double& dmudct)
{ dmudct = 0.0;
}
void PF_HighFieldMobility::
Compute_dmudmulow (const double pot, const double n,
    const double p, const double t, const double ct,
    const double mulow, const double F, double& dmudmulow)
{ TempData data;
    Compute_internal (data, t, mulow, F);
    dmudmulow = 1;
}
void PF_HighFieldMobility::
Compute_dmudF (const double pot, const double n,
    const double p, const double t, const double ct,
    const double mulow, const double F, double& dmudF)
{ TempData data;
    Compute_internal (data, t, mulow, F);
    if (data.Fabs<data.ec)
    {
        dmudF=0.5*data.B*F*exp(data.arg)/pow(F+F+data.x1*data.x1,0.75);
    }
}
else {dmudF = data.dmudF;}
}
class PF_e_HighFieldMobility : public PF_HighFieldMobility {

public:
    PF_e_HighFieldMobility (const PMI_Environment& env,
        const PMI_HighFieldDrivingForce force,
        const PMI_AnisotropyType anisotype);

~PF_e_HighFieldMobility () {};
};

PF_e_HighFieldMobility::

PF_e_HighFieldMobility (const PMI_Environment& env,
    const PMI_HighFieldDrivingForce force,
    const PMI_AnisotropyType anisotype) :
    PF_HighFieldMobility (env, force, anisotype)
{
    // default values
    beta_PF = InitParameter ("beta_PF_e", 1e-5);
    gamma_PF = InitParameter ("gamma_PF_e", 1e-10);
    phi0 = InitParameter ("phi0_e", 0.7);
}

class PF_h_HighFieldMobility : public PF_HighFieldMobility {

public:
    PF_h_HighFieldMobility (const PMI_Environment& env,
        const PMI_HighFieldDrivingForce force,
        const PMI_AnisotropyType anisotype);

~PF_h_HighFieldMobility () {};
};

PF_h_HighFieldMobility::

PF_h_HighFieldMobility (const PMI_Environment& env,
    const PMI_HighFieldDrivingForce force,
    const PMI_AnisotropyType anisotype) :
    PF_HighFieldMobility (env, force, anisotype)
{
    // default values
    beta_PF = InitParameter ("beta_PF_h", 1e-5);
    gamma_PF = InitParameter ("gamma_PF_h", 1e-10);
    phi0 = InitParameter ("phi0_h", 0.7);
}

extern "C"

PMI_HighFieldMobility* new_PMI_HighField_e_Mobility
    (const PMI_Environment& env, const PMI_HighFieldDrivingForce force,
    const PMI_AnisotropyType anisotype)
{
    return new PF_e_HighFieldMobility (env, force, anisotype);
}

extern "C"

PMI_HighFieldMobility* new_PMI_HighField_h_Mobility
    (const PMI_Environment& env, const PMI_HighFieldDrivingForce force,
    const PMI_AnisotropyType anisotype)
{
    return new PF_h_HighFieldMobility (env, force, anisotype);
}