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Author
Sands, T.

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T. Sands, K.M. Yu, S.K. Cheung, and V.G. Keramidas

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PdₓGaAs/GaAs: CORRELATION BETWEEN INTERFACE STRUCTURE, MORPHOLOGY AND ELECTRICAL PROPERTIES

T. Sands,†‡ K. M. Yu, ‡ S. K. Cheung † and V. G. Keramidas †

† Bell Communications Research, Inc.  
600 Mountain Ave., Murray Hill, NJ 07974  
and  
‡ Center for Advanced Materials  
Lawrence Berkeley Laboratory  
University of California  
Berkeley, CA 94720

Abstract

The structure, morphology, composition and electrical properties of ternary phase (PdₓGaAs) films on GaAs have been studied by transmission electron microscopy, energy dispersive x-ray spectrometry, Rutherford backscattering spectrometry and current-voltage measurements. Annealing 15 nm of Pd on (100) GaAs at 250°C yields a planar monocrystalline film of the first ternary phase (Pd₃.₉Ga₁.₁As₀.₉) which is a rectifying contact to n-GaAs with a barrier height of ~0.76 eV. A subsequent annealing treatment at 350°C converts the film to a second ternary phase (Pd₃₃Ga₁₂As₀₈) that exhibits a rough interface with GaAs, severely degraded electrical properties and a lower barrier height. The reduction in the measured barrier height is attributed to thermionic-field emission at sharp corners and protrusions in the PdₓGaAs/GaAs interface. The implications of these results for the utilization of Pd in multielemental contacts to GaAs are also discussed.
Introduction

Palladium is an important component in several recently developed multielemental ohmic contacts to n-GaAs. Marshall et al. (1) have used a thin layer of Pd to serve as an atomic transport medium for the epitaxial growth of Ge on n-GaAs. The resulting contacts are ohmic even if the epitaxial Ge layer is not intentionally n+-doped. Palladium has also been used instead of Ni in the conventional Au-Ge/Ni contact yielding comparable electrical properties and a superior morphology (2). The utility of Pd in both of these examples is related, in part, to the observation by Sands et al. (3,4) that a thin layer of Pd mechanically disperses the native oxide on GaAs at low temperatures (≤ 80°C), thereby removing the oxide layer as an obstacle to the transport of atoms across the interface. Further investigations of the simpler Pd/GaAs system are necessary to elucidate the role of Pd in determining the morphology, stability and electrical properties of multielemental ohmic contacts containing Pd.

Previous studies of the Pd/GaAs reaction showed that the low temperature (≤ 500°C) reaction is dominated by the formation of two ternary "pseudo-silicide" (MxGaAs) phases (3,5-7). The first phase, designated as "phase I," begins to form during deposition and is the primary product phase at annealing temperatures up to 250°C (3,5-7). Phase I is hexagonal (a₀ = 0.67 nm, c₀ = 0.34 nm (3,5-7)) and exhibits the orientation relationship 0001] || [011]GaAs and (2110) || (100)GaAs (8). A second PdxGaAs phase, "phase II," (hexagonal, a₀ = 0.9 nm, c₀ = 0.37 nm (3,5,7)) forms above 250°C and is the dominant reaction product in samples annealed at 350°C in forming gas (7,8).

The compositions of phases I and II are strongly dependent on Pd film thickness, annealing temperature and annealing ambient (3,6-8). The maximum Pd content for both phases corresponds to a nominal composition of Pd₄GaAs. Kuan et al. (7) report that for thin (15 nm) Pd films, phase I films with composition Pd₄Ga₁₉As₀₈ formed at 250°C. Sands et al. (3,8) found that phase II adopts the nominal composition Pd₄GaAs after annealing thicker Pd films (45 and 60 nm) at temperatures between 275 and 410°C. If annealing continues after the Pd is completely consumed, both phases become deficient in Pd resulting in compositions in the range Pd₂₋₃GaAs (3,7,8). Furthermore, Sands et al. (3,8) and Kuan et al. (7) have shown that annealing at high temperatures (2410°C) or in an ultrahigh-vacuum environment leads to extensive sublimation of As from the PdₓGaAs ternary phases. Phase II, for example, can accommodate As:Ga ratios as low as 0.5 at 480°C (3).

The objective of this study was to seek answers to two important questions not addressed by the studies described above: 1) What are the relative stabilities of the two ternary PdₓGaAs phases? and 2) how do the interfacial phases and their morphologies affect the electrical properties of PdₓGaAs/GaAs interfaces?

Experimental Methods

Undoped and Te-doped (n = 10¹⁷/cm³) LEC (100) GaAs wafers were used as substrates for physical and electrical characterization, respectively. Prior to Pd deposition, Au-Ge layers were deposited onto the n-type wafers and then annealed to produce backside ohmic contacts for I-V measurements. The GaAs wafers were degreased and etched in 1:1 DI H₂O:HCl. After rinsing in DI H₂O the wafers were blown dry with N₂ and inserted into an electron beam deposition chamber. Palladium was deposited to the desired thickness (15-100 nm) at 1 x 10⁻⁶ torr. Dots of 1 mm diameter were deposited onto the n-type wafers for I-V measurements. Each wafer was
cleaved into four pieces. Two of the quarters from each wafer were annealed in flowing forming gas for 10 min. at 250°C. One of these quarters and a third quarter were then annealed for 10 min. at 350°C.

In order to investigate the effect of substrate crystallinity on the stability of phase I, an additional wafer was implanted with 75 keV As+ to a dose of $5 \times 10^{14}$/cm$^2$ to amorphize the surface layer. After deposition of ~15 nm of Pd the amorphized sample was annealed for 20 min. at 200°C.

Specimens for transmission electron microscopy (TEM) were prepared in both plan-view and cross-sectional ([011] surface normal) geometries. Imaging and diffraction were performed in a Siemens 102 TEM at 100 keV and a JEOL JEM 200 CX at 200 keV.

Energy dispersive x-ray spectra (EDS) were acquired from plan-view specimens at 200 keV in a JEOL JEM 200 CX TEM/STEM using a high-angle detector. The Pd:Ga ratios were estimated using theoretical K-factors in the thin foil approximation (9). A GaAs standard allowed accurate measurements of the Ga:As ratios. These results were compared with Rutherford backscattering (RBS) analyses of the same samples to provide an independent and more accurate measure of x in Pd$_x$GaAs. The RBS spectra were acquired with a 2.0 MeV He$^+$ beam incident at an angle of 63° to the specimen normal and with the detector located at a backscattering angle of 170°.

Current-voltage measurements were performed using an HP 4140B current meter with a built-in DC voltage source. Specimens were shielded from light during the measurements. A least-squares fit to the experimental data allowed estimation of the barrier height and ideality factor using the non-ideal thermionic emission equation

$$J = A* T^2 \exp(-q\phi_b/kT) \left[ \exp(qV_a/nkT) - 1 \right]$$

where $A*$ is the effective Richardson constant (taken to be 8.6A/cm$^2$/K$^2$ in this work), T is the absolute temperature in degrees Kelvin, k is the Boltzmann constant, $V_a$ is the applied voltage, $q\phi_b$ is the Schottky barrier height and n is the ideality factor (n ~1 if thermionic emission dominates).

Results and Discussion

Film Morphology

Gallium arsenide wafers with two deposited thicknesses of Pd, 15 and 22 nm, were annealed as described above and then examined by TEM, electron diffraction, EDS and RBS. The results are summarized in Table I.

As Figure 1 reveals, approximately 9 nm of phase I forms during TEM specimen preparation (maximum temperature ~80°C). This layer of phase I is nominally planar and monocristalline. Small angle rotations of phase I grains, however, are evident in the diffraction pattern. The region of light contrast between the phase I layer and the unreacted Pd consists of dispersed patches of the original native oxide and voids resulting from the fact that Pd is the dominant moving species. These voids are visible at the Pd/phase I interface at temperatures up to ~220°C (3). At 250°C, the voids have disappeared and the native oxide has been completely dispersed during the formation of ~17 nm of phase I (Fig. 2(b)). The composition of this phase I layer was determined to be ~Pd$_{3.9}$Ga$_{1.1}$As$_{0.9}$ by combined EDS and RBS analysis (Figs. 3 and 4). A subsequent annealing treatment at 350°C converts the film to polycrystalline phase II with only a trace of
Table I. Structure and Composition of Pd$_x$GaAs Films

<table>
<thead>
<tr>
<th>Thickness Pd deposited [nm]</th>
<th>Annealing treatment temp. [°C], time [min.]</th>
<th>Phases present (electron diffraction)</th>
<th>x in Pd$_x$GaAs (RBS)</th>
<th>Ga:As (EDS)</th>
<th>Film composition (RBS + EDS)</th>
</tr>
</thead>
<tbody>
<tr>
<td>15</td>
<td>as-deposited</td>
<td>I(epi.), Pd</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>22</td>
<td>as-deposited</td>
<td>I(epi.), Pd</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>15</td>
<td>250,20</td>
<td>I(epi.) Pd (trace)</td>
<td>3.9$^a$</td>
<td>1.07:0.93</td>
<td>Pd$<em>{3.9}$Ga$</em>{1.1}$As$_{0.9}$</td>
</tr>
<tr>
<td>22</td>
<td>250,20</td>
<td>I(epi.), Pd</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>15</td>
<td>250,20+350,20</td>
<td>II, I (trace) possibly Pd-Ga (trace)</td>
<td>3.3</td>
<td></td>
<td></td>
</tr>
<tr>
<td>22</td>
<td>250,20+350,20</td>
<td>II, I (trace) possibly Pd-Ga (trace)</td>
<td>3.6</td>
<td></td>
<td></td>
</tr>
<tr>
<td>15</td>
<td>350,20</td>
<td>II, I (trace) possibly Pd-Ga (trace)</td>
<td>3.3</td>
<td></td>
<td></td>
</tr>
<tr>
<td>22</td>
<td>350,20</td>
<td>II, I (trace) possibly Pd-Ga (trace)</td>
<td>3.5$^b$</td>
<td>1.23:0.77</td>
<td>Pd$<em>{3.5}$Ga$</em>{1.2}$As$_{0.8}$</td>
</tr>
<tr>
<td>15 on amorphous GaAs</td>
<td>200,20</td>
<td>I (poly)</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

$^a$ Standardless EDS analysis of this film gave $x = 3.7$

$^b$ Standardless EDS analysis of this film gave $x = 3.0$
Figure 1 - Cross-sectional TEM image of 15 nm Pd on GaAs prior to annealing. Sample was subjected to a maximum temperature of ~80°C during TEM specimen preparation. Phase I layer in [0001] orientation is ~9 nm thick. Inset diffraction pattern reveals small-angle rotations between phase I grains. Unreacted Pd and phase I are separated by voids and native oxide patches. GaAs is in [011] zone-axis orientation.

Figure 2 - Low magnification ((a) and (c)) and high magnification ((b) and (d)) images of 22 nm Pd on GaAs after annealing at 250°C for 20 min. ((a) and (b)) and after an additional annealing treatment at 350°C for 20 min. ((c) and (d)). Images in (a) and (b) reveal relatively planar phase I layer after annealing at 250°C. Additional annealing at 350°C results in phase II film with irregular interface and surface trenches ((c)).
phase I remaining. The cross-sectional images in Fig. 2 show that this interface (phase II/GaAs) contains sharp cusps. As explained in Reference 8, these deep penetrations result from nucleation of phase II at large-angle grain boundaries in the phase I film. These large-angle grain boundaries in the phase I layer are present in low density compared to the density of small-angle grain boundaries. The availability of excess unreacted Pd is very important since at 350°C, any unreacted Pd has very high mobility (3) and can laterally diffuse several microns to the phase II nucleation sites. Consequently, the resulting interface morphology is laterally nonuniform. As discussed below, this irregular interface morphology can play an important role in determining the electrical properties of phase II/GaAs interfaces.

The micrograph in Fig. 2(c) reveals that small "trenches" have also formed in the surface of the phase II film. These trenches emanate from the phase II/phase I interface (Fig. 5) and are always oriented perpendicular to that interface. This characteristic feature provides a record of the motion of the transformation interfaces from images of phase II such as shown in Fig. 6. The exact origin of the trenches is not completely understood. The observation of faint and diffuse diffraction rings at 0.242, 0.223 and 0.198 nm suggests that the trenches contain small amounts of Pd$_{3.3}$Ga$_{1.8}$As$_{0.2}$ (3) or PdGa. Thus, a likely explanation for the trench morphology is that the high diffusivity of arsenic in the phase I/phase II interface allows the out diffusion and sublimation of As, leaving behind arsenic-deficient phase II (~Pd$_{3.3-3.6}$Ga$_{1.2}$As$_{0.8}$) between trenches containing trace amounts of Pd-Ga compounds. Consequently, the spacing between trenches (~70 nm) may be related to the effective diffusion distance of As in the phase I/phase II interface at 350°C.

Stabilities of the Ternary Phases

In the current work we have shown that annealing 15 nm of Pd on GaAs at 250°C results in a uniform film of phase I with little or no unreacted Pd. A subsequent anneal at 350°C yields a film that is almost entirely phase II at a somewhat Pd-deficient composition. Thus, phase I can be converted to phase II above 250°C without the presence of unreacted Pd (recall that a
Figure 4 - RBS spectrum (2.0 MeV He⁺) from 15 nm Pd on GaAs after annealing. Spectrum shown as dotted line (••••••) is from phase I formed during annealing at 250°C for 20 min. This spectrum is deconvoluted to reveal signals from Ga and As in phase I. During additional anneal at 350°C for 20 min, phase II is formed (spectra shown as solid line, ——). Film compositions estimated from these spectra are shown in Table I. He⁺ beam was incident at 63° from sample normal to increase effective film thickness.

Previous study (8) of thicker Pd films (up to 60 nm) revealed that phase II formed with a Pd-rich composition of ~Pd₄GaAs in the presence of excess unreacted Pd). Consequently, phase II is the stable phase above 250°C. Since the compositional existence regions of phases I and II apparently coincide (Pd₂₋₆GaAs) it is possible that phase II is also the stable phase below 250°C, except in the presence of the interface with crystalline GaAs. The observation that phase I is epitaxial (or perhaps more properly, topotaxial, since the orientation relationship between phase I and GaAs results from the indiffusion and reaction of Pd with GaAs rather than from
Figure 5 - Plan-view TEM image of Pd$_x$GaAs film formed during annealing 22 nm Pd on GaAs at 350°C. Inset diffraction patterns reveal monocrystalline phase I patch surrounded by polycrystalline phase II. Phase II accounts for ~95% of film area. Note trenches in phase II at right.

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Figure 6 - Plan-view TEM image of phase II film formed during two-stage annealing at 250 and 350°C, respectively. Trenches form at 90 degrees to the moving phase I/phase II interfaces.

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the deposition of PdxGaAs onto GaAs whereas phase II is polycrystalline supports this stability argument.

To test this hypothesis, 15 nm of Pd was deposited onto amorphous GaAs (As⁺-implanted) and then annealed at 200°C for 20 min. The plan-view diffraction pattern (not shown) revealed a polycrystalline film consisting exclusively of phase I. Thus, phase I is the stable phase below 250°C, even in the absence of a low energy interface with crystalline GaAs.

Electrical Properties

Electrical (I-V) measurements, summarized in Table II, show similar trends for thin (15 nm) as well as thick (100 nm) Pd films. The as-deposited samples and the samples annealed at 250°C yield a barrier height of ~0.76 eV. It is the ideality factor that is reduced from ~1.45 to ~1.2 by annealing at 250°C. This improvement coincides with the development of the phase I layer from small grains interspersed with native oxide patches and voids (3,8) to a uniform and nominally monocrystalline phase I film. This result is significant since it is a direct correlation between the metallurgical behavior and the electrical properties of a single metal/compound semiconductor system.

After annealing under conditions which yield phase II films, the I-V characteristics become difficult to reproduce, in some cases exhibiting nonrectifying or ohmic behavior. Those I-V characteristics which can be satisfactorily described with a non-ideal thermionic emission model indicate that annealing at 350°C results in a significant reduction (7-20%) in the measured barrier height. As was shown above, the transformation to phase II is accompanied by a considerable roughening of the interface with GaAs. The phase II/GaAs interface exhibits sharp corners and protrusions. The enhanced electric field in the vicinity of sharp corners and protrusions decreases the width of the potential barrier. The barrier may become sufficiently thin so as to greatly increase the probability of quantum mechanical tunneling through the top of the barrier (thermionic-field emission). Thus, the effective barrier height in the vicinity of an interfacial cusp or protrusion is reduced. Since current flow through the interface is concentrated in the regions with the lowest effective barrier heights, I-V measurements are particularly sensitive to interfacial irregularities (10). This sensitivity is reflected in the irreproducible electrical properties of phase II/GaAs interfaces (Table II). A similar model was invoked by Leung et al. (11) to explain, in part, their data on Au-Ga contacts to GaAs.

Conclusions

The results of this investigation lead to four principal conclusions:
1) Regarding the stability of the PdxGaAs phases, the first ternary phase (phase I) is stable below 250°C; the second ternary phase (phase II) is stable above 250°C. 2) The compositions of the ternary phases and the reacted film morphologies depend on the initial thickness of the deposited Pd layer. 3) Phase I forms a rectifying contact to n-GaAs with a barrier height of ~0.76 eV. 4) The nonrectifying behavior of phase II layers can be attributed to a lowering of the measured barrier height by thermionic-field emission at sharp cusps and protrusions in the phase II/GaAs interface.

Although the behavior of Pd in multielemented contacts to GaAs cannot be directly inferred from these findings, it is apparent that Pd, unlike Pt, is not suitable as a rectifying gate contact to n-GaAs since only moderate heating (~250°C) results in nonrectifying behavior. Another im-
Table II. Current-voltage measurements of Pd-GaAs diodes a)

<table>
<thead>
<tr>
<th>Thickness Pd deposited [nm]</th>
<th>Annealing treatment temp. [°C], time [min.]</th>
<th>$q_b$ [eV]</th>
<th>$n$</th>
<th>Interface morphology</th>
</tr>
</thead>
<tbody>
<tr>
<td>15</td>
<td>as-deposited</td>
<td>0.76</td>
<td>1.45</td>
<td>oxide patches, voids and textured grains of phase I (grain size 10-20 nm)</td>
</tr>
<tr>
<td>100</td>
<td>as-deposited</td>
<td>0.73</td>
<td>1.45</td>
<td>same as above</td>
</tr>
<tr>
<td>15</td>
<td>250,20</td>
<td>0.77</td>
<td>1.20</td>
<td>nominally monocrystalline and uniform phase I layer 15-20 nm thick</td>
</tr>
<tr>
<td>100</td>
<td>250,20</td>
<td>0.76</td>
<td>1.21</td>
<td>same as above</td>
</tr>
<tr>
<td>100 b)</td>
<td>250,20</td>
<td>0.78</td>
<td>1.20</td>
<td>same as above</td>
</tr>
<tr>
<td>15</td>
<td>350,20</td>
<td>0.62</td>
<td>2.08</td>
<td>$\sim$95% phase II. Interface with GaAs is irregular with sharp corners</td>
</tr>
<tr>
<td>100</td>
<td>350,20</td>
<td>0.71</td>
<td>1.24</td>
<td>same as above</td>
</tr>
</tbody>
</table>

a) Only data that could be satisfactorily modeled with the non-ideal thermionic emission model are included in this table. Additional samples annealed at 350°C were found to be non-rectifying, even with a mesa etch.

b) Mesa-etched sample.
Important observation is that thick Pd films are inappropriate as ohmic contacts to shallow devices because the penetration depth of phase II is laterally nonuniform. Palladium, however, does have one important property that is perhaps unique among the elements; a thin layer (≤10 nm) (3,4, this study) is sufficient to disperse the native GaAs oxide at low temperatures (≤80°C). Thus, a thin layer of Pd deposited prior to deposition of the ohmic contact metallization will serve to promote a uniform and complete reaction with GaAs in annealed contacts.

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References


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