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A Broadband Millimeter Wave LNA in 65nm CMOS Technology with Minimized Gain and Noise Variations

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A Broadband Millimeter Wave LNA in 65nm CMOS Technology

with Minimized Gain and Noise Variations

A thesis submitted in partial satisfaction of the
requirements for the degree Master of Science in

Electrical Engineering

by

Fariborz Dadnam

2013
ABSTRACT OF THE THESIS

A Broadband Millimeter Wave LNA in 65nm CMOS Technology with Minimized Gain and Noise Variations

by

Fariborz Dadnam

Master of Science in Electrical Engineering
University of California, Los Angeles, 2013
Professor Mau-Chung Frank Chang, Chair

A 60GHz band LNA in 65nm CMOS technology is presented in this paper with minimum noise figure of 3.6dB and maximum DC power dissipation of 8.5mW. This LNA operates in -3dB fractional bandwidth of over 20% with maximum voltage gain and noise variations of 1.64dB and 0.3dB, respectively, over the whole band of operation.
The thesis of Fariborz Dadnam is approved.

Tatsuo Itoh

William J. Kaiser

Mau-Chung Frank Chang, Committee Chair

University of California, Los Angeles

2013
To my parents, Shahnaz and Yazdgerd
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Chapter 1

INTRODUCTION

In recent decades the digital implementation of circuits based on CMOS technology has had enormous growth in industry. The precise controllability of such systems by software has built up this temptation to convert all traditional analog architectures to new digital versions. This attempt has had such a great success in wide range of devices being used in the “baseband“ side. Nevertheless, it has shown to be a very challenging task to implement RF front-end circuits based on digital architectures. The cost inefficiency and high power consumption have made it impossible, at least in near future, to construct a complete digital transceiver circuit.

On the other hand, the low cost and reliability of CMOS technology have attracted the companies in the industry to improve the CMOS technology for the size and frequency. These improvements have created a room for analog devices in CMOS process to meet their requirements of frequency and noise. It has become possible to integrate analog devices on the same chip along with baseband circuits.

The first active stage of a front-end receiver path, which processes the signal, is usually a low-noise amplifier (LNA). Being the first stage, the sensitivity of an LNA to noise and signal is crucial. In addition, an LNA is a device that has connections with the outside the chip and should follow the preceding device requirements. The preceding stage of an LNA is generally an
antenna, a select-band filter, or an RX/TX duplexer. One important requirement of these devices is the impedance matching with the LNA. In order to transfer the maximum power from the previous stage to the receiver path, the connection has to be matched. In RF circuits, the convention of $50\Omega$ impedance is being used. Hence another important factor in design of an LNA is to achieve a real input impedance of $50\Omega$ within the frequency range of operation.

In the following text, an LNA for the unlicensed millimeter wave frequency range has been designed and simulated while pursuing the above main objectives.

1.1 Unlicensed Millimeter Wave Frequency Range

The frequency range between 30 and $300\text{GHz}$ is considered *millimeter wave (mm-wave)* band [1]. The signal wavelength in this band ranges from 1 to $10\text{mm}$. The $57 – 66\text{GHz}$ spectrum (also called $60\text{GHz}$ band) is internationally recognized as the unlicensed mm-wave band. This range is part of V-band ($50 – 75\text{GHz}$). However, this unlicensed band is limited to $57 – 64\text{GHz}$ in the United States as stated by Federal Communications Commission (FCC) [2].

Due to oxygen molecules resonance, the signals attenuate severely in this region. In addition, because of high frequency nature of mm-waves, the path loss is more significant. For example, for a link of $10\text{m}$, the path loss in free-space at $60\text{GHz}$ is $88\text{dB}$. Another specification of $60\text{GHz}$ band is that it requires line of sight between receiver and transmitter for the communications. Consequently, this spectrum is suitable for short-distance communications limited to few kilometers with clear line of sight through the channel.

As a result of above characteristics, millimeter wave has several advantages that make it appropriate for some specific applications. Amongst these advantages are: highly secure data transmission in short distances due to oxygen absorption, reusability of the frequency channels
with minimal interference in a small area, and high data rate transmission due to the large bandwidth.

60GHz band has found many wideband applications that require high-speed communications. IEEE WPAN 802.15.3c was first introduced in 2005 as a physical layer (PHY). This standard supports minimum data rate of 2Gbps and optional data rate of greater than 3Gbps over few meters range. The channel plan for this standard is divided into four channels. Only first three channels can be used in the US, though. 802.15.3c is suitable for high quality video streaming and downloading. Another technology that has been developed in 60GHz range is WirelessHD. It was introduced in 2007, which was aimed for transferring lightly compressed or uncompressed high-definition (HD) video and audio contents. The ideal speed of this technology is 5Gbps over the range of up to 10m. Ecma International in Europe has developed Ecma TC48 for 60GHz WPAN physical layers for multimedia and bulk data transfer in short distance [3]. This standard, similar to 802.15.3c, has four channel allocations. It is stated that TC48 has the ability to be used in a heterogeneous network with different device physical layer capabilities. The optimum data rate has been declared up to 5Gbps over 10m distance. Wireless Gigabit Alliance (WiGig) announced IEEE 802.11ad in 2009. 802.11ad is aimed to be backward compatible with existing WLAN standards (i.e. IEEE 802.11) [4]. It provides data rate of up to 7Gbps, ten times faster than 802.11n.

1.2 Project Overview

As one of the most important modules in an RF receiver, this project has targeted an LNA covering the whole international unlicensed mm-wave band (57 – 66GHz) with minimum gain and noise variations. Besides wideband requirement of this project, the second priority is to
keep the noise of the LNA as low as possible over the whole band. However, the tradeoff among noise figure, input resistance, and power dissipation has been considered throughout the design process. The third priority is the input impedance that has been tried to match to real resistance of 50Ω with minimum input return loss. The power dissipation of the circuit has been placed as the fourth priority because it is already expected to be low enough by employing the particular topology used in this two-stage LNA. Finally, the voltage gain of the circuit has been tracked throughout the design process to provide large enough voltage swing to drive the future mixers at the output of the LNA.

TSMC 65nm is a suitable choice for our specific LNA. The main reason is the metal and dielectric thicknesses make this technology almost perfect in such a frequency range for electromagnetic (EM) devices, such as spiral inductors and transmission lines. We expect such a high quality factor (Q) from designed inductors in this project.

1.3 Circuit Connections with Outside World

Single-ended amplifiers have been used in this project. Since the common antennas are designed single-ended, the input of the first stage of the LNA can be directly connected to any proper 50Ω antenna or any other 50Ω device preceding the LNA.

On the other hand, it is usual to use differential mixers thereafter the LNAs. For this purpose, a monolithic transformer with center-tapped secondary has been utilized as a balun to provide a differential output. This transformer has several advantages that will be explained in the following chapters.
Chapter 2

LOW-NOISE AMPLIFIER

An LNA as a critical input circuit has to meet several specifications. These parameters will be discussed, in the following subsections.

Stability

Oscillation in a two-port network happens when either the input or the output port of the network presents a negative resistance [5]. From another perspective, a positive feedback from the output to the input port makes the network unstable. Since an LNA is connected to the outside of the chip, its input impedance might not be fixed over whole frequency spectrum [6]. Also, parasitic inductances of the wire bonding, in the chip packaging can easily make the circuit unstable. For these reasons, a careful attention has to be paid to make the LNA stable for all the frequencies. The Stern stability factor characterizes a two-port network stability.

\[
K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{12}S_{21}|^2} \tag{2.1}
\]

\[
\Delta = S_{11}S_{22} - S_{12}S_{21} \tag{2.2}
\]

For unconditional stability of a circuit, the necessary and sufficient conditions are,

\[ K > 1 \quad \text{and} \quad \Delta < 1 \]
Indeed, the circuit topology used in this project provides a robust unconditional stability over the whole frequency spectrum.

**Input return loss**

In order to obtain the maximum power transferred from the outside of the chip to the LNA, the input impedance has to match the preceding stage’s impedance. This off-chip stage is usually an antenna, a select-band filter, or an RX/TX switch. As a standard, the output impedance of these devices is designed to be 50Ω. As a result, the input impedance of an LNA is tried to meet this value. It is recommended to use the characteristics of the LNA’s transistor and elements surrounding it to acquire this desired input impedance in order to avoid any additional matching network that may increase the loss and noise at the input.

**Noise figure**

The noise of the first stage – LNA – has the greatest contribution on the overall noise of the system. The famous *Friis’ formula* for noise shows the significance of this statement.

\[
F = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + \cdots + \frac{F_n - 1}{G_1 G_2 \cdots G_{n-1}} \tag{2.3}
\]

where \( F_n \) and \( G_n \) are the noise factor and the power gain of the \( n \)-th device, respectively, in a cascaded configuration. Please note that in this equation no impedance matching is assumed.

Because of this low noise requirement, the choice of the very first stage is limited to few amplifier circuit topologies such as common-source or -emitter.

**Gain**

As seen in (2.3), increase in the gain of the first stage will reduce the impact of the noise of the subsequent stages. Nonetheless, larger gain in the early stages makes the system more

\(^*\) Noise and power gain terms in this equation are ratios and are not in dB/dBm.
vulnerable to the nonlinearity of the following stages. This is especially important when an LNA has to drive a mixer. An approximate calculation of the total $IP_3$ clarifies this point.

\[
\frac{1}{IP_3} \approx \frac{1}{IP_{31}} + \frac{G_1}{IP_{32}} + \frac{G_1G_2}{IP_{33}} + \cdots + \frac{G_1G_2 \cdots G_{n-1}}{IP_{3n}} \tag{2.4}
\]

where $IP_{3n}$ is the third-order-intercept point of the $n$-th stage.

Foreseeing some future circuits connected to the output of our LNA, we tried to design a circuit with a moderate gain.

**Linearity**

As seen in (2.4), the early stages do not impact the overall nonlinearity of the system significantly when the later circuits are more nonlinear. Indeed, LNA does not limit the linearity of a system, so the nonlinearity of an LNA requires less attention in the design process. Although for wideband LNAs, nonlinearity becomes critical – due to strong interferences – it is not the case for 60GHz spectrum because of low interference sensitivity nature of this band.

**Bandwidth**

The bandwidth of LNAs is usually considered in $1dB$ variation of the gain. So the $-3dB$ bandwidth of the frequency response has to be wider. In the case of 60GHz band, a fractional bandwidth of greater than 15% is required.

**Power dissipation**

In an LNA, there is a tradeoff among power dissipation, noise figure, and linearity. The simple single-ended topology used in this project, makes the power dissipation small enough in comparison to later devices being connected after the LNA.
2.1 Stage 1 Topology

To meet the best noise figure and input return loss, a cascode common-source (CS) configuration with inductive degeneration has been designed for the first stage. Figure 2.1 shows such a configuration.

![Figure 2.1 - First stage circuit schematic](image)

In the following subsections, every part of this circuit will be explained in details.

2.1.1 Input Impedance Matching

The idea is to design an input resistance of 50Ω without noise of a 50Ω resistor. This can be done by employing inductive source degeneration. The input impedance of the CS stage with existence of the inductive degeneration can be approximately calculated as below,

\[
Z_{in} = \frac{g_{m1}L_s}{C_{GS1}} + \frac{1}{C_{GS1} \cdot s} + (L_s + L_{series}) \cdot s
\]  

(2.5)
where $g_{m_1}$ and $C_{GS_1}$ are the transconductance and gate-source capacitance of $M_1$ in Figure 2.1. $L_s$ is the source inductor and $L_{series}$ is the series inductor in the input path (not shown in Figure 2.1).

The first term of this equation shows a real number which needs to set equal to 50$\Omega$ and the next two imaginary terms have to cancel out. The following expressions show these results.

\[
L_s = 50\Omega \cdot \frac{C_{GS_1}}{g_{m_1}}
\]

\[
L_{series} = \frac{1}{C_{GS_1} \cdot \omega^2} - L_s
\]

where $s$ is replaced with $j\omega_0$ and $\omega_0$ is the resonant angular frequency.

The coefficient of $L_s$ in the first term highlights the cutoff frequency definition. Because of high cutoff frequency ($f_T$) of the MOS transistors in 65nm ($\approx 170GHz$) [7], we have to reduce the cutoff frequency to meet the real part requirements. Cutoff frequency is defined as below.

\[
f_T = \frac{g_m}{2\pi(C_G + C_{par})} \quad (2.6)
\]

where $C_G$ is the gate capacitance equal to $C_{GS} + C_{GD}$. $C_{par}$ is the total input parasitic capacitance due to gate-drain and gate-source connections [8].

Since $C_G$ is defined by the transistor, we do not wish to change it by changing the transistor physics that may cause to alter the LNA performance. Instead $C_{par}$ is available to us to play with. In this project, a value of very small (couple of femto Farad) is required so that it can be easily implemented in the layout. This capacitor is considered from total path capacitance from the gate to the bonding pad. However, a low capacitance RF pad is used for the input because too much capacitance will ruin the performance.
Now that the real part of the input impedance is set around $50\Omega$, the imaginary terms need to be canceled. Since the degeneration inductor is not adequate, we need to add an additional inductor in series ($L_{\text{series}}$) with the input to resonant out with the total input capacitances. This inductor can be considered off-chip. However, after some researches we were not able to find such a small (optimal value of $550\mu H$) off-chip inductor at $60\,GHz$. Therefore, either two to four parallel off-chip inductors should be used or an on-chip inductor with relatively high Q may be designed for this purpose.

### 2.1.2 Cascode Configuration

To achieve an unconditional stability over a wide frequency range, we added a cascode transistor at the cost of extra noise and extra overhead voltage consumption. In this case the load seen by the LNA transistor ($M_1$) is this common-gate (CG) transistor ($M_2$ Figure 2.1). This CG transistor improves the stability by improving the reverse isolation ($S_{21}$) appeared in (2.1). This is possible because of the high input/output isolation of a common-gate topology.

However, the gain of the LNA may be dropped by this addition due to consuming extra voltage overhead. To overcome this issue, an inductive feedback is added to the gate in the bias line of the CG stage [9]. This improvement in gain happens because the voltage drop across $C_{GS}$ of the cascode transistor enhances and leads to higher voltage swing at the output. In fact, this gate inductor resonates with adjacent parasitic capacitances and hence the drain impedance increases. The drawback is the usage of an additional inductor in layout.

Besides, an inductor ($L_i$ in Figure 2.1) between the CS and CG transistors can improve the LNA performance further [10]. Since both the output of the CS and input of the CG stages are capacitive, a good impedance matching does not occur between the two [11]. In this case, this inductor can resonant with some capacitance and provide the best cutoff frequency for the
CG stage. Accordingly, the overall gain is enhanced. Since this inductor is placed before the CG stage, it can be used to tune the noise figure and input impedance as well.

### 2.1.3 Inductive Load

Finally, an inductive load (\(L_d\) in Figure 2.1) is used to save overhead voltage while enhancing the LNA voltage gain. In addition, this inductor resonates with the total capacitance at the output and makes it possible to operate at mm-wave frequency. The resonant frequency is chosen around 58GHz for this stage. In fact, the first stage has a narrower bandwidth in comparison to the total bandwidth and, in fact, covers the lower part of the overall bandwidth.

This inductive load has a little impact on the input impedance in the presence of the cascode stage, appreciating the CG configuration.

A three-terminal inductor is chosen here. While the entire inductor is seen by the first stage as a load, smaller portion of this inductance is seen by the next stage. This is because the middle terminal passes the signal to stage 2. The reason of doing this is to obtain a better input matching on the next stage while the center frequency of the first stage does not change.

### 2.2 Stage 2 Topology

The main purpose of adding the second stage is to improve the bandwidth. As indicated in Figure 2.2, the lower part of the bandwidth is taken care by the first stage. The overall bandwidth is further extended by the second stage.

*Figure 2.2 – Frequency response of the first stage on the left and frequency response of the second stage on the right*
Stage 2 also increases the voltage gain of the overall LNA and provides a larger isolation between the input port of the LNA and the mixer after the LNA. In addition, this stage provides a differential output that is suitable for high efficiency mixers. Figure 2.3 depicts the stage 2 schematic.

![Figure 2.3 – Stage 2 CS configuration](image)

### 2.2.1 Capacitive Coupling

The signal is coupled from the first stage to the second one by means of a capacitor. This capacitor isolates the DC biasing of two stages. In addition, as a high-pass-filter it forms and prepares the signal for stage 2. The corner frequency is chosen such that the gain at the center frequency of stage 1 compresses a little bit and as a result a flatter response is produced to be fed to stage 2.

### 2.2.2 Common-source Configuration

Again, in this stage a CS topology is used. Here, stability is less concerned because the stage is designed with known input and output impedances. So we omitted using a CG stage as a load. The primary of a transformer, indeed, plays the role of the load in this stage.
The signal is fed to the gate by means of a coupling capacitor. Therefore the gate of the transistor can have its own bias while the drain of the previous stage still receives the maximum DC supply voltage.

The CS stage still requires an inductive source degeneration for the best input matching. Please note that we do not need to conjugate match to the previous stage because the maximum power transfer is not the case. Instead, the maximum voltage swing at the output and minimum noise are pursued. As was expected, adding the second stage had just a little impact on the total noise figure. The reason is that the first stage had a large enough gain to reduce the noise contribution of the following stages.

2.2.3 Differential Output

The differential output is produced by a planner monolithic transformer from the single-ended transistor output. In the beginning, many active balun circuits were considered to be used either as the third stage or in place of current transformer [12] [13] [14] nevertheless we finally discovered that a monolithic transformer can offer the best performance.

In addition to extra power consumption by these active baluns, they suffer from phase and/or gain error between their differential outputs. Consequently, it was decided to use a simple 1:2 transformer at the output. This transformer has several advantages: converting single-ended signal to differential, AC coupling of signal between two modules (output of LNA and input of mixer), and voltage amplification. Since there has not been considered any specific circuit at the output, no impedance matching has done at the output of the LNA. Though, this transformer makes it easy to build a matching circuit for the next module with the minimal impact on the LNA’s performance. In addition, the transformer features a center tap on its secondary, which can be used to bias the next stage.
The primary inductor of this transformer – similar to the first stage – resonates with the total capacitance of the drain of the transistor at center frequency of \( \sim 62\text{GHz} \). This guarantees a large bandwidth covering the whole unlicensed mm-wave band.

### 2.3 Auxiliary Circuits

The power supply voltage level of 1.2\( V \) has been used to feed this LNA. This DC supply has to be as clean as possible when is supplied to the circuit. In addition, this voltage should provide required DC biases to the gates. These facts require additional circuits that have been discussed below.

Also, since the circuit has connection with outside world through bonding pads, it is vulnerable to electrostatic discharges that can be applied to the LNA. Our circuit is protected from this matter by means of ESD protection circuits enlightened below.

#### 2.3.1 Decoupling Capacitors

To prevent the fluctuations in DC supply due to AC current variations in transistors, bypass capacitors are required to short the AC signal to ground at DC supply connections. For this purpose, the chip is filled up with VDD and GND layers in all empty spaces on the layout. As will be discussed, these layers are arranged such that they create a big capacitor. This capacitor can be used for the purpose of bypassing AC signal to ground.

#### 2.3.2 Gate Biasing

The circuit in Figure 2.4 is used to DC bias the gate of the CS transistors in either stage. Using a voltage source configuration, this circuit generates a constant bias voltage while leaves the minimum footprint on the performance of the LNA. \( R_2 \) is picked relatively large for better
noise figure and input matching of the LNA. Also, a large decoupling capacitor ($C_1$) provides a clean DC bias to the gate.

![Bias circuit diagram](image)

*Figure 2.4 – Bias circuit for both first and second stages*

### 2.3.3 ESD Protection

Except the output pads – due to isolation of the circuit by the transformer – ESD protection circuits have been used for other bonding pads. The schematic of this circuit is given in Figure 2.5.

![ESD protection circuit](image)

*Figure 2.5 – A simple ESD protection circuitry*

The diodes in this circuit, simply short any voltage beyond the power supply levels (caused by either negative or positive charges).
Chapter 3

**PHYSICAL DESIGN**

Because of high frequency nature of this project, it is important to pay special attention to the distances and dimension of components on the layout. For this reason, except for rf components that come with TSMC 65nm library, it is better to recognize the other sensitive parts by electromagnetic (EM) simulations – specially passive devices.

In this chapter, we will go over the physical considerations of the specific devices that are subject to be affected by undesired effects and/or electromagnetic.

3.1 Passive Devices

3.1.1 Spiral Inductors

Transmission lines always have had a special position in microwave and mm-wave applications. Particularly, microstrip lines (MSL) and coplanar waveguides (CPW) have been utilized in many CMOS technology circuits [15] [16] [17]. The main reasons of using transmission lines are summarized as the well-defined return currents, lower coupling between structures, and operation in wider frequency band [9] [16]. However, large area consumption, lower gain, and higher noise make transmission lines less attractive than spiral inductors in CMOS applications.
In this project, it is decided to take advantages of spiral inductors. To overcome few issues with spiral inductors, several techniques have been employed. The isolation between spiral inductors has been improved by using proper guard metal rings surrounding spiral inductors [18]. In addition, the circuit configuration that has been already discussed proved of obtaining a wide bandwidth, still using spiral inductors.

Depending on the physical location and interconnections, two kinds of spiral inductors were used. The single-ended inductors (the spiral inductors with connections in either side) were designed for the source of the CS transistors. These inductors should have the shortest path to ground to keep the accuracy. Therefore, the asymmetric spiral inductors are the best choice. Figure 3.1 shows the source inductor employed in stage 2 along with its guard ring.

![Figure 3.1 – Source inductor of the second stage CS transistor](image)

For other places, symmetric inductors have been designed. Figure 3.2 depicts two symmetric spiral inductors. The one with center tap is used as the load of the first stage. The center tap carries the signal to the coupling capacitor of the second stage.
These inductors were characterized by ADS Momentum. The inductance and quality factor of two-terminal inductors can be extracted from S-parameters using the following equations, respectively.

\[
L = \frac{\text{Im} \{Z_{2,1}\}}{2\pi f} \tag{3.1}
\]

\[
Q = \frac{\text{Im} \{Z_{2,1}\}}{\text{Re} \{Z_{2,1}\}} \tag{3.2}
\]

where \(Z_{2,1}\) is the converted Z-parameter from two-port to one-port as defined below.

\[
Z_{2,1} = Z_{11} + Z_{22} - 2Z_{12} \tag{3.3}
\]
However, the inductance and quality factor of a three-terminal inductor is calculated differently such that the middle terminal shorted to ground. In this case, we can replace $Z_{2,1}$ in above calculations with $Z_{3,1}$ given below.

$$Z_{3,1} = Z_{2,1} - \frac{(Z_{13} - Z_{23})^2}{Z_{33}}$$  \hspace{1cm} (3.4)

where $Z_{3,1}$ is the converted Z-parameter from three-port to one-port.

3.1.2 Monolithic Transformer

For the output of the LNA a three-port\(^\dagger\) planar monolithic transformer has been employed. Depending on the application, different types of transformers can be used. Two main structural properties were being perused in choosing a specific transformer for this project: wideband response and voltage amplification. For the latter one, a 1:2 transformer was picked. A tapped transformer (concentric transformer) is the best choice in broadband applications in which the parasitic capacitances are minimized [19] [20].

This transformer is implemented on the very top layer (metal 6) with few connections using underneath layer. This helps to reduce the parasitic capacitance to the substrate. Also, by taking advantage of the metal 6 thickness the parasitic resistances and hence metal loss is minimized.

The magnetic coupling only happens laterally between adjacent conductors which has the advantage of low port-to-port capacitance and disadvantage of low mutual coupling. On the other hand, the self-inductance of this transformer is greater than other types of on-chip transformers [21]. Accordingly, the coupling coefficient of such a structure might be as low as 0.6 or less. The coupling coefficient of a transformer is defined in (3.5).

\(^\dagger\) A three-port transformer is realized as a two-terminal primary inductor and a three-terminal secondary inductor in which the center tap is often used as the common terminal for biasing the circuits at the secondary side.
\[ k_m = \frac{M}{\sqrt{L_p L_S}} \]  

(3.5)

where \( M \) is the mutual inductance. \( L_p \) and \( L_S \) are the primary and secondary inductances, respectively.

For the purpose of this project, a tapped monolithic transformer was realized. This transformer is depicted in Figure 3.3.

![Figure 3.3 – Tapped transformer at the output of the LNA](image)

In this figure, the double-port and the triple-port represent the primary and secondary terminals, respectively.

### 3.1.3 MOM Capacitors

Metal-oxide-metal (MOM) capacitors are superior in high frequency applications than metal-insulator-metal (MIM). MOM capacitors utilize the effect of lateral capacitive coupling between metal fingers. Due to a better process control of horizontal dimensions than vertical layer thickness, more accurate matching is obtained for MOM capacitors [22]. In addition, the parasitic capacitances are lower for this type of capacitors while they exhibit higher Q than MIM capacitors.
To increase the capacitance, several metal layers are connected vertically using vias. In this design, three MOM capacitors are used which are employing first four bottom metal layers.

Amongst these capacitors, the coupling capacitor has to be designed carefully. Indeed, since the general purpose TSMC 65nm lumped capacitors are only characterized up to 20\text{GHz}, we EM simulated this coupling individually by ADS Momentum to obtain a better accuracy. Figure 3.4 shows the coupling capacitor.

![Coupling Capacitor](image)

**Figure 3.4 – MOM capacitor for AC coupling between two stages**

Please note that the ports of this capacitor can be acquired on two opposite sides. The substrates of MOM capacitors are all grounded.

The capacitance and quality factor of a capacitor can be extracted from S-parameters by using the following formulae.

\[
C = \frac{\text{Im}\{Y_{11}\}}{2\pi f \cdot (1 - \text{Re}\{Y_{11}\})} \quad (3.6)
\]

\[
Q = \frac{\text{Im}\{Y_{11}\}}{\text{Re}\{Y_{11}\}} \quad (3.7)
\]

These equations have been used to design a proper capacitor. These parameters are swept over a wide frequency range as shown in the following chapter.
3.1.4 Bonding Pads

A bonding pad is the connection to the outside world. The bonding pads can have a lot of parasitic capacitance to the substrate. This is fine with VDD and GND pads but it becomes important for the RF pads. In order to reduce these parasitics we used only the top layer (metal 6) for the RF pads. However, DC pads are constructed from all metal layers stacked on top of each other and interconnected through vias.

The bonding pads are designed only for completeness of this project. Since an LNA is usually being used in integration with other circuits, the final chip might have different RF and/or input/output pads.

3.2 Active Devices

3.2.1 Deep N-well NMOS Transistors

The transistors selected from TSMC 65nm kit, nmos_rf. This NMOS is placed in a deep n-well. This makes the transistor isolated from noises produced in the common p-substrate by other components. The local bulk – which is a p-type silicon – is connected to ground. Next, the deep n-well surrounding the local bulk is connected to VDD. Figure 3.5 shows a typical deep n-well NMOS structure with proper DC connections.
**Figure 3.5** – Cross section of a typical deep n-well NMOS with proper DC connections
Chapter 4

SIMULATION RESULTS

The process of simulation was done in an iteration manner. In the beginning, we started the simulation with ideal inductors and rest of parts from TSMC 65nm library. In fact, the ideal inductors gave a very good starting point to come up with rough transistor dimensions. Later, designed inductors were EM simulated in ADS Momentum and took place of ideal inductors in the circuit.

The first stage was designed individually. After meeting input impedance, noise figure, and stability criteria, the second stage was added. These two stages were tuned together to ensure a final compatible result.

4.1 EM Simulations of Passives

4.1.1 Inductors

The spiral inductors were simulated by ADS Momentum. The S-parameters were converted to inductance value and quality factor by using (3.1) to (3.4). As samples, the inductance and quality factor of spiral inductors given in Figure 3.2 are plotted in Figure 4.1. They are simulated over a wide range to ensure the inductor doesn’t hit the self-resonance frequency (SRF) point during frequency range of operation.
The rest of inductors were characterized in the same manner. Finally the extracted S-parameters have been passed to the circuit schematic for further simulation with rest of the LNA.

### 4.1.2 Capacitors

Figure 4.2 illustrates the characteristics of the coupling capacitor shown in Figure 3.4 using given formulae in (3.6) and (3.7).
This capacitor is very significant in shaping the final frequency response of the circuit as a wideband LNA, so it has been designed carefully.

4.2 Circuit Simulations

The circuit simulations have been done by Cadence Spectre. The ideal inductors were replaced by corresponding inductor S-parameters. In the following subsections all the tests were done on the complete LNA circuit.

According to dc analysis, the power dissipation of overall LNA is measured $8.50mW$ at 1.2V power supply.

4.2.1 Stability

Stability of the entire circuit at all frequencies is critical. Therefore, the stability has been checked by Stern stability factor (K-factor) from DC to 120GHz. The upper bound has been decided based on the maximum frequency at which passive devices were EM simulated. As discussed in chapter 2 under Stability paragraph, this number has to be greater than 1 over the whole frequency spectrum. Figure 4.3 proves the stability of the designed LNA.
4.2.2 Input Impedance

Throughout the design process a great effort was spent to achieve the lowest input return loss ($S_{11}$) over the frequency range of operation ($57 – 66GHz$). However, an off-chip inductor was added in series to the input path to give this extra degree of freedom to adjust the input impedance and noise figure after fabrication. The following simulations are all done with the existence of this off-chip inductor with value of $550pH$.

Figure 4.4 demonstrates the input return loss of less than $-10dB$ up to $65GHz$. Please note that this can be improved by adjusting the off-chip inductor with scarifying the noise figure and voltage gain variations. This point will be discussed in section 4.3. However, since the most applications of unlicensed mm-wave are limited to $57 – 64GHz$, this value was left as is to avoid greater variations in gain and noise.
The input return loss is an indication of input impedance matching. The goal for the input impedance is the real value of 50Ω. Figure 4.5 shows the deviation of input impedance from this value over the frequency range of operation.

Figure 4.4 – Input return loss of the circuit

Figure 4.5 – Real and imaginary parts of the input impedance

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The imaginary part indicates a positive value in most part of the bandwidth which specifies somehow inductive impedance. The real part varies between 37.7 and 59.9Ω which is within the acceptable range.

### 4.2.3 Noise Figure

The noise figure of the circuit is in a tight tradeoff with the input impedance. Also, it is important to consider keeping the noise level as steady as possible over the whole bandwidth. In this project, we were very successful to achieve noise figure of under 4dB for the entire band with maximum variation of ~0.3dB. Figure 4.6 proves this statement.

![Noise Figure](image)

**Figure 4.6 – Noise figure of complete circuit**

As indicated, the minimum noise figure is read 3.61dB at center frequency of 60.67GHz which is very close to the center frequency of unlicensed mm-wave band.
### 4.2.4 Voltage Gain

Although the voltage gain has the least priority in design of an LNA, we attained fairly high voltage gain over a large bandwidth. The maximum voltage gain is measured 26.58\(dB\) at 58.34\(GHz\). Another important factor of an LNA is to retain the gain variation even less than 3\(dB\) over the band of operation. This variation is, in fact, \(~1.64dB\) for 57 – 66\(GHz\) and \(~1.13dB\) for 57 – 64\(GHz\) in our project. The total –3\(dB\) bandwidth and fractional bandwidth are measured 12.76\(GHz\) and 20.44\%, respectively. These facts are pointed out in Figure 4.7.

![Voltage Gain](image)

**Figure 4.7 – Voltage gain of the first stage and overall LNA**

As discussed previously, the center frequency of the first stage was chosen lower than the overall circuit center frequency in order to improve the bandwidth. Then by means of the coupling capacitor and second stage configuration the right side of this center frequency (57.57\(GHz\)) was amplified more to achieve this nice broadband response.
4.3 Off-chip Tuning

As discussed, an off-chip inductor is considered in series with the input. This off-chip inductor gives additional flexibility to the circuit after fabrication for exact tuning. This inductor can impact on the input impedance, noise figure, and gain of the LNA as shown in Figure 4.8.

![Figure 4.8](image)

*Figure 4.8 – The impact of off-chip series inductor on the (a) input return loss, (b) noise figure, and (c) voltage gain*
The results given in previous sections are provided with value of $550\text{pH}$ inductance. We have swept this value from $450\text{pH}$ to $550\text{pH}$ with step of $50\text{pH}$. Although $500\text{pH}$ gives a better input return loss while the noise figure will not be affected too much, a careful look indicates that the variation in voltage gain increases up to $2dB$. Since one of our objectives is to keep the gain and noise variations as low as possible, we stick with former value of $550\text{pH}$. Moreover, these results might be slightly different after fabrication, so choosing the final value is postponed after fabrication.
Chapter 5

LAYOUT AND PHYSICAL CONSIDERATIONS

After obtaining desirable results from simulation, it is the time for arranging the components on the silicon substrate and construct the physical circuit layout. Each stage was laid out individually and verified by Calibre tools. Final layout, with all interconnects and connection pads, was also verified one more time by these tools.

In the following short sections, the proof of these verifications along with final chip layout is sketched.

5.1 Integrated Circuit Layout

The circuit components were laid out based on general purpose TSMC 65nm CMOS technology rules. The main objective was to design a compact layout while maintaining enough isolation between parts concerning noise and signal coupling. For this reason, all the inductors are surrounded by metal guard rings where the most electromagnetic coupling was expected. On the other hand, as discussed earlier, using MOSFETs in deep n-well averts the noise influence generated by other components in the substrate.

In addition, it was considered to utilize VDD and GND layers all over the places where were not occupied by other components. This itself not only reduces the coupling between devices but also provides a consistent and clean DC supply all over the chip. The arrangement of
VDD and GND layers is such that a capacitor like structure between the layers is constructed and hence offering a big decoupling/bypass capacitor covering the whole chip.

Besides, the interconnections between the components were considered as short as possible to avoid any unwanted parasitic effect. Since the length of every and each interconnect is much less than the wavelength ($\lambda \approx 5000\mu m$ vs $L_{\text{max}} \approx 120\mu m$), no EM simulation is required for the paths.

The complete chip area size excluding the pads is measured $343\mu m \times 282\mu m$ (area= 0.097$nm^2$). Figure 5.1 shows the LNA layout produced in Cadence Virtuoso Layout.

![Figure 5.1 – Final LNA layout without bonding pads](image)

Finally, the LNA was enclosed by the bonding pads and finished with extra interconnections for ESD protection circuits. Figure 5.2 shows the final chip layout.
5.2 Physical Examinations

In order to make the designed integrated circuit ready for tape-out and fabrication, the circuit must follow the technology rules, as well as, matching the layout to the schematic. Considering this matter, Calibre DRC tool was used to “design rule check” the circuit. Figure 5.3 shows the proof of passing all DRC rules except some density rules – which are due to existence of free spaces around and under the spiral inductors and can be skipped.
After passing the DRC rules, the layout was “layout v.s. schematic” checked by Calibre LVS. This tool checks the layout against schematic netlist. Passing LVS rules means the layout totally matches the design schematic components and connections. The LVS result window is shown in Figure 5.4. This report shows that the layout completely matches the schematic.

*Figure 5.3 – DRC rules verification report*
Figure 5.4 – LVS rules verification report
Chapter 6

**Final Notes**

We were able to successfully build and simulate a broadband low-noise amplifier meeting decent specifications in comparison with similar works. We showed that the designed LNA had small variations on voltage gain and noise figure across the whole mm-wave band. To complete the design, the final circuit was laid out and verified by software. Finally, the layout was finished with bonding pads and ESD protection circuits.

In the following sections, we conclude the project with comparison with similar works and suggest some idea about further improvement of the circuit.

### 6.1 Comparison with Similar Projects

An LNA is one of the most attractive circuits that many papers have been published about. Most of the designed LNAs are optimized for specific parameters and attempted to provide the best performance for those parameters.

Our design is specially designed for minimum gain and noise figure variation over the wide 60GHz bandwidth. Despite that, our LNA’s other parameters are comparable with similar works. In the following table, the performance of several LNAs is summarized and compared with our work.
Please note that in this table, the power gains in previous works are converted to voltage gains assuming 50Ω impedance matching.

### 6.2 Future Considerations

The performance of this project can be improved further by more optimizations of the layout. However, the only parameter that might need more improvement is the input return loss. Since we have utilized an off-chip inductor in series with the input, the input return loss can be easily tuned even after fabrication.

Since we have added bonding pads, this design could be used as an individual chip. The layout has been verified against technology rules and is ready to tape-out.
REFERENCES


[22] M. Ershov, "MOM capacitor simulation challenges and solutions".

