Title
Vertical Tunneling Hot Carrier Transport in 2D van der Waals Material-Based Devices for Optoelectronic Applications

Permalink
https://escholarship.org/uc/item/179395wb

Author
Torres Jr., Carlos Manuel

Publication Date
2015

Peer reviewed|Thesis/dissertation
Vertical Tunneling Hot Carrier Transport in 2D van der Waals Material-Based Devices for Optoelectronic Applications

A dissertation submitted in partial satisfaction of the requirements for the degree Doctor of Philosophy in Electrical Engineering

by

Carlos Manuel Torres Jr.

2015
ABSTRACT OF THE DISSERTATION

Vertical Tunneling Hot Carrier Transport in 2D van der Waals Material-Based Devices for Optoelectronic Applications

by

Carlos Manuel Torres Jr.

Doctor of Philosophy in Electrical Engineering
University of California, Los Angeles, 2015
Professor Kang Lung Wang, Chair

For over half a century, Moore’s law has driven the silicon electronics industry towards smaller and faster transistors. However, as the scaling limit of silicon Complementary Metal-Oxide-Semiconductor (CMOS) technology draws to an end, novel materials and device concepts have been eagerly sought out and investigated with hopes to augment the next generation of information processing. In this dissertation, I introduce a new paradigm of device concepts based on a vertical tunneling transistor structure incorporating individual 2D van der Waals (2D vdW) materials, such as graphene and MoS₂, in the active region. The essential physics relies upon the injection of non-equilibrium, or hot, electrons via the quantum tunneling process through a vertical heterostructure.

For the electronics aspect, we demonstrate 2D vdW material-based ambipolar hot carrier transistors (2D vdW-AHCTs), in which the injected hot electrons traverse vertically through the
2D vdW material in the base region and either reach the collector or back-scatter into the base region. For the optoelectronics aspect, the hot electrons are injected into the conduction band of the specific 2D vdW material in the base region where they relax and emit photons via hot carrier luminescence. Furthermore, it will be shown that the application of a top-gate voltage offers several functionalities. In the case of the 2D vdW-AHCTs, the top-gate/collector voltage controls the filter barrier height at the collector-base oxide.

We discovered that by choosing MoS$_2$ and HfO$_2$ for the filter barrier interface in addition to implementing a non-crystalline semiconductor such as ITO for the collector electrode, allows for the simultaneous emergence of ambipolar transport, an unprecedentedly high and voltage-tunable current gain ($\alpha \sim 0.95$, $\beta > 15$), and a voltage-tunable recombination current in the base region of MoS$_2$. Depending upon the collector electrode’s bias polarity, either a hot electron mode of operation or a hole mode of operation dominates the transport mechanism of the 2D vdW-AHCTs. In the case of the 2D vdW wavelength-agile light-emitting transistors (2D vdW-LETs), the top-gate voltage can tune the wavelength of the emitted photons via the band-filling effect in the Graphene Broadband Infrared Light-Emitting Transistor (GBILET) or by tuning the direct bandgap of monolayer MoS$_2$ in the MoS$_2$ Visible Light-Emitting Transistor (MoS$_2$-VLET) with the application of a perpendicular electric field.
The dissertation of Carlos Manuel Torres Jr. is approved.

Suneel Kodambaka

Oscar M. Stafsudd

Dwight C. Streit

Kang Lung Wang, Committee Chair

University of California, Los Angeles

2015
Dedicated to my family

and to the loving memory

of my grandfather,

Jaime Torres Marrero (1930-2014)
# TABLE OF CONTENTS

**Chapter 1. Introduction**

1.1 The Advent of 2D van der Waals (2D vdW) Materials and their Heterostructures ..............1

1.1.1 Electronic Properties of Graphene ..............................................................2

1.1.2 Electronic Properties of Transition Metal Dichalcogenides (TMDs) ..................5

1.2 Emergent Optoelectronic Properties of 2D van der Waals Materials ...................8

1.2.1 Hot Electron Luminescence in Graphene .......................................................10

1.2.2 Tunable Electronic Band Structures in TMDs with Perpendicular Electric Fields ..........................................................15

1.3 Hot Electron Transistors (HETs) ..................................................................16

1.3.1 Operational Principle of HETs .................................................................16

1.4 Graphene-Base Hot Electron Transistors (GB-HETs) .....................................18

1.4.1 Operational Principle of GB-HETs ..........................................................19

1.4.2 The Current Status and Limitations of GB-HETs ....................................20

1.5 Synopsis ........................................................................................................23

**Chapter 2. Fabrication of 2D vdW-AHCTs and LETs** ..............................................25

2.1 Complete Fabrication Process Flow of 2D vdW-AHCTs and LETs ..................25

**Chapter 3. The MoS$_2$-Base Ambipolar Hot Carrier Transistor (MoS$_2$-AHCT)** ............52

3.1 Introduction and Motivation for the MoS$_2$-AHCT ........................................52

3.2 Device Structure for the MoS$_2$-AHCT .........................................................54

3.3 Energy Band Diagrams for the MoS$_2$-AHCT .............................................57

3.4 Electrical Characteristics of the MoS$_2$-AHCT ...........................................61

3.4.1 Hot Electron Dominating Mode of Operation of the MoS$_2$-AHCT ............61
3.4.1.i  Input and Transfer I-V Characteristics ............................. 62
3.4.1.ii  Common-Base Current Gain Characteristics ............................. 63
3.4.2  Hole Dominating Mode of Operation of the MoS2-AHCT ................. 64
3.4.2.i  Input and Transfer I-V Characteristics ................................. 66
3.4.2.ii  Common-Base Current Gain Characteristics ............................. 66
3.4.3  Output Characteristics and Tunable Current Gain of the MoS2-AHCT .... 67
3.5  Summary .................................................................................. 71

Chapter 4. Towards 2D vdW Wavelength-Agile Light-Emitting Transistors (2DvdW-LETs) .................................................................................................................... 73

4.1  The Graphene Broadband Infrared Light-Emitting Transistor (GBILET) .... 73
4.2  Device Structure of the GBILET .................................................... 75
4.3  Principle of Operation of the GBILET ............................................. 76
4.3.1  Method to Calculate the Luminescence Power of the GBILET ............. 80
4.3.2  Method to Calculate the Luminescence Cutoff Wavelength of the GBILET ... 82
4.4  Raman Spectroscopy of Monolayer CVD Graphene ............................. 83
4.5  Electrical Characteristics of the GBILET ......................................... 84
4.5.1  Output Characteristics of the GBILET (I_{DS} vs V_{DS}) ...................... 86
4.5.2  Top-Gate Modulation of the GBILET (I_{DS} vs V_{TG}) ....................... 87
4.5.3  Tunnel Oxide Characteristics of the GBILET (I_{EB} vs V_{EB}) .............. 88
4.6  The MoS2 Visible Light-Emitting Transistor (MoS2-VLET) .................... 89
4.7  Device Structure and Principle of Operation of the MoS2-VLET .......... 90
4.7.1  Method to Calculate the Luminescence Power of the MoS2-VLET .......... 92
4.7.2  Method to Calculate the Luminescence Wavelength of the MoS2-VLET .... 92
Chapter 4. \textbf{Raman Spectroscopy of Monolayer CVD MoS$_2$} ..........................................................93

4.9 Characterization of the ITO Top-Gate Electrode for the MoS$_2$-VLETs .................................................94

4.10 Electrical Characteristics of MoS$_2$-VLET .................................................................................................96

4.10.1 Output Characteristics of the MoS$_2$-VLET ($I_{DS}$ vs $V_{DS}$) ..........................................................97

4.10.2 Top-Gate Modulation of the MoS$_2$-VLET ($I_{DS}$ vs $V_{TG}$) ...........................................................98

4.10.3 Tunnel Oxide Characteristics of the MoS$_2$-VLET ($I_{EB}$ vs $V_{EB}$) ..................................................99

Chapter 5. \textbf{Conclusion and Future Works} .................................................................................................102

5.1 Conclusion ..................................................................................................................................................102

5.2 Suggested Future Works ...........................................................................................................................104

References .........................................................................................................................................................106
LIST OF FIGURES

Figure 1-1. Constructing van der Waals heterostructures from 2D crystals ......................... 2
Figure 1-2. Electronic band structure of monolayer graphene ........................................... 3
Figure 1-3. Energy band alignments of various 2D van der Waals crystals ......................... 6
Figure 1-4. 3D structure of monolayer MoS$_2$ ................................................................. 7
Figure 1-5. Electronic band structure of bulk MoS$_2$ ....................................................... 8
Figure 1-6. 2D plot of the inelastic light scattering intensity versus Raman shift (cm$^{-1}$) and $2|E_F|$ in monolayer graphene ................................................................. 11
Figure 1-7. Hot electron luminescence (HEL) in monolayer graphene via photoexcitation ... 12
Figure 1-8. HEL in monolayer graphene excited by electron tunneling .............................. 13
Figure 1-9. Schematic of the HEL process and its spectrum ............................................. 14
Figure 1-10. Tunable bandgaps with applied perpendicular electric fields for various bilayer Transition Metal Dichalcogenides ................................................................. 16
Figure 1-11. Energy band diagram illustrating the operational principle of a hot electron transistor .............................................................................................................. 17
Figure 1-12. Energy band diagram of a graphene-base hot electron transistor (GB-HET) in the off-state and the on-state ................................................................. 20
Figure 1-13. Energy band diagrams showing the different filter potential barrier heights for two different GB-HETs ................................................................. 22
Figure 1-14. Common-base current gain ($\alpha$) as a function of filter barrier height .......... 22
Figure 2-1. Pre-furnace clean the silicon wafer ................................................................. 26
Figure 2-2. Grow the pad/buffer SiO$_2$ oxide for the LOCOS process .............................. 27
Figure 2-3. Deposit the Si$_3$N$_4$ film that will serve as a mask for the LOCOS process ....... 28
Figure 2-4.  Dry etch through the Si$_3$N$_4$ and the pad oxide for the LOCOS process……………..30
Figure 2-5.  Grow the SiO$_2$ field oxide to complete the LOCOS process……………………..31
Figure 2-6.  Photograph of the 4” silicon wafer after the growth of the field oxide……………..31
Figure 2-7.  Selectively wet etch the Si$_3$N$_4$ masks in heated phosphoric acid…………………33
Figure 2-8.  Grow the SiO$_2$ tunnel oxide via rapid thermal oxidation…………………………..34
Figure 2-9.  Transfer the 2D vdW material onto the active regions of the substrate………………37
Figure 2-10.  Dry etch the 2D vdW material in order to isolate the arrays of devices………………38
Figure 2-11.  Optical micrograph of CVD MoS$_2$ defined over the active region of the MoS$_2$-AHCT devices………………………………………………………………………………..39
Figure 2-12.  Pattern and deposit the base contacts………………………………………………..41
Figure 2-13.  Deposit the top-gate dielectric via atomic layer deposition……………………….43
Figure 2-14.  Sputter the ITO transparent top-gate electrodes…………………………………46
Figure 2-15.  Pattern and deposit the collector side gates to contact the central ITO regions……48
Figure 2-16.  Optical image of various arrays of fabricated MoS$_2$-AHCTs…………………..49
Figure 2-17.  Optical micrograph (10x) of a GB-HET with a thin semi-transparent metal top-gate electrode………………………………………………………………………………..49
Figure 2-18.  Optical micrograph (20x) of a GB-HET with a thin semi-transparent metal top-gate electrode………………………………………………………………………………..50
Figure 2-19.  Optical micrograph (50x) of a GB-HET with a thin semi-transparent metal top-gate electrode………………………………………………………………………………..51
Figure 3-1.  Device structure and schematic of the MoS$_2$-AHCT……………………………..56
Figure 3-2.  Cross-sectional view of the current confinement scheme into the vertical active region of the MoS$_2$-AHCT……………………………………………………………………57
Figure 3-3. Measurement setup for the MoS$_2$-AHCTs: common-emitter and common-base configurations

Figure 3-4. Energy band diagrams for the various operating conditions of the MoS$_2$-AHCTs

Figure 3-5. MoS$_2$-AHCT operating in the hot electron dominating mode

Figure 3-6. MoS$_2$-AHCT operating in the hole dominating mode

Figure 3-7. Output characteristics and tunable current gain of the MoS$_2$-AHCT

Figure 3-8. Tunable common-base current gain for a MoS$_2$-AHCT (Device 3) by varying the polarity of $V_{CB}$

Figure 4-1. Basic device structure and operational biasing procedure of a GBILET

Figure 4-2. Operational principle of the GBILET

Figure 4-3. Energy band diagram of the GBILET in thermal equilibrium

Figure 4-4. Energy band diagram of the GBILET with applied top-gate and back-gate negative voltage biases

Figure 4-5. Raman spectrum of monolayer CVD graphene transferred onto the GBILET

Figure 4-6. The three electrical biasing schemes used to characterize the GBILETs

Figure 4-7. Output characteristics ($I_{DS}$ vs $V_{DS}$) of the CVD graphene for a GBILET

Figure 4-8. Top-gate modulation ($I_{DS}$ vs $V_{TG}$) for a GBILET

Figure 4-9. Tunnel oxide characteristics ($I_{EB}$ vs $V_{EB}$) for a GBILET

Figure 4-10. Basic device structure and operational biasing procedure of a MoS$_2$-VLET

Figure 4-11. Raman spectrum of monolayer CVD MoS$_2$ transferred onto the MoS$_2$-VLET

Figure 4-12. The measured transmission spectrum of a control sample of ITO that was sputtered at the same time as the ITO top-gate electrode of our MoS$_2$-VLETs
Figure 4-13. Tauc plot (absorption coefficient versus photon energy) used for extrapolating the bandgap of the sputtered ITO ...........................................96

Figure 4-14. Output characteristics (I_{DS} vs V_{DS}) of the CVD MoS\textsubscript{2} for a MoS\textsubscript{2}-VLET ..............98

Figure 4-15. Top-gate modulation (I_{DS} vs V_{TG}) for a MoS\textsubscript{2}-VLET ...........................................99

Figure 4-16. Tunnel oxide characteristics (I_{EB} vs V_{EB}) for a MoS\textsubscript{2}-VLET .................................100
ACKNOWLEDGMENTS

I am very blessed to have the opportunity to collaborate with my friends and colleagues at the Device Research Laboratory at UCLA Electrical Engineering. First, I would like to express my sincere gratitude to Professor Kang L. Wang for taking me in as one of his graduate students, for his continual guidance throughout my development as a researcher, for his persistently optimistic and positive attitude and encouragement, and also for always providing me with an abundance of resources necessary to accomplish our research missions. Furthermore, I deeply appreciate my PhD dissertation committee, specifically Professor Dwight C. Streit of the UCLA Department of Electrical Engineering and the UCLA Department of Materials Science and Engineering, Professor Oscar M. Stafsudd of the UCLA Department of Electrical Engineering, and Professor Suneel Kodambaka of the UCLA Department of Materials Science and Engineering for their willingness to participate in the review of my PhD dissertation and their insightful and critical comments, which greatly improved the quality of this dissertation. I would also like to thank all of the members in DRL (too many to name) for their friendship, unselfish help, and insightful discussions, especially Guangyu Xu, Caifu Zeng, Yann-Wen “Blue” Lan, Jianshi Tang, Aryan Navabi, and Mohammad Montazeri. I greatly appreciate all of the kind assistance, advice, and training from the cleanroom staff of the UCLA Nanoelectronics Research Facility, especially Joe Zendejas, Max Ho, Wilson Lin, and Hoc Ngo.

I am also very grateful to the Department of Defense SMART (Science, Mathematics, and Research for Transformation) Scholarship for providing me with funding from 2008-2013 in order to pursue my graduate studies (MS and PhD) at UCLA Electrical Engineering and providing me annual summer internship opportunities (2009-2012) at the Space and Naval Warfare Systems
Center (SPAWAR) in San Diego, CA. I dearly thank my kind mentors and collaborators at the Advanced Photonic Technologies Branch as well as the Advanced Systems and Applied Sciences Division at SPAWAR (SSC-Pacific) in San Diego, California: Dr. James R. Adleman, Dr. Mitchell B. Lerner, Markham E. Lasher, Dr. Frank Hanson, and Ayax D. Ramirez, for all of their patience, guidance, insight, and support during my growth as a researcher during the last several years. I am greatly indebted to Dr. James R. Adleman’s close mentorship and guidance since we first met during my summer internship in 2012. With his assistance, we were able to establish and spearhead a collaboration between Professor Kang L. Wang’s Device Research Laboratory at UCLA and SPAWAR based upon my PhD dissertation proposal of the GBILET since April 2013. Finally, I would like to thank my family for the continual guidance, hope, and faith they provide me with each phone call.

Chapter 3 of this dissertation is a version of a submitted manuscript which is currently under the review process in Nature. The full citation is as follows: Torres Jr., C. M.*; Lan, Y.-W.*; Zeng, C.; Chen, J.-H.; Kou, X.; Navabi, A.; Tang, J.; Montazeri, M.; Adleman, J. R.; Lerner, M. B.; Zhong, Y.-L.; Li, L.-J.; Chen, C.-D.; Wang, K. L. “High-Current Gain Two-Dimensional MoS\textsubscript{2}-Base Ambipolar Hot-Carrier Transistors,” Under Review Process, Nature (2015). K.L.W., Y.W.L., and C.M.T.Jr. conceived the idea and designed the experiments; Y.W.L. and C.M.T.Jr. performed the electrical measurements; L.J.L., J.H.C., Y.L.Z., and C.D.C. synthesized and contributed the materials; C.M.T.Jr. and C.Z. developed the entire fabrication process and fabricated the devices; Y.W.L., C.M.T.Jr., X.K., and K.L.W. analyzed the data. All of the authors discussed the results and wrote the paper together.
VITA

Education

2008 – 2011  Master of Science, Electrical Engineering
  University of California at Los Angeles, Los Angeles, CA United States

2003 – 2008  Bachelor of Science, Electrical Engineering *(Magna Cum Laude)*
  University of Florida, Gainesville, FL United States

2003 – 2008  Bachelor of Arts, Physics *(Cum Laude)*
  University of Florida, Gainesville, FL United States

Honors, Awards, and Distinctions

Department of Defense SMART (Science, Mathematics, and Research for Transformation) Scholarship (2008-2013)

AFCEA (Armed Forces Communications and Electronics Association) STEM Major Graduate Scholarship (2014)

GMiS (Great Minds in STEM) HENAAC (Hispanic Engineer National Achievement Awards Corporation) Scholarship (2014)

Research Experience

Advanced Photonic Technologies Branch, Space and Naval Warfare Systems Center Pacific (SPAWAR)

The Molecular Foundry, Lawrence Berkeley National Laboratory (LBNL)

Center for Nanoscale Science and Technology, National Institute of Standards and Technology (NIST)
  Summer 2008.

Device Research Laboratory, UCLA Department of Electrical Engineering
  August 2008 – present.

Publications

Journal (* co-first author/corresponding author):


Conference


3. Xu, G., Torres Jr., C. M. et al., DRC (Device Research Conference) 2010, “Nanowire-Mask Based Fabrication of High Mobility and Low Noise Graphene Nanoribbon Short-Channel Field-Effect Transistors,” poster session, South Bend, IN (June 2010).


Chapter 1

Introduction

1.1 The Advent of 2D van der Waals (2D vdW) Materials and their Heterostructures

The recent advent of 2D van der Waals (2D vdW) materials, such as graphene\textsuperscript{1–3} and the transition metal dichalcogenides\textsuperscript{4–6} (TMDs), bestows upon us radically unique building blocks of unit cell thickness from which we can amalgamate into atomic-scale heterostructures\textsuperscript{7} featuring novel optoelectronic phenomena\textsuperscript{8–12} and functionalities\textsuperscript{13} (see Figure 1-1). Since their physical isolation in 2004\textsuperscript{2} and 2005\textsuperscript{14}, semimetallic graphene and other 2D vdW materials, such as the semiconducting TMDs and the insulating hexagonal boron nitride\textsuperscript{15,16}, have ushered in a new era in material science. These 2D crystals feature drastically different electronic band structures in their monolayer forms compared to their bulk counterparts due to quantum confinement effects\textsuperscript{5,9}. Their atomic-scale thicknesses and lack of dangling bonds\textsuperscript{17} allow for the custom-design of atomically-abrupt and clean heterointerfaces without the need for epitaxial growth\textsuperscript{7}. Furthermore, with the recent demonstration of the large-scale growth of high-mobility polycrystalline monolayer TMDs with wafer-scale homogeneity\textsuperscript{18}, it seems that practical applications in transparent and flexible optoelectronics\textsuperscript{19}, amongst other arenas, are just within our reach.
Figure 1-1. Constructing van der Waals heterostructures from 2D crystals. The myriad of currently available 2D crystals allows one to stack them together (e.g. reminiscent of atomic-scale Lego blocks) in various permutations of atomically abrupt heterostructures featuring diverse optoelectronic functionalities.7 [A. K. Geim et al., Nature, 499, 419-425 (2013)]

1.1.1 Electronic Properties of Graphene

Graphene is a two-dimensional single atomic layer of sp²-bonded carbon atoms that are arranged in a honeycomb lattice. The basis of graphene consists of two carbon atoms attached to a hexagonal planar lattice. Each carbon atom in graphene has four valence electrons. Three of the valence electrons (the 2s orbital, 2pₓ orbital, and 2pᵧ orbital) hybridize into sp² orbitals forming a trigonal planar structure consisting of three in-plane covalent carbon-carbon bonds (e.g. σ-bonds). These σ-bonds are responsible for graphene’s two-dimensional structure and its high mechanical strength. The remaining valence electron (2pₓ orbital) for each carbon atom lies out-of-plane and overlaps with the associated 2pₓ orbital of the nearest-neighbor carbon atom forming a π-bond, which accounts for the electronic conduction in graphene17,20.

The electronic band structure of monolayer graphene can be numerically computed via the tight-binding approach, by taking into account the hopping for electrons in the π orbitals of
graphene between the nearest-neighbor carbon atoms and the next-nearest-neighbor carbon atoms. The Hamiltonian for monolayer graphene can be written as:\(^{20}\):

\[
H = -t \sum_{\langle i, j \rangle, \sigma} (a_{\sigma, i}^* b_{\sigma, j} + b_{\sigma, j}^* a_{\sigma, i}) - t' \sum_{\langle\langle i, j \rangle\rangle, \sigma} (a_{\sigma, i}^* a_{\sigma, j} + b_{\sigma, i}^* b_{\sigma, j} + a_{\sigma, j}^* a_{\sigma, i} + b_{\sigma, j}^* b_{\sigma, i})
\]

where \(a_{i,\sigma} (a_{i,\sigma}^*)\) annihilates (creates) an electron with spin \(\sigma\) (\(\sigma = \uparrow, \downarrow\)) on site \(R_i\) on sub-lattice A (an equivalent definition is used for sub-lattice B), \(t\) is the nearest-neighbor hopping energy, and \(t'\) is the next-nearest-neighbor hopping energy. Figure 1-2 shows the electronic band structure of monolayer graphene computed via the tight-binding approach, while accounting for the nearest-neighbor (\(t\)) and the next-nearest-neighbor (\(t'\)) hopping terms in the aforementioned Hamiltonian\(^{20}\).

**Figure 1-2.** Left: The electronic bandstructure of monolayer graphene showcasing its six Dirac points (K, K') at the corners of its hexagonal Brillouin zone. The nearest-neighbor hopping energy is \(t = 2.7\text{eV}\) and the next-nearest-neighbor hopping energy is \(t' = 0.2t\). Right: The zoomed inset displays the peculiar linear energy-momentum (E-k) dispersion relation of monolayer graphene. Note that the conduction band and the valence band touch at each of the Dirac points, which renders graphene semi-metallic.\(^{20}\) [A. H. Castro Neto et al., RMP, 81, 109-162 (2009)]
We now focus on the energy dispersion relation near the Dirac points \((K, K')\) in the hexagonal Brillouin zone and ignore the hopping between the next-nearest-neighbor carbon atoms \((t' = 0)\). In this condition, the energy bands can be approximated as: \(E = \hbar v_F k\), where \(v_F\) is the Fermi velocity, \(\hbar\) is the reduced Planck constant, and \(k\) is the linear momentum of the electrons in graphene relative to the Dirac points. Referring to its band structure, it is evident that graphene is a semi-metal, or similarly a zero-bandgap semiconductor, since its conduction band (e.g. the top cone) and valence band (e.g. the bottom cone) touch at each of its Dirac points. Ignoring any extrinsic doping effects, intrinsic graphene has its Fermi level positioned at its Dirac points (e.g. its Fermi surface reduces to six points in its Brillouin zone\(^{20}\)). That is, the \(\pi\)-band and \(\pi^*\)-band of graphene meet exactly at the Dirac point. Thus, at zero temperature, monolayer graphene’s valence band is completely occupied by electrons while its conduction band is completely unoccupied. Furthermore, graphene features a peculiar linear energy dispersion relation \(E = \hbar v_F k\) in the vicinity of its Dirac points, which drastically differs from the parabolic energy dispersion relation \(E = \frac{\hbar^2 k^2}{2m^*}\) of conventional semiconductors such as silicon and gallium arsenide. Hence, the effective mass \(m^* = \hbar^2 \left(\frac{dE}{dk^2}\right)^{-1}\) of the carriers in monolayer graphene is zero due to its linear energy dispersion in contrast to the constant effective mass in conventional semiconductors with parabolic energy dispersion. As a result, monolayer graphene’s quasi-particles exhibit a constant Fermi velocity of \(v_F = 10^6 \frac{m}{s}\), or \(\frac{c}{300}\), where \(c\) is the speed of light, and is independent of energy and momentum. This is the reason why graphene’s quasi-particles are often referred to as massless Dirac fermions in the vicinity of its Dirac \((K, K')\) points. Finally, the density of states of intrinsic monolayer graphene vanishes at its Dirac points and is given by:
\[ \rho_{Gr}^{2D}(E) = \frac{g_s g_v |E|}{2\pi(hv_F)^2}, \]
where \( g_s = 2 \) is the spin degeneracy, \( g_v = 2 \) is the valley degeneracy, \( E \) is the quasiparticle’s energy, \( h \) is the reduced Planck constant, and \( v_F \) is the Fermi velocity\(^{20}\).

### 1.1.2 Electronic Properties of Transition Metal Dichalcogenides (TMDs)

Monolayers of Transition Metal Dichalcogenides (TMDs) also exhibit the same planar geometry of graphene but their basis consists of three atoms of the form \( MX_2 \), where \( M \) is a transition metal (e.g. Mo, W) surrounded by two chemically-bonded chalcogen atoms \( X \) (e.g. S, Se)\(^{4,5,17}\). In contrast to graphene, the chemical bonds in 2D TMDs feature s-, p-, and d-orbitals and the two M-X bonds stick out of the central 2D plane which contains the transition metal M. Hence, differing from its lattice, the basis of 2D TMDs is not exactly planar. Monolayers of 2D crystals are typically less than 1nm in thickness. Furthermore, in contrast to 3D bulk crystals, pristine 2D crystals do not feature dangling bonds on their surface. In addition, these 2D crystals feature strong in-plane covalent bonds and can be stacked on top of each other to form 3D structures with weak van der Waals interlayer bonding. Figure 1-3 shows the energy band alignment of various 2D crystals with respect to silicon as well as the bandgaps of various 2D monolayer TMDs, which reside in the visible or near-infrared spectral range.
Figure 1-3. Left: Energy band alignments of various 2D vdW crystals. The relative energy band offsets of various 2D crystals are listed. An energy scale with respect to the vacuum level is shown and a monolayer of graphene with zero-band gap features a work function of ~4.5eV. The band gaps of various TMDs reside near or within the visible wavelength range. Right: Electron orbitals of 2D crystals. Note that the conduction and valence band edges of monolayers of graphene and hexagonal boron nitride feature linear combinations s- and p-orbitals, whereas monolayers of TMDs feature d-orbitals near their band edges.[D. Jena, PIEEE, 101, 7, 1585-1602 (2013)]

Molybdenum disulfide, or MoS$_2$, was the first 2D semiconducting TMD physically isolated in 2005 and served as the impetus for investigating various other 2D TMDs. Bulk MoS$_2$ features an indirect bandgap of ~1.2eV, which lies below its direct bandgap, and it consists of stacked van der Waals bonded S-Mo-S units. Each of these units is referred to as a MoS$_2$ monolayer and consists of two hexagonal planes of S atoms sandwiching an intermediate hexagonal plane of Mo atoms coordinated through ionic-covalent interactions with the S atoms in a trigonal prismatic arrangement (see Figure 1-4). Interestingly, MoS$_2$ undergoes a crossover from an indirect-to-direct bandgap as its thickness is reduced from its bulk form to its monolayer form due to perpendicular quantum confinement. Essentially, this causes its indirect bandgap (e.g. in the $\Gamma$-K direction of its hexagonal Brillouin zone) to shift upwards in energy in excess of 0.6eV, which in turn exceeds the direct bandgap located at the K point of the Brillouin zone for the monolayer case (see Figure 1-5). The reason for this is that the out-of-plane effective mass ($m_\perp$) for both electrons and holes at the K point greatly exceed the free electron mass ($m_o$), whereas the out-of-plane effective mass for holes ($m_\perp \sim 0.4m_o$) at the $\Gamma$ point and for electrons around the conduction band minimum
along the Γ-K direction \((m_\perp \sim 0.6m_0)\) are much lighter\(^5\). This results in a large quantum confinement-induced increase of the indirect bandgap \((E_{g^*})\) in the Γ-K direction, whereas the direct bandgap \((E_g)\) remains unaltered. Hence, monolayer MoS\(_2\) features a direct bandgap of \(~1.8\text{eV}\) at the K points of its Brillouin zone and is a promising material for optoelectronic applications\(^5,8,10\). Furthermore, the luminescence quantum yield or efficiency (e.g. number of photons out/number of electrons in) of monolayer MoS\(_2\) was measured\(^5\) to be QE \(~10^{-3}\), which is over \(10^4\) times higher than the measured quantum efficiency for bulk MoS\(_2\).

**Figure 1-4.** 3D Structure of individual monolayers of MoS\(_2\) separated by weak van der Waals interlayer bonding. The thickness of a monolayer of MoS\(_2\) is 0.65nm.\(^6\) [B. Radisavljevic et al., Nature Nano, 6, 147-150 (2011)]
Figure 1-5. Lattice structure and simplified electronic band structure of bulk MoS$_2$. The lowest conduction band (c1) and the highest spin-split valence band (v1, v2) are shown. A and B are the direct bandgap transitions at the K point of the Brillouin zone. I is the indirect bandgap transition along the Γ-K direction of the Brillouin zone. $E_g$ is the direct bandgap for monolayer MoS$_2$ and $E_g'$ is the indirect bandgap for bulk MoS$_2$.\textsuperscript{5} [K. F. Mak \textit{et al.}, PRL, 105, 136805 (2010)]

Similar to the case of MoS$_2$, other TMDs also feature a crossover from an indirect-to-direct bandgap as they reach their monolayer limit. Most of the monolayer TMDs feature direct bandgaps at the K points of the Brillouin zone with magnitudes of 1eV - 2.5eV (e.g. in the visible or near-infrared spectrum). This makes them particularly suitable for optoelectronic applications\textsuperscript{8,10}.

1.2 Emergent Optoelectronic Properties of 2D van der Waals Materials

Ever since its discovery in 2004 by the Manchester group\textsuperscript{2}, graphene has captivated the interest of many researchers and has exploded into all avenues of research\textsuperscript{21} and potential commercial applications\textsuperscript{22} that it has been the subject of the Nobel Prize in Physics of 2010\textsuperscript{23} and continues to be one of the most highly-cited materials in the scientific literature\textsuperscript{24}. However, it has only been since 2008\textsuperscript{25-27} that the optoelectronic, plasmonic, and photonic implications of this intriguing material have become apparent\textsuperscript{28-30}. As a semi-metal, single-layer graphene lacks a bandgap and its Fermi level can be tuned continuously from the valence band (p-type) to the
conduction band (n-type) via the electric field effect due to its low density of states near its Dirac point. These features allow for gate-variable optical transitions in graphene\textsuperscript{26,29,31} by considering the relation between the input photon energy and the graphene Femi level.

In addition, the unique linearly dispersive energy bands in single-layer graphene allow for optical resonances (both absorption\textsuperscript{25} and emission\textsuperscript{32}) across a wider range of frequencies that does not occur for conventional semiconductor materials with parabolic dispersion relation (e.g. linear dispersive energy bands lead to a greater accessible Fourier phase space than parabolic dispersive energy bands per differential energy and momentum in k-space\textsuperscript{33,34}). It was shown that a single layer of graphene absorbs around 2.3\% of normally incident light from the ultra-violet to the infrared regime and features a flat transmission spectrum\textsuperscript{25,27}. More recently, however, attention has turned to the more applicable case of highly p-doping the graphene via electrostatic gating such that it is possible to tune its optical transitions\textsuperscript{26,31,35,36}. This phenomena, which is distinct to graphene, is reminiscent of the electric field effect utilized in solid-state electronic devices. This discovery is based on the band-filling effect\textsuperscript{26,32,34,36}, which is prevalent at photon energies corresponding to optical transitions originating from states near the Fermi surface (e.g. $| 2 E_F | = \hbar \omega$). For instance, if the graphene Fermi energy lies in the valence band and is greater than half of the input photon energy, then the photon will not be absorbed (e.g. it will be transmitted) since there is no available electron in the graphene valence band (e.g. initial quantum state) to be photo-excited into the conduction band (e.g. final quantum state). Since the graphene Fermi level can be continuously tuned and its linearly dispersive energy bands allow for optical transitions across a wide range of energies, this makes graphene a unique single-atomic-layer material in which to study tunable light-matter interactions in the solid-state\textsuperscript{32,36–39}. 
1.2.1 Hot Electron Luminescence in Graphene

Although radiative recombination (e.g. light emission) in intrinsic monolayer graphene is negligible due to the fact that it does not feature a bandgap, in 2011, Chen et al.$^{32}$ discovered that highly p-doped graphene can allow for the emergence of a novel physical mechanism known as hot electron luminescence (HEL)$^{32,40}$, whereby the radiative recombination process becomes non-negligible. By tuning the Fermi level of the graphene via a transparent ion-gel top-gate, C.-F. Chen et al.$^{32}$ showed that photo-excited graphene can indeed be a light emitter depending on the relative p-doping (e.g. Fermi level position in the valence band) with respect to the impinging photon energy. If the Fermi level in graphene resides in the valence band and is slightly less than or equal to half of the impinging photon energy, then there exist available valence electrons which can be promoted to the conduction band of graphene via photo-excitation. This generates an electron-hole pair (EHP), in which the hot electron quickly relaxes down the conduction band of graphene until it reaches an energy equal to half of the photon energy. At this instance and at lower energies in the conduction band, the hot electron can rapidly recombine with the many available empty states (e.g. or holes) in the valence band and emit a red-shifted photon with respect to the energy of the input photon. Figure 1-6 shows the first experimental signature of HEL in monolayer graphene. Specifically, Figure 1-6 shows a 2D contour plot of the measured inelastic light scattering intensity as a function of Stokes Raman redshift and $|2E_F|$, where $|E_F|$ is the Fermi level shift with respect to the Dirac point in monolayer graphene. A 1.58eV ($\lambda = 785$nm) continuous-wave laser photo excited the monolayer graphene as its Fermi level was tuned via a top-gate voltage. A broadband photoluminescence due to HEL exists (green colored region labeled “HL”) from $\sim$1,450cm$^{-1}$ to $\sim$2,000cm$^{-1}$ and for energies between $1\text{eV} < |2E_F| < 1.5\text{eV}$.
Figure 1-6. 2D contour plot of the inelastic light scattering intensity (color scale, arbitrary units) as a function of Stokes Raman redshift (cm$^{-1}$) and 2|E$_F$|, where |E$_F$| is the Fermi level shift (eV) with respect to the Dirac point in monolayer graphene. The evolution of the G and 2D bands of monolayer graphene with electrostatic doping (|E$_F$|) is evident. A broadband HEL spectrum exists (green color, region labeled “HL”) from ~1,450cm$^{-1}$ to ~2,000cm$^{-1}$ and for energies between 1eV < 2|E$_F$| <1.5eV. This was the first experimental signature of hot electron luminescence (HEL) in monolayer graphene via photoexcitation. The excitation was from a 1.58eV ($\lambda$ = 785nm) laser.$^{32}$ [C.-F. Chen et al., Nature, 471, 617-620 (2011)]

Figure 1-7a shows the HEL spectrum at 2|E$_F$| = 1.4eV (e.g. the p-doped monolayer graphene exhibits a Fermi level shift of |E$_F$| = 0.7eV below its Dirac point) and it is clearly characterized by a broadband emission. Its integrated intensity from 1.2eV – 1.4eV is over 100 times stronger than that of phonon Raman scattering$^{32}$. Figure 1-7b shows the effect that electrostatic doping has on the HEL spectrum. Specifically, it shows the normalized luminescence intensity as a function of 2|E$_F$| for three separate photon emission energies (e.g. 1.199eV, 1.283eV, and 1.364eV). It is evident that higher photon emission energies have correspondingly higher onset values for 2|E$_F$|. The peak observed in the HEL spectrum when 2|E$_F$| approaches the laser excitation energy (e.g. 1.58eV) is a result of newly opened dynamic energy relaxation pathways for the photo excited hot carriers in monolayer graphene$^{32}$. This novel dynamic relaxation
pathway characteristic of HEL is depicted in Figure 1-7c. The linear energy dispersion of monolayer graphene near its Dirac point is shown with the Fermi level positioned within the valence band (e.g. p-doped graphene). The red lines and circles correspond to filled states, whereas the green lines and circles indicate empty states. An incident photon generates an electron and a hole (blue arrow), which then relax to the Fermi level via electron-electron and electron-phonon scattering mechanisms. During the relaxation process (dashed arrow), there exists a finite probability that the hot electron can emit a photon (orange arrow), but the final valence band state must be empty for this to occur due to Pauli blocking\textsuperscript{26,32}. This dynamic relaxation pathway (HEL) is allowed when $2|E_F|$ exceeds the light emission energy, which defines the threshold doping level for HEL to occur. This process results in a broadband emission of photons for energies below $2|E_F|$. Hence, luminescence for a particular frequency emerges when $2|E_F|$ approaches the light emission energy and disappears when $2|E_F|$ exceeds the laser excitation energy (e.g. since in this case there are no initial electrons in the valence band to photo excite).

\textbf{Figure 1-7.} Hot electron luminescence in monolayer graphene via photoexcitation.\textsuperscript{32} [C.-F. Chen \textit{et al.}, Nature, 471, 617-620 (2011)]

Furthermore, in 2014, Beams \textit{et al.}\textsuperscript{41} showed that electroluminescence from monolayer graphene is possible by the injection of hot carriers into its conduction band via the quantum
The tunneling process\textsuperscript{42}. Essentially, an electrical bias was applied between the mechanically exfoliated monolayer graphene flake and the scanning tunneling microscope (STM) tip in order to inject hot electrons into the conduction band of the graphene. The electroluminescence was attributed to HEL\textsuperscript{32,40–42} in a similar formulation as explained previously by Chen et al.\textsuperscript{32} Figure 1-8 shows the measured scanning tunneling luminescence (e.g. the monolayer graphene flake emits light) due to HEL and its associated biasing schematic for the graphene flake when hot electrons are injected into the conduction band of graphene (Figure 1-8a, Figure 1-8b) and when holes are injected (Figure 1-8c, Figure1-8d) into the valence band of graphene. Clearly, HEL exists only when hot electrons are injected into the conduction band of graphene since inter-band radiative recombination does not exist for the case of hole injection into the valence band of graphene. Furthermore, the emitted luminescence power is on the order of 0.1fW (10\textsuperscript{-16}W) due to monolayer graphene’s low quantum efficiency\textsuperscript{41} (e.g. electron-to-photon conversion) of \sim 10\textsuperscript{-6}.

**Figure 1-8.** Hot electron luminescence in graphene excited by electron tunneling. Left: Hot electrons tunnel into the conduction band of graphene and emit photons. Right: Holes tunnel into the valence band of graphene and do not emit photons.\textsuperscript{31} [R. Beams et al., Nanotechnology, 25, 055206 (2014)]
Figure 1-9a shows a sketch of the HEL process due to electron tunneling into the conduction band of graphene. The gray shaded area represents the electron energies which can radiatively recombine. Once the hot electrons tunnel into the conduction band of graphene, they relax to the Fermi level via electron-electron and electron-phonon scattering mechanisms$^{30,43,44}$. During the relaxation process (dashed arrow), there exists a finite probability that the hot electron can emit a photon (gray shaded area), but the final valence band state must be empty for this to occur due to Pauli blocking$^{26,32,41}$. It is important to mention that in this experiment, the graphene was heavily p-doped (e.g. its Fermi level with respect to the Dirac point shifted into the valence band by at least 0.5eV) due to the initial contact doping from the ITO underneath it, which has a large work function and thus extracts electrons from graphene. In addition to this initial contact doping, further p-doping in graphene occurs due to band-bending from the STM tip. Figure 1-9b shows the measured HEL spectrum which exists in the visible spectral range due to the high p-doping of the monolayer graphene flake. The peak of the broadband HEL spectrum occurs near 700nm and it exhibits a full width at half-maximum (FWHM) of ~150nm.

Figure 1-9. (a) Sketch of the hot electron luminescence process in graphene when excited by electron tunneling via an STM tip. (b) The measured electroluminescence spectrum of monolayer graphene due to HEL. Graphene emits in this visible spectral range due to the extremely high p-doping condition in this experiment.$^{41}$ [R. Beams et al., Nanotechnology, 25, 055206 (2014)]
1.2.2 Tunable Electronic Band Structures in TMDs with Perpendicular Electric Fields

Besides the fact that monolayer TMDs feature direct band gaps at the K points of their Brillouin zones, several studies have recently proposed that a large electric field perpendicular to the plane of the TMDs could shrink their direct band gaps to some extent due to a giant Stark effect. The motivation behind these studies originated from the 2006 study by McCann which showed that it is possible to induce a bandgap in bilayer graphene with the application of a perpendicular electric field. Essentially, the electric field applied normal to the bilayer graphene plane breaks the inversion symmetry of the bilayer and opens up a bandgap. Furthermore, this gap is reversible and continuously tunable up to 0.25eV.

Figure 1-10 shows density functional theory (DFT) simulation results of how the natural bandgaps in bilayer TMDs (for MoS$_2$, MoSe$_2$, MoTe$_2$, and WS$_2$) can undergo a semiconductor-to-metal transition (e.g. the bandgap can actually close) with the application of large electric fields normal to their plane. The rate of change of bandgap with the applied perpendicular electric field depends upon the interlayer spacing between the particular bilayer TMD. Essentially, the external electric field localizes charge along the direction of the applied electric field, confining charge to atomic planes of the bilayer TMD structure while simultaneously delocalizing charge within these planes. The importance of this finding is that it extends the tunability of bandgaps in 2D materials with perpendicular electric fields from the previous 0.25eV limit of bilayer graphene towards the typical 1eV – 1.5eV bandgaps in bilayer TMDs. Furthermore, a similar bandgap modulation effect with applied perpendicular electric field occurs for monolayer MoS$_2$, although the degree of bandgap shift is considerably less.
Figure 1-10. Tunable bandgaps with applied perpendicular electric fields for various bilayer TMDs.\textsuperscript{47} [A. Ramasubramaniam \textit{et al.}, PRB, 84, 205325 (2011)]

1.3 Hot Electron Transistors (HETs)

Hot electron transistors (HETs) have been investigated and implemented in a variety of material systems ever since their underlying device concept was first proposed in 1960\textsuperscript{51,52}. HETs are promising for high-speed electronic switching due to their short base transit times\textsuperscript{53}. They rely upon the vertical transport of a controlled source of hot electrons and their device structure is reminiscent of the bipolar junction transistor. HETs typically consist of three active regions: the emitter, the base, and the collector. The emitter and base regions are separated by a tunneling potential barrier, whereas the base and the collector regions are separated by an energy filtering potential barrier.

1.3.1 Operational Principle of HETs

The majority carriers of a HET consist of “cold” electrons which are in thermal equilibrium with the lattice temperature, whereas the minority carriers consist of non-equilibrium or “hot” electrons with an effective elevated carrier temperature compared to that of the lattice. The conductivity throughout the various regions of the device such as the emitter, base, and collector
is contributed by the cold electrons, whereas the hot electrons propagate the input signal that is to be amplified. A thin emitter-base tunneling barrier allows for the vertical injection of hot electrons into the base region, whereas the base-collector potential barrier is thick enough to preclude tunneling. Figure 1-11 illustrates the basic operational features for the HET in terms of an energy band diagram.

![Energy Band Diagram](image)

**Figure 1-11.** Energy band diagram of the HET biased in the common-base configuration and with biases applied to the emitter \((V_{EB})\) and the collector \((V_{CB})\). Hot electrons are injected into the base from the emitter via quantum tunneling through a thin tunnel barrier. These hot electrons lose some of their kinetic energy due to various scattering events in the base region. If their kinetic energy is higher than the filter potential barrier height at the base-collector interface, then a portion of these hot electrons will surpass the filter potential barrier and reach the collector. Otherwise, the hot electrons will back-scatter into the base region and contribute to the base current. [C. Zeng, “Graphene-Base Hot-Electron Transistor,” Ph.D. dissertation, University of California, Los Angeles, p. 9, 2014]

Upon applying a base-emitter bias, electrons will tunnel from the emitter to the base region with energies near the Fermi level of the emitter. The reason for this is due to the fact that the electron density exponentially decays for energies above the Fermi level of the emitter in addition to the fact that the tunneling probability also significantly decreases for electrons farther away from the top of the potential barrier. Once in the base region, the hot electrons suffer from various
scattering events\(^5\) (e.g. electron-electron collisions, electron-phonon collisions, electron-impurity collisions) beyond traversing a length greater than the mean free path. The base transit time determines the frequency response of transistors. Since HETs rely on ballistic rather than drift-diffusion carrier transport, they inherently feature very short base transit times and are suitable for high-speed operation.

The switching mechanism (e.g. ON state versus OFF state) of the HET depends upon the input kinetic energy of the injected hot electrons and the filter potential barrier height. When the base-emitter bias (\(V_{BE}\)) is less than the filter potential barrier height (\(\phi_{ce}\)) and a positive bias is applied to the collector with respect to the base (\(V_{CB} > 0\)), then the injected hot electrons that are incident on the base-collector interface will back-scatter to the base region and contribute to the base current (\(I_E = -I_B\)). This condition results in the OFF state of the HET. However, when \(V_{BE}\) exceeds the filter potential barrier height (\(\phi_{ce}\)), a significant portion of the injected hot electrons traverse the base and reach the collector region. Thus, in this condition, a portion of the injected hot electrons contribute to the measured output collector current (\(I_C = -\alpha I_E\)), where \(\alpha\) is defined as the common-base current gain. This condition results in the ON state of the HET.

1.4 Graphene-Base Hot Electron Transistors (GB-HETs)

Graphene Field-Effect Transistors\(^5\) (G-FETs), which implement graphene as the channel region, are not suitable for digital logic applications because graphene lacks a bandgap\(^5\). The zero bandgap in graphene makes it difficult to completely deplete the carriers in the graphene channel and hence the G-FETs cannot be switched off. Their current on/off (\(I_{ON}/I_{OFF}\)) ratio is typically less than 10, which results in large static power consumption. Recently, however, there were a few demonstrations of Graphene-Base Hot Electron Transistors\(^5\) (GB-HETs), whose switching mechanism differs from the G-FETs.
GB-HETs utilize graphene as the base electrode since it is semi-metallic, features a high conductivity, and is a single-atom thick. Graphene’s lack of a bandgap results in a low base series resistance. Furthermore, the atomic-scale thickness of graphene (0.335nm thick) as the base region results in extremely short base transit times and ballistic transport across the base region\(^59\). These experiments\(^57,58\) demonstrated large \(I_{\text{ON}}/I_{\text{OFF}}\) ratios in excess of \(10^4\) since the switching mechanism of the GB-HET relies on both the emitter-base bias (\(V_{\text{BE}}\)) and the filter potential barrier height (\(\Phi_{\text{e}}\)), rather than relying on the bandgap of graphene\(^56\). Unlike G-FETs, GB-HETs could potentially be used for digital logic application\(^60\) due to their large \(I_{\text{ON}}/I_{\text{OFF}}\) ratios. In addition, various simulations of optimized GB-HETs show that cutoff frequencies in the 1-10THz is possible due to the atomically-thin base region\(^61,59,62,63\).

### 1.4.1 Operational Principle of GB-HETs

Figure 1-12 shows the energy band diagram of a GB-HET in both the off-state and the on-state. Hot electrons tunnel from the silicon emitter to the graphene base through a SiO\(_2\) tunneling barrier. When operated in the off-state, the base-emitter bias (\(V_{\text{BE}}\)) is small and most of the hot electrons do not have sufficient kinetic energy to surpass the filter barrier. Instead, the hot electrons back-scatter into the base region without contributing to the collector current. When operated in the on-state, \(V_{\text{BE}}\) is large enough and the hot electrons have sufficient kinetic energy to surpass the filter barrier and contribute to the collector current. Hence, the switching mechanism is determined by raising or lowering the filter potential barrier with the application of a collector-base voltage (\(V_{\text{CB}}\)).
1.4.2. The Current Status and Limitations of GB-HETs

Although GB-HETs and related vertical transport devices\textsuperscript{60} have recently garnered much attention due to their potential for digital logic and high-frequency applications, most of these studies have been purely theoretical\textsuperscript{59,61–63}. To this date, there are only a few experimental groups in the world who have demonstrated and reported the DC characterization of GB-HETs\textsuperscript{57,58}. We are one of those groups\textsuperscript{58}. As of recently, only GB-HETs implementing graphene as the base and either Al\textsubscript{2}O\textsubscript{3} or HfO\textsubscript{2} as the filter barrier dielectric have been reported. However, there exist several limitations to GB-HETs which must first be circumvented in order to then pursue their potential in high-frequency operations.

The main limitations GB-HETs currently face are that they feature large filter potential barrier heights (e.g. $\Delta c > 2$eV), very low collector current values (e.g. $J_c < 5$μAcm$^{-2}$), very poor common-base current gain values (e.g. $\alpha < 0.1$), and unipolar transport\textsuperscript{57,58}. Figure 1-13 shows

\textbf{Figure 1-12.} Left: Energy band diagram of the GB-HET in the off-state. The injected hot electrons do not have sufficient kinetic energy to surpass the filter barrier and are back-scattered into the base region. Right: Energy band diagram of the GB-HET in the on-state. The injected hot electrons have sufficient kinetic energy to surpass the filter barrier and reach the collector region.\textsuperscript{58} [C. Zeng, \textit{et al.}, \textit{Nano Letters}, 13, 2370-2375 (2013)]

[Image of energy band diagrams]
the energy band diagrams of two of our GB-HETs. The energy band diagram on the left shows the GB-HET with a graphene base and Al₂O₃ as the filter barrier dielectric. This combination presents a filter barrier height of \( \Delta_e = 3.3\text{eV} \) to the injected hot electrons. The energy band diagram on the right shows the GB-HET with a graphene base and HfO₂ as the filter barrier dielectric. This combination presents a filter barrier height of \( \Delta_e = 2.05\text{eV} \) to the injected hot electrons.

Since the transmission probability of hot electrons through a potential barrier depends exponentially on the filter potential barrier height\(^{64} \), these relatively large filter barrier heights act as an impediment towards achieving both a larger collector current and higher common-base current gain (\( \alpha \)) in our devices. Both the graphene/Al₂O₃ and the graphene/HfO₂ GB-HETs feature very low current gains in the range \( 10^{-3} < \alpha < 10^{-1} \). Hence, we decided to fabricate a HET with a lower filter barrier height by choosing a proper 2D vdW material/filter barrier oxide combination, and test whether this would improve the measured current gain. We chose to implement MoS₂ as the base and HfO₂ as the filter barrier dielectric, which results in a filter barrier height (e.g. conduction band offset) of \( \Delta_e = 1.52\text{eV} \). This indeed resulted in a high current gain for the MoS₂-Base HET (e.g. MB-HET).

Figure 1-14 shows the common-base current gain (\( \alpha \)) as a function of the filter barrier heights. The experimentally measured values of \( \alpha \) for various HETs with different combinations of 2D vdW material/filter barrier oxide is plotted in log-scale as a function of the calculated filter potential barrier heights (e.g. conduction band offsets). Indeed, we measured much higher current gain values in our MB-HETs compared to our GB-HETs, with values typically reaching up to \( \alpha \sim 0.9 \). It is worth mentioning that in order to further improve the
HET performance, we could also pursue fabricating a HET based on WSe$_2$/HfO$_2$, which would feature an even smaller filter barrier height of $\Delta_e \sim 1$eV.

Figure 1-13. Energy band diagrams showing the different filter potential barrier heights for two different GB-HETs. Left: Graphene is the base and Al$_2$O$_3$ is the filter barrier oxide. The filter barrier height in this system is $\Delta_e = 3.3$eV. Right: Graphene is the base and HfO$_2$ is the filter barrier oxide. The filter barrier height in this system is $\Delta_e = 2.05$eV.$^{58}$ [C. Zeng,…, C. M. Torres Jr. et al., Nano Letters, 13, 2370-2375 (2013)]

Figure 1-14. Common-base current gain ($\alpha$) as a function of filter barrier height. The experimentally measured values of $\alpha$ for various HETs with different combinations of 2D vdW material/filter barrier oxide is plotted in log-scale as a function of the calculated filter potential barrier heights (e.g. conduction band offsets). The transmission probability of the hot electrons, and hence $\alpha$, exponentially depends on the filter potential barrier height.
1.5 Synopsis

This dissertation covers various novel device concepts (e.g. electronics and optoelectronics) that are essentially all based on the same device structure. This 2D vdW material-based multifunctional device platform can be utilized either as an ambipolar hot carrier transistor (2D vdW-AHCT) or as a wavelength-agile light-emitting transistor (2D vdW-LET). Although this dissertation only focuses on monolayer graphene and monolayer MoS$_2$, there exist a myriad of other 2D vdW materials which can be transferred onto this device structure and investigated in the near future.

Chapter 2 presents the detailed fabrication process flow of this 2D vdW-AHCT/LET device platform. Either CVD monolayer graphene or CVD monolayer MoS$_2$ was transferred onto a particular substrate during the fabrication process.

Chapter 3 describes the MoS$_2$-Base Ambipolar Hot Carrier Transistor (MoS$_2$-AHCT). We introduce the motivation for the MoS$_2$-AHCT and then proceed with presenting its device structure and its principle of operation by making use of energy band diagrams. Afterwards, its electrical (current-voltage) characteristics are investigated and it will be shown that by choosing MoS$_2$ and HfO$_2$ for the filter barrier interface in addition to implementing a non-crystalline semiconductor such as ITO for the collector electrode, we can simultaneously achieve a novel ambipolar transport, an unprecedentedly high and voltage-tunable current gain ($\alpha \sim 0.95, \beta > 15$), and a voltage-tunable recombination current in the base region of MoS$_2$. Furthermore, depending upon the collector electrode’s bias polarity, either a hot electron mode of operation or a hole mode of operation dominates the transport mechanism of the MoS$_2$-AHCTs.

Chapter 4 introduces the concept of 2D vdW wavelength-agile light-emitting transistors (2D vdW-LETs) in terms of two independently proposed and ongoing research projects.
commence with the Graphene Broadband Infrared Light-Emitting Transistor (GBILET) which relies on hot electron luminescence to enable light-emission from graphene -- a material with no bandgap. The GBILET is expected to emit broadband near-infrared (NIR) light near the $\lambda = 1.55\mu$m telecommunications spectral range with peak intensity in the pico-watt regime. Furthermore, the top-gate voltage should allow for the in-situ tuning of the peak NIR light emission wavelength. We present the device structure and its principle of operation by making use of energy band diagrams. Afterwards, its preliminary electrical (current-voltage) characteristics are investigated and this concludes the current status of the GBILET project. Then, we proceed with the MoS$_2$-Visible Light-Emitting Transistor (MoS$_2$-VLET) which also relies on hot electron luminescence for light emission at $\lambda = 689$nm (e.g. the direct bandgap of monolayer MoS$_2$ is 1.8eV). However, this device concept also relies on the fact that a perpendicular electric field via a gate-voltage can slightly shrink the direct bandgap of monolayer MoS$_2$ and hence tune the wavelength of the emitted photons in the visible range. We present the device structure and its principle of operation by making use of energy band diagrams. Afterwards, its electrical (current-voltage) characteristics are investigated and this concludes the current status of the MoS$_2$-VLET project.

Finally, we conclude the dissertation and propose suggested future works.
Chapter 2

Fabrication of 2D vdW-AHCTs and LETs

In this chapter, the complete fabrication process flow is presented for the 2D vdW material-based multi-functional device structure which will later function as either a 2D vdW-AHCT or 2D vdW-LET. Certain fabrication process steps, such as the CVD transfer of different 2D vdW materials or the deposition of either a thin semi-transparent metal top-gate electrode or a transparent ITO top-gate electrode, will differ depending upon the desired outcome/research project. A clear indication of these particular process steps will be provided in their sub-headings. However, the overall fabrication process flow is mostly the same for either 2D vdW-AHCTs or 2D vdW-LETs. Schematics (both cross-sectional view and top-view) are provided for the main fabrication process steps. The left panels show the cross-sectional view of the substrate when sliced along the dotted line which is indicated in the right panels (e.g. top-view). Optical micrographs of the completed devices are shown at the end of this chapter.

2.1 Complete Fabrication Process Flow of 2D vdW-AHCTs and LETs

1. Pre-furnace Clean the 4 inch Silicon Wafer:

We commence the fabrication procedures with a 4 inch (100mm) degenerately doped n++ silicon <100> wafer (Arsenic donor dopant concentration of ~ 1x10¹⁹ cm⁻³). We perform a “pre-furnace clean” on this wafer by dipping it into a Piranha (H₂SO₄:H₂O₂) bath heated to around 90°C for 10 minutes, followed by a 5-cycle dump rinse clean in DI (de-ionized) H₂O bath. This removes any organic residues and contaminants at the surface of the silicon wafer. Then, we dip the silicon wafer into an HF (hydrofluoric acid) bath for 30 seconds, followed by a 5-cycle dump rinse clean in DI H₂O bath. This HF dip removes any native oxide that was present on the silicon wafer.
26

Figure 2-1. Pre-furnace clean the silicon wafer in order to remove its native oxide in preparation for its placement into the oxidation furnace.

2. Grow SiO$_2$ Pad/Buffer Oxide:

The wafer is then dried using a nitrogen blow gun and immediately placed into a Tystar oxidation furnace in order to grow a silicon dioxide (SiO$_2$) pad/buffer oxide of about 50nm. We used a NanoSpec computerized film thickness measurement system to measure the thickness of this SiO$_2$ pad/buffer oxide layer. This pad/buffer oxide will serve as a stress-relieving layer between the silicon substrate underneath and the to-be deposited silicon nitride (Si$_3$N$_4$) layer above since the viscosity of SiO$_2$ decreases at higher temperatures.
Figure 2-2. Grow the pad/buffer oxide in the thermal oxidation furnace as the first step of the LOCOS process.

3. Deposit Si$_3$N$_4$ LOCOS Mask:

The next procedure involves defining a silicon nitride (Si$_3$N$_4$) mask for the LOCOS (LOCal Oxidation of Silicon) process. We take advantage of the LOCOS process in order to isolate the active areas of our arrays of AHCTs/LETs. The LOCOS process allows us to grow a “field oxide (FOX)” consisting of silicon dioxide in certain areas on the silicon wafer in which the silicon-silicon dioxide (Si-SiO$_2$) interface resides at a lower point than the rest of the silicon surface. We first perform a heated Piranha clean followed by a 5-cycle dump rinse clean in DI H$_2$O bath in order to remove any organic residues on the SiO$_2$ pad/buffer oxide surface. Then, we use a STS-MESC PECVD (Plasma Enhanced Chemical Vapor Deposition) Multiplex system from Surface Technology Systems to deposit a Si$_3$N$_4$ layer of about 225nm thickness on top of the 50nm SiO$_2$ pad/buffer oxide layer across the entire surface of the 4 inch silicon wafer.
4. 1st Photolithography – Define Field Oxide:

We proceed with the first photolithography in our AHCT/LET device fabrication process flow. This first photolithography will define various arrays of circular disks of photoresist on top of the Si$_3$N$_4$ layer. These disks will eventually protect the Si$_3$N$_4$ underneath their areas, whereas the regions outside these disks will be dry etched away in order to result in arrays of Si$_3$N$_4$ disks on top of the SiO$_2$ pad/buffer oxide layer across the entire wafer. We place the 4 inch silicon wafer in an HMDS (hexamethyldisilazane) vapor environment for about 15 minutes for adhesion promotion between the to-be spin coated photoresist and the substrate surface. We then spin coat photoresist (AZ 5214) at 4000rpm for 60 seconds. Afterwards, we place the 4 inch silicon wafer on a hotplate in order to bake the photoresist at 100°C for 60 seconds. We then use a Karl Suss MA6 Mask Aligner to expose the photoresist for 20 seconds with an exposure dose of 80mJcm$^{-2}$. After the photoresist is exposed, we develop it in AZ400K:DI H$_2$O (1:4) for 45 seconds, followed by a DI H$_2$O rinse for 60 seconds and then dry the wafer with a nitrogen blow gun. We then use the optical microscope in the yellow room to inspect the quality of the photoresist development.
5. Dry Etching the Si$_3$N$_4$:

We then use a STS-MESC Multiplex AOE (Advanced Oxide Etcher) from Surface Technology Systems to dry etch the Si$_3$N$_4$ which is not covered by the photoresist disks. We prepared control substrates consisting of Si$_3$N$_4$/n$^{++}$ silicon substrates in order to determine the average etch rate of Si$_3$N$_4$ in this AOE system. The average etch rate was found to be 5.2nm per second. Recall that our Si$_3$N$_4$ layer across the entire 4 inch wafer is about 225nm thick. We set the etch time to 60 seconds (expected to etch through 313nm of Si$_3$N$_4$) in order to over-etch through the Si$_3$N$_4$ layer, the SiO$_2$ pad/buffer oxide layer, and reach the silicon surface. Afterwards, we used a NanoSpec film thickness measurement system in order to confirm that the regions that used to be Si$_3$N$_4$ outside of the photoresist disks were completely etched away. Finally, we want to strip the photoresist so that only the Si$_3$N$_4$ disks remain on top of the SiO$_2$ pad/buffer oxide layers across the entire wafer. Hence, we ultra-sonicated the 4 inch silicon wafer in an acetone-filled petri dish for 20 seconds, followed by leaving the 4 inch silicon wafer in a freshly-poured acetone-filled petri dish overnight. The next day, we took the wafer out of the acetone-filled petri dish and rinsed it with an acetone spray bottle, followed by rinsing it with an IPA spray bottle and drying it with a nitrogen blow gun. A Dektak 6 Surface Profile Measuring System was used to measure the step height of a few of the Si$_3$N$_4$ masks/discs. The average step height measured for these two Si$_3$N$_4$ masks/discs were 238nm and 267nm. This step height is consistent with the fact that about 225nm Si$_3$N$_4$ lies on top of about 50nm SiO$_2$ pad/buffer oxide layer with respect to the silicon substrate surface.
Figure 2-4. Dry etch through the silicon nitride, the pad oxide, and into the silicon substrate for the regions of the silicon nitride which are not covered by the photoresist masks (not shown) which were defined during the first photolithography step.

6. Field Oxide (FOX) Growth:

We now focus on growing the thick field oxide (FOX) which serves to isolate the various active areas of the arrays of AHCTs/LETs throughout our 4 inch silicon wafer. We first perform a heated Piranha clean followed by a 5-cycle dump rinse clean in DI H₂O bath in order to remove any organic and/or PMMA residues on the Si₃N₄ and/or SiO₂ pad/buffer oxide surface. We also “pre-furnace cleaned” a new 4 inch silicon wafer (e.g. control substrate) and placed both 4 inch silicon wafers into the Tystar thermal oxidation furnace. The recipe we used was “Wet 1050°C” for 50 minutes and resulted in about 200nm SiO₂ layer. However, we expected to grow around 520nm SiO₂ with these growth parameters. The reason for this discrepancy was that there was an MFS1 Fault error on the Tystar thermal oxidation furnace (e.g. most likely the oxygen source was depleted at some point during the growth). On the following day, we ran the same recipe “Wet 1050°C” for 46 minutes and 25 seconds which resulted in a final FOX thickness of 566nm as determined from the control 4 inch silicon wafer. This step completes the LOCOS process.
Figure 2-5. Grow the field oxide (FOX) in the thermal oxidation furnace to complete the LOCOS process.

Figure 2-6. 4 inch (100 mm) silicon wafer after the SiO₂ field oxide (FOX) growth for device isolation. The figure shows an image of the initial 4 inch (100 mm) silicon wafer after the thick (~560 nm) SiO₂ field oxide was grown via the LOCOS process. Each die features 20 active regions of 2D vdW-AHCTs/LETs.
7. Selective Wet Etching of the Si$_3$N$_4$ Masks:

The next step involves removing the Si$_3$N$_4$ discs which served as masks during the growth of the field oxide (LOCOS process). We used a diamond scriber to cleave the 4 inch silicon wafer into four quadrants. We take one of these quadrants and dip it into Buffered Oxide Etchant [HF:NH$_4$OH] BOE (6:1) for 35 seconds in order to remove any SiO$_2$ that may have grown on top of the Si$_3$N$_4$ discs during the thermal oxidation step. Our motivation for performing this step is due to the fact that hot phosphoric acid (H$_3$PO$_4$) is highly selective towards etching Si$_3$N$_4$ but not so for SiO$_2$. Removing any SiO$_2$ that may have oxidized on top of the Si$_3$N$_4$ masks prior to the introduction of hot phosphoric acid will allow us to etch Si$_3$N$_4$. Then, we rinse the substrate with running DI H$_2$O on a petri dish for 5 minutes and dry it with a nitrogen blow gun. By using a Nano Spec to measure the FOX thickness before and after the 35 second dip in BOE (6:1), we can determine the amount of FOX (SiO$_2$) that was etched during the 35 second dip in BOE (6:1). We had previously prepared control substrates consisting of SiO$_2$ on n$^{++}$ silicon in order to determine the average etch rate of SiO$_2$ in BOE (6:1), which is about 2nm per second. With the Si$_3$N$_4$ discs now exposed to air (e.g. safe to assume that any SiO$_2$ above the Si$_3$N$_4$ discs was all etched away), we place the substrate into a glass beaker container filled with 600mL of 85% concentration phosphoric acid (H$_3$PO$_4$) and heat it to 160$^\circ$C - 165$^\circ$C. Once the temperature is stabilized to 160$^\circ$C, we wait for 1 hour so that the H$_3$PO$_4$ completely etches through all of the Si$_3$N$_4$. We turn off the hotplate and allow the H$_3$PO$_4$ to cool down to room temperature. Afterwards, we take the substrate out of the H$_3$PO$_4$ and place it into a clean petri dish and allow running DI H$_2$O to continually rinse the substrate for 5 minutes, followed by drying it with a nitrogen blow gun. We use a Dektak 6 Surface Profile Measuring System in order to measure the average step height from the SiO$_2$ pad/Buffer oxide or the silicon surface and the top surface of the FOX. A few typical
step heights for substrate G035_Quadrant 4 were 250nm and 297nm. Furthermore, we use a Nano Spec to measure the FOX thickness after the hot phosphoric acid etch. The measured FOX thickness after both the BOE (6:1) 35 second etch and heated H₃PO₄ etch at 160°C - 165°C for 1 hour (steady state) was 435nm for substrate G035_Quadrant 4. Thus, the total FOX etched during both of these wet etch steps was 131nm. Finally, we use a diamond scriber to cleave this “quadrant” substrate into smaller substrate pieces.

Figure 2.7. Selectively wet etch the silicon nitride masks in a heated solution of phosphoric acid.

8. Grow the Tunnel Oxide:

The next step in our AHCT/LET fabrication process flow is growing an ultrathin silicon dioxide (SiO₂) tunneling barrier which will allow us to inject hot electrons from the underlying highly doped n⁺⁺ silicon substrate and into the conduction band of graphene via quantum tunneling. We first dip the substrate in BOE (6:1) for 30 seconds, followed by a 5-cycle dump rinse clean in DI H₂O bath. This step removes any remaining <50nm SiO₂ pad/buffer oxide layer and exposes the underlying silicon substrate surface. We immediately place the substrate into an RTP 610 Rapid Thermal Annealer from Modular Process Technology Corporation in order to avoid any significant growth of native oxide on the freshly exposed silicon surface. We also place a control
n++ silicon substrate piece which was “pre-furnace cleaned” in order to measure the grown tunnel oxide thickness afterwards using an ellipsometer. We used a Type-K thermocouple in direct contact with the backside of a “pre-furnace cleaned” 4 inch n++ silicon wafer (which serves as the substrate holder for our actual and control substrate pieces) in order to monitor the substrate temperature. The following recipe was used to grow our SiO₂ tunnel oxides: Delay = 120 seconds, Ramp 1 = 20 seconds up to 400°C, Ramp 2 = 10 seconds up to 800°C, Steady State = 10 seconds at 800°C, Delay = 120 seconds. Note that immediately before running this recipe, the nitrogen flow line was shut off whereas the oxygen flow line was turned on. Once the 10 second steady state recipe step at 800°C completed, the oxygen flow line was shut off whereas the nitrogen flow line was re-opened. We opened the RTP 610 furnace once the measured temperature was less than 200°C and took out our actual AHCT/LET substrate and the control substrate. We utilized both a Sopra GES5 ellipsometer and an ULVAC ellipsometer to measure the grown tunnel oxide thickness from our SiO₂/n++ silicon control sample. The aforementioned RTP 610 recipe always yielded a SiO₂ tunnel oxide with thickness less than or equal to 3nm.

![Diagram](image)

**Figure 2-8.** Grow the tunnel oxide via the rapid thermal oxidation furnace.
9. Wet Transfer of CVD Graphene Grown on Copper Foil (or CVD MoS$_2$ Grown on Sapphire) onto the Active Regions of the Substrate—This Process Step Will Vary Depending Upon the 2D material used:

**Graphene Scenario:**

Graphene was grown on copper foil using a chemical vapor deposition (CVD) method\(^{65}\). Afterwards, the graphene on copper foil was placed on top of a clean 4 inch silicon wafer. Kapton tape was tightly pressed along the perimeter of the graphene/copper foil in order to harness it onto the silicon wafer. Then, a thin layer of 495 PMMA A5 was spin coated onto the graphene/copper foil. The spin coating recipe used was: step 1) 500 rpm at 100 rpm/sec for 7 seconds, step 2) 1500 rpm at 500 rpm/sec for 60 seconds, and step 3) 0 rpm at 500 rpm/sec. This spin coating procedure resulted in a thin film of PMMA on top of the graphene/copper foil. A razor blade was used to separate the PMMA/graphene/copper foil stack from the silicon wafer. The PMMA/graphene/copper foil stack was then placed in a glass container filled with copper etchant (FeCL$_3$) with the PMMA side of the stack facing up and the PMMA/graphene/copper foil stack floated on the surface of the copper etchant. The copper foil was etched after about 20 to 30 minutes; the exact etching time depends on the thickness of the copper foil. Once the copper was etched away, the graphene on the bottom side remained submerged in the copper etchant while the PMMA on top of it floated on the copper etchant solution. Afterwards, a pre-cleaned SiO$_2$ “fishing” substrate was used to transfer the PMMA/graphene stack into a glass container filled with de-ionized (DI) water in order to rinse off the copper etchant residue that was in contact with the PMMA/graphene stack. After about 10 minutes, the DI water rinsed the PMMA/graphene stack from the copper etchant residue and it was transferred into a different glass container filled with DI water for further rinsing. The process was repeated two more
times, and the target substrate (e.g. the device substrate with the active areas for the 2D vdW-AHCT/LETs) was used to fish the PMMA/graphene stack onto it. The device substrate and the PMMA/graphene film were left to dry in an ambient condition overnight. The following day, the substrate was heated to 150°C for 3 hours in order to promote the adhesion of graphene onto the substrate. Afterwards, the substrate was left in a glass container filled with acetone for at least 2 hours in order to dissolve the PMMA. Then, the substrate was taken out of the acetone-filled container, was gently rinsed with IPA, and was gently dried with a nitrogen gun.

**MoS₂ Scenario:**

MoS₂ was grown directly on a sapphire substrate via a CVD method. We spin coated a layer of PMMA onto the CVD MoS₂/sapphire substrate using a similar procedure as described above for CVD graphene. Then, we placed the PMMA/MoS₂/sapphire substrate onto a hotplate heated to 100°C for 1 minute. Afterwards, we scratched along the edges of the PMMA/MoS₂/sapphire substrate with a tweezer, exposing the underlying sapphire substrate along its perimeter. Then, we submerged the entire substrate into a glass container filled with a fresh solution of KOH at room temperature. After about 30 minutes, the KOH etched away the surface of the sapphire substrate that made direct contact with the CVD MoS₂. Hence, the PMMA/MoS₂ stack was found floating on the surface of the KOH solution. Similar to the aforementioned transfer procedure for CVD graphene, we used a freshly cleaned SiO₂ substrate to “fish” out the PMMA/MoS₂ stack and placed it into a glass container filled with DI H₂O. After about 10 minutes, we used our target substrate to scoop out the PMMA/MoS₂ film onto the device substrate. We let this substrate naturally dry overnight. The following day, we removed the PMMA by submerging the PMMA/CVD MoS₂/substrate in a glass container filled
with acetone for about 2 hours. Then, the substrate was taken out of the acetone-filled container, was gently rinsed with IPA, and was gently dried with a nitrogen gun.

**Figure 2-9.** Transfer the 2D vdW material of choice onto the active regions of the substrate.

10. Evaporate Aluminum Protection Layer:

   Afterwards, we place the substrate with the transferred CVD graphene (or CVD MoS$_2$) into a CHA Mark 40 E-beam Evaporated Metal Deposition chamber. We deposit a 5nm thick aluminum film at a deposition rate of 0.1 angstroms per second in order to protect the CVD graphene (or CVD MoS$_2$) from coming into direct contact with photoresist in future photolithography steps.

11. 2$^{nd}$ Photolithography – Define the Active Area (Etch and Isolate the Graphene or MoS$_2$):

   We proceed with the second photolithography in our AHCT/LET device fabrication process flow. This second photolithography will define circular disc regions of photoresist that will mask and protect the underlying graphene or MoS$_2$ while we dry etch with oxygen plasma the exposed regions of graphene or MoS$_2$. Doing so will result in active regions of graphene or MoS$_2$ circles with diameters slightly larger than the diameters of the circular hot electron injection regions which were defined in the first photolithography step. We place the AHCT/LET substrate in an HMDS
(hexamethyldisilazane) vapor environment for about 15 minutes for adhesion promotion between the to-be spin coated photoresist and the substrate surface. We then spin coat photoresist (AZ 5214) at 4000rpm for 60 seconds. Afterwards, we place the AHCT/LET substrate on a hotplate in order to bake the photoresist at 100°C for 60 seconds. We then use a Karl Suss MA6 Mask Aligner to expose the photoresist for 10 seconds with an exposure dose of 80mJcm². After the photoresist is exposed, we develop it in AZ400K:DI H₂O (1:4) for 45 seconds, followed by a DI H₂O rinse for 60 seconds and drying the wafer with a nitrogen blow gun. We then use the optical microscope in the yellow room to inspect the quality of the photoresist development. Afterwards, we place the AHCT/LET substrate into a Tegal PlasmaLine 515 Photoresist Asher and dry etch the exposed graphene or MoS₂ in oxygen plasma with a forward RF power of 150W for 60 seconds. Finally, we place the AHCT/LET substrate into a freshly-poured acetone petri dish in order to strip the photoresist overnight.

**Figure 2-10.** Etch the 2D vdW material which are not covered by the photoresist masks that were defined during the second photolithography step via oxygen plasma in order to isolate the various devices.
Figure 2-11. Optical micrograph of CVD MoS$_2$ defined over the active region of MoS$_2$-AHCT/LET. The figure shows an optical micrograph of CVD MoS$_2$ which was transferred and subsequently patterned via a photolithography masking step and oxygen plasma etch. The large-area and continuous CVD MoS$_2$ circular region encompasses the entire hot electron injection region (e.g. active area of the MoS$_2$-AHCTs/LETs). This allows for device isolation among various arrays of devices. The MoS$_2$ area of each device is about 8x10$^4$ µm$^2$.

12. Remove the Aluminum protection layer:

The next day, we took the AHCT/LET substrate out of the acetone-filled petri dish and rinsed it with an acetone spray bottle, followed by rinsing it with an IPA spray bottle and drying it with a nitrogen blow gun. We took optical microscope images in the yellow room of the isolated circular graphene or MoS$_2$ areas which were previously defined. Then, we soaked the AHCT/LET substrate in AZ400K:DI H$_2$O (1:4) for 30 seconds, followed by a DI H$_2$O rinse for 60 seconds and drying the wafer with a nitrogen blow gun. This step allowed the potassium ions in the diluted AZ400K to react with and etch away the aluminum protection layer on top of the graphene or MoS$_2$. 

39
13. Evaporate Aluminum Protection Layer:

Afterwards, we place the AHCT/LET substrate into a CHA Mark 40 E-beam Evaporated Metal Deposition chamber. We deposit a 5nm thick aluminum film at a deposition rate of 0.1 angstroms per second in order to protect the graphene or MoS$_2$ from coming into direct contact with photoresist in future photolithography steps.

14. 3rd Photolithography – Define the Base Contacts:

We proceed with the third photolithography in our AHCT/LET device fabrication process flow. This third photolithography will define the base contact regions which connect to the outer perimeter of the circular graphene or MoS$_2$ area defined during the previous photolithography step. We place the AHCT/LET substrate in an HMDS (hexamethyldisilazane) vapor environment for about 15 minutes for adhesion promotion between the to-be spin coated photoresist and the substrate surface. We then spin coat photoresist (AZ 5214) at 4000rpm for 60 seconds. Afterwards, we place the AHCT/LET substrate on a hotplate in order to bake the photoresist at 100°C for 60 seconds. We then use a Karl Suss MA6 Mask Aligner to expose the photoresist for 10 seconds with an exposure dose of 80mJcm$^{-2}$. After the photoresist is exposed, we develop it in AZ400K:DI H$_2$O (1:4) for 45 seconds, followed by a DI H$_2$O rinse for 60 seconds and drying the wafer with a nitrogen blow gun. We then use the optical microscope in the yellow room to inspect the quality of the photoresist development.

15. E-Beam Evaporation of Metal onto Base Contact Regions:

Afterwards, we place the AHCT/LET substrate into a CHA Mark 40 E-beam Evaporated Metal Deposition chamber. We deposit via e-beam a 20nm thick chromium/100nm thick gold film at deposition rates of 0.5 angstroms per second/1 angstroms per second. The thin chromium film
serves as an adhesion layer between the gold and graphene. For the case of MoS$_2$-based ACHT/LETs, we deposit via e-beam a 20nm thick titanium/100nm thick gold film at deposition rates of 0.5 angstroms per second/1 angstroms per second.

**Figure 2-12.** Pattern and deposit the base contacts onto the regions which were defined during the third photolithography step via the e-beam evaporator.

16. **Lift-Off for 3$^{rd}$ Photolithography Step:**

We then place the AHCT/LET substrate into an acetone-filled petri dish to soak for 20 minutes. Then, we rinse the AHCT/LET substrate with an acetone spray bottle to remove any of the photoresist and metal residues that were primarily lifted-off during the pre-20minute lift-off. Finally, we place the AHCT/LET substrate into a freshly-poured acetone petri dish and allow it to soak overnight.

17. **Remove the Aluminum Sacrificial (Protection) Layer:**

The next day, we slightly rinse the AHCT/LET substrate with an acetone spray bottle, followed by slight rinse with an IPA spray bottle, and dry it with a nitrogen blow gun. Now, we are ready to remove the aluminum protection (sacrificial) layer which protected the graphene or MoS$_2$ from coming into direct contact with photoresist residues during the 3$^{rd}$ photolithography step. We place the AHCT/LET substrate into a solution of AZ400K:DI H$_2$O (1:4) for 2 minutes, followed
by a DI H₂O rinse for 60 seconds and drying the substrate with a nitrogen blow gun. We then use the optical microscope in the yellow room to confirm that the 5nm aluminum protection layer was removed. Afterwards, we rinse the substrate with an acetone spray bottle, followed by an IPA spray bottle, and finally dry it using a nitrogen blow gun. Then, we place the AHCT/LET substrate on a hotplate in order to bake it and get rid of any moisture at 100°C for 60 seconds.

18. E-beam Evaporate the Seed Layer for Atomic Layer Deposition of Top-Gate Dielectric:

Now, we are ready to grow the seed layer (either titanium for HfO₂ top-gate dielectric or aluminum for Al₂O₃ top-gate dielectric) for our future growth of top-gate dielectrics via atomic layer deposition (ALD). We place the AHCT/LET substrate into a CHA Mark 40 E-beam Evaporated Metal Deposition chamber. We deposit via e-beam a 1.1nm thick titanium film at a deposition rate of 0.1 angstroms per second. Afterwards, we leave the AHCT/LET substrate exposed to air overnight so that the titanium will oxide.

19. Deposit Top-Gate Dielectric via Atomic Layer Deposition (ALD) System:

The next day, we proceed with the ALD growth of the top-gate dielectric. We place the AHCT/LET substrate and an n³⁺ silicon control substrate into the load-lock tray of the Fiji Thermal Atomic Layer Deposition (ALD) system by Ultratech Cambridge. Note that prior to this, we had “pre-furnace cleaned” a piece of n⁺⁺ silicon substrate to serve as a control sample in order to measure the ALD deposited dielectric thickness via ellipsometer after the ALD growth procedure. Also, note that prior to opening the load-lock, we had heated the Hafnium precursor [Tetrakis(Dimethylamido)Hafnium] bottle (which should be closed) to 75°C for at least 20 minutes. We prefer to grow HfO₂ as a top-gate dielectric because of its larger dielectric constant (ε_HfO₂ ~ 25 whereas ε_Al₂O₃ ~ 9) than Al₂O₃. Once the samples are loaded into the reactor chamber and the system is pumped down, we set the recipe to “Thermal - HfO₂ - 200°C.” We set the
number of cycles to 210. Each cycle consists of a Hafnium precursor pulse of 0.25 second duration, followed by a 15 second Hafnium precursor purge (wait), followed by a H$_2$O pulse of 0.06 second duration, followed by a 15 second H$_2$O purge (wait). We set the appropriate processing conditions for our run as follows: the heater temperature is set to 200°C, the precursor delivery line and precursor manifold are both set to 150°C, and the precursor bottle temperature is already set to 75°C. We wait 10 minutes to allow for temperature stabilization between the substrate and chamber. Then, we open the Hafnium precursor valve and start the recipe. After the process is complete, we close the Hafnium precursor valve and unload the substrates from the load-lock tray. We then measure the thickness of the deposited HfO$_2$ dielectric on the control substrate using both a Sopra GES5 ellipsometer and an ULVAC ellipsometer. The measured thickness for the control substrate corresponding to AHCT/LET substrate G035_Q4_S4B was around 23nm and its refractive index at a wavelength of 633.5nm was around 1.90 for 210 cycles of ALD.

**Figure 2-13.** Deposit the top-gate dielectric (e.g. Al$_2$O$_3$ or HfO$_2$) via atomic layer deposition.
20. 4th Photolithography – Define the Top-Gate Circular Region:

We proceed with the fourth photolithography in our AHCT/LET device fabrication process flow. This fourth photolithography will define the top-gate circular region which will eventually tune the Fermi level of the graphene or MoS$_2$. We place the AHCT/LET substrate in an HMDS (hexamethyldisilazane) vapor environment for about 15 minutes for adhesion promotion between the to-be spin coated photoresist and the substrate surface. We then spin coat photoresist (AZ 5214) at 4000rpm for 60 seconds. Afterwards, we place the AHCT/LET substrate on a hotplate in order to bake the photoresist at 100°C for 60 seconds. We then use a Karl Suss MA6 Mask Aligner to expose the photoresist for 10 seconds with an exposure dose of 80mJcm$^{-2}$. After the photoresist is exposed, we develop it in AZ Developer:DI H$_2$O (1:2) for 3 minutes, followed by a DI H$_2$O rinse for 60 seconds and drying the wafer with a nitrogen blow gun. We then use the optical microscope in the yellow room to inspect the quality of the photoresist development.

21. Descum:

We then place the AHCT/LET substrate into a Tegal PlasmaLine 515 Photoresist Asher in order to descum any photoresist residues by utilizing an oxygen plasma with a forward RF power of 200W for 60 seconds. This step allows for good metal contact via e-beam evaporation or good ITO contact via RF sputtering.

22. E-beam Evaporation of Thin Metal Top-Gate (for Batch 0, 1, and 2) – Implement this process step if a conventional metal collector electrode is desired for the 2D vdW-HET, otherwise skip this step and sputter ITO as the collector electrode instead for the 2D vdW-AHCTs/LETs:
Afterwards, we place the AHCT/LET substrate into a CHA Mark 40 E-beam Evaporated Metal Deposition chamber. We deposit via e-beam a 1nm titanium/5nm platinum layer, which serves as the semi-transparent top-gate, at a deposition rate of 0.1 angstroms per second. We chose platinum as the top-gate since it is an unreactive metal and unlikely to oxidize.

23. RF sputtering of ITO Top-Gate (for Batch 3) – Implement this step for the 2D vdW-AHCTs/LETs:

For Batch 3 AHCT/LETs, we decided to implement ITO, a transparent conducting oxide, as the top-gate material in order to allow the expected light emission from MoS$_2$ to transmit through the ITO. We placed the AHCT/LET substrate into a Denton Discovery 550 Reacted Sputtered Deposition chamber in order to RF sputter a 45nm thick ITO in ambient environment at room temperature. The RF power was set to 50W. Prior to sputtering, a “pre-furnace cleaned” n$^{++}$ silicon control substrate was used to test the average deposition rate of ITO in this chamber. The average deposition rate was found to be around 2.5nm per minute. Hence, we RF sputtered ITO onto our actual AHCT/LET substrates for a total of 18 minutes, which resulted in around 45nm thick ITO.
Figure 2-14. Sputter the ITO onto the top-gate central circular regions which were defined during the fourth photolithography step. ITO is a transparent conducting oxide and serves as the top-gate electrode in our devices.

24. Lift-Off for 4th Photolithography Step:

We then place the AHCT/LET substrate into an acetone-filled petri dish to soak for 20 minutes. Then, we rinse the AHCT/LET substrate with an acetone spray bottle to remove any of the photoresist and metal residues that were primarily lifted-off during the pre-20minute lift-off. Afterwards, we place the AHCT/LET substrate into a freshly-poured acetone petri dish and ultrasonicate it for 5 seconds. Finally, we allow it to soak in the acetone petri dish overnight.

25. 5th Photolithography – Collector Side Pad Gates:

We proceed with the fifth and final photolithography in our AHCT/LET device fabrication process flow. This fifth photolithography will define the collector side pad gates which will contact the top-gate circular region that was defined during the 4th photolithography step. We place the AHCT/LET substrate in an HMDS (hexamethyldisilazane) vapor environment for about 15 minutes for adhesion promotion between the to-be spin coated photoresist and the substrate surface. We then spin coat photoresist (AZ 5214) at 4000rpm for 60 seconds. Afterwards, we place the AHCT/LET substrate on a hotplate in order to bake the photoresist at 100°C for 60
seconds. We then use a Karl Suss MA6 Mask Aligner to expose the photoresist for 10 seconds with an exposure dose of 80mJcm$^{-2}$. After the photoresist is exposed, we develop it in AZ Developer:DI H$_2$O (1:2) for 3 minutes, followed by a DI H$_2$O rinse for 60 seconds and drying the wafer with a nitrogen blow gun. We then use the optical microscope in the yellow room to inspect the quality of the photoresist development.

26. Back Contact:

We then use a diamond scribe to scratch deeply into the n$^{++}$ silicon substrate on the outer perimeter of the AHCT/LET substrate, followed by rinsing it with DI H$_2$O and drying it with a nitrogen blow gun.

27. E-beam Evaporation of Collector Side Pad Gates:

Afterwards, we place the AHCT/LET substrate into a CHA Mark 40 E-beam Evaporated Metal Deposition chamber. We deposit via e-beam a 150nm aluminum/50nm gold metal stack, which makes contact to the circular thin top-gate region, at a deposition rate of 1 angstroms per second. The 50nm gold allows for good contact when wire-bonding these particular collector side pad gates to a DIP (dual in-line package) mount in the future.
Figure 2-15. Pattern and deposit the collector side gates onto the regions which were defined during the fifth photolithography step via the e-beam evaporator. These metallic side gates make intimate contact with the central ITO top-gate electrode and allow easy access towards probing of the devices.

28. Lift-Off for 5th Photolithography Step:

We then place the AHCT/LET substrate into an acetone-filled petri dish to soak for 20 minutes. Then, we rinse the AHCT/LET substrate with an acetone spray bottle to remove any of the photoresist and metal residues that were primarily lifted-off during the pre-20minute lift-off. Afterwards, we place the AHCT/LET substrate into a freshly-poured acetone petri dish and allow it to soak overnight. The following day, we rinse the AHCT/LET substrate with an acetone spray bottle, followed by an IPA spray bottle, and dry it using a nitrogen blow gun.

This completes the AHCT/LET device fabrication process flow. The following figures show optical micrographs of the completed device structures.
Figure 2-16. Optical image of various fabricated arrays of MoS$_2$-AHCTs. The figure shows an optical image of a silicon substrate with various arrays of MoS$_2$-AHCTs after the fabrication process was completed.

Figure 2-17. Optical micrograph (10X objective lens) of a GB-HET with a thin semi-transparent metal top-gate. The white dashed circle encompasses the perimeter of the CVD graphene. The scale bar is 100µm.
Figure 2-18. Optical micrograph (20X objective lens) of a GB-HET with a thin semi-transparent metal top-gate. The white dashed circle encompasses the perimeter of the CVD graphene. The scale bar is 50µm.
Figure 2.19. Optical micrograph (50X objective lens) of a GB-HET with a thin semi-transparent metal top-gate. The scale bar is 20µm.
Chapter 3

The MoS₂-Base Ambipolar Hot Carrier Transistor (MoS₂-AHCT)

The vertical transport of non-equilibrium charge carriers through semiconductor heterostructures has led to milestones in electronics with the development of the hot electron transistor. Recently, significant advances have been made with atomically-sharp heterostructures implementing various two-dimensional materials. Although graphene-base hot electron transistors show great promise for electronic switching at terahertz frequencies, they are limited by their low current gain and unipolar transport.

Here we show that by choosing MoS₂ and HfO₂ for the filter barrier interface and using a non-crystalline semiconductor such as ITO for the collector, we can simultaneously achieve high-current gain (α ~ 0.95, β > 15) and ambipolar transport in our novel vertical ambipolar hot carrier transistors operating at room temperature. Furthermore, the current gain can be tuned over two orders of magnitude with the collector-base voltage. We anticipate our transistors will pave the way towards the realization of novel flexible 2D material-based high-density, low-energy, and high-frequency hot carrier electronic applications.

3.1 Introduction and Motivation for the MoS₂-AHCT

For over half a century, Moore’s law has driven the silicon electronics industry towards smaller and faster transistors. However, as the scaling limit of silicon Complementary Metal-Oxide-Semiconductor (CMOS) technology draws to an end, novel materials and device concepts have been eagerly sought out and investigated with hopes to augment the next generation of information processing. One promising device concept is the hot electron transistor (HET), which relies on the vertical transport of a controlled source of hot electrons. Ever since
Mead first proposed this device concept in 1960\textsuperscript{51,52}, there have been plethora of HET variants implementing diverse material systems\textsuperscript{51-53,71-74}.

Usually, these HETs feature substantial current gain ($\alpha \sim 0.75$) at cryogenic temperatures ($T = 4.2$ K) but very poor current gain at room temperature\textsuperscript{53,71}. Only a few HETs have shown high current gain ($\alpha \sim 0.9$) at room temperature\textsuperscript{73,74}, but rely on precise yet complicated epitaxial layered structures grown by molecular beam epitaxy (MBE). HETs implementing two-dimensional (2D) materials\textsuperscript{2,7,14}, such as graphene\textsuperscript{2,75,76}, in the base region\textsuperscript{57,59,60} have recently shown great promise for ultra-high frequency operation with intrinsic cutoff frequencies in the 1-10 THz range\textsuperscript{59,61-63,77-79}. These vertical transport three-terminal electronic devices can be designed with atomically sharp heterostructures by the stacking of various van der Waals materials\textsuperscript{7}. This allows one to play with the conduction and valence band offsets\textsuperscript{80} which determine the potential landscape experienced by hot carriers and ultimately the device performance\textsuperscript{81}.

Until now, only vertical graphene-base hot electron transistors have been experimentally demonstrated\textsuperscript{57,58}, yet their transport characteristics feature a significantly low common-base current gain ($\alpha \sim 10^{-2}$) and unipolar transport. These shortcomings prevent the fulfillment of realizing 2D vertical hot carrier transistors operating at THz frequencies. To surmount these obstacles, we propose and demonstrate a novel device concept. In this chapter, we demonstrate a novel vertical Ambipolar Hot Carrier (e.g. hot electron and hole) Transistor (AHCT) incorporating single-layer MoS$_2$\textsuperscript{5,6,8} in the base region (MoS$_2$-AHCT). To the best of our knowledge, all previous vertical transport transistors based on 2D materials implemented a metal for the collector electrode and exhibited unipolar transport with an extremely low gain.

In this work, by utilizing a non-crystalline semiconductor such as ITO (an n-type transparent conducting oxide) as the collector electrode\textsuperscript{68-70}, we demonstrate for the first time that ambipolar
transport due to hot electrons as well as holes can contribute to an overall improved device performance and functionality. The use of a non-crystalline collector electrode eliminates the need for rigid crystalline substrates and allows for potential applications in flexible electronics. Furthermore, the MoS$_2$-AHCTs operate at room temperature and exhibit a high common-base current gain ($\alpha \sim 0.95$) over the entire base-emitter bias ($V_{BE}$) range, which can be dynamically tuned greater than two orders of magnitude by varying the collector-base voltage ($V_{CB}$).

3.2 Device Structure for the MoS$_2$-AHCT

The device structure and schematic of the MoS$_2$-AHCTs are introduced in Figure 3-1. An isometric view of the MoS$_2$-AHCT device structure is shown in Figure 3-1a and a cross-sectional view of its vertical heterostructure active region is depicted in Figure 3-1b. The three-terminal device consists of a degenerately-doped n$^{++}$ silicon substrate ($N_D \sim 10^{19} \text{cm}^{-3}$) as the emitter (E), a monolayer of chemical vapor deposition (CVD) grown MoS$_2$ as the base (B), and sputtered (~45 nm) ITO as the collector (C). A thermally grown thin (~3 nm) SiO$_2$ tunnel barrier separates the emitter and base terminals, whereas an atomic-layer deposited (~55 nm) HfO$_2$ separates the base and collector and serves as the filtering barrier.

In this fabrication process, arrays of MoS$_2$-AHCT devices are isolated from each other via a thick (~300 nm) SiO$_2$ field oxide. The underlying silicon surface which is not covered by the thick SiO$_2$ field oxide, but rather surrounded by it, serves to confine the current into the emitter region of the device for hot electron injection through the SiO$_2$ tunnel barrier (see Figure 3-2). Accordingly, the fabrication process was designed to be compatible with silicon CMOS technology. An optical micrograph of an actual MoS$_2$-AHCT (top-view) is presented in Figure 3-1c.
In this particular study, a common-base configuration was employed during the electrical measurements and the biasing circuit incorporating the schematic symbol for the MoS\textsubscript{2}-AHCT device is shown in Figure 3-1d. Note that both of the base contacts are grounded during the electrical measurements in order to achieve a uniform potential distribution across the MoS\textsubscript{2} base region. A common-emitter configuration was also employed during the electrical measurements for a few devices in order to confirm the consistent high-current gain results presented in this work. Figure 3-3 shows the electrical biasing schematics of the MoS\textsubscript{2}-AHCTs for both the common-base and common-emitter configurations.

The electrical measurements were performed with a Keithley 4200 Semiconductor Characterization System. All measurements were performed in air and at 300K. The leakage current was subtracted for all of the data presented in the main text. Specifically, the base-collector (emitter-collector) leakage current when I\textsubscript{E} = 0 (I\textsubscript{B} = 0) was subtracted from the measured collector current when biased in the common-base (common-emitter) configuration\textsuperscript{74}. 


Figure 3-1. Device structure and schematic of the MoS$_2$-AHCT.  a) An isometric view of an MoS$_2$-AHCT device structure.  The capital letters E, B, and C represent the emitter, base, and collector, respectively.  

b) Cross-sectional view of the vertical heterostructure active region with single-layer MoS$_2$ (0.65 nm) as the base.  ITO (~45 nm) serves as the collector electrode and an n$^{++}$ silicon substrate is used as the emitter.  A thin SiO$_2$ (~3 nm) tunnel barrier is utilized for hot electron injection and HfO$_2$ (~55 nm) serves as the filtering barrier.  The hot electrons injected from the emitter (red arrows) are schematically shown.  
c) Optical micrograph (top-view) of an actual MoS$_2$-AHCT device.  The scale bar is 100 μm.  The dashed circle outlines the MoS$_2$ region.  
d) Common-base configuration circuit incorporating the schematic symbol for the MoS$_2$-AHCT device.
A current confinement scheme was implemented during the design of the fabrication process in order to confine the hot electron emitter current (originating from the n" silicon substrate) to an area slightly smaller than the collector top-gate region (ITO). This enables a uniform current density across the vertical active region of the MoS$_2$-AHCTs. Specifically, a ~300 nm thick SiO$_2$ field oxide, grown via the LOCOS process, isolates each of the active emitter injection regions of the MoS$_2$-AHCTs and hence each of the devices. The active emitter injection regions range in area from $6.4 \times 10^3 \, \mu m^2$ to $4.5 \times 10^4 \, \mu m^2$.

3.3 Energy Band Diagrams for the MoS$_2$-AHCT

In order to clearly understand the physics, we first focus on describing the various modes of operation for the MoS$_2$-AHCTs using energy band diagrams. The flat band condition is shown in Figure 3-4a. The conduction band offset between the monolayer MoS$_2$ and HfO$_2$ is 1.52 eV. This forms the filter potential barrier height ($\Delta e$) for the hot electrons. The filter potential barrier
height and width at the collector-base junction are important parameters that determine the collector current after the hot electrons tunnel through the 3 nm SiO$_2$ emitter-base tunnel barrier. In the previous graphene-base hot electron transistors$^{57,58}$, the filter barrier height between graphene and Al$_2$O$_3$ was 3.3 eV$^{57,58}$, whereas between graphene and HfO$_2$ it was 2.05 eV$^{58}$. In both prior cases, the filter barrier heights are greater than that between MoS$_2$ and HfO$_2$ (1.52eV), thus an improvement of the ratio, in our case, between the collector current and the emitter current ($\alpha = \frac{I_C}{I_E}$) is expected.

In general, the potential barrier height, the potential barrier width, and the strength of the applied electric field are key parameters that determine the tunneling current across a tunnel junction$^{13,19,64}$. The tunneling current across a tunnel junction is generally described by$^{13,19,64}$:

$$I(V) \propto \int dE \cdot \rho_1(E) \cdot \rho_2(E - eV) \cdot [f(E - eV) - f(E)] \cdot T(E)$$

(1)

where $f(E)$ is the Fermi distribution function, $\rho_1(E)$ is the density of states of the first electrode, $\rho_2(E)$ is the density of states of the second electrode, and $T(E)$ is the transmission probability which, for the MoS$_2$-AHCT device structure, is dominated by its exponential sensitivity to the barrier height$^{19}$ ($\Delta$) as opposed to the tunneling density of states$^{13}$. $T(E)$ depends on the energy $E$ of the tunneling electrons as follows:

$$T(E) \sim e^{-W(E)}$$

(2)

where $W(E)$ is related to the effective width and height of the potential barrier and strongly depends on the strength of the electric field. $W(E)$ can be generalized within the WKB approximation$^{13}$:

$$W = 2 \int_0^d dx \cdot \Im k_z(\Delta(x))$$

(3)

Thus, the application of a strong electric field can dramatically alter the shape (e.g. both the effective height and width) of the potential barrier (see Equation 3) and result in an increased collector current.
Moreover, when designing vertical hot carrier transistors\textsuperscript{82,83}, it is paramount to choose the proper combination of 2D material for the base as well as the filtering barrier dielectric which yields the desired conduction band offset\textsuperscript{60} or filter potential barrier height for the hot electrons. Instead of relying on complicated and expensive methods to produce atomically sharp interfaces\textsuperscript{51–53,71–74}, it is now possible to design the equilibrium filter potential barrier height in vertical transport devices by choosing from plethora of 2D materials since the conduction band offset results from material specific parameters such as the electron affinity of the collector-oxide and the work function (e.g. in the case of graphene) or electron affinity (e.g. for all other 2D materials with bandgaps) of the particular 2D material used (recall the energy band alignments of 2D materials shown in Figure 1-3 in Chapter 1).

Having established the significance of the barrier height for the hot electrons (\(\Delta_e\)) in the MoS\(_2\)-AHCTs, we next illustrate the current components governing the device transport. The current components for both the electron contribution (red arrow) and hole contribution (blue arrow) to the total current flow through the MoS\(_2\)-AHCT are shown in Figure 3-4b. The emitter current across the SiO\(_2\) tunnel oxide is due to hot electrons (I\(_E\)) injected from the n\(^{++}\) silicon substrate. Furthermore, the total collector current across the HfO\(_2\) collector-base oxide includes contributions from hot electrons (I\(_C_e\)) and holes (I\(_C_p\)).

Now that the current components and the barrier heights experienced by hot carriers in the MoS\(_2\)-AHCTs have been shown, we proceed to describe the modes of operation of these novel transistors. Figure 3-4c shows the energy band diagram for the off-state condition of the MoS\(_2\)-AHCT. In the absence of an applied V\(_{CB}\), the hot electrons injected through the tunnel oxide have insufficient kinetic energy to overcome the filter barrier at the collector-base junction and do not
reach the collector. Instead, they back-scatter and thermalize into the MoS$_2$ base region. However, the situation drastically changes with the application of a large positive $V_{CB}$.

Figure 3-4d shows the energy band diagram depicting the collector current contributions at the on-state condition of the MoS$_2$-AHCT. There are two possible cases for the on-state condition of the MoS$_2$-AHCTs, depending upon the polarity of the applied $V_{CB}$. The first case describes hot electron dominating behavior and occurs for $V_{CB} > 0$. In this scenario, hot electrons tunneling through the emitter-base tunnel oxide have sufficient kinetic energy to overcome the filter barrier and reach the collector.

The second case describes the hole dominating behavior and occurs for $V_{CB} < 0$. In this scenario, the injected hot electrons do not have sufficient kinetic energy to surpass the raised filter barrier and are scattered back into the MoS$_2$ base region. Subsequently, these electrons recombine with the holes in the HfO$_2$ valence band which forms the electron-hole recombination current and contributes to the total hole current ($I_{Cp}$). The degenerately doped n-type amorphous ITO contact completes the conduction path as its conduction band electrons recombine with the holes in the HfO$_2$ valence band, followed by electron conduction in the n-type ITO. Interestingly, $I_{Cp}$, which is related to the electron-hole recombination rate in the MoS$_2$ base region, can be tuned with the applied $V_{CB}$ in this mode of operation. Thus, by adjusting the polarity of $V_{CB}$, it is possible to operate the MoS$_2$-AHCTs such that their collector current is mainly contributed by either hot electrons or holes.
Figure 3-4. Energy band diagrams for the various operating conditions of the MoS$_2$-AHCTs. a) Flat band condition. Note that the conduction band offset, or the filter barrier height for the hot electrons ($\Delta_e$), between the single-layer MoS$_2$ and the HfO$_2$ is $\Delta_e = 1.52$ eV.  b) The current components are depicted for both electron contribution (red dotted arrow) and hole contribution (blue dotted arrow) to the total current. c) Energy band diagram depicting the off-state condition. Electrons have insufficient kinetic energy to overcome the filter barrier at the collector-base junction and do not reach the collector. d) Energy band diagram depicting the collector current contributions at the on-state condition for two different polarities of the collector-base voltage. For $V_{CB} > 0$ (dashed red lines), the hot electrons tunneling through the emitter-base tunnel barrier have sufficient kinetic energy to overcome the filter barrier and reach the collector, whereas for $V_{CB} < 0$ (dotted blue lines), holes travel from the base to the collector.

3.4 Electrical Characteristics of the MoS$_2$-AHCT

3.4.1 Hot Electron Dominating Mode of Operation of the MoS$_2$-AHCT

Based on the physical concepts just described, the device performance of the MoS$_2$-AHCTs were characterized using the common-base configuration. In the following, we first characterize the MoS$_2$-AHCT in the hot electron dominating mode of operation by applying positive $V_{CB}$. 

61
Figure 3-5a shows the energy band diagram depicting the hot electron dominating mode of operation for the MoS$_2$-AHCT. Specifically, Figure 3-5a shows the conduction and valence band edges at the collector-base junction with a positive $V_{CB}$ applied.

In this mode of operation, once hot electrons tunneling through the emitter-base tunnel barrier have sufficient kinetic energy, they can vertically transport through the MoS$_2$ base region, surpass the filter barrier at the collector-base junction, and reach the collector. Consequently, an increasingly positive $V_{CB}$ will continue to effectively make the filter potential barrier thinner and promote hot electrons reaching the collector due to an increase in their transmission probability. This qualitative behavior is exhibited in the input and transfer characteristics of the MoS$_2$-AHCTs.

3.4.1.i Input and Transfer I-V Characteristics

The input characteristics ($I_E-V_{BE}$) correspond to how the emitter current depends on $V_{BE}$, whereas the transfer characteristics ($I_C-V_{BE}$) correspond to the manner in which the collector current varies with $V_{BE}$. Figure 3-5b shows the input and transfer characteristics for Device 1. In this device, the maximum $V_{BE}$ is limited to 3 V to avoid dielectric breakdown of the tunnel oxide. The emitter current ($I_E$) and the collector current ($I_C$) are shown as a function of $V_{BE}$ ($V_{BE}$ was swept from 0 to +3 V) at a $V_{CB}$ of +1 V. Both currents rapidly increase at larger $V_{BE}$, as is typical for HETs.

Similarly, Figure 3-5c shows a family of transfer characteristics for Device 1 exhibiting a hot electron dominating behavior. The collector current as a function of $V_{BE}$ is shown for various positive $V_{CB}$. It is evident that the collector current increases with increasingly positive $V_{CB}$. This is due to the fact that the filter potential barrier width at the collector-base junction is effectively reduced as the applied $V_{CB}$ becomes more positive. Correspondingly, a greater portion of the injected hot electrons from the emitter have high enough kinetic energy to vertically
transport through the MoS$_2$ base region, surpass the filter barrier, and reach the collector, thus contributing to an increasing collector current.

Furthermore, the reason as to why the transfer characteristics change from sub-linear to linear-like as $V_{CB}$ becomes more positive is explained below. It was previously shown that 2D materials such as graphene weakly screen perpendicular electric fields due to their atomic-scale thicknesses and that an applied electric field can penetrate through the 2D material and cause some band-bending on neighboring oxides$^{13,19}$. Thus, we attribute this change in slope of the transfer characteristics as a direct manifestation of the changing potential barrier shapes and associated transmission probabilities at both the emitter-base junction and the collector-base junction with increasingly positive $V_{CB}$ due to the weak screening by the monolayer MoS$_2$.

### 3.4.1.ii Common-Base Current Gain Characteristics

From the input and transfer characteristics, we can next ascertain the common-base current gain ($\alpha$) of Device 1, which is a figure of merit for HETs and is defined as $\alpha = I_C/I_E$. Figure 3-5d shows $\alpha$ as a function of $V_{BE}$ at $V_{CB} = +8$ V. Interestingly, the current gain, $\alpha$, features a nearly constant characteristic at all $V_{BE}$ with a value of at least 90% for this particular case of $V_{CB} = +8$ V. This implies that even at a low $V_{BE}$, at least 90% of the injected hot electrons ballistically traverse the single-layer MoS$_2$ base region at room temperature. The inset of Figure 3-5d shows a family of $\alpha$ characteristics as a function of $V_{BE}$ at several positive $V_{CB}$ ($V_{CB} = 0, +2, +4, +6,$ and $+8$ V). The current gain, $\alpha$, monotonically increases with positive $V_{CB}$ due to the reduced potential barrier and associated increase in the transmission probability of hot electrons, and exhibits a nearly constant characteristic throughout the entire $V_{BE}$ range with an average magnitude of about 95% at $V_{CB} = +8$ V.
Figure 3.5. MoS₂-AHCT operating in the hot electron dominating mode. a) Energy band diagram depicting the hot electron dominating behavior of the MoS₂-AHCTs. The conduction and valence band edges at the collector-base junction are shown for a positive $V_{CB}$, which reduces the filter barrier for the hot electrons. b) Input and transfer characteristics for Device 1. The emitter current (black diamonds) and the collector current (red circles) are shown as a function of $V_{BE}$ at $V_{CB} = +1$ V. c) Transfer characteristics. The collector current as a function of $V_{BE}$ is shown for various positive $V_{CB}$. d) Common-base current gain ($\alpha$) as a function of $V_{BE}$ at $V_{CB} = +8$ V. The inset shows $\alpha$ as a function of $V_{BE}$ at various positive $V_{CB}$: $V_{CB} = 0, +2, +4, +6$ and $+8$ V.

3.4.2 Hole Dominating Mode of Operation of the MoS₂-AHCT

Shifting from the hot electron dominating mode of the MoS₂-AHCT, we next investigate the device characteristics operated under the hole dominating condition. Figure 3-6a shows the energy band diagram depicting the hole dominating mode of operation for the MoS₂-AHCT. Specifically, Figure 3-6a shows the conduction and valence band edges at the collector-base junction with a negative $V_{CB}$ applied. In this mode of operation, the increasingly negative $V_{CB}$ continues to increase the filter barrier such that the hot electrons which tunnel from the emitter
always have insufficient kinetic energy to reach the collector and thus back-scatter into the MoS$_2$ base region. Consequently, these back-scattered electrons in the MoS$_2$ base region recombine with the holes from the HfO$_2$ valence band.

It is well known that HfO$_2$ features various defect states near its valence band due to oxygen interstitials$^{84,85}$. These oxygen interstitials in the HfO$_2$ dielectric supply holes in the HfO$_2$ valence band. Therefore, we may treat HfO$_2$ as a doped insulator and regard it as a p-type wide-bandgap semiconductor sandwiched between two n-type regions (e.g. the MoS$_2$ base region and the ITO collector region). This electron-hole recombination mechanism in the MoS$_2$ base region forms the electron-hole recombination current and contributes to the total hole current ($I_{Cp}$). Furthermore, the degenerately doped n-type amorphous ITO contact completes the conduction path from the base through the collector barrier and into the ITO contact whose conduction band electrons recombine with the holes from the HfO$_2$ valence band to complete the conduction path to the collector.

Thus, in the hole dominating mode of operation ($V_{CB} < 0$), we define the effective current gain: $\alpha^* = \frac{|I_{Cp}|}{|I_E|}$ as the ratio of the measured collector current to the injected emitter current in the MoS$_2$ base region, where $I_{Cp}$ is defined as the hole current from the base region to the collector region. Interestingly, $I_{Cp}$, which is related to the electron-hole recombination rate, can be tuned with the applied $V_{CB}$ in this mode of operation. Thus, our MoS$_2$-AHCTs, when biased in the hole dominating mode, enable the dynamic control of the recombination rates in the MoS$_2$ by varying $V_{CB}$. This novel functionality may be exploited to investigate and control the recombination dynamics in various 2D materials incorporated into the base region of AHCTs. This qualitative behavior for the hole case is exhibited in the input and transfer characteristics of the MoS$_2$-AHCTs.
3.4.2.i Input and Transfer I-V Characteristics

Figure 3-6b shows the input and transfer characteristics for Device 1 at three different $V_{CB}$ ($V_{CB} = 0$, -8V, and -10 V). It is evident that both the emitter and collector currents increase with larger negative $V_{CB}$. Furthermore, the slopes of both the input and transfer characteristics for the hole case seem to saturate at higher negative $V_{CB}$ and specifically at the highest $V_{BE}$ biases. Similarly, Figure 3-6c shows a family of transfer characteristics for Device 1, exhibiting a hole dominating behavior. The collector current ($I_{Cp}$) as a function of $V_{BE}$ is shown for various negative $V_{CB}$. The apparent current saturation of $I_{Cp}$ with an increasingly negative $V_{CB}$ may be related to the aforementioned electron-hole recombination in the MoS$_2$ base region.

3.4.2.ii Common-Base Current Gain Characteristics

From the input and transfer characteristics, we can next ascertain the effective current gain ($\alpha^*$) of Device 1 for the hole dominant mode of operation. Figure 3-6d shows $\alpha^*$ of Device 1 as a function of $V_{BE}$ at $V_{CB} = -10$ V. Such a large negative $V_{CB}$ significantly raises the filter barrier height for the hot electrons, which causes them to back-scatter into the base region and recombine with holes in the MoS$_2$. This effectively increases the electron-hole recombination current in the base region and hence the measured collector current. Similar to the hot electron dominant case, it is evident that $\alpha^*$ exhibits a nearly constant characteristic at all $V_{BE}$ with a value of at least 90 % for this particular case of $V_{CB} = -10$ V. The inset of Figure 3-6d shows a family of $\alpha^*$ characteristics as a function of $V_{BE}$ at several negative $V_{CB}$ ($V_{CB} = 0$, -4, -6, -8, -9, and -10 V). The effective current gain, $\alpha^*$, increases with negative $V_{CB}$ and exhibits a nearly constant characteristic throughout the entire $V_{BE}$ range with a magnitude of about 94 % at $V_{CB} = -10$ V.
Figure 3.6. MoS$_2$-AHCT operating in the hole dominating mode. a) Energy band diagram depicting
the hole dominating behavior of the MoS$_2$-AHCTs. Holes travel from the base to the collector. The
conduction and valence band edges at the collector-base junction are shown for a negative $V_{CB}$, which raises
the filter barrier for the hot electrons. b) Input and transfer characteristics of Device 1. The emitter
current and the collector current are shown as a function of $V_{BE}$ at $V_{CB} = 0$, -8 and -10 V. c) Transfer
characteristics. The collector current as a function of $V_{BE}$ is shown for $V_{CB}$ from 0 to -10 V with step of -1 V. d) $\alpha$ as a function of $V_{BE}$ at $V_{CB} = -10$ V. The inset shows $\alpha$ as a function of $V_{BE}$ at $V_{CB} = 0$, -4, -6, -8, -9, and -10 V.

3.4.3 Output Characteristics and Tunable Current Gain of the MoS$_2$-AHCT

With the analysis of the input and transfer characteristics complete, we now investigate the
common-base (common-emitter) output characteristics of the MoS$_2$-AHCTs, which correspond to
how the output collector current depends on $V_{CB}$ ($V_{CE}$). Figure 3-7a shows the common-base
output characteristics for Device 2. The collector current is shown as a function of $V_{CB}$ at three
positive $V_{BE}$ biases. The ambipolar transport is evident as the device is biased in either the hot
electron ($V_{CB} > 0$) or the hole ($V_{CB} < 0$) dominant mode of operation. The collector current is
insensitive to modulation below a critical electric field, or correspondingly a $V_{\text{CB}}$ voltage, across the HfO$_2$ collector-base oxide.

However, above a critical electric field across the HfO$_2$, the collector current is quite sensitive to modulation and rapidly increases with a further increase in $V_{\text{CB}}$ for both cases of $V_{\text{CB}} > 0$ and $V_{\text{CB}} < 0$. This behavior can be explained as follows. Above a certain threshold $V_{\text{CB}}$, the electric field can significantly alter the shape of the potential barriers (e.g. $\Delta e$ in Figure 3-4a) in the vertical heterostructure, which include both the emitter-base tunnel barrier and collector-base filter barrier due to the weak screening of MoS$_2$, and thus dramatically increase the transmission probability of either hot electrons ($V_{\text{CB}} > 0$) or holes ($V_{\text{CB}} < 0$) to the collector current. This behavior is reproducible and repeatable in all our fabricated MoS$_2$-AHCTs. Especially, the room temperature common-base current gain ($\alpha$) in this type of novel 2D material-based vertical device is unprecedentedly high for the largest $V_{\text{CB}}$ applied.

In order to convey the robust and ambipolar nature of this high current gain in the MoS$_2$-AHCTs, Figure 3-7b shows a semi-log plot of $\alpha^*$ as a function of $V_{\text{BE}}$ at various negative $V_{\text{CB}}$ for a different device (Device 3) which is biased in the hole dominating mode of operation. The effective current gain, $\alpha^*$, increases with larger negative $V_{\text{CB}}$ as a result of an increase in the electron-hole recombination current in the base region, which promotes hole current from the base region to the collector region and exhibits a nearly constant characteristic with a value of about 80% at $V_{\text{CB}} = -9$ V. It is evident that $\alpha^*$ can be tuned over two orders of magnitude by varying $V_{\text{CB}}$ throughout the entire $V_{\text{BE}}$ bias range. A similar dependence of $\alpha$ on $V_{\text{CB}}$ for the hot electron dominating case exists (see Figure 3-8).

Next, we investigate the MoS$_2$-AHCT characteristics when biased in the common-emitter configuration in order to corroborate the high and tunable current gain we achieved in the common-
base configuration. The Gummel plot is used as a figure of merit when analyzing bipolar transistors. It is a simultaneous semi-log plot of the collector and base currents as a function of the input voltage ($V_{BE}$) at a fixed output voltage ($V_{CE}$). The common-emitter current gain ($\beta = \frac{I_C}{I_B}$) can be ascertained from the Gummel plot by taking the ratio of the collector current to the base current at a fixed $V_{BE}$. Figure 3-7c shows the Gummel plot for Device 1 when biased in the common-emitter configuration and in the hot electron dominating mode of operation ($V_{CE} > 0$). The collector and base currents are shown in log-scale as a function of $V_{BE}$ at a fixed output voltage of $V_{CE} = +10$ V. The Gummel plot confirms the transistor action of the MoS$_2$-AHCT as the input base current is directly amplified to the output collector current.

Finally, Figure 3-7d shows the common-emitter output characteristics for Device 1 in the hot electron dominating mode of operation ($V_{CE} > 0$). The collector current is shown as a function of $V_{CE}$ at three positive $V_{BE}$ biases in addition to $V_{BE} = 0$V. The inset shows the common-emitter current gain ($\beta$) for Device 1 as a function of $V_{CE}$ at $V_{BE} = +2$ V. Current gain is achieved for both the hole mode of operation ($\beta \sim 17$ for $V_{CE} < 0$) as well as the hot electron mode of operation ($\beta \sim 4$ for $V_{CE} > 0$) and it can be tuned with the output voltage $V_{CE}$. Hence, by biasing the MoS$_2$-AHCTs in both the common-base and the common-emitter configurations, we have explicitly shown that the measured current gains ($\alpha$, $\beta$) in either scenario corroborate each other and further attest the high and tunable current gain and the ambipolar transport in our novel transistors.
Figure 3-7. Output characteristics and tunable current gain of the MoS$_2$-AHCT. a) Common-base output characteristics for Device 2. The collector current is shown as a function of $V_{CB}$ at $V_{BE} = +1$ V, +2 V, and +3 V. b) The effective current gain ($\alpha'$) for Device 3 is shown in log scale as a function of $V_{BE}$ at $V_{CB} = 0$ to -9 V in steps of -1 V. c) Gummel plot for Device 1 biased in the common-emitter configuration. The collector and base currents are shown as a function of $V_{BE}$ at a fixed output voltage of $V_{CE} = +10$ V. d) The common-emitter output characteristics for Device 1. The collector current is shown as a function of $V_{CE}$ at $V_{BE} = 0$ V, +1 V, +2 V, and +3 V. The inset shows the common-emitter current gain ($\beta$) for Device 1 as a function of $V_{CE}$ at $V_{BE} = +2$ V. Current gain is achieved for both the hole ($\beta \sim 17$ for $V_{CE} < 0$) and hot electron ($\beta \sim 4$ for $V_{CE} > 0$) modes of operation and it can be tuned with the output voltage $V_{CE}$. 
Figure 3-8. Tunable common-base current gain for Device 3 by varying the polarity of $V_{CB}$. The figure shows both the common-base current gain ($\alpha$) and the effective current gain ($\alpha^*$) for Device 3 in log-scale as a function of $V_{CB}$ for $V_{BE} = +3$ V. Left: In the hole dominating mode of operation ($V_{CB} < 0$), $\alpha^*$ increases with an increasingly negative $V_{CB}$ and can be tuned over two orders of magnitude. This is due to an increase in the electron-hole recombination current with an increasingly negative $V_{CB}$ as more hot electrons which are injected into the base region ($V_{BE} = +3$ V) scatter and recombine with holes in the valence band and contribute to an increased collector current. Right: In the hot electron dominating mode of operation ($V_{CB} > 0$), $\alpha$ increases with an increasingly positive $V_{CB}$ and can be tuned over an order of magnitude since this lowers the filter potential barrier experienced by the hot electrons and allows them to reach the collector.

3.5 Summary

In conclusion, we have demonstrated a novel vertical ambipolar hot carrier transistor incorporating single-layer MoS$_2$ in the base region. This MoS$_2$-AHCT device can operate in either hot electron or hole conducting mode depending upon the particular bias configuration. The MoS$_2$-AHCTs operate at room temperature and exhibit a high common-base current gain $\alpha$ of about 0.95 over the entire $V_{BE}$ bias range, which can be dynamically tuned greater than two orders of magnitude by varying $V_{CB}$. The majority of the fabrication process was designed to be compatible with CMOS technology.
The heterostructure materials used in this work can be extended to other material combinations to further enhance the performance as well as functionalities. By implementing different 2D materials for the emitter-base tunneling barrier (e.g. hexagonal boron nitride), base, and collector on flexible substrates, a new family of flexible hot carrier electronics could emerge. Our results illustrate that MoS₂-AHCTs may pave the way towards the realization of 2D material-based high-density, low-energy, and high-frequency hot carrier complementary transistors (e.g. p-AHCT and n-AHCT) for complementary-logic circuits. Moreover, the MoS₂-AHCTs presented in this work were fabricated from large-area CVD single-layer MoS₂, which promotes the scalability and potential commercialization of such devices.
Chapter 4
Towards 2D vdW Wavelength-Agile Light-Emitting Transistors (2D vdW-LETs)

Disclaimer: Although I included the recent demonstration of the existence of injection
electroluminescence into graphene via the quantum tunneling of hot electrons by R. Beams et
al.\textsuperscript{41} in Chapter 1 of this dissertation, we had actually independently developed a similar device
concept since the start of our graphene light-emission project on November 20, 2012. This
chapter presents the development and current progress of this on-going research project both in
graphene and for other 2D vdW materials. Note that the prior works\textsuperscript{32,41} prove that light emission
from graphene (e.g. a material with no band gap) is possible due to hot electron luminescence (HEL).
C.-F. Chen \textit{et al.}\textsuperscript{32} showed that HEL exists in the near-infrared spectrum. R. Beams \textit{et al.}\textsuperscript{41} showed
that HEL exists in the visible spectrum. Hence, our novelty in this section of the dissertation is to
scale up the contribution from R. Beams \textit{et al.}\textsuperscript{41} towards a practical CMOS-compatible and large-
scale device instead of a single atomic scale and localized light emission via STM tip. Furthermore,
our significant novelty is to tune this light emission wavelength via a top-gate voltage since it was
proven that HEL exists from the visible spectrum\textsuperscript{41} to the near-infrared spectrum\textsuperscript{32}.

4.1 The Graphene Broadband Infrared Light-Emitting Transistor (GBILET)

There is a dire need across the public and private sectors for low-power and ultra-fast switching
technologies. Optoelectronic switching is widely regarded to be one such enabling technology.
Graphene has great potential for optoelectronic functionalities since it supports tunable light
absorption\textsuperscript{26}, broadband plasmonic phenomena\textsuperscript{36–38}, has the capability to allow for electrical
switching at up to terahertz frequencies\textsuperscript{59}, and features broadband emission in the near-infrared\textsuperscript{32}.
However, electrically-induced light emission is a key missing piece that would allow a graphene-
based semiconductor optoelectronics platform for information processing operating in the
commercially relevant infrared telecommunication bands of 1300nm and 1550nm. Demonstration of electrically-tunable hot electron luminescence would constitute a major breakthrough in graphene-silicon optoelectronics.

We propose to design, fabricate, and characterize a novel type of graphene-based light-emitting transistor. Our mission is to be the first group ever to demonstrate voltage-tunable injection electroluminescence (spontaneous emission) of graphene. Although radiative recombination in intrinsic graphene is negligible\textsuperscript{34}, it has been recently shown that highly p-doped graphene can allow for the emergence of a physical mechanism known as hot electron luminescence, whereby the radiative recombination process becomes non-negligible\textsuperscript{32}. This previous report\textsuperscript{32} relied on optically exciting electrons in the graphene devices using a fixed laser energy. However, we seek to observe and demonstrate hot electron luminescence without any laser excitation but rather by tunneling electrons into the conduction band of highly p-doped graphene via applied voltage biases.

Based on preliminary calculations, our current device structure is expected to emit broadband near-infrared (NIR) light near the 1550 nm telecommunications band with peak intensity in the pico-watt regime. Note that this intensity could be increased by several orders of magnitude with future optimization of our device structure, such as increasing the tunneling current density through an optimized tunneling barrier (e.g. MgO, Gd$_2$O$_3$, or monolayer hexagonal boron nitride). In addition, our unique device structure could allow for voltage-controlled tuning of the peak NIR light emission wavelength. The successful demonstration of such a prototypical graphene-based light-emitting transistor could allow for novel CMOS compatible scalable graphene optoelectronic devices and information processing platforms.
4.2 Device Structure of the GBILET

Figure 4-1 shows the basic device structure and operational biasing procedure of our graphene broadband infrared light-emitting transistor (GBILET). The GBILET is a novel optoelectronic light source (e.g. graphene is the active material) with a broadband emission spectrum whose peak value can be tuned by the application of a top-gate voltage. GBILET operates via injection electroluminescence but it is not a diode (e.g. not an LED) and thus an entirely different device concept in itself. It benefits from the band-gap less nature and linear energy dispersion relation of graphene in order to provide a highly wavelength tunable (e.g. wavelength agile) and broadband photon emission spectrum. GBILET exploits hot electron luminescence as a non-negligible radiative recombination pathway whose onset of which can be induced by electrostatic gating in order to tune the graphene Fermi level. GBILET is a dual-gated transistor with a top-gate dielectric (e.g. HfO₂, Al₂O₃, ion-gel, ionic liquid, etc.) and an ultrathin tunneling oxide (e.g. SiO₂, hexagonal boron nitride, MgO, Gd₂O₃, etc.) sandwiching the graphene in between them.

First, an electrostatic potential (V₁) is applied across the top-gate dielectric and graphene in order to induce a Fermi level shift with respect to the graphene Dirac point, which moves the graphene Fermi level deep into the valence band of the graphene. The top-gate electrode material could be an ultrathin semi-transparent metal layer (e.g. 1nm Ti/5nm Pt), a large area (e.g. CVD grown and transferred) graphene layer, or a thicker transparent conducting oxide such as ITO. Then, a non-equilibrium or “hot” carrier distribution of electrons is injected via quantum tunneling through an ultrathin tunneling oxide (e.g. SiO₂, hexagonal boron nitride, MgO, Gd₂O₃, etc.) into the conduction band of graphene. This is accomplished by applying a separate electrostatic potential (V₂) across the underlying degenerately doped n⁺⁺ silicon substrate (e.g. the source of the hot electrons), the tunnel oxide, and the graphene.
Figure 4-1. Basic device structure and operational biasing procedure of a GBILET. A 3D isometric view (top left corner) of the GBILET is rotated counter-clockwise by 90° in order to match the orientation of the device structure (main panel). A negative top-gate voltage bias ($V_1$) is applied in order to shift the Fermi level of graphene into its valence band (e.g. initialize the system). Afterwards, a negative back-gate voltage bias ($V_2$) is applied in order to inject hot electrons (red circles) from the n++ silicon substrate, through a tunneling oxide, and into the conduction band of graphene. As the hot electrons relax via various scattering mechanisms, they can eventually exhibit a finite probability of emitting photons for energies below $2|E_F|$.

4.3 Principle of Operation of the GBILET

Figure 4–2 shows a flowchart of the operational principle of the GBILET, that is, injection hot electron luminescence. Since quantum tunneling is an elastic scattering process, the hot electron energy distribution peaks near the applied $V_2$ (e.g. back-gate electrode) voltage bias and we can assume that this is the initial kinetic energy of hot electrons as they enter the conduction band of the already highly p-doped graphene (e.g. via the top-gate electrode, $V_1$). Once the hot electrons are injected into the graphene conduction band, they start to lose their kinetic energy via various energy relaxation pathways\cite{40,43,44} due to radiative or non-radiative mechanisms. The hot carrier distribution (e.g. described by an elevated effective temperature) can undergo intra-band scattering in the conduction band via electron-electron scattering, the emission of optical phonons,
and eventually the emission of acoustic phonons until the distribution reaches thermal equilibrium with the graphene lattice temperature. The peak value of broadband hot electron luminescence (e.g. peak/cutoff photon emission wavelength) occurs near twice the value of the Fermi level shift with respect to the Dirac point in the graphene (e.g. $2|E_F| = \hbar \omega_{\text{emission}}$).

For hot electrons with energies higher than $2|E_F|$ (e.g. with respect to the Fermi level in the valence band) in the conduction band, there are no available empty valence band states for them to recombine to, hence, there is no light emission. However, for hot electrons in the conduction band at energies below the $2|E_F|$ threshold, there are many available empty valence band states for them to recombine with, and hence light emission is possible. Thus, this voltage-tunable $2|E_F|$ threshold mimics the function of a “tunable band gap” in the sense that electrons in the conduction band recombine with holes in the valence band of graphene itself (e.g. reminiscent to inter-band radiative recombination in materials with a bandgap).
Figure 4-2. Operational principle of the GBILET. The light emission mechanism due to hot electron luminescence (HEL) is explained throughout the flowchart above.

Figure 4-3 shows the energy band diagram of the GBILET in thermal equilibrium. Note that titanium (e.g. adhesion layer) is listed in the band diagram since it makes intimate contact with the top-gate dielectric (e.g. HfO$_2$). Furthermore, the graphene is drawn and assumed to be initially intrinsic (e.g. $E_{\text{Dirac}} = E_{F\text{Graphene}}$) for simplicity. In reality, the graphene will be slightly p-doped due to exposure to the ambience (e.g. O$_2$ and H$_2$O deplete the negative charge carriers from graphene hence making it p-doped).
Figure 4-3. Energy band diagram of the GBILET in thermal equilibrium.

Figure 4-4 shows the energy band diagram of the GBILET with applied top-gate and back-gate negative voltage biases. The band diagram shows a Fermi-level shift in graphene (e.g. $\delta E_F$ in the zoomed-in section) due to the influence of both electric fields across the top-gate and bottom-gate dielectrics in addition to graphene’s quantum capacitance \(^{86-88}\). The Fermi-level shift in graphene due to $V_1$ can be calculated from the equation: 

$$V_1 = \frac{E_{FG}}{e} + \phi_1$$

with

$$\frac{E_{FG}}{e} = \frac{sgn(n)\hbar v_F \sqrt{n}}{e}$$

being determined by the quantum capacitance of graphene, where $E_{FG}$ is the graphene Fermi level, $\hbar$ is the reduced Planck constant, $v_F$ is the Fermi velocity of graphene, $n$ is the carrier concentration in graphene; $\phi_1 = \frac{ne}{C_1}$ is the potential drop across the top-gate dielectric and is determined by the geometrical capacitance $C_1 = \frac{\varepsilon_1 \varepsilon_0}{t_{ox1}}$ of the high-k top-gate dielectric (e.g. HfO$_2$), where $\varepsilon_1$ is the top-gate dielectric constant, $\varepsilon_0$ is the permittivity of free space, and $t_{ox1}$ is the thickness of the top-gate dielectric. A similar expression as above exists for the Fermi-level shift in graphene due to $V_2$. These two-coupled expressions will lead to the overall Fermi-level shift $\delta E_F$ in graphene shown in the zoomed-in section of Figure 4-4. Finally, the red horizontal arrow indicates the input kinetic energy of the injected hot electrons.
from the underlying degenerately doped n++ silicon substrate through the ultra-thin tunneling oxide (e.g. SiO$_2$) and into the graphene conduction band.

![Energy band diagram of the GBILET with applied top-gate and back-gate negative voltage biases.](image)

**Figure 4-4.** Energy band diagram of the GBILET with applied top-gate and back-gate negative voltage biases.

### 4.3.1 Method to Calculate the Luminescence Power of the GBILET

The following method is used to calculate the expected luminescence power emanating from the properly biased GBILET. For our current batch of GBILETs, the maximum tunneling current we can safely inject without fatiguing or breaking the ~3nm SiO$_2$ tunneling oxide is about 500nA (e.g. tunneling current densities up to $10^{-3}$Acm$^{-2}$). In the next batch, we will grow an ultrathin 1.5nm or thinner SiO$_2$ tunneling oxide to achieve safe tunneling current densities up to 50Acm$^{-2}$.
(e.g. 5000 times improvement in tunneling current density was already measured in our new batch of control substrates). Assuming that we constantly inject a tunnel current of \( I_{EB} = 500\text{nA} \) into the graphene conduction band, and using the measured internal quantum efficiency\(^{41} \) of monolayer graphene as \( 10^{-6} \) in our calculations, we arrive at about 3 million photons per second emanating from the GBILET active area. Note that we are calculating for the peak photon energy even though the emission is broadband.

\[
l = \frac{ne}{t} \rightarrow n = \frac{lt}{e} = \frac{(500 \times 10^{-9}A) \cdot (1s)}{(1.602 \times 10^{-19}C)} = 3.1211 \times 10^{12} \text{electrons/sec}
\]

\[
\left(3.1211 \times 10^{12} \text{electrons/sec}\right) \cdot \left(10^{-6} \text{photons/electron}\right) = 3.1211 \times 10^{6} \text{photons/sec}
\]

Our current batch of GBILETs feature a ~55nm thick HfO\(_2\) top-gate dielectric with a measured average dielectric constant \( (\varepsilon) \) of ~ 17 and a corresponding capacitance of \( C_{HfO_2} = 2.8 \times 10^{-7} \frac{F}{cm^2} \). Furthermore, the graphene is unintentionally p-doped by its exposure to the ambient environment and features its Fermi level shifted by ~ 0.2eV below its Dirac point (e.g. inside the valence band). The maximum that we can electrostatically shift the Fermi level of graphene into its valence band (e.g. p-dope) using HfO\(_2\) is \( |E| = 0.5\text{eV} \) for an applied top-gate voltage of \( V_{TG} = -10\text{V} \). Thus, the corresponding maximum energy of the emitted photon from graphene is

\[
2|E| = 2 \cdot (0.5\text{eV}) = 1\text{eV} = \hbar \omega_{emit} \quad \text{and this corresponds to a cutoff photon emission}
\]

wavelength of \( E_{photon} \) (eV) = \( \frac{1.24}{\lambda (\mu m)} \) → \( \lambda_{emit} = \frac{1.24}{\hbar \omega_{emit}} = \frac{1.24}{1\text{eV}} = 1.24\mu m \) when \( V_{TG} = -10\text{V} \).

The power corresponding to this peak photon emission is:

\[
\left(3.1211 \times 10^{6} \text{photons/sec}\right) \cdot \left(1\text{eV/photons}\right) = \left(3.1211 \times 10^{6} \text{eV/sec}\right) \cdot \left(1.602 \times 10^{-19} \frac{J}{eV}\right) = 5 \times 10^{-13}W = 500\text{fW} = 0.5\text{pW}
\]
Thus, when our current batch of GBILETs are biased at $I_{EB} = 500\text{nA}$ and $V_{TG} = -10\text{V}$, the peak of the broadband HEL spectrum should have a power of $0.5\text{pW}$ at a wavelength of $1.24\mu\text{m}$ (e.g. in the near-infrared spectral range).

### 4.3.2 Method to Calculate the Luminescence Cutoff Wavelength of the GBILET

The following method is used to calculate the expected cutoff photon emission wavelength from the properly biased GBILET for a particular top-gate voltage ($V_{TG}$). First, we assume the particular value of the top-gate voltage that we will apply to the GBILET. Then, we solve for the corresponding Fermi level shift, $|E_F|$, (e.g. in eV) into the valence band of graphene due to this $V_{TG}$. Afterwards, we multiply this value by two to get the emitted photon energy:

$$2|E_F| = E_{emission}.$$  

The Fermi-level shift in graphene due to $V_1$ can be calculated from the equation:

$$V_1 = \frac{E_{FG}}{e} + \phi_1 \text{ with } \frac{E_{FG}}{e} = \frac{\text{sgn}(n) \cdot h \nu_F \sqrt{\pi|n|}}{e}$$

being determined by the quantum capacitance of graphene, where $E_{FG}$ is the graphene Fermi level, $h$ is the reduced Planck constant, $\nu_F$ is the Fermi velocity of graphene, $n$ is the carrier concentration in graphene; $\phi_1 = \frac{ne}{C_1}$ is the potential drop across the top-gate dielectric and is determined by the geometrical capacitance $C_1 = \frac{\varepsilon_1 \varepsilon_0}{t_{ox1}}$ of the high-k top-gate dielectric (e.g. HfO$_2$), where $\varepsilon_1$ is the top-gate dielectric constant, $\varepsilon_0$ is the permittivity of free space, and $t_{ox1}$ is the thickness of the top-gate dielectric. We can then solve for the electrostatically induced carrier density ($n$) in the valence band of graphene by inserting a particular top-gate voltage value and the material parameters of the current batch of our GBILET into the above equation.

We then calculate the maximum Fermi level shift into the valence band of graphene (e.g. p-dope) due to the above conditions and the electrostatically induced charge carrier density. This
is done inserting the calculated carrier density into the linear energy dispersion relation unique to monolayer graphene: \( E_F = \hbar |v_F| k_F = \hbar |v_F| \sqrt{\pi |n|} \). This yields a particular Fermi level shift, \(|E_F|\), into the valence band of graphene. We then multiply this value by two to get the expected maximum emitted photon energy, \( 2|E_F| = E_{emit} \). Finally, we insert this photon emission value into the following relation: \( E_{emit} = 2|E_F| (eV) = \frac{1.24}{\lambda_{emit} (\mu m)} \) to arrive at the cutoff photon emission wavelength of the HEL spectrum emanating from the biased GBILET.

4.4 Raman Spectroscopy of Monolayer CVD Graphene

Figure 4-5 shows the measured Raman spectrum of the monolayer CVD graphene that was transferred onto the GBILET. There is a prominent D peak \( \sim 1350 \text{cm}^{-1} \), which indicates that this graphene has many defects. The CVD graphene is confirmed to be monolayer as the 2D peak can be fit with a single Lorentzian curve and the 2D peak is \( \sim 3.6 \) times higher than the G peak\(^ {89,90} \). A 514nm laser was incident on the graphene during the measurements. Knowing that the CVD graphene is a monolayer, we can now proceed with the electrical characterization of the GBILETs.
Figure 4-5.  Raman spectrum of monolayer CVD graphene transferred onto the GBILET.  There is a prominent D peak $\sim 1350\text{cm}^{-1}$, which indicates that this graphene has many defects.  The CVD graphene is confirmed to be monolayer as the 2D peak can be fit with one Lorentzian and the 2D peak is $\sim 3.6$ times higher than the G peak.

4.5 Electrical Characteristics of the GBILET

Once the GBILETs are fabricated, we proceed to perform preliminary electrical measurements on each device in order to ascertain the quality of the CVD graphene channel, the quality of the top-gate dielectric (e.g. HfO$_2$), and the quality of the $\sim 3\text{nm}$ thick SiO$_2$ tunnel oxide.  Figure 4-6 shows the three different biasing schemes we use to study these three material properties.  Scheme 1 is used to measure the output characteristics (e.g. resistance) of CVD graphene between the source and drain (or similarly, the base) contacts.  Scheme 2 is used to measure the top-gate modulation of the CVD graphene and to ascertain its initial p-type doping as inferred from its initial Dirac point voltage (e.g. top-gate voltage which exhibits the lowest conductivity).
In addition, we simultaneously measured the leakage current \((I_{GS})\) through the top-gate dielectric (e.g. HfO\(_2\)) during this top-gate modulation measurement. Scheme 3 is used to measure the tunnel oxide’s characteristics. We are usually limited to applying a voltage of ~3V across the tunnel oxide since its thickness is ~3nm. This measurement allows us to determine the maximum tunneling current that we can inject into the graphene without causing dielectric breakdown of the SiO\(_2\) tunnel oxide. Note that since the GBILET structure is the same as that for the 2D vdW-AHCT structure, we may refer to its base contacts as the source and drain contacts interchangeably throughout this chapter. Furthermore, all of the electrical characteristics in this section were measured for a GBILET featuring a thin semi-transparent metal (1nm Ti/5nm Pt) as the top-gate electrode.

![Scheme 1: Voltage Biasing Schematic For Measuring the Resistance of Graphene (VDS vs VG)](image1)

![Scheme 2: Voltage Biasing Schematic For Measuring the Dirac Point of Graphene (VDS vs VG)](image2)

![Scheme 3: Voltage Biasing Schematic For Measuring the Tunnel Diode’s I-V Characteristics (I_{EB} vs V_{EB})](image3)

**Figure 4-6.** The three electrical biasing schemes used to characterize the GBILETs. Scheme 1 is for the output characteristics \((I_{DS} \text{ vs } V_{DS})\) of the graphene. Scheme 2 is for the top-gate modulation \((I_{DS} \text{ vs } V_{TG})\) of the graphene. Scheme 3 is for the tunnel oxide’s I-V characteristics \((I_{EB} \text{ vs } V_{EB})\). Note that the graphene is actually patterned to exist directly underneath the top-gate dielectric and that it does not extend beyond the base contacts contrary to what is shown in this figure.
4.5.1 Output Characteristics of the GBILET (I_{DS} vs V_{DS})

Figure 4-7 shows the output characteristics for the CVD graphene. We bias the device as shown in Scheme 1. The top-gate electrode is left floating. This particular device features a CVD graphene with a resistance of ~440Ω. The graphene resistance could change from batch to batch, depending upon the particular growth and transfer process used as well as any residues and contamination introduced throughout the fabrication process flow. An Ohmic contact is evident from the I-V characteristics. The drain and source contacts on top of the CVD graphene are Cr (20nm)/Au (100nm). However, for our GBILET project, the planar properties of the CVD graphene, such as its resistance and mobility, are not crucial since we will be vertically injecting hot electrons into its conduction band in order to achieve light emission.

![Output Characteristics for Graphene in a GBILET](image)

**Figure 4-7.** Output characteristics (I_{DS} vs V_{DS}) of the CVD graphene for a GBILET. The gate-voltage is left floating. The resistance of the graphene channel is ~440Ω. An Ohmic contact is evident from the I-V characteristics.
4.5.2 Top-Gate Modulation of the GBILET (\(I_{DS} \text{ vs } V_{TG}\))

Figure 4-8 shows the top-gate modulation characteristics of the GBILET. We bias the device as shown in Scheme 2. A constant drain-source bias of \(V_{DS} = +10\text{mV}\) is applied across the graphene in order to generate a constant drain current across the graphene. Then, we sweep the top-gate voltage \(V_{TG}\) from 0 to +1.75V and back while simultaneously measuring the drain current \((I_{DS})\) and the leakage current \((I_{GS})\) across the HfO\(_2\) top-gate dielectric. The ambipolar transport behavior of graphene is observed with the hole branch to the left \((V_{TG} < +0.5V)\) and the electron branch to the right \((V_{TG} > +0.5V)\) of the Dirac point voltage. More importantly, the Dirac point voltage \((V_{TG} = V_{Dirac})\) is equal to \(V_{TG} = +0.5V\) during the forward sweep, which indicates that the CVD graphene is unintentionally p-doped due to its exposure to the ambient environment (e.g. air and water).

![Top-Gate Modulation for Graphene in a GBILET](image)

**Figure 4-8.** Top-gate modulation \((I_{DS} \text{ vs } V_{TG})\) for a GBILET. The drain-source bias is set to +10mV. Both the forward and the backward sweeps are included to show the typical hysteresis of a GBILET due to the HfO\(_2\) top-gate dielectric. The Dirac point voltage is located at \(V_{TG} = +0.5V\) (forward sweep) and \(V_{TG} = +1.1V\) (backward sweep). This shows that the CVD graphene is unintentionally p-doped due to the
ambient environment. The leakage current through the HfO$_2$ top-gate dielectric is shown on the right axis of the figure and is less than I$_{GS} = 800$ pA for V$_{TG} = +1.75$V.

### 4.5.3 Tunnel Oxide Characteristics of the GBILET (I$_{EB}$ vs V$_{EB}$)

Figure 4-9 shows the tunnel oxide characteristics of the GBILET. We bias the device as shown in Scheme 3. The base contact (e.g. graphene) is grounded. We sweep the emitter-base voltage (V$_{EB}$) across the ~3nm thick SiO$_2$ tunnel oxide from V$_{EB} = 0$ to -3V (forward sweep) and back to 0 (backward sweep). A maximum tunneling (e.g. hot electron injection from silicon to graphene’s conduction band) current of I$_{EB} \sim 90$ nA occurs at V$_{EB} = -3$V. Furthermore, we sweep V$_{EB}$ from 0 to +3V (forward sweep) and back to 0 (backward sweep). A maximum tunneling (e.g. from graphene’s conduction band into the silicon) current of I$_{EB} \sim +40$ nA occurs at V$_{EB} = +3$V. Note that the conduction band offset (CBO) between SiO$_2$ and graphene is calculated to be $\Delta_e = 3.7$ eV, whereas the CBO between silicon and SiO$_2$ is $\Delta_e = 3.15$ eV. Thus, we attribute the asymmetry in the I$_{EB}$-V$_{EB}$ characteristics to be due to the different barrier heights on either side of the SiO$_2$ tunnel oxide. The lack of significant hysteresis in the I$_{EB}$-V$_{EB}$ curves shows the good quality of the SiO$_2$ tunnel oxide. Also, the hot electron (e.g. tunneling) injection area is $\sim 6 \times 10^{-5}$ cm$^2$. The top-gate voltage was left floating throughout the measurements.
Figure 4-9. Tunnel oxide characteristics ($I_{EB}$ vs $V_{EB}$) for a GBILET. The base contacts (or similarly, the source and drain contacts) are grounded. The top-gate voltage is left floating during the measurements. The hot electron injection current through the ~3nm thick SiO$_2$ tunnel oxide is about $I_{EB} = -90nA$ at $V_{EB} = -3V$. Data from both the forward and the backward sweeps are shown and displays a negligible hysteresis due to the SiO$_2$ tunnel oxide. The hot electron injection area for this particular GBILET is $\sim6\times10^{-5}$ cm$^2$.

This concludes the preliminary electrical characterization of the GBILET. This particular GBILET is a good candidate for light emission because we can clearly see its initial Dirac point voltage and thus we know its initial p-doping condition via the aforementioned calculations. We are currently performing the electroluminescence measurements on various GBILETs from different batches, such as those with a thin semi-transparent metal top-gate electrode (e.g. data shown here) and the newer batch with a transparent ITO top-gate electrode.

4.6 The MoS$_2$ Visible Light-Emitting Transistor (MoS$_2$-VLET)

The optoelectronics of 2D van der Waals materials$^{8-10}$ allows for a wide spectral range of light emission and detection due to the different values of direct bandgaps present in the monolayer TMDs (e.g. visible and near-infrared spectral range) and the more recent 2D material black
phosphorous (e.g. mid-infrared to visible spectral range)$^{10,91}$. In this section, we introduce the MoS$_2$ Visible Light-Emitting Transistor (MoS$_2$-VLET), which exploits both the direct-bandgap of monolayer MoS$_2$ and the giant Stark effect$^{45,48,92}$ in order to tune the photon emission wavelengths with a top-gate voltage.

4.7 Device Structure and Principle of Operation of the MoS$_2$-VLET

Figure 4-10 shows the basic device structure and operational biasing procedure of our MoS$_2$ visible light-emitting transistor (MoS$_2$-VLET). The MoS$_2$-VLET is a novel optoelectronic light source (e.g. MoS$_2$ is the active material) with a visible light emission spectrum centered near $\lambda = 689$nm, corresponding to the natural direct bandgap of monolayer MoS$_2$ ($E_G = 1.8$eV). Furthermore, the emitted photon wavelength can be tuned by the application of a top-gate voltage due to the giant Stark effect$^{45,48,92}$. MoS$_2$-VLET operates via injection electroluminescence (e.g. hot electron luminescence) but it is not a diode (e.g. not an LED) and thus an entirely different device concept in itself. It benefits from the direct bandgap of monolayer MoS$_2$ and the fact that its direct bandgap can be reduced with the application of a perpendicular electric field in order to provide a wavelength tunable (e.g. wavelength agile) visible light emission spectrum. MoS$_2$-VLET is a dual-gated transistor with a top-gate dielectric (e.g. HfO$_2$, Al$_2$O$_3$, ion-gel, ionic liquid, etc.) and an ultrathin tunneling oxide (e.g. SiO$_2$, hexagonal boron nitride, MgO, Gd$_2$O$_3$, etc.) sandwiching the monolayer MoS$_2$ in between them.

An electrostatic potential ($V_{BG}$) is applied across the underlying degenerately doped $n^{++}$ silicon substrate (e.g. the source of the hot electrons), the tunnel oxide, and the monolayer MoS$_2$. This results in a non-equilibrium or “hot” carrier distribution of electrons being injected via quantum tunneling through an ultrathin tunneling oxide (e.g. SiO$_2$, hexagonal boron nitride, MgO, Gd$_2$O$_3$, etc.) into the conduction band of monolayer MoS$_2$. The hot electrons relax to the bottom of the conduction band...
of MoS\textsubscript{2} via various scattering mechanisms\textsuperscript{93} and eventually emit photons with a wavelength of $\lambda = 689$nm, corresponding to MoS\textsubscript{2}’s direct bandgap of $E_G = 1.8$eV. Furthermore, the bandgap (and hence the photon emission wavelength) can be tuned via a top-gate voltage ($V_{TG}$) due to the giant Stark effect\textsuperscript{45,48,92}. $E_G$ is the initial bandgap of monolayer MoS\textsubscript{2}, and $E'_G$ is its reduced bandgap due to $V_{TG}$.

**Figure 4-10.** Basic device structure and operational biasing procedure of a MoS\textsubscript{2}-VLET. A 3D isometric view (top left corner) of the MoS\textsubscript{2}-VLET is rotated counter-clockwise by 90° in order to match the orientation of the of the device structure (main panel). The active area of the device is the MoS\textsubscript{2} region directly underneath the transparent ITO top-gate electrode. A negative back-gate voltage bias ($V_{BG}$) is applied in order to inject hot electrons (red circles) from the n\textsuperscript{++} silicon substrate, through a tunnel barrier, and into the conduction band of MoS\textsubscript{2}. The hot electrons relax to the bottom of the conduction band via various scattering mechanisms and eventually emit photons with a wavelength of $\lambda = 689$nm, corresponding to MoS\textsubscript{2}’s direct bandgap of $E_G = 1.8$eV. Furthermore, the bandgap (and hence the photon emission wavelength) can be tuned via a top-gate voltage due to the giant Stark effect. $E_G$ is the initial bandgap of monolayer MoS\textsubscript{2} (opaque area, solid lines in the figure), and $E'_G$ is its reduced bandgap (transparent area, dotted lines in the figure) due to $V_{TG}$.
4.7.1 Method to Calculate the Luminescence Power of the MoS$_2$-VLET

The following method is used to calculate the expected luminescence power emanating from the properly biased MoS$_2$-VLET. For our current batch of MoS$_2$-VLETs, the maximum tunneling current we can safely inject without fatiguing or breaking the ~3nm SiO$_2$ tunneling oxide is about 1-5nA. In the next batch, we will grow an ultrathin 1.5nm or thinner SiO$_2$ tunneling oxide to achieve safe tunneling current densities up to 50Acm$^{-2}$ (e.g. over 3 orders of magnitude improvement). Assuming that we constantly inject a tunneling current of $I_{EB} = 1nA$ into the monolayer MoS$_2$’s conduction band, and using the measured internal quantum efficiency$^{5,94}$ of monolayer MoS$_2$ as $10^{-3}$ in our calculations, we arrive at about 6 million photons per second emanating from the MoS$_2$-VLET active area. Note that we are calculating for the peak photon energy of the HEL spectrum which is centered near $\lambda = 689$nm (e.g. $E_G = 1.8$eV).

$$I = \frac{ne}{t} \rightarrow n = \frac{It}{e} = \frac{(1 \times 10^{-9}A) \cdot (1s)}{(1.602 \times 10^{-19}C)} = 6.2422 \times 10^9 \text{electrons/ sec}$$

$$\left(6.2422 \times 10^9 \text{electrons/ sec}\right) \cdot \left(10^{-3} \text{photons/ electron}\right) = 6.2422 \times 10^6 \text{photons/ sec}$$

The power corresponding to this peak photon emission is:

$$\left(6.2422 \times 10^6 \text{photons/ sec}\right) \cdot \left(1.8eV/ \text{photon}\right) =$$

$$\left(1.1236 \times 10^7 \text{eV/ sec}\right) \cdot \left(1.602 \times 10^{-19} J/ eV\right) = 1.8 \times 10^{-12} W = 1.8pW$$

4.7.2 Method to Calculate the Luminescence Wavelength of the MoS$_2$-VLET

The following method is used to calculate the expected photon emission wavelength from the properly biased MoS$_2$-VLET for a particular top-gate voltage ($V_{TG}$). Using a tight-binding model based on the hybridization of the d orbitals of molybdenum and the p orbitals of sulfur atoms, H. Rostami et al.’s numerical results$^{45}$ showed that applying a gate-voltage perpendicular to the plane of the monolayer MoS$_2$ can shrink its bandgap due to the induced potential ($U_b'$) modifying the
on-site energies of the atoms in its three sublayers (e.g. S-Mo-S layers). The relation between the perpendicular gate-voltage \( (V_{TG}) \) and the induced potential across the three sublayers of the monolayer MoS\(_2\) is given by: \( U'_b = \left( \frac{d}{L} \right) \left( \frac{\varepsilon'}{\varepsilon} \right) eV_{TG} \), where \( \varepsilon \) is the relative dielectric constant of the monolayer MoS\(_2\) and \( d \) is the thickness of monolayer MoS\(_2\), \( \varepsilon' \) is the relative dielectric constant of the top-gate dielectric (e.g. HfO\(_2\)), and \( L \) is the thickness of the top-gate dielectric. We can then solve for the induced potential across the three sublayers of monolayer MoS\(_2\) by inserting a particular top-gate voltage value and the material parameters of the current batch of our MoS\(_2\)-VLETs into the above equation.

Our current batch of MoS\(_2\)-VLETs feature a ~55nm thick HfO\(_2\) top-gate dielectric with a measured average dielectric constant (\( \varepsilon \)) of ~17 and a corresponding capacitance of \( C_{HfO_2} = 2.8 \times 10^{-7} \ \frac{F}{cm^2} \). A top-gate voltage of \( V_{TG} = -10V \) corresponds to an induced potential of \( U'_b = 0.335 eV \) and correspondingly a perpendicular electric field of \( E = 0.18 \ \frac{V}{nm} \). This means that the direct bandgap of monolayer MoS\(_2\) reduces from \( E_G = 1.8 eV \) to \( E'_G = 1.8 eV - 0.335 eV = 1.465 eV \) when \( V_{TG} = -10V \). Thus, when our current batch of MoS\(_2\)-VLETs are biased at \( I_{EB} = 1 nA \) and \( V_{TG} = 0V \), the peak of the HEL spectrum should have a power of 1.8pW at a wavelength of 689nm (e.g. \( E_G = 1.8 eV \) is in the visible spectral range), whereas when the MoS\(_2\)-VLETs are biased at \( I_{EB} = 1 nA \) and \( V_{TG} = -10V \), the peak of the HEL spectrum should have a power of 1.8pW at a wavelength of 846nm (e.g. \( E'_G = 1.465 eV \)).

### 4.8 Raman Spectroscopy of Monolayer CVD MoS\(_2\)

Figure 4-11 shows the measured Raman spectrum of the monolayer CVD MoS\(_2\) that was transferred onto the MoS\(_2\)-VLET. The Raman spectrum of MoS\(_2\) exhibits two characteristic bands: the in-plane phonon mode, \( E^{1}_{2g} \), centered near 387 cm\(^{-1}\) and the out-of-plane phonon
mode, $A_{1g}$, centered near $406\,\text{cm}^{-1}$, with a peak frequency difference of $18.9\,\text{cm}^{-1}$, which is a clear signature of monolayer MoS$_2$. A 514nm laser was incident on the MoS$_2$ during the measurements. Knowing that the CVD MoS$_2$ is a monolayer, we can now proceed with the electrical characterization of the MoS$_2$-VLETs.

![Raman Spectrum of Monolayer CVD MoS$_2$](image)

**Figure 4-11.** Raman spectrum of monolayer CVD MoS$_2$ transferred onto the MoS$_2$-VLET. The Raman spectrum of MoS$_2$ exhibits two characteristic bands: the in-plane phonon mode, $E_{12g}$, centered near $387\,\text{cm}^{-1}$ and the out-of-plane phonon mode, $A_{1g}$, centered near $406\,\text{cm}^{-1}$, with a peak frequency difference of $18.9\,\text{cm}^{-1}$, which is a clear signature of monolayer MoS$_2$.

### 4.9 Characterization of the ITO Top-Gate Electrode for the MoS$_2$-VLETs

Figure 4-12 shows the measured transmission spectrum of a control sample of ITO that was sputtered at the same time as the ITO top-gate electrode of our MoS$_2$-VLETs. A ~45nm thick degenerately doped n-type amorphous ITO film was RF sputtered at room temperature. It features a relatively smooth >80% transmission spectrum throughout the entire visible spectral range and into the near-infrared. Since we expect light emission from MoS$_2$ in this spectral range
(e.g. 689nm < λMoS2 < 850nm), it is critical that the top-gate electrode be transparent to the generated light so that we can detect it in our optical setup.

**Figure 4-12.** The measured transmission spectrum of a control sample of ITO that was sputtered at the same time as the ITO top-gate electrode of our MoS2-VLETs. A ~45nm thick degenerately doped n-type amorphous ITO film was RF sputtered at room temperature. It features a relatively smooth >80% transmission spectrum throughout the entire visible spectral range and into the near-infrared.

Furthermore, Figure 4-13 shows the Tauc plot (e.g. absorption coefficient versus photon energy) used for extrapolating the optical bandgap of the sputtered ITO. The data plotted is for the same control sample shown in Figure 4-12, which was sputtered at the same time as the ITO top-gate electrode of our MoS2-VLETs. A ~45nm thick degenerately doped n-type amorphous ITO film was RF sputtered at room temperature. The linear region on the left side denotes the onset of absorption. We can determine the optical bandgap of the ITO by extrapolating this linear region to the abscissa (e.g. the red line is a linear fit). Thus, our sputtered ITO features a bandgap of E_g ~ 4.5eV. This relatively large bandgap is attributed to the Burnstein-Moss shift, in which the absorption edge shifts higher with a higher carrier concentration (e.g. doping)\textsuperscript{68,96,97}. 


Figure 4-13. Tauc plot (absorption coefficient versus photon energy) used for extrapolating the bandgap of the sputtered ITO. The control sample of ITO that was sputtered at the same time as the ITO top-gate electrode of our MoS$_2$-VLETs. A ~45nm thick degenerately doped n-type amorphous ITO film was RF sputtered at room temperature.

4.10 Electrical Characteristics of the MoS$_2$-VLET

Once the MoS$_2$-VLETs are fabricated, we proceed to perform preliminary electrical measurements on each device in order to determine the quality of the CVD MoS$_2$ channel, the quality of the top-gate dielectric (e.g. HfO$_2$), and the quality of the ~3nm thick SiO$_2$ tunnel oxide. Similar to the case of the GBILETs, Figure 4-6 shows the three different biasing schemes we used to study these three material properties of the MoS$_2$-VLETs. Scheme 1 is used to measure the output characteristics (e.g. resistance) of the CVD MoS$_2$ between the source and drain (or
similarly, the base) contacts. Scheme 2 is used to measure the top-gate modulation of the CVD MoS$_2$. Scheme 3 is used to measure the tunnel oxide’s characteristics.

We are usually limited to applying a voltage of $\sim$3V across the tunnel oxide since its thickness is $\sim$3nm. This measurement allows us to ascertain the maximum tunneling current that we can inject into the conduction band of CVD MoS$_2$ without causing dielectric breakdown of the SiO$_2$ tunnel oxide. Note that since the MoS$_2$-VLET structure is the same as that for the 2D vdW-AHCT structure, we may refer to its base contacts as the source and drain contacts interchangeably throughout this chapter. Furthermore, all of the electrical characteristics in this section were measured for a MoS$_2$-VLET featuring a $\sim$45nm thick ITO transparent top-gate electrode (e.g. $>80\%$ smooth transmission spectrum throughout the entire visible spectral range).

4.10.1 Output Characteristics of the MoS$_2$-VLET (I$_{DS}$ vs V$_{DS}$)

Figure 4-14 shows the output characteristics for the CVD MoS$_2$. We bias the device as shown in Scheme 1 of Figure 4-6. The top-gate electrode is left floating. This particular device features a CVD MoS$_2$ with a resistance of $\sim$5-10G$\Omega$ in the range $-3V < V_{DS} < -2V$. The MoS$_2$ resistance could change from batch to batch, depending upon the particular growth and transfer process used as well as any residues and contamination introduced throughout the fabrication process flow. A Schottky contact is evident from the I-V characteristics. The drain and source contacts on top of the CVD MoS$_2$ are Ti (20nm)/Au (100nm). However, for our MoS$_2$-VLET project, the planar properties of the CVD MoS$_2$, such as its resistance and mobility, may not be as crucial since we will be vertically injecting hot electrons into its conduction band in order to achieve light emission.
Figure 4-14. Output characteristics (I_{DS} vs V_{DS}) of the CVD MoS\(_2\) for a MoS\(_2\)-VLET. The gate-voltage is left floating. A Schottky contact is evident from the I-V characteristics. The resistance of the MoS\(_2\) channel is \~5-10GΩ in the range -3V < V_{DS} < -2V.

4.10.2 Top-Gate Modulation of the MoS\(_2\)-VLET (I_{DS} vs V_{TG})

Figure 4-15 shows the top-gate modulation (I_{DS} vs V_{TG}) for a MoS\(_2\)-VLET. We bias the device as shown in Scheme 2 of Figure 4-6. The drain-source bias is set to +2V. The I-V characteristics clearly show n-type behavior. Recall that intrinsic monolayer MoS\(_2\) is n-type with an electron affinity of 4.07eV < q\(\chi\) < 4.2eV and a work function of 4.6eV < q\(\phi\) < 4.9eV. The leakage current through the HfO\(_2\) top-gate dielectric is shown on the right axis of the figure and is less than I_{GS} = 3pA for V_{TG} = +2V.
Figure 4-15. Top-gate modulation ($I_{DS}$ vs $V_{TG}$) for a MoS$_2$-VLET. The drain-source bias is set to +2V. The I-V characteristics show n-type behavior. The leakage current through the HfO$_2$ top-gate dielectric is shown on the right axis of the figure and is less than $I_{GS} = 3$ pA for $V_{TG} = +2$V.

### 4.10.3 Tunnel Oxide Characteristics of the MoS$_2$-VLET ($I_{EB}$ vs $V_{EB}$)

Figure 4-16 shows the tunnel oxide characteristics of the MoS$_2$-VLET. We bias the device as shown in Scheme 3 of Figure 4-6. The base contacts (e.g. MoS$_2$) are grounded. A diode-like (e.g. rectifying) behavior is evident from the I-V characteristics, in stark contrast to the case of graphene. We sweep the emitter-base voltage ($V_{EB}$) across the ~3nm thick SiO$_2$ tunnel oxide from $V_{EB} = 0$ to -3V (forward sweep) and back to 0 (backward sweep). A negligible tunneling current of $I_{EB} \sim -18$ pA occurs at $V_{EB} = -2.5$V for this reverse-bias condition. Furthermore, we sweep $V_{EB}$ from 0 to +3V (forward sweep) and back to 0 (backward sweep). A maximum tunneling current of $I_{EB} \sim +2.5$ nA occurs at $V_{EB} = +2.5$V for this forward-bias condition. The lack of significant hysteresis in the $I_{EB}$-$V_{EB}$ curves shows the good quality of the SiO$_2$ tunnel oxide.
Also, the hot electron (e.g. tunneling) injection area is $\sim 2 \times 10^{-4} \text{cm}^2$. The top-gate voltage was left floating throughout the measurements.

![Tunnel Oxide Characteristics for MoS$_2$ in a MoS$_2$-VLET](image)

**Figure 4-16.** Tunnel oxide characteristics ($I_{EB}$ vs $V_{EB}$) for a MoS$_2$-VLET. The base contacts (or similarly, the source and drain contacts) are grounded. The top-gate voltage is left floating during the measurements. The hot electron injection current through the ~3nm thick SiO$_2$ tunnel oxide is about $I_{EB} = +2.5 \text{nA}$ at $V_{EB} = +2.5 \text{V}$. Data from both the forward and the backward sweeps are shown and displays a negligible hysteresis due to the SiO$_2$ tunnel oxide. The hot electron injection area for this particular MoS$_2$-VLET is $\sim 2 \times 10^{-4} \text{cm}^2$.

This concludes the preliminary electrical characterization of the MoS$_2$-VLET. This particular batch of MoS$_2$-VLETs are expected to emit very weak optical power due to the very low tunneling currents involved (e.g. $I_{EB} = 1-5 \text{nA}$), but should still be detectable using our current optical setup (e.g. New Focus silicon femtowatt photoreceiver and Stanford Research Systems SR830 lock-in amplifier) with sensitivity (e.g. noise equivalent power) down to hundreds of femtowatts. We are currently performing the electroluminescence measurements on these MoS$_2$-VLETs with
transparent ITO top-gate electrodes. The next batch of MoS₂-VLETs will feature at least 3 orders of magnitude improvement in the tunneling current by using an ultrathin ~1.5nm SiO₂ tunnel oxide, and hence the optical power should be ~1nW.
Chapter 5

Conclusion and Future Works

5.1 Conclusion

The work presented in this dissertation focused on the introduction of a new paradigm of device concepts based on a vertical tunneling transistor structure incorporating individual 2D van der Waals (2D vdW) materials, such as graphene and MoS$_2$, in the active region. The essential physics relied upon the injection of non-equilibrium, or hot, electrons via the quantum tunneling process through a vertical heterostructure. For the electronics aspect, we demonstrated 2D vdW material-based ambipolar hot carrier transistors (2D vdW-AHCTs), in which the injected hot electrons traversed vertically through the 2D vdW material in the base region and either reached the collector or back-scattered into the base region. For the optoelectronics aspect, the hot electrons were injected into the conduction band of the specific 2D vdW material in the base region where they relaxed and emitted photons via hot carrier luminescence. Furthermore, it was shown that the application of a top-gate voltage offers several functionalities. In the case of the 2D vdW-AHCTs, the top-gate/collector voltage controls the filter barrier height at the collector-base oxide.

We discovered that by choosing MoS$_2$ and HfO$_2$ for the filter barrier interface in addition to implementing a non-crystalline semiconductor such as ITO for the collector electrode, allowed for the simultaneous emergence of ambipolar transport, an unprecedentedly high and voltage-tunable current gain ($\alpha \sim 0.95$, $\beta > 15$), and a voltage-tunable recombination current in the base region of MoS$_2$. Depending upon the collector electrode’s bias polarity, either a hot electron mode of operation or a hole mode of operation dominated the transport mechanism of the 2D vdW-AHCTs. In the case of the 2D vdW wavelength-agile light-emitting transistors (2D vdW-LETs), the top-
gate voltage can tune the wavelength of the emitted photons via the band-filling effect\textsuperscript{26,32} in the Graphene Broadband Infrared Light-Emitting Transistor (GBILET) or by tuning the direct bandgap of monolayer MoS\textsubscript{2} in the MoS\textsubscript{2}-based Visible Light-Emitting Transistor (MoS\textsubscript{2}-VLET) with the application of a perpendicular electric field due to the giant Stark effect\textsuperscript{45,48,92}.

Chapter 1 introduced the main electronic and photonic properties of 2D vdW materials, including the recently discovered physical mechanisms of hot electron luminescence and the ability to tune the electronic band structure (e.g. direct bandgaps) of TMDs with a perpendicular electric field (e.g. gate voltage). This set the foundation and motivation for our 2D vdW-LETs. The concept of a hot electron transistor was introduced followed by our recent work on the graphene-base hot electron transistor (GB-HET) and the limitations that they currently face. This set the foundation and motivation for our 2D vdW-AHCTs.

Chapter 2 presented the detailed fabrication process flow of the multi-functional 2D vdW material-based device structure which can serve as either a 2D vdW-AHCT or 2D vdW-LET.

Chapter 3 focused on the MoS\textsubscript{2}-AHCT, which is the successor of our first-generation GB-HETs. Our investigation into the MoS\textsubscript{2}-AHCT led to the discovery of ambipolar transport in this novel device structure, a high current gain, a tunable recombination current in the MoS\textsubscript{2} base region, and the observation that the current gain can be tuned over two orders of magnitude with the collector-base voltage (V\textsubscript{CB}).

Chapter 4 introduced our proposals for a new paradigm of light-emitting transistors based on 2D vdW materials. The experimental demonstrations of the underlying physical phenomena were introduced in Chapter 1. In this chapter, a few novel device concepts were proposed and developed in detail based upon the concept of hot electron luminescence in graphene (e.g. GBILET) and MoS\textsubscript{2} (e.g. MoS\textsubscript{2}-VLET) and the giant Stark effect in TMDs (e.g. MoS\textsubscript{2}-VLET).
5.2 Suggested Future Works

There are several suggestions for future work concerning both the 2D vdW-AHCTs and 2D vdW-LETs. Very little is truly known about the vertical electronic transport of hot carriers perpendicular to the plane of 2D vdW materials, such as graphene and MoS$_2$. The electronic band structures in the perpendicular directions should be further investigated both theoretically and experimentally. Furthermore, it is worthwhile to incorporate various other 2D layered materials (e.g. WSe$_2$, WS$_2$, and In$_2$Se$_3$) in addition to exotic materials such as topological insulators (e.g. Bi$_2$Se$_3$) into the base (e.g. active area) region of our vertical tunneling transistor platform.

Each of these materials feature different bandgaps, electron affinities, and work functions, which will result in different conduction band offsets for the injected hot electrons at the filter barrier interface. It would be interesting to study the resulting device performance for these future AHCTs/LETs as well as their potential applications in light emission and detection in the visible (e.g. WSe$_2$, WS$_2$, and In$_2$Se$_3$) and the mid-infrared (e.g. Bi$_2$Se$_3$) spectral ranges. Furthermore, future device batches should increase the tunneling current density by several orders of magnitude from the current batches presented in this dissertation. This can be achieved by growing an ultrathin SiO$_2$ tunnel oxide with thickness less than 1.5nm or implementing other materials as the tunnel barrier (e.g. MgO, Gd$_2$O$_3$, monolayer hexagonal boron nitride).

Optimization of the tunneling current density can be accomplished by considering the conduction band offset between the silicon substrate and each of these tunnel oxide materials, which sets the tunnel barrier height, and growing as thin a tunnel barrier as possible without introducing significant pinholes. Finally, it would be interesting to fabricate a variety of these
AHCTs/LETs with a top-gate electrode consisting of graphene, a transparent ITO thin film, or a thin semi-transparent metal and compare their resulting electrical characteristics.
References


79. Venica, S., Driussi, F., Palestri, P. & Selmi, L. Graphene base transistors with optimized emitter and dielectrics. in *2014 37th International Convention on Information and


