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Design and fabrication of field-emission tips with self-aligned gates

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A novel approach to the design and fabrication of field-emission tips with self-aligned gates intended for electric propulsion micro-thruster applications is presented. Their micro-electromechanical systems fabrication process is derived from the recent proliferation of research toward developing field emitter arrays, which are used primarily for field-emission flat-panel display applications. An array of micron-sized tips for electric field enhancement via wet isotropic etching of silicon, using silicon nitride as a hard mask is fabricated. The wet etching is accomplished using a combination of hydrofluoric, nitric, and acetic acids. The tips were then coated with a metal layer to enhance wetting by indium, the proposed propellant. Next, a layer of SU-8 photoresist was applied by spin coating and patterned to serve as a dielectric spacer. A second layer of metal was then applied to serve as a gate electrode. In addition, the results of electrostatic simulations of the prototype is described.

1. Introduction: Micropropulsion has become an increasingly active field of research within the space community. The interest in these devices stems from a number of promising characteristics that have been either predicted by models or demonstrated in practice – low impulse bits, high specific impulse (I_{SP}), and significant reductions in size, mass, and power [1]. Future advanced spacecraft missions will require a variety of unique propulsion capabilities that are not currently available. Micropropulsion offers promises to fulfil many of these needs, from precision attitude control of traditional spacecraft to primary propulsion and control of microspacecraft with wet masses of <100 kg.

The motivation for examining micropropulsion stems from three trends in spacecraft design: mass reduction, the benefit of large fleets of microspacecraft, and higher demands on spacecraft performance. Mass reduction has always been a key consideration in the design of spacecraft. The historical trend toward increasing spacecraft mass results in launches becoming progressively less cost-effective. Up to 30% of the entire mission cost is spent simply getting the spacecraft off the ground [1]. As the size of spacecraft becomes increasingly small, bulky traditional propulsion engines become less practical or even obsolete. Micropropulsion promises a practical solution to this problem by offering the obvious advantage of drastically reducing size and mass of the propulsion unit. Furthermore, mass reduction lends additional plausibility to the idea of multiple small spacecraft flying in closely controlled constellations. Synergistic operation of micro-spacecraft is particularly attractive in terms of minimising mission risk in view of the spectacular loss of several high profile and expensive spacecraft [2]. Novel microfabrication techniques also allow for higher degrees of capability for both micro and traditional spacecraft, improving maneuverability, attitude control, communication data rates, and sensing capabilities [1].

Several micropropulsion technologies are currently being studied, including both chemical and electric designs. Chemical propulsion engines include monopropellant engines [3], cold gas thrusters [4], solid rocket motors [5], and hybrid rocket motors [6]. Ion engines [7], Hall thrusters [8], field emission electric propulsion (FEEP) engines, colloid thrusters [9], and pulsed plasma thrusters [10] are several examples of electric propulsion. This Letter presents a micro-electromechanical systems (MEMS)-based fabrication approach to implement a FEEP thruster design.

FEEP thruster designs are similar to field emitter arrays, which are currently employed as vacuum electron sources [11]. With FEEP, electrostatic forces are applied to a liquid metal surface (typically cesium, rubidium, or indium). The high electric field induces ionisation of the metal through a field-emission mechanism. The metal ions are accelerated to high velocities by the imposed field, producing thrust. The main characteristic that differentiates FEEP from other electric propulsion is its absence of a gaseous discharge. This can be beneficial for several reasons, some of which will be detailed in the next section.

To reduce the necessary operating voltage, the FEEP thruster is designed such that the liquid metal is introduced at a site where the electric field is geometrically enhanced (i.e. at a sharp point). When an extraction voltage is applied between a gate electrode and the propellant surface, the liquid metal begins to deform at these points and form cusps known as Taylor cones. This results in a further increase in the local electric field strength. Once this field reaches a strength of $\sim 10^9$ V/m, electrons are removed from the neutral metal atoms, and the positive metal ions are accelerated from the surface. Typical FEEP geometries include pin or needle type emitters [12], capillary type emitters [13], and slit emitters [14]. Propellants are fed from the reservoir to the emission tips through one of two alternative approaches [15]. One is by transport through enclosed channels to hollow emission tips such as the capillary and slit emitters. The other is by liquid transport over the external surface and ejected from the solid tips. Both approaches offer their own uniqueness and functional characteristics [15]. The key advantages of externally-fed emission tips over capillary and slit emitters are their substantially easier fabrication process, easier visual examination, and measurement of the propellant transport process during characterisation steps, and, as a result, more research and development work have been performed and reported on MEMS-fabricated externally-fed emitters [16]. An example of a needle emitter is illustrated in Fig. 1.

Our approach to FEEP design employs an original MEMS process to fabricate an array of nine micron-sized tips etched in a silicon substrate. When coupled with a power supply and fuel source, this device represents a prototype MEMS FEEP thruster. Our design results in lower power consumption because of significantly reduced voltage requirements at the gate when compared with alternative FEEP designs, as well as dramatic reductions in the size and mass of the eventual propulsion engine. Thus, our FEEP design is a feasible alternative to larger traditional propulsion engines. Finally, MEMS devices, including this device, are readily amenable to scale-up.

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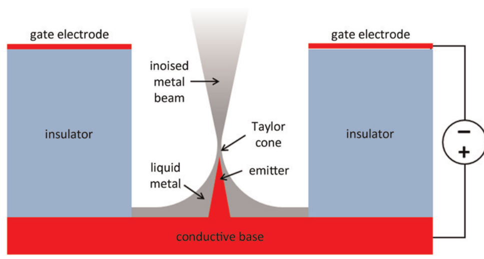

Fig. 1 *Illustration of the external wetting of a needle type emitter*

2. Design principles: When compared with other electric propulsion designs, FEEP has several unique advantages. First, the absence of gaseous discharges permits a higher degree of miniaturisation than is possible with other electric propulsion techniques [1]. This also eliminates many problems with high surface-to-volume ratios and high potential electron wall losses that often accompany gaseous discharge. Second, FEEP engines have low impulse noise; i.e. each firing produces a consistent, predictable impulse. This consistent thrust output permits extremely precise position control and drag make-up, simplifying navigation tasks for spacecraft flying in constellation [17]. Finally, very low engine mass and a high thrust-to-input power ratio can be achieved. As a result, the total system impulse for a given engine mass is greatly enhanced.

In March of 2004, Tajmar *et al.* [18] demonstrated and tested the first successful indium propellant FEEP thruster possessing all of these advantages. Using standard machining techniques, they fabricated a millimetre scale needle ion source, using external wetting of indium for the propellant as is shown in Fig. 1. They then applied a voltage at the extractor electrode, which was located ~0.6 mm from the tip. As ionisation and acceleration took place in the same electric field – a feature unique to FEEP devices – they were able to demonstrate an unparalleled electric efficiency of over 95%.

The FEEP design is further advantageous in that it requires smaller extraction voltages for high I_{SP} values, especially when compared with colloid thrusters. Simple conservation of energy predicts that the accelerated ions achieve a velocity u

$$u = \sqrt{\frac{2eV}{m_{\text{ion}}}} \tag{1}$$

where V is the extraction voltage, m_{ion} is the mass of an individual ion, and e is the elementary charge. This velocity is linearly related to specific impulse (the specific impulse is linearly related to the velocity). Thus, to achieve high specific impulse values, either high acceleration voltages or small ion masses are required. Colloid thrusters in general employ large, heavy molecules, decreasing the acceleration velocity and therefore specific impulse. FEEP thrusters therefore require significantly smaller extraction voltages for the same types of high I_{SP} values as colloid thrusters.

One of the primary reasons for the implementation of FEEP thrusters is their amenability to MEMS fabrication. Up until now very little work has been done towards producing FEEP thrusters using a MEMS fabrication process. Using a MEMS fabrication process permits us to fabricate thruster arrays containing a large number of small ion sources as opposed to the small number (one to four) of large sources employed in macroscale FEEP designs. This leads to an increase in mass efficiency, one of the primary benefits of a MEMS-based design. Mass efficiency describes the ratio of the propellant mass emitted in ionic form to that emitted as neutral micro-droplets. Higher operating currents lead to a greater emission of micro-droplets. As the neutral micro-droplets are not accelerated by the electric field, they contribute little to the overall thrust. Ionised propellant, on the other hand, provides maximum thrust for the mass used because it experiences maximum acceleration in the applied electric field. Mass efficiency (η_{mass}) for a FEEP system can be determined by weighing the thruster before and after operation (Δm), and measuring the total emission current (I_E) caused by the ejected propellant ions for the entire duration of thrust

$$\eta_{\text{mass}} = \frac{m_{\text{ion}}}{e}\frac{\int I_E \, dt}{\Delta m} \tag{2}$$

When only a few large ion sources are used, as in the needle emitter mentioned previously, mass efficiency is limited by a threshold emitter current. A lower mass efficiency indicates that more neutral droplets are being emitted, which increases the amount of propellant needed in the fuel reservoir to achieve a target total impulse. The obvious consequence of this is an increase in the total mass of the micro-rocket.

Tajmar *et al.* [18] have also developed a model for the mass efficiency of their FEEP system. By examining the I–V characteristic of their emitter, where I is the emitter current and V is the extraction voltage, they were able to formulate an expression for mass efficiency

$$\eta_{\text{mass}} \propto \left(\frac{rI_E}{U_E^2}\right) f(\tau) \tag{3}$$

where r is the radius of the tip, U_E is the extraction voltage, and $f(\tau)$ is a function of temperature that is highest around the melting temperature for the proposed propellant, indium. Fitting this to experimental data, they discovered that

$$\eta_{\text{mass}} \propto I_E^{-0.42} \tag{4}$$

is a good approximation for the mass efficiency as a function of emitter current. From this relation, it is evident that the thrust-to-power ratio is reduced by a factor greater than three when the current for a single emitter is increased from 20 to 200 μA. As the emitter current observed for a single ion source increases, more clusters of propellant form at the tip of the source and it becomes more likely to emit neutrally charged droplets in combination with ions. When this droplet of propellant is then exposed to the electric field, the exit velocity is substantially lowered due to the reduction of charge to mass ratio in the droplet.

MEMS fabrication techniques permit the creation of significantly smaller ion sources (on the order of about 25 μm). Each small ion source functions as an element in an array, and as such can be operated at current levels below the threshold for neutral droplet formation. Due to the smaller separation distance between the emission tips and acceleration electrodes, as well as the nanometre scale sharpness of the tips, the MEMS FEEP design requires very small extraction voltages (200–300 V) to achieve emission. From (3), it is easy to see how decreasing extraction voltage dramatically increases mass efficiency. According to the experimental plots developed by Tajmar *et al.* [18], thrust-to-power ratio increases as well with decreased emitter currents. Increased mass efficiency directly correlates to reduction of total mass, which is presently one of the primary goals for micro-rocket research and design.

Significant reductions in size and mass are intrinsic benefits of using MEMS fabrication. Apart from the mass efficiency benefits already described, our MEMS FEEP thruster results in a much smaller size while maintaining reasonable output levels. Our design uses tips ~25 μm in base diameter. The smallest ion sources for FEEP designs fabricated currently are on the order of millimetres [1].

Other advantages of a MEMS-based approach include integration and scalability. If all components can be microfabricated, it is relatively easy to integrate them, as well as the required control

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microelectronics. A MEMS-based approach is theoretically capable of higher levels of fabrication integration than has been seen in any rocket production line, either micro or large scale. Furthermore, the lithography techniques used in most MEMS processes allow easy scaling to larger units. The majority of research effort is directed at developing an exceptional modular prototype with a small number of elements. After this is completed, only incremental effort is required to scale the prototype to a functional thruster with thousands of emitters. This Letter presents such a modular prototype. We developed a fabrication process for a 3 × 3 array of MEMS FEEP – including functional emitter tips, a dielectric layer, and gate electrodes. This process can be used for larger arrays of tips, and arrays of 6400 tips are conceivable.

Though the concept of using MEMS for FEEP is not new, successful implementation has not yet been reported [19]. This Letter describes the fabrication and simulation of such a prototype.

3. Fabrication: Our objective was to produce a microfabricated FEEP with the following specifications:

(i) Sharp, high-quality tips with tip radii of <1 µm.

(ii) Provide reservoirs for introduction of indium fuel.

(iii) Allow liquid indium to wet the surface of the tips and reservoirs.

(iv) Withstand the specified gate voltage and operating temperature.

(v) A conductive layer to serve as the common gate electrode for all tips while electrically insulated from the wetting layer.

Electrostatic simulation has shown that a circular gate electrode with a diameter of 50 and 25 µm spacing between the tips and the gate provides the required electric fields for emission of indium. A diagram summarising our criteria for optimal emission is shown in Fig. 2.

3.1. Process overview: The construction of our FEEP emitter can be divided into two major steps: fabrication of tips etched out of silicon and the deposition of dielectric and metal layers.

Fig. 3 shows the cross-sections of the process flow. We fabricated the tips using silicon wafers coated with a 3000 Å LPCVD Si_3N_4 layer. We applied Shipley 1827 photoresist to the nitride surface, and patterned it using a Karl Suss MA6 mask aligner. We then etched the nitride layer using CHF_3/O_2 plasma in a Plasma-Therm 790 RIE. After etching, the photoresist was stripped in acetone, followed by a brief treatment in an oxygen plasma to remove any remaining resist. We then placed the wafer into a mixture of hydrofluoric, nitric, and acetic acid (HNA), which acts as an isotropic silicon etchant. Given the correct acid ratio, proper mask design, and close control of etch conditions, HNA etching produces sharp, well-defined tips. In thinner regions, the silicon underneath was completely etched away, leaving the nitride layer freely suspended, as can be seen in Fig. 4. A 200 Å layer of titanium followed by a 1000 Å layer of gold was then thermally evaporated over the entire wafer in order to enhance indium wetting. To deposit metal in regions of the wafer masked by the suspended nitride layer, an omni-directional work holding fixture was used in the coating process.

We then applied a layer of Shipley 1827 photoresist to fill the etched regions of the wafer. This step was added after initial experiments indicated that the SU-8 employed in the next step would enter the etched areas. Scattered light during the SU-8 exposure step resulted in an undesirable residue in the etched areas.

The next step was the deposition of the dielectric layer. SU-8 is a commonly used thick film negative photoresist in MEMS for a variety of reasons. We have manually tested the breakdown voltage of SU-8, and have found it to be suitable for our application. Using a spin coater, we deposited a 25 µm layer of SU-8 and patterned it by photolithography. The developer used to pattern SU-8 also dissolved the Shipley 1827, resulting in the removal of both materials simultaneously. Fig. 4 is the scanning electron microscope (SEM) image of a finished device.

3.2. Mask design: Several important issues were considered during the mask design process. Two masks were used in our fabrication process. The first mask was used to define the emitter tips as well as the required nitride structures on the silicon substrate. A second mask was required to form holes and channels in the dielectric layer. The masks were overall very similar, but had subtle differences, particularly in the tip areas. The most important requirement for the first mask was a design that resulted in sharp emitter tips while providing reservoirs and

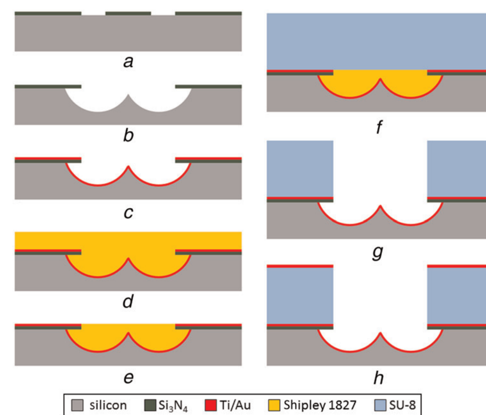

Fig. 3 *Cross-sectional illustration of process flow*
a Deposit and pattern 3000 Å Si_3N_4
b HNA etch
c Thermal evaporation of 200 Å Ti followed by 1000 Å Au
d Fill cavity with Shipley 1827
e Expose and develop Shipley 1827
f Spin 25 µm SU-8
g Expose and develop SU-8
h Au/Ti gate electrode metallisation

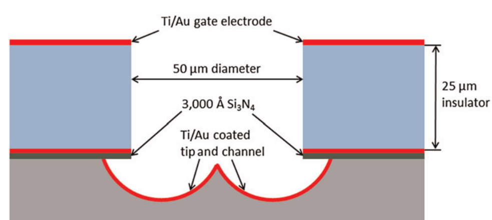

Fig. 2 *Illustration of the desired geometry of an emitter tip*

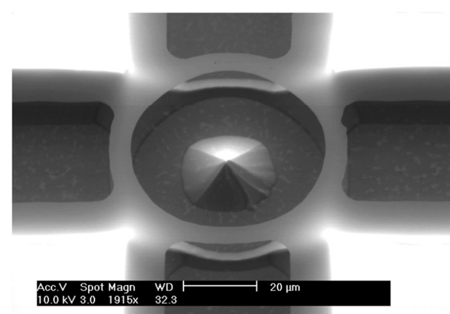

Fig. 4 *SEM image displaying hanging silicon nitride structures*

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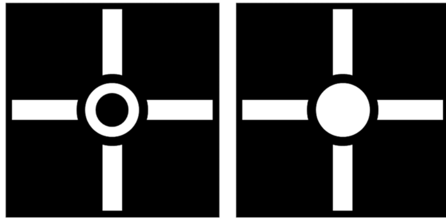

Fig. 5 *Single emitter mask design: pattern on the left is used to pattern the silicon nitride mask for HNA etch. The pattern on the right is used to pattern both the cavity-filling Shipley 1827 and the SU-8 dielectric spacer layer. The final masks contain nine copies of this design arranged in a 3 × 3 array*

channels for indium flow. To accomplish this, we designed a mask with donut shaped holes (Fig. 5). In an isotropic etchant, silicon is removed in all directions at approximately the same rate. Thus, the etchant will gradually undercut the centre nitride caps while etching downwards, creating silicon plateaus with caps of silicon nitride. Eventually, the diameter of the plateau is reduced to a point and the nitride cap falls off, forming tips (Fig. 4). The diameter of the centre caps has an immediate impact on the shape of the tips. We have found the optimum size for these centre caps to be ∼25–30 μm. For our final design, 30 μm caps were employed because of other considerations that will be discussed shortly.

To provide the indium channels and reservoirs, we incorporated wide spaces around the perimeter as well as rectangular holes between all tips and reservoirs. Extending the indium flow channels into the annular tip etch area would disrupt electrical continuity between all the gate electrodes, and could possibly affect the final tip form. To maintain continuity, a thin strip of silicon nitride was provided to separate the tip holes from the channels. During etching, the silicon beneath this strip was removed and the nitride was left as a hanging structure, producing a channel for indium to reach the tip. The time required to etch the silicon underneath these thin strips must be similar to the time required to produce the emitter tips.

The major difference between first and second masks is the lack of the centre circles of the first mask. These circles are not required, because our second mask is used only for patterning the dielectric with holes 50 μm in diameter on top of the emitter tip wafers. Since maximum efficiency is achieved when the tips and accelerating electrode are coaxial, alignment of the structures is essential.

3.3. Isotropic etch of silicon: After nitride etching, the exposed silicon is isotropically etched. An isotropic etchant was selected to provide uniform etching in all directions to produce conical emitter tips. Fabrication processes using anisotropic etches instead produce pyramidal structures aligned with the crystal planes of the silicon [20]. Though in theory isotropic etches should remove silicon in all directions at the same rate, in practice there is some deviation from a completely isotropic process. For our process, the ratio of lateral to depth etch rate is crucial. This ratio can drastically affect the shape of the fabricated emitter tips, and thus the efficiency of the entire system.

The most common dry isotropic etch of silicon in the past has been a tailored RIE process [21]. These processes are primarily used as a means of sharpening tips after a basic structure has been established. However, when used as the primary etch, etch rates can be extremely slow and tend to leave very rough surfaces behind on the silicon substrate. It is almost impossible to establish the necessary electric fields over such a surface, even with a sharp tip.

Another silicon dry etch process uses xenon difluoride (XeF_2). Xenon difluoride has been shown to have very good selectivity for etching silicon compared with almost any other common material used in MEMS. Cone structures have been fabricated using xenon difluoride in combination with a mask similar to ours [22].

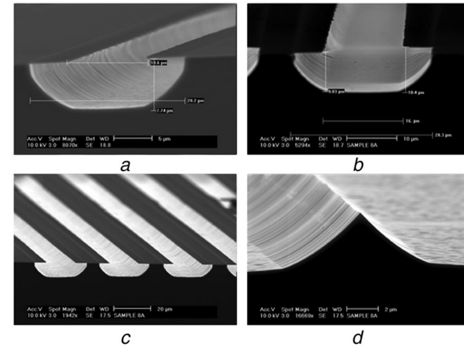

Fig. 6 *SEM images of HNA etch characterisation*
a Partial etch to a depth of 7.7 μm while lateral undercut reaching 4.8 μm
b Partial etch continued
c Etch uniformity test
d Final release of nitride cap

However, by using an HNA etch we were able to achieve better results in terms of surface texture, tip radius, and repeatability.

HNA is a combination of hydrofluoric, nitric, and acetic acid. Nitric acid reacts with the surface of silicon, forming layers of silicon dioxide isotropically. Hydrofluoric acid then dissolves the silicon dioxide, completing the silicon etch. Acetic acid is used as a buffer. Several factors can affect the results of HNA etch. First, the concentrations of the acids in the solution have dramatic effects on the rate of etch, the finished surface of the silicon, and the lateral to depth etch ratio – all of which have vital effects on the shape of the completed emitter tips. Temperature, agitation while etching, etching time, and area of the surface to be etched all impact the quality and rate of the etch process in various ways.

We performed a variety of tests with different concentrations of acids to track the progress of a silicon etch with HNA over time. Three different formulations were tested (hydrofluoric:nitric: acetic) – 1:3:1, 1:7.5:3, 1:2:2. SEM images of etch rate tests are shown in Fig. 6. From similar images, we were able to determine the best concentration ratio and timing to achieve the most efficient emitter tips. We were also able to calculate an accurate lateral to depth etching ratio for each of the different HNA solutions, which is essential to mask design as well as to the characterisation of the emitter tips after they have been fabricated. The process we have developed and described here can be repeated with high fidelity. After we completed characterisation of HNA etching, we were able to routinely achieve emitter tips with tip radii of <100 nm. Some emitters with tip radii as small as 50 nm are shown in Fig. 7.

3.4. Metallisation: After etching, the tips are coated with a metal layer consisting of 200 Å of titanium and 1000 Å of gold in order to improve the wetting and flow of the indium propellant. Surfaces that must be coated include the reservoirs for

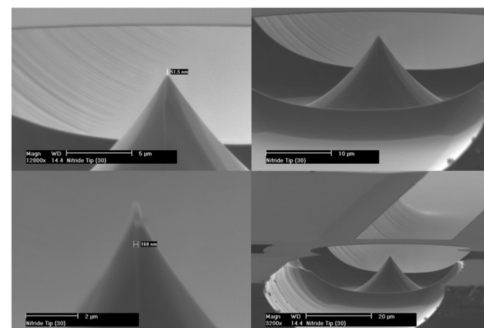

Fig. 7 *SEM images of emitter tips showing tip radii about 50 nm*

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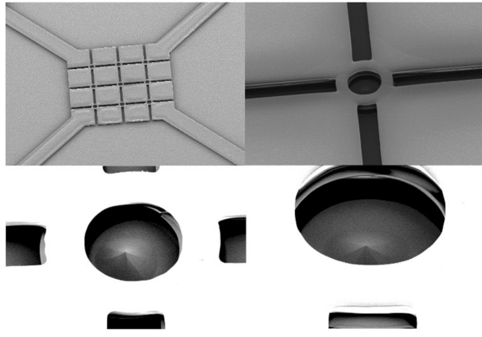

Fig. 8 *SEM images of completed devices*

introducing the indium, the channels for indium flow, and the regions surrounding the tips. Preliminary tests indicate low contact energy between indium and gold. Provided that melting is performed in an atmosphere which prevents the formation of a surface oxide, indium will spontaneously flow over the gold surface. We deposit both metals using a thermal evaporation process, because our thermal evaporator is equipped with a rotation fixture to permit uniform deposition, including areas under the overhanging nitride structures.

3.5. Dielectric: Previous calculations have suggested that a 25 µm dielectric layer with a 50 µm diameter gate electrode provides an optimum geometry for most efficient indium emission. Our application requires a dielectric capable of withstanding over 300 V without breakdown that can be fabricated without damage to the emitter tips. We initially considered several different materials before continuing with polyimide, parylene, and SU-8.

Several manufacturers offer photo-definable polyimide materials. They can be spin coated, exposed to UV light, developed, and cured in the same manner as conventional photoresists. A 25 µm cured film has a breakdown voltage in excess of 1000 V. However, achieving the required feature resolution proved to be very difficult using photolithography techniques. We obtained satisfactory results using deep reactive ion etching to etch cured polyimide films, but this process required a number of additional steps to prepare the etch mask.

Parylene is a popular dielectric material that is currently used as an encapsulating material in electronic devices, as well as for structural applications in MEMS. Its breakdown voltage is well above our required limit (>1000 V), and thick layers are easily deposited using automated equipment. Due to the nature of the deposition process, etching is the only option for patterning a layer of parylene. We found that the conditions necessary for etching parylene also caused pitting of our metal layers. A different metal layer composition might circumvent this, but may not have the desired wetting properties exhibited by the gold layer.

SU-8 is a commonly used negative photoresist in MEMS, due to its good mechanical properties and the relative ease with which it can be patterned into high aspect ratio features [23]. Our original fabrication scheme entailed spinning a 25 µm layer of SU-8 directly onto the wafer and patterning it using standard lithography techniques. During UV exposure, light scattering from the etched surfaces resulted in cross-linking of SU-8 in areas blocked by the mask, including over the tips. In order to circumvent this problem, we filled the etched regions of the wafer with photoresist prior to coating with SU-8. Both layers are patterned with the same mask. As Shipley 1827 is a positive photoresist, the result is a Boolean complement to what is produced when patterning SU-8. A 25 µm layer of SU-8 is then applied and patterned. When we develop this wafer in PGMEA, the Shipley photoresist and the SU-8 are simultaneously removed.

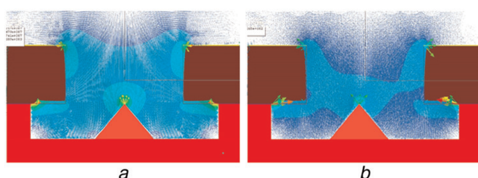

Fig. 9 *Electric field simulations of a FEEP emitter*
a With ideal geometry
b With a 3 µm misalignment between the gate electrode and the tip

3.6. Gate electrodes: The accelerating (gate) electrode consists of a second titanium/gold layer deposited on the top surface of the SU-8 dielectric layer. This metal layer is deposited using an electron beam evaporation source. As the e-beam system is not equipped with a sample rotation mechanism, the deposition is essentially perpendicular to the surface. The line of sight deposition ensures that the accelerating electrode is not shorted to the wafer.

Fig. 8 shows the SEM images of our completed device. As can be seen, the centres of the tips do not exactly coincide with the centre of the accelerating electrodes. Although substantial misalignment may adversely affect mass efficiency, electrostatic simulation reveals that these effects are not significant for the slight deviation of our device.

4. Electrostatic simulation: We performed two-dimensional electrostatic simulations using the dimensions obtained from SEM photographs of our actual device using Maxwell software (Ansoft Corporation). These results are summarised in Fig. 9. As can be seen from Fig. 9*a*, electric fields on the order of 10^7 V/m are achieved only at the tips. With the application of 300 V at the gate electrodes and the formation of Taylor cones of indium, the required electric fields of 10^9 V/m for ionisation of the indium will be easily achieved. We are therefore confident that our prototypes meet functional requirements as MEMS FEEP thrusters.

Some issues exist with misalignment of tips with the gate electrodes. Simulations have been performed with misalignment values very close to what is observed in the SEM pictures. The electric field at the tip is not significantly reduced. More complicated electrostatic simulations with our given parameters reveal our device to be functional, even with misalignment, as shown in Fig. 9*b*.

5. Conclusion: We have described the development of the first MEMS process for field-emission tips that could be used as part of a FEEP thruster. This entailed the fabrication of a 3×3 array of FEEP emitter tips, complete with a 25 µm thick dielectric layer of SU-8 and extraction electrode. Metal layers were provided to ensure that the proposed propellant, indium, will adequately wet the surface of the emitter tips. Electrostatic simulation has indicated that the necessary electric field values resulting in indium emission could be achieved with our tip dimensions and dielectric thickness. Future work will include loading the prototype with indium and conducting performance tests to measure thrust, mass efficiency, specific impulse, and other important device characteristics. The scale-up development should include extensive studies on the device-to-device geometric tolerance to satisfy functional requirements and experimental characterisation of fabrication variability. Strategies to enhance device-to-device consistency to meet the tolerance requirement would be crucial next steps to achieve arrays as large as 6400 tips.

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