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Ultra Wide-Band Circulator through Sequentially-Switched Delay Line (SSDL)

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Ultra Wide-Band Circulator through
Sequentially-Switched Delay Line (SSDL)

A thesis submitted in partial satisfaction
of the requirements for the degree Master of Science
in Electrical Engineering

by

Mathew Michael Biedka

2016
ABSTRACT OF THE THESIS

Ultra Wide-Band Circulator through Sequentially-Switched Delay Line (SSDL)

by

Mathew Michael Biedka

Master of Science in Electrical Engineering
University of California, Los Angeles, 2016
Professor Yuanxun Wang, Chair

Achieving non-reciprocity through unconventional methods without magnetic material has been a topic of great interest in past years. Towards the effort to achieve non-reciprocity, a time switching strategy is proposed that resembles real-time traffic flow. This technique is known as Sequentially-Switched Delay Line (SSDL), which is used to produce a true passive circulator over a broad frequency range. The SSDL concept essentially consists of six transmission lines of equal length with a specified time delay, along with 5 SPDT switches. Each switch is turned on and off sequentially, which allows for the simultaneous transmission and receiving of signals. Results are presented with and without filtering with the transmission lines switched on and off at 6MHz. Non-reciprocal behavior is observed from 200KHz to 200MHz. Theory and experiments show that the SSDL concept is a promising alternative to traditional circulators while offering ultra wide-band performance.
The thesis of Mathew Michael Biedka is approved.

Tatsuo Itoh

Yahya Rahmat-Samii

Yuanxun Wang, Committee Chair

University of California, Los Angeles

2016
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Chapter 1

Introduction

1.1. Background on traditional circulators and limitations

Traditional circulators have found extensive use in various communication systems as a means of separating transmitted and received signals. It is widely accepted that a three-port passive component that is lossless and matched requires the use of non-reciprocal, ferrite-based magnetic materials [1], [2]. Ferrite circulators are effectively cavities that have the ability to support non-reciprocal resonant modes. This classical form of the circulator doesn’t possess wideband performance, and is not easily incorporated into modern integrated circuits (ICs). In addition to the cavity circulator, active circulators have been realized based on the non-reciprocal transfer behavior of transistors. As a comparison with traditional circulators, they occupy a smaller physical area and are compatible with IC technology [3]-[5]. On the other hand, active circulators tend to have a limit on their noise and power performance. These shortcomings keep them from being utilized in systems that require high dynamic range [6]-[8].

1.2. Recent developments in circulator realizations

The realization of non-reciprocity without exploiting magnetic materials has been introduced in a number of previous works in which the dielectric property of a conventional transmission line was parametrically modulated. This concept, which is appropriately named as the Time-Varying Transmission Line (TVTL), breaks space-time symmetry and allows for non-reciprocal behavior [9]-[11]. The lowest operating frequency utilizing this concept is inherent upon the longest delay of the TVTL that can be implemented. This could potentially lead to a large on-chip area for operation at the low end of the RF spectrum. Also, the isolation capabilities of the TVTL circulator over a large bandwidth are limited by a SINC function. A
more complex non-uniform modulation scheme or balanced architecture could improve the isolation. In order to realize non-reciprocity without the use of parametric modulation, the Sequentially-Switched Delay Line (SSDL) concept is used to create a passive circulator over a large frequency range.

1.3. Thesis Outline

This work presents a true passive circulator that is realized by utilizing the Sequentially-Switched Delay Line concept. A rigorous look at the theory behind the SSDL concept will be presented first, followed by the initial system specifications and setup. Here, the original physical layout is observed along with the problems and solutions that accompanied its design. Next, the final experimental setup is presented along with data that verifies its successful operation. Lastly, concluding remarks are given along with some courses of action for the future.
Chapter 2
The SSDL Concept

2.1. Explanation of Signal Propagation

As a precursor to Fig. 2.1.1 to Fig. 2.1.5 that explains the operation of the SSDL circulator, it is necessary to provide some explanations on the behavior of the entire system. Each switch is effectively turned “on” to the correct transmission line for a time of 2T, and each figure is with respect to the switching position of the T/R and R/T switches. The transmitted wave leaves the transmitter switch, which is labeled TX. The signal is split into two waves, each with a duration of 2T. One of these two waves traverses a path from TX along T1, through the T/R switch, along the length of A1, and finally to the antenna switch, which is designated as ANT. The other transmitted wave follows a path from TX along T2, through the R/T switch, along A2, and finally to the ANT switch. The switches are turned on to the correct transmission lines right before the transmitted signal arrives, so that the signal can pass without reflection or alteration to the waveform. Also, the switches are effectively turned “off” by switching to the opposite transmission line immediately after the transmitted wave departs. The two transmitted pulses are then combined at the ANT switch port. This means that the same transmitted signal from the TX port leaves the ANT port with a delay time of 2T. Similarly, the received wave is split into two pulses, each with a duration of 2T, by the ANT switch. However, the received signal is divided into two pulses with a time delay of 2T with respect to the TX switch. The control signal sequence for the SSDL circulator is presented in Fig. 2.1.5, which demonstrates the time delay of 2T for the ANT switch. One of the received pulses travels a path from ANT along A2, through the R/T switch, along R2, and lastly to the receiver, which is designated as RX. The other received wave follows a route from ANT along A1, through the T/R switch, along
R1, and finally to the RX switch. As with the transmitted pulses, the switches are turned on to the correct path right before the received signal arrives. This allows for the received signal to propagate without being disturbed. Immediately after the signal passes, the switches are effectively turned “off” by switching to the other signal path. Since the transmitted and received signals are non-stop in time, there must always be a transmitted and received signal that populates a total of 2T of transmission line length.

With these operating characteristics in mind, Fig. 2.1.1 will begin an in-depth explanation of how signals propagate through the SSDL circulator. The red arrows represent the transmitted wave, and the blue arrows represent the received electromagnetic wave.

![Image of SSDL Circulator Diagram]

**Figure. 2.1.1: Principle of Operation for the SSDL Circulator at time 0\(^+\). Above are the positions of the transmitted and received waves at time 0\(^+\).**

This figure represents the locations of the transmitted as well as received waves at time 0\(^+\). The (+) sign indicates that the devices have just completed their switching action. The T/R and R/T switches have just moved to the transmission lines T1 and R2, respectively. The TX and RX switches have been in their current state for a time of T\(^+\), which allows for the first transmitted
pulse to leave TX and populate T1. Also, the second received pulse is observed populating the R1 transmission line which arrives at the RX port. The ANT switch has also been on for time $T^+$, which allows for the first received pulse to begin populating A2. Also, the second transmitted pulse populates A2 and arrives at the ANT switch. The ANT switch will always have a switching action that is opposite to that of TX and RX. This is because the control signal for the ANT is delayed by $2T$ relative to TX and RX. The transmitted and received signals that simultaneously populate A2 will not interfere with each other because the complete waveform has a duration of $2T$, while each transmission line has a duration of $T$.

Next, time is shown progressing to $T^+$ in Fig. 2.1.2 as shown below.

![Figure 2.1.2: Principle of Operation for the SSDL Circulator at time $T^+$. Above are the positions of the transmitted and received waves at time $T^+$.](image)

Here, we can see the updated positions of the transmitted and received signals at time $T^+$. In these figures, each instance in time is with respect to the switching action of the T/R and R/T switches. This indicates that the TX, RX and ANT switches flip from their previous positions in Fig. 2.1.1, and the T/R and R/T switches remain in their respective positions. Now, the first
transmitted pulse populates the complete 2T length of transmission line from T1 to A1. Also, the first received pulse is allowed to populate the entire 2T length of transmission line from A2 to R2. The switches are now in the proper positions so that the first transmitted pulse can be captured at the ANT port, and the first received wave can be collected at the RX port. It is worth noting that right before the switches flipped, the second transmitted pulse was captured at the ANT port, and the second received pulse arrived at the RX port.

Time is now allowed to move to 2T+, as shown below in Fig. 2.1.3.

![Diagram](image)

Figure. 2.1.3: Principle of Operation for the SSDL Circulator at time 2T+. Above are the positions of the transmitted and received waves at time 2T+.

Now, the transmitted and received waves are observed in the SSDL circulator at time 2T+. The T/R and R/T switches have finished their switching action after being in their previous states for time 2T. The TX, RX, and ANT switches remain in their respective positions. The first transmitted pulse populates A1 and can be seen entering the ANT port. At the same time, the second received pulse exits the ANT port and propagates along A1. The first received pulse can
be seen entering the RX switch along transmission line R2, and the second transmitted pulse has left TX and populates T2.

Moving ahead to time $3T^+$ takes us to Fig. 2.1.4 as shown below.

![Figure 2.1.4: Principle of Operation for the SSDL Circulator at time $3T^+$. Above are the positions of the transmitted and received waves at time $3T^+$.](image)

Here, we can visualize where the transmitted and received pulses are in the circuit at time $3T^+$. The T/R and R/T switches stay in their respective positions. The TX, RX, and ANT switches have completed their switching action after being in their previous states for a time of $2T$. The second transmitted pulse now populates the entire $2T$ length of transmission line from T2 to A2. Also, the second received pulse is allowed to populate the entire $2T$ length of transmission line from A1 to R1. If time progresses further to $4T^+$, the transmitted and received waves will return to their positions as seen in Fig. 2.1.1.

Below, the control sequence diagram is presented as Fig. 2.1.5.
Figure. 2.1.5: Control Sequence Diagram for the SSDL Circulator. $V_{sw1}(t)$ controls the TX and RX switches, $V_{sw2}(t)$ controls the T/R and R/T set of switches, and $V_{sw3}(t)$ provides the control signal for the ANT switch.

2.2. Theoretical Derivations for the Transmitted Wave

To provide a more complete analysis of the SSDL circulator, the following mathematical derivations are performed: The investigation begins by looking at the transmitted signal leaving the TX port. The original signal is denoted as $TX(t)$. The upper branch is denoted as “a” where
the first TX pulse, denoted as $TX^{(a)}(t)$, travels a transmission line sequence from T1 to A1, and finally to the ANT port. $V_{sw1}(t)$ has the following summation representing its switching behavior:

$$V_{sw1}(t) = \sum_{n=0}^{\infty} u(t - 2nT)(-1)^n$$  \hspace{1cm} (2.2.1)$$

According to Eq. 2.2.1, $V_{sw2}(t)$ and $V_{sw3}(t)$ are respectively defined as follows:

$$V_{sw2}(t) = V_{sw1}(t - T)$$  \hspace{1cm} (2.2.2)$$

$$V_{sw3}(t) = V_{sw1}(t - 2T)$$  \hspace{1cm} (2.2.3)$$

$V_1(t)$ represents the wave just to the right of the TX switch that populates T1. $V_1(t)$ has the following expression:

$$V_1(t) = TX^{(a)}(t)V_{sw1}(t)$$  \hspace{1cm} (2.2.4)$$

Next, $V_2(t)$ represents the signal just to the right of the T/R switch. It is the multiplication of $V_1(t)$ delayed by time $T$, and $V_2(t)$. The following expression represents $V_2(t)$:

$$V_2(t) = V_1(t - T)V_{sw2}(t) = TX^{(a)}(t - T)V_{sw1}(t - T)V_{sw2}(t)$$  \hspace{1cm} (2.2.5)$$

Finally, $V_3(t)$ represents the signal just before it leaves the ANT port. $V_3(t)$ has the following form:

$$V_3(t) = V_2(t - T)V_{sw3}(t) = TX^{(a)}(t - 2T)V_{sw1}(t - 2T)V_{sw2}(t - T)V_{sw3}(t)$$  \hspace{1cm} (2.2.6)$$

After referencing Fig. 2.1.5, it can be concluded that $V_{sw1}(t - 2T)$, $V_{sw2}(t - T)$, and $V_{sw3}(t)$ are all equivalent to each other. Therefore, Eq. 2.2.6 reduces to the following:

$$V_3(t) = TX^{(a)}(t - 2T)$$  \hspace{1cm} (2.2.7)$$

Eq. 2.2.7 explains that the signal leaving the TX port through upper branch “a” is the same signal that appears at the ANT port. The only difference is that the signal at the ANT port is delayed by $2T$, which is expected.
The analysis performed on the lower branch “b” is similar to that completed in the above section for upper branch “a”. In this case, the second TX pulse, designated as $TX^{(b)}(t)$, traverses a path from T2 to A2, and lastly to the ANT switch. $V_{sw1}(t)$ has the following summation to represent its switching behavior:

$$V_{sw1}(t) = \sum_{n=0}^{\infty} u(t - 2nT)(-1)^{n+1}$$  \hspace{1cm} (2.2.8)

According to Eq. 2.2.8, $V_{sw2}(t)$ and $V_{sw3}(t)$ respectively have the following forms:

$$V_{sw2}(t) = V_{sw1}(t - T)$$  \hspace{1cm} (2.2.9)

$$V_{sw3}(t) = V_{sw1}(t - 2T)$$  \hspace{1cm} (2.2.10)

First, $V_1(t)$ represents the signal just to the right of the TX switch which presently populates T2. $V_1(t)$ has the following form:

$$V_1(t) = TX^{(b)}(t)V_{sw1}(t)$$  \hspace{1cm} (2.2.11)

Next, the expression for $V_2(t)$ is constructed. This is the expression of the transmitted signal just after it leaves the R/T switch. It is the signal $V_1(t)$ delayed by time T, multiplied by the control signal for the R/T switch as shown below:

$$V_2(t) = V_1(t - T)V_{sw2}(t)$$  \hspace{1cm} (2.2.12)

Lastly, $V_3(t)$ is the signal just before it leaves the ANT port. $V_3(t)$ is $V_2(t)$ delayed by time T, multiplied by the switching signal for ANT as constructed below:

$$V_3(t) = V_2(t - T)V_{sw3}(t)$$  \hspace{1cm} (2.2.13)
Using similar logic as with the upper branch “a”, the control signals in Eq. 2.2.13 are all equivalent. This means that $\bar{V}_3(t)$ reduces to the expression seen below:

$$\bar{V}_3(t) = TX^{(b)}(t - 2T)$$  \hspace{1cm} (2.2.14)

Eq. 2.2.14 validates that the original signal leaving the TX port is the same signal that arrives at the ANT port. It is shifted by a time of $2T$ after traveling along the lower branch “b”, as expected.

The signals $V_3(t)$ and $\bar{V}_3(t)$ are combined at the ANT port so that the entire signal $TX(t - 2T)$ is guided out of the ANT port. Using a similar process, the same conclusions can be drawn for the signal path from ANT to RX.
Chapter 3

Initial Experimental Setup

3.1. Preliminary layout and calculations

Fig. 3.1.1 presents the initial design of the SSDL circulator.

![Initial SSDL circulator layout.](image)

There are six equal length transmission lines that are used to connect 5 SPDT switches. SPDT stands for single-pole double-throw. The TX switch can be seen on the upper left of Fig. 3.1.1, along with the RX switch on the lower left. The T/R switch is positioned to the right of the TX switch, and the R/T switch is positioned to the right of the RX switch. The ANT switch is positioned at the far right of the figure. The 5 SPDT switches are commercially available from Mini-circuits (part number ZFSW-2-46). Referring back to Fig. 2.1.5, the switching time for each device in the SSDL circulator equates to a period of 4T. This means that each switch is “on” for a time of 2T, and then “off” for a duration of 2T. For this design, the switching
frequency was chosen to be approximately 30MHz. These parameters were used to solve for $T$ in the following equation:

$$\frac{1}{4T} = (30 \times 10^6)$$  \hspace{1cm} (3.1.1)

Solving for $T$ gives:

$$T \approx 8.33ns$$  \hspace{1cm} (3.1.2)

Next, the following distance formula was used as an approximate figure to calculate the cable length needed:

$$d = rt$$  \hspace{1cm} (3.1.3)

The coaxial transmission lines that were selected for this design are commercially available from Crystek Corporation. The data sheet specified a velocity of propagation of 0.7 times the speed of light in free space.

The factor of 0.7 can be explained by the propagation of electromagnetic waves through a dielectric media. Here, the velocity is decreased due to the properties of the medium that the wave is traveling through. The dielectric material for the coaxial cable is PTFE, which stands for Polytetrafluoroethylene. This material has a relative permittivity of 2.1, meaning that the velocity of propagation in the coaxial cable is:

$$V = \frac{c}{\sqrt{\varepsilon_r}} = \frac{c}{\sqrt{2.1}} = 0.7c$$  \hspace{1cm} (3.1.4)

Using this information, along with $t = T = 8.33ns$, distance can be solved for as follows:

$$d = 0.7 \times c \times T = 1.75m$$  \hspace{1cm} (3.1.4)

After converting meters to feet, a cable length of 5.74 feet was desired. Finally, a standard cable length of 6 feet was selected from Crystek Corporation (Manufacturer part number CCSMA18-MM-086F-72).
The next phase of the system setup was to measure the delay time of each of the six transmission lines in the circulator layout. The delay time was calculated using an S-parameter network analyzer manufactured by Agilent (part number 8753ES). The network analyzer was first calibrated to ensure that the measurements were as exact as possible. Next, one end of the coaxial cable was attached to the FWD port of the analyzer, while the opposing end was attached to the REV port of the analyzer. This allowed for the delay time to be measured as an RF signal was passed through the transmission line. The network analyzer test power was set at 0dBm, with start and stop frequencies of 10MHz and 1.2GHz, respectively. Delay time measurements were taken at around 600MHz. Table 3.1.1, shown below, gives the delay time measurements for each of the six cables used for this preliminary setup. Each coaxial cable was labeled with a piece of tape before it was measured.

<table>
<thead>
<tr>
<th>Transmission Line Number</th>
<th>Delay Time [ns]</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>8.57</td>
</tr>
<tr>
<td>2</td>
<td>8.57</td>
</tr>
<tr>
<td>3</td>
<td>8.59</td>
</tr>
<tr>
<td>4</td>
<td>8.57</td>
</tr>
<tr>
<td>5</td>
<td>8.60</td>
</tr>
<tr>
<td>6</td>
<td>8.59</td>
</tr>
</tbody>
</table>

Table 3.1.1: Delay times for the Crystek Corporation coaxial cables. Each transmission line was measured using the Agilent 8753ES S-parameter network analyzer.

As can be seen by the above data, all of the six coaxial cables measured within 0.05ns of each other.

After successfully capturing the delay time data for the six transmission lines, the next step in the measurement process was to verify the operation of a single switch with a 10MHz
signal incident upon its input port. The input signal was chosen to be a 10MHz, 1Vpp sine wave with no phase delay or offset. This input signal was provided by a Tektronix Arbitrary Function Generator (part number AFG3021). The control signals for the switch were provided by a Sony Tektronix Arbitrary Waveform Generator (part number AWG520). The time delay for the Crystek coaxial cables was slightly higher than 8.33ns that was calculated theoretically. Because of this, a 29MHz rectangular pulse operating at a duty cycle of 50% was chosen to switch the input signal between the two output RF paths. To verify that the 29MHz signal was a better choice for the switching speed, the calculation for $T$ was rerun:

$$\frac{1}{4T} = (29 \times 10^6)$$

(3.1.5)

Solving for $T$ gives:

$$T \approx 8.62\text{ns}$$

(3.1.6)

This switching frequency provides a time delay that is 0.05ns higher than the measured cable delay time, at the worst case. This result agrees much better with the experimental setup as opposed to the 0.25ns difference provided by the 30MHz signal. The Mini-Circuits SPDT switch was set up for measurements as follows: A 10MHz, 1Vpp sine wave was provided to the switch input, with the two RF outputs monitored on a Tektronix Digital Phosphor Oscilloscope (part number TDS7404). Two of the digital outputs available from the AWG520 were used to generate two 29MHz rectangular pulses. The pulses were manually adjusted on the AWG520 so that the 50% on-time was switched between the RF outputs 1 and 2. This makes sure that each RF switch is on for a time of $2T$. The RF outputs measured on the oscilloscope showed a signal loss of approximately 40% from the input for the single switch, which equates to a loss of approximately 4.5dB. This amount of loss from a single switch varied greatly from the 1.1dB listed on the Mini-Circuits data sheet. The initial thought was that the SPDT switch was reaching
saturation, due to a high input level. However, a 1Vpp RF signal equates to approximately +4dBm, which is well under the +24dBm maximum as quoted on the data sheet. It was also noted that the AWG520 is unable to provide the DC voltage level in order to turn the device fully “on”. With these things in mind, the decision was made to progress to the construction of the entire circulator with the available equipment.

Next, the SSDL circulator layout was fabricated to realize the theory as explained using Fig. 2.1.1 to Fig. 2.1.5. There are a total of 10 digital outputs available from the Sony Tektronix Arbitrary Waveform Generator (part number AWG520). The 5 SPDT switches in the SSDL circulator layout each require 2 control signals, so all of the digital outputs were utilized. The TX and RX switches were controlled with the 29MHz rectangular pulses from the AWG520 as described previously. These control signals correspond to $V_{sw1}(t)$. The T/R and R/T switches were controlled by the same 29MHz signals, but delayed by approximately 8ns. Obviously, the optimal time delay of these control signals would have been 8.6ns, but the manual adjustments performed on the AWG520 to achieve this exact figure were unsuccessful. The control signals used to operate the T/R and R/T switches corresponds to $V_{sw2}(t)$. Finally, the ANT switch is operated with the same control signals as the TX and RX switches. However, the control inputs for the ANT switch are in opposition to those of the TX and RX switches. This enforces the requirement that the ANT switch is controlled by $V_{sw3}(t)$. For the first test of the circulator, a 10MHz 1Vpp sine wave was applied to the input of the TX switch. The RX and ANT outputs were monitored on the oscilloscope. The control signals were applied first, followed by the RF input signal. The signal level measured at the ANT output equated to a loss of approximately 14dB, which was much higher than the 5 or 6dB that was expected. Speculation about the high amount of loss was centered around the potential saturation of the RF switches, even though the
1Vpp signal was well below the maximum specified on the data sheet. Some courses of action were then proposed. First, individually test each switch under the same test conditions to find out what is causing the high amount of signal loss. Second, the cable length connecting the RF switches was to be increased. This would require a larger T, and a slower switching frequency.

3.2. Investigation of Possible Power Saturation Issues

In this section of the SSDL circulator development, the issue of potential switch saturation was investigated. The original SSDL circulator layout was disassembled so that each switch could be individually characterized under the same test conditions. The Sony Tektronix Arbitrary Waveform Generator (part number AWG520) has another signal output option that is referred to as a “marker”. This output was also utilized to generate 29MHz and 20.3MHz rectangular pulses to control the switches. The RF output levels of each individual switch for the two “marker” cases were judged against the same output levels generated using the digital outputs. The following table shows the first test using a 29MHz signal from the “markers” and digital outputs. The input for this test is a 10MHz 1Vpp sine wave with no phase delay or offset. This signal is provided by the Tektronix Arbitrary Function Generator (part number AFG3021).

<table>
<thead>
<tr>
<th>Switch Name</th>
<th>Output Level (using Markers) [mV]</th>
<th>Output Level (using digital outputs) [mV]</th>
</tr>
</thead>
<tbody>
<tr>
<td>TX</td>
<td>584</td>
<td>500</td>
</tr>
<tr>
<td>RX</td>
<td>588</td>
<td>512</td>
</tr>
<tr>
<td>MID1</td>
<td>792</td>
<td>688</td>
</tr>
<tr>
<td>MID2</td>
<td>780</td>
<td>688</td>
</tr>
<tr>
<td>ANT</td>
<td>528</td>
<td>468</td>
</tr>
</tbody>
</table>

Table. 3.2.1: Output levels for the switches used in the preliminary layout at 29MHz switching. The input is a 10MHz 1Vpp sine wave with no phase delay or offset.
Next, Table 3.2.2 presents data gathered when the “markers” and digital outputs are used to operate the switches at a frequency of 20.3MHz. The input signal specifications are the same as that presented in Table 3.2.1.

<table>
<thead>
<tr>
<th>Switch Name</th>
<th>Output Level (using Markers) [mV]</th>
<th>Output Level (using digital outputs) [mV]</th>
</tr>
</thead>
<tbody>
<tr>
<td>TX</td>
<td>660</td>
<td>572</td>
</tr>
<tr>
<td>RX</td>
<td>696</td>
<td>568</td>
</tr>
<tr>
<td>MID1</td>
<td>960</td>
<td>832</td>
</tr>
<tr>
<td>MID2</td>
<td>944</td>
<td>836</td>
</tr>
<tr>
<td>ANT</td>
<td>616</td>
<td>544</td>
</tr>
</tbody>
</table>

Table 3.2.2: Output levels for the switches used in the preliminary circulator layout at 20.3MHz switching. The input is a 10MHz 1Vpp sine wave with no phase delay or offset.

The results as presented in Tables 3.2.1 and 3.2.2, although approximate, provided some useful insights to the performance of the initial SSDL circulator design. As the above data shows, the “marker” outputs seem to be able to generate an output with less loss than that produced when using the digital outputs as control signals. Next, the output signal levels using the digital outputs show some interesting behavior. The TX, RX, and ANT switches experience signal losses of approximately 50% and 40% at switching rates of 29MHz and 20.3MHz, respectively. In contrast to these readings, the MID1 and MID2 switches experience signal losses of approximately 30% and 20% at switching frequencies of 29MHz and 20.3MHz, respectively.

The performance of the TX, RX, and ANT switches definitely played a role in the high amount of loss experienced during the initial test, as described in the previous section. Initially, it was speculated that these switches may have been damaged during the first power-on sequence of the circulator. This suspicion was quickly excused due to the exceptional performance of the MID1 and MID2 switches.
3.3. Further Characterizations

The conclusion was reached that the initial test of the SSDL circulator contained SPDT switches that varied in performance. A total of 10 ZFSW-2-46 switches were purchased from Mini-Circuits during the purchasing phase of the project. To get a better understanding of the performance of each individual switch, the remaining switches were characterized using the same testing scenario as in Section 3.2.

Table 3.3.1 represents the data collected when a 29MHz signal is used to control each switch. As in the previous section, data is gathered from both the “markers” and digital outputs.

<table>
<thead>
<tr>
<th>Switch Name</th>
<th>Output Level (using Markers) [mV]</th>
<th>Output Level (using digital outputs) [mV]</th>
</tr>
</thead>
<tbody>
<tr>
<td>Test Switch</td>
<td>684</td>
<td>592</td>
</tr>
<tr>
<td>Test Switch 2</td>
<td>736</td>
<td>656</td>
</tr>
<tr>
<td>Test Switch 3</td>
<td>704</td>
<td>596</td>
</tr>
<tr>
<td>Test Switch 4</td>
<td>740</td>
<td>680</td>
</tr>
<tr>
<td>Test Switch 5</td>
<td>520</td>
<td>444</td>
</tr>
</tbody>
</table>

Table 3.3.1: Output levels for the remaining switches from Mini-Circuits at 29MHz switching. The input is a 10MHz 1Vpp sine wave with no phase delay or offset.

It was quickly becoming apparent that some of the switches obtained from Mini-Circuits behaved differently from others under the same test conditions. Next, Table 3.3.2 presents data gathered when the “markers” and digital outputs are used to operate the switches at a frequency of 20.3MHz. The test specifications are the same as those presented in the previous table.
<table>
<thead>
<tr>
<th>Switch Name</th>
<th>Output Level (using Markers) [mV]</th>
<th>Output Level (using digital outputs) [mV]</th>
</tr>
</thead>
<tbody>
<tr>
<td>Test Switch</td>
<td>832</td>
<td>728</td>
</tr>
<tr>
<td>Test Switch 2</td>
<td>896</td>
<td>772</td>
</tr>
<tr>
<td>Test Switch 3</td>
<td>840</td>
<td>740</td>
</tr>
<tr>
<td>Test Switch 4</td>
<td>936</td>
<td>828</td>
</tr>
<tr>
<td>Test Switch 5</td>
<td>604</td>
<td>516</td>
</tr>
</tbody>
</table>

Table 3.3.2: Output levels for the remaining switches from Mini-Circuits at 20.3MHz switching. The input is a 10MHz 1Vpp sine wave with no phase delay or offset.

As can be seen in the above two tables, Test Switch 4 performed with output levels similar to those obtained using the MID1 and MID2 switches. Test Switch 5 performed similar to the TX, RX, and ANT switches. However, Test Switch 5 was not used in the initial layout and test of the SSDL circulator, as explained in Section 3.1. This led to the conclusion that the TX, RX, and ANT switches were not damaged during the preliminary test of the circulator.

The next step was to select two of the switches that performed the best, and connect them to simulate the output performance from TX to ANT. This method allowed for the exclusion of the middle switch, so that the amount of variability in the setup was decreased. MID1 was chosen to represent TX, and Test Switch 4 was utilized in place of the ANT switch. The RF connections were made using the same 6 feet cables from the initial setup. The input port of MID1 was fed with a 10MHz 1Vpp sine wave with no phase delay or DC offset. The output port of Test Switch 4 was monitored on the oscilloscope. Table 3.3.3 lists the output levels measured with a switching rate of 20.3MHz provided by both the “markers” and digital outputs.
Output Level (using Markers) [mV] | Output Level (using digital outputs) [mV]
---|---
768 | 616

Table. 3.3.3: Output levels for the two-switch configuration at 20.3MHz switching, case 1. The input is a 10MHz 1Vpp sine wave with no phase delay or offset.

The RF input was then adjusted to 2MHz, and data was taken from the two-switch configuration. This collected information is listed in Table 3.3.4 below.

<table>
<thead>
<tr>
<th>Output Level (using Markers) [mV]</th>
<th>Output Level (using digital outputs) [mV]</th>
</tr>
</thead>
<tbody>
<tr>
<td>796</td>
<td>644</td>
</tr>
</tbody>
</table>

Table. 3.3.4: Output levels for the two-switch configuration at 20.3MHz switching, case 2. The input is a 2MHz 1Vpp sine wave with no phase delay or offset.

This simple test showed that decreasing the RF input frequency improved the output signal integrity. To gather more data, the switching frequency was adjusted to 23.3MHz, and all of the remaining system parameters were left unchanged. Table 3.3.5 presents the signal levels recorded under the new switching rate.

<table>
<thead>
<tr>
<th>Output Level (using Markers) [mV]</th>
<th>Output Level (using digital outputs) [mV]</th>
</tr>
</thead>
<tbody>
<tr>
<td>840</td>
<td>684</td>
</tr>
</tbody>
</table>

Table. 3.3.5: Output levels for the two-switch configuration at 23.3MHz. The input is a 2MHz 1Vpp sine wave with no phase delay or offset.

The question still remained as to why the signal output was lower when using the digital outputs to control the switches. Two of the digital outputs were compared against two “markers” on the oscilloscope. It was discovered that the digital output signals led the “markers” by 1ns. The waveform generator allows for slight manual adjustments of the time delay for output signals, so this property was exploited to correct the mismatch. Even after this adjustment, no signal improvement was witnessed.
As a final test with this two-switch setup, the digital outputs were used to control the switches. Now, the input was a 2MHz 500mVpp sine wave, with the output monitored on the oscilloscope. The switching rate can be adjusted manually under the “Horizontal” tab of the AWG520. The switching frequency was adjusted while monitoring the oscilloscope for the peak output signal level. With a switching rate of 23.75MHz, the output was recorded at 448mVpp, but the waveform had asymmetric peaks.

At this stage of testing, it was concluded that some switches performed better than others. Also, input frequency and amplitude, along with the switching rate had to be optimized to maximize the performance of the SSDL circulator. Further testing was still required.

3.4. New Approaches to System Troubleshooting

To further understand the behavior of each individual switch, the next course of action was to characterize all of the Mini-Circuits switches at a lower input amplitude level. The two digital output signals that were used for testing were first verified on the oscilloscope as the correct waveforms. A switching frequency of 23.75MHz was selected. The input of each switch was fed a 2MHz 500mVpp sine wave with no phase delay or DC offset. The exact same cables and test conditions were used to measure the output signal levels for all 10 Mini-Circuits switches. The results from this test are presented below in Table 3.4.1.
<table>
<thead>
<tr>
<th>Switch Name</th>
<th>Output Level (using digital outputs) [mV]</th>
</tr>
</thead>
<tbody>
<tr>
<td>TX</td>
<td>374</td>
</tr>
<tr>
<td>RX</td>
<td>356</td>
</tr>
<tr>
<td>MID1</td>
<td>500</td>
</tr>
<tr>
<td>MID2</td>
<td>500</td>
</tr>
<tr>
<td>ANT</td>
<td>326</td>
</tr>
<tr>
<td>Test Switch</td>
<td>500</td>
</tr>
<tr>
<td>Test Switch 2</td>
<td>500</td>
</tr>
<tr>
<td>Test Switch 3</td>
<td>500</td>
</tr>
<tr>
<td>Test Switch 4</td>
<td>500</td>
</tr>
<tr>
<td>Test Switch 5</td>
<td>316</td>
</tr>
</tbody>
</table>

Table 3.4.1: Output signal levels for all Mini-Circuits switches, case 1. Switching is carried out at 23.75MHz using the digital output signals. The input signal is a 2MHz 500mVpp sine wave without phase delay or a DC offset.

The above results showed that switches MID1, MID2, Test Switch, Test Switch 2, Test Switch 3, and Test Switch 4 performed very well under the analysis. However, the TX, RX, ANT, and Test Switch 5 devices experienced a signal loss of approximately 180mVpp at the worst case. To further explore these new findings, the same test was rerun, but with an input amplitude of 250mVpp. All of the test specifications are the same as described for Table 3.4.1, except that the new input amplitude is cut in half. This data was collected, and is presented below in Table 3.4.2.
<table>
<thead>
<tr>
<th>Switch Name</th>
<th>Output Level (using digital outputs) [mV]</th>
</tr>
</thead>
<tbody>
<tr>
<td>TX</td>
<td>202</td>
</tr>
<tr>
<td>RX</td>
<td>208</td>
</tr>
<tr>
<td>MID1</td>
<td>250</td>
</tr>
<tr>
<td>MID2</td>
<td>250</td>
</tr>
<tr>
<td>ANT</td>
<td>186</td>
</tr>
<tr>
<td>Test Switch</td>
<td>250</td>
</tr>
<tr>
<td>Test Switch 2</td>
<td>250</td>
</tr>
<tr>
<td>Test Switch 3</td>
<td>250</td>
</tr>
<tr>
<td>Test Switch 4</td>
<td>250</td>
</tr>
<tr>
<td>Test Switch 5</td>
<td>178</td>
</tr>
</tbody>
</table>

Table 3.4.2: Output signal levels for all Mini-Circuits switches, case 2. Switching is carried out at 23.75MHz using the digital output signals. The input signal is a 2MHz 250mVpp sine wave without phase delay or a DC offset.

The above results showed that switches MID1, MID2, Test Switch, Test Switch 2, Test Switch 3, and Test Switch 4 were able to reproduce the signal at the switch output with little to no loss. These are the same switches that performed exceptionally well in the previous 500mVpp input case. Again, it is discovered that the TX, RX, ANT, and Test Switch 5 devices experienced a signal loss of about 70mVpp at the worst case. It was now apparent that lowering the input amplitude helped to preserve the output signal level under the given test equipment and criteria. Although the source of the undesirable performance of 4 SPDT switches was not yet discovered, testing of the SSDL circulator continued with the 6 SPDT switches that performed the best. This would provide an additional switch as backup, in the event of another failure.

The next step was to rerun the test of the first SSDL design. The TX switch was replaced by Test Switch 2, RX was replaced by Test Switch, MID1 and MID2 were left the same, and
Test Switch 4 was utilized in place of ANT. It was also discovered during the verification of the AWG520 that digital output D1 was not functioning. Instead, 4 pairs of digital outputs along with a pair of “marker” outputs were used to control the 5 switches. The RF connections were made using the same 6 feet blue RF cables from the initial test of Section 3.1. The input port of the circulator, which was now Test Switch 2, was supplied a 10MHz 500mVpp sine wave without phase delay or a DC offset. The switching frequency was adjusted back to 28.75MHz to provide a more accurate replication of the initial test. The ANT and RX output ports were monitored on the oscilloscope. The signal outputs measured approximately 250mVpp and 20.8mVpp at the ANT and RX ports, respectively. These results were much better than those recorded during the initial test of Section 3.1, but the results could still be improved. So, testing progressed to an SSDL circulator with 30 foot cables connecting the SPDT switches, as explained in the following chapter. This new design would be implemented alongside a decrease in the input signal amplitude.
Chapter 4

Final Experimental Setup

4.1. Revised Layout and Calculations

Figure 4.1.1 shows the final design of the SSDL circulator.

![SSDL Circulator Diagram]

Figure. 4.1.1: Final SSDL circulator layout. The design consists of 6 coaxial cables of equal length and 5 SPDT switches.

The above figure has a physical layout that is very similar to that presented in Fig. 3.1.1. Using the previously discovered data, the TX, RX, and ANT switches were replaced by Test Switch 2, Test Switch, and Test Switch 4, respectively. The T/R and R/T switches are represented by MID1 and MID2, respectively. Also, 30 foot cables are used to connect the SPDT switches to realize the theoretical behavior described in Chapter 2. Each 30 foot section of transmission line is composed of two 15 foot coaxial cables, connected with an SMA female-to-female adapter. The coaxial cables are commercially available from Times Microwave Systems (part number LMR-195).
After assembling all six of the new transmission lines, the delay time of each cable was measured using the S-parameter network analyzer manufactured by Agilent (part number 8753ES). The network analyzer was calibrated with the 85033D 3.5mm Calibration Kit manufactured by HP. The input power was set to -20dBm, with start and stop frequencies of 200KHz and 200MHz, respectively. SMA female-to-female adapters had to be included at both ports of the network analyzer to enforce proper mating with the SMA male connectors of the test cable. So, the female-to-female adapters were attached to the FWD and REV ports of the network analyzer and included in the calibration for measurement preciseness. Table 4.1.1 presents the time delay data recorded for each 30 foot cable assembly, as shown below.

<table>
<thead>
<tr>
<th>Transmission Line Number</th>
<th>Delay time at 1.2MHz [ns]</th>
<th>Delay time at 125MHz [ns]</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>44.3</td>
<td>43.4</td>
</tr>
<tr>
<td>2</td>
<td>43.3</td>
<td>41.9</td>
</tr>
<tr>
<td>3</td>
<td>42.8</td>
<td>41.8</td>
</tr>
<tr>
<td>4</td>
<td>43.7</td>
<td>42.7</td>
</tr>
<tr>
<td>5</td>
<td>43.5</td>
<td>42.7</td>
</tr>
<tr>
<td>6</td>
<td>44.3</td>
<td>42.2</td>
</tr>
</tbody>
</table>

Table 4.1.1: Delay times for the Times Microwave coaxial cables. Each transmission line was measured using the Agilent 8753ES S-parameter network analyzer.

As the above data shows, the delay time for each cable assembly has a greater variability when compared to the delay times of the 6 foot cables. In reference to Fig. 4.1.1, transmission lines 1 through 6 correspond to T1, R1, T2, R2, A1, and A2, respectively. However, fabrication of the SSDL circulator continued. The delay was measured in real time on the network analyzer, and approximated to 44ns. This number was then used as the delay time T to calculate the new switching frequency.
The calculated switching frequency is consistent with the expectation that a factor of 5 increase in cable length corresponds to a factor of 5 reduction in the switching speed. The LMR-195 coaxial cables have a velocity of propagation that is 80% of the speed of light in free space. This factor comes from the presence of the dielectric in the cable. The dielectric is Foam PE, which has a dielectric constant of 1.56. Using this information, the velocity of propagation of the coaxial cable is:

\[
V = \frac{c}{\sqrt{\varepsilon}} = \frac{c}{\sqrt{1.56}} = 0.8c
\]  

\[\text{(4.1.2)}\]

The Sony Tektronix Arbitrary Waveform Generator (part number AWG520) was used to initially generate a 6MHz switching signal. The four sets of digital outputs along with a set of “marker” outputs were operated at this frequency to control the 5 SPDT switches. The following three sections present the results gathered using this experimental setup of the SSDL circulator.

4.2. Experimental Results Captured on the Oscilloscope

This section covers the data captured on the oscilloscope for the SSDL circulator utilizing the 30 foot cable arrangement. The input signal is supplied by a Tektronix Arbitrary Function Generator (part number AFG3021). A Mini-Circuits Low Pass Filter (part number BLP-1.9+) was attached at the ANT switch and RX switch outputs. Filtering was utilized at the ANT and RX ports to make identification of the waveforms more clear. The input signal is a 1MHz 250mVpp sine wave generated by the Tektronix AFG3021. Figure 4.2.1 showcases the signals captured by a Tektronix Digital Phosphor Oscilloscope (part number TDS7404). The data was collected from the oscilloscope and plotted using Matlab codes. Here, the input signal is supplied
to the low pass filter, which is attached to the ANT port. The RX and TX output ports are monitored on the oscilloscope.

Matlab scripts were used to calculate the peaks of each of the waveforms. The input signal incident upon the ANT port has a maximum value of 126mV, and the output seen at the RX port has a maximum value of 74mV. This corresponds to a 41.3% signal loss, or equivalently a loss of 4.6dB. The output waveform seen at the TX port has a peak value of 16mV. This equates to an 87.3% signal loss from the ANT port, which is approximately a loss of 17.3dB. These results show that the input signal is successfully recovered at the RX port. A very small signal is seen at the TX port which is expected.
Figure 4.2.2 represents the data gathered from the oscilloscope when the same input signal is supplied to the TX port. The ANT and RX ports are monitored on the oscilloscope channels. Again, Matlab codes were generated to plot the data collected from the oscilloscope.

The input signal seen at the TX port has a max value of 126mV, while the output seen at the ANT measures a maximum value of 72mV. This equates to a 42.9% signal loss, which approximates to a signal loss of 4.9dB. The output signal captured at the RX port reaches a peak value of 12mV. When compared with the maximum of the input signal, there is a signal loss of 90.5% seen at the RX port. The signal loss is equivalent to 20.4dB in this case. These results show that the input signal is successfully recovered at the ANT port. Here, a very small signal is seen at the RX port, which is expected.
In addition to the SSDL circulator’s ability to transmit and receive a single frequency, the two figures below show the transmission and receiving of information stored in a modulated waveform. The signal is a 1MHz sine wave amplitude modulated by a 50KHz square wave. Results are gathered from the oscilloscope and plotted using Matlab codes. Figure 4.2.3 demonstrates the results of the ANT to RX case. As before, low pass filters are present at the ANT and RX ports. The signal is applied to the ANT port, with the TX and RX ports monitored on the oscilloscope.

Figure 4.2.3: ANT to RX modulated waveform case. The frequency of the input signal is preserved at the output port.

The signal seen at the RX port is the same signal as that sent from the ANT port, with approximately 4.1dB of signal loss. There is very little signal level observed at the TX port, which is expected for this case.
Figure 4.2.4 represents the information collected when the same AM signal is applied to the TX port. The ANT and RX ports are monitored on the oscilloscope.

Figure 4.2.4: TX to ANT modulated waveform case. The frequency of the input signal is preserved at the output port.

The signal seen at the ANT port is the same as that observed at the TX port, with approximately 4.6dB of signal loss. There is a very low level of signal present at the RX port, which is the expected result for this case.

A significant portion of the signal loss seen in the results of this section can be explained by the data sheet for the SPDT switches. The ZFSW-2-46 incurs a loss of 1dB in the frequency range from DC-200MHz. If the loss of the coaxial cables is neglected, then there is approximately a 3dB loss that the signal encounters in its propagation through the SSDL circulator. The remaining losses could be explained by the AWG520 lacking the DC voltage level to fully turn on the switches.
4.3. Network Analyzer Results without Filtering

Here, S-parameter results are collected from the SSDL circulator setup as described in Section 4.1. The use of a network analyzer provides a more accurate and convincing picture of the system’s overall behavior. The system loss, isolation, and port matching parameters were measured and collected for the case with no filtration at the ANT and RX ports. Results were measured and collected using an S-parameter network analyzer manufactured by Agilent (part number 8753ES) at a power level of -20dBm. The start and stop frequencies were set to 200KHz and 200MHz, respectively. The TX, ANT, and RX ports are defined as ports 1, 2, and 3, respectively. The system loss is measured in two ways. In the first scenario, the forward and reverse ports of the network analyzer are connected to the ANT and RX ports, respectively. The TX port is attached to a matched 50 ohm load, and the system loss is measured as $S_{32}$. In the second scenario, the network analyzer’s forward and reverse ports are connected to the TX and ANT ports, respectively. The RX port is terminated in a matched 50 ohm load, and the loss is captured as $S_{21}$. To measure isolation, the forward and reverse ports of the network analyzer are attached to the TX and RX ports, respectively. The ANT port is terminated in a matched 50 ohm load, and the loss is measured as $S_{31}$. Fig. 4.3.1 represents the system loss and isolation measured for the circulator, as shown below.
As can be seen in Fig. 4.3.1, non-reciprocal behavior is demonstrated from 200KHz to 200MHz. System losses of approximately 5dB and 10dB are recorded at 200KHz and 200MHz, respectively. The system isolation, measured as $S_{31}$, is very good. Isolation is -40dB at the worst case, which occurs at around 200KHz.

A significant portion of the signal losses seen at 200KHz and 200MHz can be explained by referencing Appendix A. Appendix A reports the switch and cable losses recorded using the network analyzer at a power of -20dBm. The switch loss figures are for the static case, in which only RF output 2 is operating. At 200KHz, the cable losses are negligible. For the ANT to RX case, the signal passes through 2 sets of 3 switches, as explained in Sec. 2.1. A loss of approximately 3.5dB is accumulated along these paths. For the TX to ANT case, a signal loss of approximately 3.6dB is incurred. As indicated by the loss measurements at 200MHz, the cable
loss can no longer be ignored. Now, as the signal propagates from ANT to RX, it incurs a loss of approximately 6.6dB. A signal traversing the path from TX to ANT encounters a signal loss of roughly 6.7dB. The additional losses that are measured using the network analyzer could be explained by the dynamic state of the switches during the circulator measurements. When the circulator is operational, both RF outputs are on for a time 2T.

Fig. 4.3.2 showcases the port matching results for all three SSDL circulator ports.

![Port matching results](image)

**Figure. 4.3.2:** Port matching without filtration. Results show that a very small signal level is reflected from each circulator port.

The measured data shows that all three ports are matched quite well to the system characteristic impedance of 50 ohms. These results validate that the SSDL circulator demonstrates non-reciprocal behavior from 200KHz to 200MHz. In fact, non-reciprocal behavior is verified at 20KHz, which is the lowest operating frequency of the vector network analyzer. This demonstrates that there is no lower frequency limit of the SSDL circulator’s operation.

4.4. Network Analyzer Results with Filtering
The system loss, isolation, and port matching is presented in this section with filtering at the ANT and RX ports. The start and stop frequencies of the network analyzer are set to 200KHz and 1.5MHz, respectively. The system loss, isolation, and port matching are measured in the same manner as the unfiltered case, but with the addition of the BLP-1.9 filters at the ANT and RX ports. Figure 4.4.1, shown below, represents the system loss and isolation for the SSDL circulator.

Non-reciprocal behavior is seen from 200KHz to 1.5MHz, with a loss of approximately 5dB across the measured band. The isolation measured in this case is more realistic due to the additional filtering at the ANT and RX ports. The isolation is less than -25dB at the worst case.

The loss of the filters is negligible at 200KHz. The ANT to RX and TX to ANT paths have approximate losses of 3.5dB and 3.6dB, respectively. At 1.5MHz, the cutoff frequency of
the filter is being approached, which adds to the losses recorded. As with the results for the unfiltered case, the additional losses are due possibly to the dynamic states of the SPDT switches during operation.

Fig. 4.4.2 presents the port matching parameters measured for the filtered case.

![Port matching with filtration](image)

Figure. 4.4.2: Port matching with filtration. Results show that a very small signal level is reflected from each circulator port.

The measured data shows that all three ports are matched quite well to the system characteristic impedance of 50 ohms. These results validate that the SSDL circulator demonstrates non-reciprocal behavior from 200KHz to 1.5MHz.
Chapter 5

Conclusion

5.1. Concluding Remarks

A true passive circulator has been implemented by utilizing the SSDL concept. The initial test setup and results were presented and discussed, along with some solutions to the problems encountered. The final test setup demonstrated non-reciprocal behavior for two cases. In the first case, there was no filtering applied to the ANT and RX ports. This was done so that a comparison could be made against the second case with filtering at the ANT and RX ports. The comparison between these two scenarios provides a more realistic scenario, where filtering is required to distinguish the transmitted or received signal from the switching signals. The results presented for these two scenarios prove the validity of the SSDL circulator. The experiments and troubleshooting that were required for the successful implementation of the SSDL circulator proved to be an excellent learning experience.

5.2. Future Work

The results presented in this work open up a whole new world of possibilities. The switch and cable losses, as presented in Appendix A, show that a significant amount of the signal loss reported comes from these components. Future courses of action include research into a compact design that is integrated seamlessly with IC technology.

Theoretically, the concept of the SSDL circulator is valid from DC to light, as long as switches and delay lines can be fabricated to operate at those frequencies. An ultra-wide band SSDL circulator can be implemented with any standard integrated circuit technology. In practical situations, the switching noise may become a problem. This occurs when the switching frequency is close to that of the frequency of operation. For the noise-sensitive applications, like
full-duplex communications, the switching frequency is set much higher (or lower) than the operating frequency. As the frequency of operation increases, the suitability for on-chip integration becomes more apparent, as shorter delay lines can be used. Since the SSDL concept is entirely passive, the only power consumption of the circulator is the power that is dissipated in switching the devices. Transistor switches with small gate capacitances are able to achieve less power consumption. High-speed switches are desired for these reasons, and they also help to minimize signal loss as well as the interference of noise from dynamic switching actions.

For operations that require low power, it is possible for the SSDL circulator to operate in an undersampled mode. As an example, if we combine the long delay time of surface acoustic waves (SAW) delay lines with the speed of semiconductor switches, we can realize an SSDL circulator with very low power consumption.
APPENDIX A

Switch and 30 foot cable losses at 200KHz and 200MHz

Tables A.1 and A.2, listed below, provide the loss measurements for the switches and cables used in the final experimental setup.

<table>
<thead>
<tr>
<th>Switch Name</th>
<th>$S_{21}$ at 200KHz [dB]</th>
<th>$S_{21}$ at 200MHz [dB]</th>
</tr>
</thead>
<tbody>
<tr>
<td>TX</td>
<td>1.50</td>
<td>2.84</td>
</tr>
<tr>
<td>RX</td>
<td>1.43</td>
<td>2.77</td>
</tr>
<tr>
<td>T/R</td>
<td>1.09</td>
<td>2.47</td>
</tr>
<tr>
<td>R/T</td>
<td>1.04</td>
<td>2.43</td>
</tr>
<tr>
<td>ANT</td>
<td>1.07</td>
<td>2.36</td>
</tr>
</tbody>
</table>

Table. A.1: Individual Switch Loss. The input power level from the network analyzer is set to -20dBm. These results are for the static switching case, where RF output 2 is operating.

<table>
<thead>
<tr>
<th>Transmission Line Name</th>
<th>$S_{21}$ at 200KHz [dB]</th>
<th>$S_{21}$ at 200MHz [dB]</th>
</tr>
</thead>
<tbody>
<tr>
<td>T1</td>
<td>0.06</td>
<td>1.59</td>
</tr>
<tr>
<td>T2</td>
<td>0.06</td>
<td>1.54</td>
</tr>
<tr>
<td>R1</td>
<td>0.05</td>
<td>1.48</td>
</tr>
<tr>
<td>R2</td>
<td>0.06</td>
<td>1.60</td>
</tr>
<tr>
<td>A1</td>
<td>0.05</td>
<td>1.50</td>
</tr>
<tr>
<td>A2</td>
<td>0.04</td>
<td>1.58</td>
</tr>
</tbody>
</table>

Table. A.2: Individual Cable Loss. The input power level from the network analyzer is set to -20dBm.
REFERENCES


