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Microwave, Wideband Outphasing Modulators in Silicon Integrated Circuit Technology

A dissertation submitted in partial satisfaction of the requirements for the degree
Doctor of Philosophy

in

Electrical Engineering (Electronic Circuits and Systems)

by

Mohammad Sadegh Mehrjoo

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2015
The dissertation of Mohammad Sadegh Mehrjoo is approved, and it is acceptable in quality and form for publication on microfilm and electronically:

Chair

University of California, San Diego

2015
DEDICATION

To my parents - Mrs. Sedigheh Sahimpour and Mr. Abdollah Mehrjoo.
TABLE OF CONTENTS

Signature Page ............................................................... iii
Dedication ........................................................................ iv
Table of Contents .......................................................... v
List of Figures ..................................................................... vii
List of Tables ....................................................................... ix
Acknowledgements ........................................................... x
Vita .................................................................................. xii
Abstract of the Dissertation ............................................... xiii

Chapter 1  Introduction ...................................................... 1

Chapter 2  High Linearity Power DAC ................................. 7
  2.1 Low Breakdown Voltage in Fineline CMOS Technologies 7
  2.2 Analysis of Stacked-FET Current Buffer ....................... 8
    2.2.1 Stacked-FET Voltage Handling ......................... 8
    2.2.2 Volterra Analysis of Stacked-FET Buffer ............... 11
    2.2.3 Linearity Analysis for Stacked-FET Buffer ............. 13
    2.2.4 Cascade of Buffer Stages ................................. 17
    2.2.5 Current Bleeding ............................................ 17
  2.3 Power DAC Implementation ........................................ 19
    2.3.1 Unit Current Cell ........................................... 20
    2.3.2 Block Diagram .............................................. 22
  2.4 Measurement Results ............................................... 24
  2.5 Conclusion ............................................................. 31

Chapter 3  Wideband Outphasing modulator ....................... 34
  3.1 Outphasing versus Envelope Tracking .......................... 34
  3.2 Outphasing Modulator Architecture ............................. 36
    3.2.1 Outphasing Description .................................. 36
    3.2.2 Outphasing Accuracy for High-Dynamic Range ...... 36
    3.2.3 Outphasing Architecture ................................ 37
  3.3 Circuit Implementation of the Outphasing Modulator ....... 40
    3.3.1 RF ............................................................ 41
    3.3.2 Serial Deserializer ......................................... 44
    3.3.3 Digital-to-Analog Conversion ............................ 46
LIST OF FIGURES

Figure 1.1: Applications of X-band wireless systems. 1
Figure 1.2: Block diagram of an envelope tracking power amplifier [1]. 2
Figure 1.3: (a) Doherty PA. (b) Currents and voltages. (c) Efficiency [2]. 4
Figure 1.4: Block diagram of an outphasing modulator [3]. 5

Figure 2.1: Current buffer between power DAC and load. 9
Figure 2.2: Voltage swing at different nodes of the stacked-FET buffer. 10
Figure 2.3: Small-signal model for a stacked-FET current buffer stage. 11
Figure 2.4: Linearity analysis and transistor-level simulation for one stage. 14
Figure 2.5: Monte-Carlo simulation for one stage of the stacked-FET buffer. 14
Figure 2.6: Calculated $HD_3$ for a single stage of the stacked-FET current buffer. 15
Figure 2.7: Calculated $HD_3$ for a single stage versus $r_o$. 16
Figure 2.8: Numerical and simulated HD3 versus number of stages at 500 MHz. 18
Figure 2.9: $|Z_{in}|$ versus $I_S$ for different $I_B$. 18
Figure 2.10: HD3 of a 3-stages current buffer versus current bleeder ($I_B$). 19
Figure 2.11: Unit current cell with the bias circuit schematic. 21
Figure 2.12: Block diagram of the 10-bit power DAC. 21
Figure 2.13: Output impedance of the thermometer unit current cell. 23
Figure 2.14: Layout for current source array to minimize layout variations. 24
Figure 2.15: Chip photograph of the power DAC. 25
Figure 2.16: Measured DNL versus input code. 26
Figure 2.17: Measured INL versus input code. 26
Figure 2.18: Dynamic measurement setup. 28
Figure 2.19: 6.3 $V_{PPd}$ measured differential output swing at 150 kHz. 28
Figure 2.20: Measured output power over 100 Ω differential load. 29
Figure 2.21: Measured SFDR at 375 kHz. 29
Figure 2.22: Measured SFDR, DC to Nyquist. One-tone test at full swing. 30
Figure 2.23: Measured IM3 at 4 MHz. 30
Figure 2.24: Measured IM3, DC to Nyquist. 31

Figure 3.1: Representations of signals in an outphasing modulator. 35
Figure 3.2: Dynamic range as a function of the error in the outphasing angle. 38
Figure 3.3: Block diagram of the implemented outphasing modulator. 38
Figure 3.4: Phase resolution for DACs with different resolutions. 40
Figure 3.5: Quadrature double-balanced upconversion mixer. 41
Figure 3.6: (a) Simulated $OIP3$. (b) Simulated $P_{1dB}$ compression point. 43
Figure 3.7: LO signal chain. 44
Figure 3.8: Circuit schematic of the 1-to-10 bit deserializer. 45
Figure 3.9: Circuit schematic of the 10-bit current steering DAC. 47
Figure 3.10: Die photograph of the outphasing modulator. 48
Figure 3.11: Measurement setup of the outphasing modulator. 50
Figure 3.12: (a) before calibration. (b) After calibration. 51
Figure 3.13: (a) Measured $P_{\text{dB}}$ compression point (b) Measured $OIP_3$. 52
Figure 3.14: Measured power versus outphasing angle $\phi$. 53
Figure 3.15: Measured output power and differential non-linearity versus $\cos^2\phi$. 54
Figure 3.16: Measured output swings. 55
Figure 3.17: Measured constellation and spectrum for a 16-QAM modulation. 56
Figure 3.18: Measured constellation and spectrum for a 64-QAM modulation. 56
Figure 3.19: Measured constellation and spectrum for a 256-QAM modulation. 57
Figure 3.20: 100-MHz LTE-Advanced carrier aggregation. 58

Figure 4.1: Amplitude to phase modulation. 62
Figure 4.2: Capacitance of a MOS varactor versus bias voltage. 63
Figure 4.3: Amplitude-to-phase modulation with coupled-oscillator. 64
Figure 4.4: Outphasing angle as a function of the signal amplitude. 64
Figure 4.5: Oscillation frequency for different signal amplitudes. 65
Figure 4.6: Amplitude-to-phase modulation with three coupled-oscillator. 66
Figure 4.7: Outphasing angle for three coupled-oscillators. 66
Figure 4.8: Oscillation frequency for different signal amplitudes. 67
Figure 4.9: Locking the center oscillator to an external oscillator. 68
Figure 4.10: Outphasing angle with an external oscillator. 68
Figure 4.11: Stable progressive phase enhancement using frequency multiplier [4]. 70
Figure 4.12: Adding doubler and amplifier after coupled-oscillators. 70
Figure 4.13: Illustration of the desired outphasing angle with doublers. 71
Figure 4.14: Block diagram of the proposed modulator. 72
Figure 4.15: Detuning the coupled oscillators with sine wave signal. 73
Figure 4.16: Calculated HD2 and HD3. 73
Figure 4.17: Cross-coupled LC oscillator. 74
Figure 4.18: Schematic of frequency doubler in 45-nm CMOS SOI. 75
Figure 4.19: Chip microphotograph of the 45-nm CMOS SOI prototype. 76
Figure 4.20: Measurement Setup. 77
Figure 4.21: Free-running frequency versus tuning voltage. 78
Figure 4.22: Single-ended output spectrum of each channel. 78
Figure 4.23: Phase of the coupled oscillator versus detuning voltage. 80
Figure 4.24: Phase of the coupled oscillator versus injection frequency. 80
Figure 4.25: Output power from the combined outphasing. 81
Figure 4.26: Output power ($S_1 + S_2$) versus detuning voltage. 82
Figure 4.27: Step function of the outphasing modulator. 83
Figure 4.28: Measured and calculated HD2 and HD3 versus amplitude. 83
Figure 4.29: Measured HD2 and HD3 versus frequency for sine-wave detuning. 84
LIST OF TABLES

Table 2.1: Comparison With Published Data . . . . . . . . . . . . . . . . . . 32
Table 3.1: Comparison With Published Data . . . . . . . . . . . . . . . . . . 59
Table 4.1: Locking range of the coupled oscillator versus injection power. . 79
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ABSTRACT OF THE DISSERTATION

Microwave, Wideband Outphasing Modulators in Silicon Integrated Circuit Technology

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Professor James Buckwalter, Chair

Wideband, high-data rate wireless communication systems generally suffer from low-efficiency or poor linearity. To realize both a linear response and high-efficiency, a variety of linearization approaches have been proposed. Polar transmitters separate the signal into amplitude and phase components. The phase component drives a high-efficiency power amplifier (PA) while the amplitude component drives the power supply. While this improves the efficiency of the PA, the amplitude modulator requires much higher bandwidth compared to the input signal. Envelope tracking systems generally struggle to reach bandwidths exceeding 100 MHz due to the difficulty to realize supply modulators that remain efficient over wide bandwidth.
An alternative to envelope tracking is linear amplification with nonlinear components (LINC) also called outphasing. In an outphasing transmitter, an input signal is separated into amplitude and phase components that are used to construct two constant-envelope phase-modulated signals. Therefore, high-efficiency PAs amplify the constant envelope signals and this improves the efficiency without degrading the linearity. The amplified signals are combined together to restore the amplitude and phase components of the output signal. Although, in theory, for an outphasing system combining two outphased signals would restore the original signal, any imbalance results in error. For example a phase mismatch between the two signals translates into phase and amplitude error in the combined signal which limits the control over the output power dynamic range.

In this dissertation first the system level of the proposed outphasing modulator is presented to highlight the main blocks. Digital to analog converter (DAC) is introduced as one of the main blocks and the implemented 10-bit power DAC is described. This DAC is implemented in 45-nm CMOS SOI and is capable of delivering current swings sufficient for 6 V swing on a 50-Ω load. This the highest swing reported in the literature for a high-resolution DAC.

Then, the 10-GHz wideband outphasing modulator is presented which includes four of the power DACs along with two I/Q up-converters. This modulator is also in 45-nm CMOS SOI and can operate at 1.1 Gbit/s by using 265-QAM. This modulator is meant to drive off-chip GaN or GaAs PAs. Therefore, each channel of the modulator is designed to deliver 20 dBm which is sufficient to drive GaN/GaAs PAs. This is the first demonstration of the outphasing modulator for data rates above 1 Gbit/s. Finally, a polar modulator based on coupled oscillators is proposed. This modulator is taped-out in 45 nm CMOS SOI. Chip is not tested and block diagram and simulation results are presented.
Chapter 1

Introduction

X-band (8 - 12 GHz) is a segment of the microwave spectrum. Wireless communication systems at this frequency offer wide-bandwidth and therefore allow high-data rate communication. Fig. 1.1 shows two major applications of the systems operating at X-band, satellite communications and radar [5]. The modern wireless communication systems request for high data rates within a limited bandwidth. That increases the ratio between between the peak signal power and average signal power. This ratio can exceed 10 dB and if the linear RF-PA operate in the power back-off region to linearly amplify the signal, the efficiency will be so low [6]. Therefore, it can be concluded that high-data rate wireless systems generally suffer from low-efficiency or poor linearity. To realize both a

Figure 1.1: Applications of X-band wireless systems.
linear response and high-efficiency, a variety of linearization approaches have been proposed. One technique to improve the efficiency and maintain the linearity is envelop tracking [7–17]. This approach separates the signal into amplitude and phase components. The phase component drives a high-efficiency power amplifier (PA) while the amplitude component drives the power supply. Fig. 1.2 shows the block diagram of an envelope tracking PA [1].

![Block diagram of an envelope tracking power amplifier](image)

**Figure 1.2:** Block diagram of an envelope tracking power amplifier [1].

This technique utilizes a linear PA and a controlled supply voltage which tracks the signal envelope. Therefore, the collector/drain supply of the RF power transistor dynamically changes with the signal envelope and the RF transistor operates with higher efficiency over a wide dynamic range of the output power. This is a good approach for the systems with a wide carrier frequency range [18]. As Fig. 1.2 shows there is no fundamental parameter that limits the LO frequency range. However, the amplitude modulator requires much higher bandwidth compared to the input signal [19]. Envelope tracking systems generally struggle to reach signal bandwidths exceeding 100 MHz due to the difficulty to realize supply modulators that remain efficient over wide bandwidth [20–22].

Another approach to improve the efficiency of the backed-off linear PAs is the Doherty [2, 23–40]. This approach uses the load modulation technique to improve the efficiency of linear amplifiers. In the Doherty power amplifiers, the load impedance of the active device increases at lower power levels in order to maintain the efficiency peak. A classical Doherty power amplifier consists of the main and auxiliary amplifiers. The role of the auxiliary cell is to actively modulate the main
amplifier’s load impedance while contributing to the output power at the same time. The output powers of two amplifiers operating at a proper phase alignment and bias level are combined using a quarter-wave transmission line without the use of any additional components [25].

Fig. 1.3 shows the classical Doherty amplifier configuration along with the output currents and voltages [2]. In the high power region the auxiliary amplifier is activated and the main amplifier is held at the maximum voltage. Due to the voltage-saturated operation of the main amplifier, the overall efficiency of the PA is improved. The saturation power of the main amplifier is one-fourth of the maximum system output power. This results in an efficiency peak at 6-dB output power back-off from the normal peak efficiency power level [24]. Fig. 1.3 also shows that the Doherty PAs are ideally linear amplifiers. During the high power mode, contribution of the auxiliary amplifier to the output power compensates the power transfer function of the main amplifier. Therefore, the overall input-output power characteristic is linear. The Doherty PAs linearity can also be studied from the intermodulation (IM) products point of view. In the high power region, the two amplifiers generate IM products with 180 phase difference because the main amplifier has gain compression while the auxiliary one experiences gain expansion. Consequently, the IM products cancel out each other, leaving the Doherty PA with a distortion-free characteristic [2].

While in theory the input-output power characteristic of the Doherty amplifier is linear, in practice the output current of the auxiliary amplifier reaches below the main amplifier. This happens because of the lower gain of the class-C auxiliary amplifier, causing an insufficient load pull-down at high power levels. Also, another issue is that the main amplifier does not reach the perfect voltage-saturated state at back-off power levels since it faces an early load pull-down caused by the soft turn-on characteristic of the auxiliary device. Consequently, the linearity is affected since neither of the cells can generate its respective output power to allow for IM cancellation [2]. With the help of the digital pre-distortion technique, many works have been done on the high-linearity Doherty PAs [41–43]. However, due to the processing bandwidth of the DPD systems, most of the reported implementa-
Figure 1.3:  (a) Doherty PA. (b) Currents and voltages. (c) Efficiency [2].
tions were designed to work with a bandwidth of or lower than 20 MHz [41–43].

An alternative to envelope tracking and Doherty is linear amplification with nonlinear components (LINC) also called outphasing [44–57]. Fig. 1.4 shows the block diagram of an outphasing system [3]. In an outphasing transmitter, an input signal is separated into amplitude and phase components that are used to construct two constant-envelope phase-modulated signals. Therefore, high-efficiency switching mode PAs amplify the constant envelope signals and this improves the efficiency without degrading the linearity [58], [59]. The amplified signals are combined together to restore the amplitude and phase components of the output signal. One limitation of this technique is that the low loss combiners are non-isolating, therefore PAs experience load mismatch that changes with the outphasing angle. This degrades the efficiency particularly in back-off. One approach to address this issue is using duty cycles less than 0.5 to satisfy the zero-voltage-switching condition for the switching mode PAs. In that case PAs are less sensitive to the load variations [60–63]. There are other works as well that address the power combining in outphasing transmitter [64–66]. However, this dissertation focuses on the modulator not the power combining. Therefore, the power combining is not discussed further.

![Figure 1.4: Block diagram of an outphasing modulator [3].](image)

One key advantage of the outphasing approach over the other two techniques (envelope tracking and Doherty), is that the outphasing architectures are capable of transmitting very wideband signals [59]. At high frequencies (x-band and above) higher signal bandwidths are available. Therefore, outphasing technique is the most promising solution at high frequencies.

In this dissertation two modulators are presented. The first one is an outphasing modulator that offers high data rate modulations. It is designed by putting
two I/Q modulator together. Each I/Q channel has two power digital to analog converters (DAC). Chapter 2 presents the power DAC and then in chapter 3 the outphasing modulator is discussed. The second modulator is presented in chapter 4. This is a polar modulator and is designed based on coupled-oscillators. This chip is not tested yet and in the dissertation circuitry and simulation results are presented. At the end, chapter 5 concludes the dissertation.
Chapter 2

High Linearity Power DAC

2.1 Low Breakdown Voltage in Fineline CMOS Technologies

The evolution of digital-to-analog conversion (DAC) toward the antenna requires high dynamic range and peak output power. CMOS transconductors are inherently nonlinear, particularly at high frequency and contribute distortion which degrades the error vector magnitude (EVM) and adjacent channel power ratio (ACPR) of the transmitted signal [67]. To implement a highly linear transmitter, a DAC can drive a baseband current into a current-mode mixer to upconvert the signal to an RF band without the use of a high-frequency transconductor. Since the current mode mixer does not have current gain, the critical feature of a current-mode power DAC is the ability to deliver a given high peak current swing.

Using fineline CMOS technology typically offers high $f_T/f_{max}$ transistors but low (1 V) breakdown voltage. Since the DAC provides a high current swing into a 50-Ω load, the voltage swing easily exceeds the breakdown voltage of a fineline device to reach power levels greater than 10 dBm. Previous work demonstrated a 2.5 V swing in 65 nm CMOS technology using thick-oxide devices to avoid the breakdown voltage for thin-oxide devices of only 1 V [68]. However, thick-oxide transistors also have a breakdown voltage limitation.

In this work, an output voltage swing much higher than the breakdown volt-
age of either thin- or thick-oxide transistors is realized through a current buffer using a stacked-FET circuit technique. Insertion of the current buffer between a current-mode DAC and a 50-Ω load is illustrated in Fig. 2.1. The input impedance of this buffer must be sufficiently small such that the voltage swing does not approach the transistor breakdown. At the output, the current buffer increases the load line impedance to achieve high swing. The FET-stacking approach has been successfully demonstrated at high frequency for power amplifiers (PAs) [69], [70], [71], [72] as well as in low-resolution (2-bit) millimeter-wave DACs [73]. This work presents the first implementation of FET-stacking for high-speed, high-linearity data converters.

In this chapter a Volterra series analysis of the stacked-FET current buffer is presented to take into account frequency-dependent nonlinearity and investigate the fundamental trade-off between the linearity, bandwidth, and output power in a stacked-FET current buffer. Also, the design of critical blocks of the power DAC is described based on linearity requirements. This chapter also includes the measurement and comparison with previously published DACs.

2.2 Analysis of Stacked-FET Current Buffer

A three-stage, stacked-FET current buffer is shown in Fig. 2.1. The FET-stacking technique connects a capacitor to the gate of each cascode FET to control the voltage swing at the gate. Consequently, the FET-stacking technique differs from a conventional cascode amplifier which introduces a low-impedance at the gate of the FET. While stacked-FET PAs have demonstrated high power handling and efficiency, prior work has not studied the linearity of the stacked-FET techniques. Stacked-FET circuits are most readily implemented with SOI CMOS technology, which feature the floating body device shown in Fig. 2.1.

2.2.1 Stacked-FET Voltage Handling

$N$-stacked FETs evenly divide a voltage swing with amplitude as high as $N \cdot V_{DD}$ when the gate capacitance is chosen to prevent breakdown between either
Figure 2.1: Current buffer between power DAC and load.

The gate-drain or gate-source capacitances [74]. At each stage, the input impedance looking into the source of the transistors in the stacked-FET current buffer is

\[ Z_i = \left( 1 + \frac{C_{gs,i}}{C_i} \right) \left( \frac{1}{g_{m,i}} || \frac{1}{sC_{gs,i}} \right) \]  

(2.1)

where \( C_{gs,i} \) is the gate-source capacitance, \( C_i \) is the external capacitor attached to the gate, and \( g_{m,i} \) is the transconductance of the transistor at stage \( i \). From (2.1), reducing the \( C_i \) increases the \( Z_i \). As more stages are stacked, the input impedance should increase. Since the current flow through all stages is constant and determined by the current source at the bottom, higher \( Z_i \) increases the swing at each source node. In other words, current flows through the stacked-FET buffer to generate a higher voltage. To equally share the voltage swing, it has been shown that the input impedance of each stage should increase according to \( Z_i = i \times Z_{i-1} \) [74]. Fig. 2.2 demonstrates the voltage swing at different nodes of the current buffer shown in Fig. 2.1. The voltage division of \( C_{gs,i} \) and \( C_i \) determines the source-gate voltage as

\[ v_{sg,i} = \alpha_i v_{s,i} \]  

(2.2)
Figure 2.2: Voltage swing at different nodes of the stacked-FET buffer.

where $\alpha_i = C_i/(C_i + C_{gs,i})$ and $v_{s,i}$ is the voltage at the source node of the stage $i$. From (2.2), reducing the $C_i$ keeps the source-gate voltage below the breakdown voltage even if the $v_{s,i}$ is higher than the breakdown. For very large $C_i$, the stacked-FET degenerates to a cascode structure and $v_{gs,i}$ will be equal to $-v_{s,i}$.

At each stage, $v_{d,i} = (Z_{i+1}/Z_i) \cdot v_{s,i}$ where $v_{d,i}$ is the voltage at the drain node of the stage $i$. Substituting (2.1), the drain-gate voltage is

$$v_{dg,i} = \alpha_i \left( 1 + \frac{C_{gs,i}}{C_i} \left( \frac{C_i}{C_{i+1}} - 1 \right) \right) v_{s,i}. \quad (2.3)$$

As (2.3) illustrates, the ratio of $C_i/C_{i+1}$ can maintain the drain-gate voltage below the breakdown voltage. In this design, the voltage swing is determined according to (2.2) and (2.3) to bound the drain-gate and gate-source voltage swings seen at each stacked FET below the breakdown voltage of 1 V. Therefore, the output voltage swing is 3 V single-ended or three times the breakdown voltage of an individual device.
2.2.2 Volterra Analysis of Stacked-FET Buffer

While the stacked-FET current buffer could hypothetically handle more output voltage swing with additional stages, a fundamental question arises about the maximum number of stages given a linearity requirement. To investigate this question, the drawbacks of adding more stages are studied in this section. To understand the generation of frequency-dependent distortion in the stacked-FET buffer, a Volterra series analysis is derived in this section. Fig. 2.3 shows the small-signal model of a single stage of a stacked-FET current buffer and will be applied to find the output current \( i_o \) as a function of the input current \( i_s \). The input of the stacked-FET buffer is modeled by a current source \( i_s \) with impedance of \( Z_S \) and the output is modeled by an impedance \( Z_L \). For simplicity, the gate-drain capacitor \( (C_{gd}) \) is neglected and gate-source capacitor \( (C_{gs}) \) is assumed to be constant such that all FETs remain biased in saturation. The gate of the FET is tapped to ground through the capacitor \( C_g \) and \( r_o \) is the drain-source resistance of the transistor. The drain-source current of the transistor \( (i_{ds}) \) is a weakly nonlinear function of the gate-source voltage \( (v_{gs}) \);

\[
i_{ds} = g_m v_{gs} + \frac{g_m'}{2!} v_{gs}^2 + \frac{g_m''}{3!} v_{gs}^3 + \cdots \tag{2.4}
\]

where \( g_m \) is transconductance and \( g_m' \) and \( g_m'' \) are the first and second derivative of the transconductance, respectively. The voltage at the source node is determined

![Figure 2.3: Small-signal model for a stacked-FET current buffer stage.](image)
from
\[ v_s = Z_1(s) \circ i_s + Z_2(s_1, s_2) \circ i_s^2 + Z_3(s_1, s_2, s_3) \circ i_s^3, \quad (2.5a) \]
where \( Z_1() \), \( Z_2() \), and \( Z_3() \) are Volterra kernels relating the source current to the voltage swing at the source and \( \circ \) is the Volterra operator \([75]\). Details of the derivation of these kernels is provided in Appendix A. By solving KCL equation at the source and drain nodes, the Volterra kernels \( Z_i() \) are derived as

\[ Z_1(s) = \left( \frac{1}{Z_S(s)} + \alpha C_{gs} s + \frac{1}{r_o} \beta(s) + \alpha g_m \beta(s) \right)^{-1} \quad (2.5b) \]

\[ Z_2(s_1, s_2) = \frac{1}{2} \alpha^2 g'_m \beta(s_1 + s_2) Z_1(s_1) Z_1(s_2) Z_1(s_1 + s_2) \quad (2.5c) \]

\[ Z_3(s_1, s_2, s_3) = \beta(s_1 + s_2 + s_3) Z_1(s_1 + s_2 + s_3) \left[ \alpha^2 g'_m Z_1(s_1) Z_2(s_2, s_3) - \frac{1}{6} \alpha^3 g''_m \prod_{i=1}^{3} Z_1(s_i) \right] \quad (2.5d) \]

where \( \beta(s) = r_o/(r_o + Z_L(s)) \) and \( Z_1(s_1) Z_2(s_2, s_3) \) is the interaction operator. Note that \( Z_1(s) \) in (2.5b) reduces to the simplified input impedance equation shown in (2.1) when \( Z_S \) and \( r_o \) approach infinity.

The output current \( i_o \) is expressed as

\[ i_o = A_1(s) \circ i_s + A_2(s_1, s_2) \circ i_s^2 + A_3(s_1, s_2, s_3) \circ i_s^3 \quad (2.6) \]
where \( A_i() \) are the Volterra kernels for the current gain. Writing the KCL in the output node results in

\[ i_o = \beta(s) \left( i_{ds} - \frac{v_s}{r_o} \right) \quad (2.7) \]
Substituting (2.4) and (2.5a) into (2.7), the first, second, and third order Volterra kernels of \( i_o \) are derived as shown in (2.8a)-(2.8c). The frequency-dependent non-linear function describing the stacked-FET current buffer exhibits dependencies based on the device parasitics as well as the source and load impedances.
\[
A_1(s) = -\left(\frac{1}{r_o} + \alpha g_m\right) \beta(s) Z_1(s) \quad (2.8a)
\]
\[
A_2(s_1, s_2) = \left(-\left(\frac{1}{r_o} + \alpha g_m\right) Z_2(s_1, s_2) + \frac{1}{2} \alpha^2 g'_m Z_1(s_1) Z_1(s_2)\right) \beta(s_1 + s_2) \quad (2.8b)
\]
\[
A_3(s_1, s_2, s_3) = \left(-\left(\frac{1}{r_o} + \alpha g_m\right) Z_3(s_1, s_2, s_3) + \alpha^2 g'_m \frac{Z_1(s_1) Z_2(s_2, s_3) - \frac{1}{6} \alpha^3 g''_m \prod_{i=1}^{3} Z_1(s_i)}{Z_1(s_1)}\right) \beta(s_1 + s_2 + s_3) \quad (2.8c)
\]

### 2.2.3 Linearity Analysis for Stacked-FET Buffer

The linearity of the stacked-FET current buffer is quantified from the third-order harmonic distortion (HD3). Considering the Volterra kernels of the output current (2.8a)-(2.8c), the HD3 is defined as

\[
HD3 = 20 \log \left(\frac{i^2_s}{A_1(s_1)}\right). \quad (2.9)
\]

In order to calculate the HD3, circuit parameters are required for the Volterra kernels. Transistor level simulations of an NFET with \(W = 100 \mu m\) and \(L = 40 nm\) results in \(g_m = 160 mA/V\), \(g'_m = 120 mA/V^2\), \(g''_m = 800 mA/V^3\), \(r_o = 34 \Omega\) and \(C_{gs} = 65 fF\). For \(C_1 = 150 fF\), Fig. 2.4 compares the calculated HD3 from (2.9) and the transistor-level simulation using a 45-nm CMOS SOI process for one stage. The maximum deviation is 1.9 dB and is attributed to ignoring the contribution of \(C_{gd}\). In the Volterra analysis \(g_m\) is considered as the only source of the nonlinearity. The agreement between analysis and simulation in Fig. 2.4 shows that the nonlinearity of other elements such as \(C_{gs}\) and \(r_o\) can be neglected. In section E, it is explained how a proper DC bias minimizes the nonlinearity of the \(C_{gs}\). As the gate capacitance is small, the sensitivity of HD3 to the value of the gate capacitance is investigated. If the \(3\sigma\) of the capacitor is 25%, the Volterra analysis suggests 1.8 dB variation in HD3. A Monte-Carlo simulation in Fig. 2.5 agrees with theoretical analysis and suggests the \(3\sigma\) variation of HD3 is 3.1 dB. Therefore, the analysis and Monte-Carlo simulation suggested that the stacked-FET buffer is robust against process variation and mismatch.
Figure 2.4: Linearity analysis and transistor-level simulation for one stage.

Figure 2.5: Monte-Carlo simulation for one stage of the stacked-FET buffer.
Fig. 2.6 calculates $HD3$ of the output current for one stage of the stacked-FET as a function of the source impedance for low frequency (10 MHz) and high frequency (500 MHz). The plot indicates that increasing $Z_S$ improves $HD3$. For a desired bandwidth, the linearity improvement saturates. When the bandwidth is reduced by a factor of 50, $HD3$ decreases by $20 \log_{10} 50$ or 34 dB and the maximum $HD3$ occurs at a higher $Z_S$. An intuitive explanation for this dependence on $Z_S$ is found from Fig. 2.3. If $Z_S$ is much larger than the impedance seen into the buffer (2.1), then $i_{ds}$ will circulate in the transistor and the only current that goes to the output is $i_s$. For small $Z_S$, some of the $i_{ds}$ current goes to ground through $Z_S$. Therefore, the same amount of $i_{ds}$ will be pulled from output and introduce nonlinearity at the output. At high frequency, the impedance of the capacitors drops and some of the $i_{ds}$ is lost through $C_{gs}$ and $C_g$ to ground, which contributes to nonlinearity.

Similarly, $r_o$ plays a critical role on the linearity of the buffer and is extremely limited in fineline CMOS. The calculated $HD3$ for one stage is plotted in Fig. 2.7 as a function of the $r_o$ at different frequencies. As the output resistance of
the device reduces to around 10 Ω, the linearity degrades by 10 dB. This effect is present at low and high frequency. Fig. 2.7 also shows improvement in HD3 when \( r_o \) drops from 10Ω to 1Ω. For \( r_o \) smaller than \( 1/g_m \), a considerable amount of the input current flows through \( r_o \) which reduces the effect of the device nonlinearity on the output current. In the limit that \( r_o = 0Ω \), the output current is simply equal to input current and \( HD3 = -∞ \) dBc. Obviously, it is not desirable to design the stage with small \( r_o \), since the source and drain swing will be identical. If \( r_o \) and

\[
\text{Figure 2.7: Calculated } HD3 \text{ for a single stage versus } r_o.
\]

\( Z_S \) approach infinity, approximations can be made for the analytical expression in (2.9) by substituting the expressions from (2.8a)-(2.8c).

\[
HD3 = 20\log \left( \frac{i_s^2}{8 \left( 1 + \frac{s}{\omega_T} \right)^2} \left( 1 - \frac{1}{1 + 3 \frac{s}{\omega_T}} \right) \left( \frac{(g_m')^2}{g_m^4} \left( 1 + 2 \frac{s}{\omega_T} \right) \frac{1}{3 g_m^3} \right) \right)
\]

(2.10)

where \( \omega_T = g_m/C_{gs} \). This expression shows that the HD3 increases at low frequency. Note that in the low-frequency approximation, the role of \( \alpha \) is not present.
and the stacked-FET buffer does not introduce any degradation in HD3 compared to a cascode-style amplifier.

2.2.4 Cascade of Buffer Stages

For more than one stage, the Volterra kernel can be cascaded for frequency-dependent nonlinear blocks [75]. For the cascade equation, the loading effect of each stage must be appropriately captured. To decide the number of stages for a 10-bit power DAC, the analyzed and simulated HD3 for different number of stages at 500 MHz is depicted in Fig. 2.8. With each additional stage, the distortion of the buffer increases by roughly 6 dB per stage. The disagreement between the analysis and circuit simulation is attributed to neglecting $C_{gd}$ in deriving the Volterra kernels. $C_{gd}$ introduces feedback from drain to gate and second-harmonic current flows to the gate and mix with the linear voltage at the gate to produce third-order nonlinearity, which degrades HD3 [76]. This feedback path is proportional to $C_{gd}/C_i$ and as $C_i$ becomes smaller given a fixed $C_{gd}$, more feedback is present and the theoretical prediction deviates from the circuit simulation. Simulation results show a -67 dBc and -62 dBc HD3 for three and four stages, respectively. Since -62 dBc is the maximum required HD3 for a 10-bit DAC, and it is not desired that the current buffer degrades the overall linearity of the system, a 3-stage stacked-FET current buffer has been implemented.

2.2.5 Current Bleeding

Fig. 2.1 indicates two current bleeders attached to the bottom of the stacked-FET current buffer. The introduction of the current bleeder improves the linearity through two mechanisms. If all the current sources are switched to one side of the buffer, the current bleeder ensures that some current will flow in the other branch to keep the FET-stack biased in the saturation region. The current bleeder keeps the gate-source and gate-drain capacitances constant [68].

Moreover, the current bleeder reduces the input impedance variations of the buffer. Fig. 2.9 shows the input impedance of the stacked-FET current buffer
Figure 2.8: Numerical and simulated HD3 versus number of stages at 500 MHz.

Figure 2.9: $|Z_m|$ versus $I_S$ for different $I_B$. 
(|Z_in|) as a function of the signal current \(i_s\) for different current bleeder currents \(I_B\). At low \(i_s\), the transistor \(g_m\) is low and consequently the input impedance is high. Adding \(I_B\) increases the \(g_m\) and reduces the input impedance. However, at high \(i_s\), the FETs are operating closer to the linear region. The addition of \(I_B\) may force the FETs into the linear region and cause a drop in \(g_m\). Since variations of the \(|Z_{in}|\) with respect to \(i_s\) depend on the \(I_B\), for a given number of stages and current swing, an optimum choice for \(I_B\) results in the highest linearity. Fig. 2.10 shows the HD3 of the output signal versus the current bleeder for a 3-stage stacked-FET current buffer with 60 \(mA_{PP}\) current swing. The plot indicates that a 10 mA current bleeder - roughly 16% of the peak current swing - results in the highest linearity (HD3 -67 dBc).

![Figure 2.10: HD3 of a 3-stages current buffer versus current bleeder (\(I_B\)).](image)

### 2.3 Power DAC Implementation

Current-steering DACs are suitable for high sampling rate applications and are based on binary, unary, and segmented architectures [68], [77]. In the proposed
design, the DAC is divided into two MSB and LSB DACs and thermometer coding is only used for the MSB part. A higher segmentation results in a higher linearity but brings more complexity to digital part which causes higher power consumption and lower speed [78]. The 10-bit segmented DAC in this work is implemented with equal number of binary and unary bits.

2.3.1 Unit Current Cell

Fig. 2.11 shows the unit current cell and the biasing circuit. Transistor mismatch in current sources of the DAC causes nonlinearity [68]. As shown in [79], increasing the area reduces the mismatch in MOS transistors. Here $M_1$ and $M_2$ are body-contacted devices with the maximum available channel length in the technology (2 $\mu$m). The series combination of $M_1$ and $M_2$ is implemented for the same unit current to achieve larger area and consequently better matching and higher linearity. Using body-contacted transistors instead of floating-body devices improves the threshold voltage matching between current cells. To ensure the unit current cell area is sufficient, the effect of mismatch on INL has been studied [80]. Monte-Carlo simulation shows that two series transistor with 2 $\mu$m channel length and 30 $\mu$m channel width satisfies the matching requirement for a 10-bit DAC. Another consideration for designing the current cell is output impedance. As shown in [68], [80], [81], [82], [83], [84] higher output impedance of the current source improves the DAC linearity. In order to increase the output impedance, cascode transistor $M_3$ has been used. Since $M_3$ does not determine the current, it will not contribute in mismatch. Therefore, $M_3$ has the minimum available channel length in the technology (40 nm). The major advantage of having a small $M_3$ is reducing the effective switching capacitance [68].

Since the area of the current cells was chosen based on large current swing consideration, this had the disadvantage of reducing the output impedance. To compensate for the reduced output impedance associated with large current cells, gain boosting has been used to further increase the output impedance in each current cell. The gain boosting transistors are shown in Fig. 2.11 as $M_4$ and $M_5$. The core of the current cell ($M_1$, $M_2$ and $M_3$) is designed to provide the
Figure 2.11: Unit current cell with the bias circuit schematic.

Figure 2.12: Block diagram of the 10-bit power DAC.
desired unit current with sufficient matching. Therefore, to achieve enough output impedance the feedback path ($M_4$ and $M_5$) should be designed accordingly. In order to determine the output impedance, two effects of finite output impedance on linearity has been considered. First, nonlinearity due to the code-dependent loading variation. The third-order harmonic distortion is

$$HD_3 = \left( \frac{M \cdot R_{L,d}}{4 \cdot |Z_U|} \right)^2$$

(2.11)

where $M$ is the total number of the current cells and $R_{L,d}$ is the load [85]. This 10-bit DAC is built from a 5-bit fine DAC and a 5-bit coarse DAC and the coarse DAC is thermometer coded. So the number of current sources in coarse DAC is $M=32$. From (2.11) for a 100 Ω differential load and HD3 less than -62 dBC, $|Z_U|$ needs to be greater than 28 kΩ.

As discussed in section II, another consideration for the required output impedance is the effect of finite current source output impedance on linearity of the stacked-FET buffer. Solving (2.9) for a desired HD3 suggests a bound for the minimum required impedance. Fig. 2.13 shows the simulated output impedance of a thermometer unit current cell, before and after gain boosting, as well as minimum required thermometer current cell output impedance regarding the switching effect (2.11) and stacked-FET buffer (2.9). Calculation shows for a 3-stages stacked-FET current buffer with -62 dBC HD3, the output impedance of a thermometer unit current source at low frequencies should be more then 200 kΩ and should increase at high frequency. Beyond 340 MHz, HD3 cannot be better than -62 dBC even for an infinite source impedance. Applying the local negative feedback increases the output impedance from 233 kΩ to 1.65 MΩ at low frequencies and satisfies the stacked-FET linearity constraint up to 55 MHz.

### 2.3.2 Block Diagram

Fig. 2.12 demonstrates the block diagram of the implemented 10-bit power DAC. A deserializer converts the 10-bit serial input data to 10 parallel bits and divides the clock by a factor of 10. The 5 MSBs are being fed to a binary-to-thermometer decoder to generate the demanded thermometer codes to control
the 31 thermometer-coded switches. In order to synchronize the data, a delay block is introduced to the 5 LSBs path to generate the same delay as binary-to-thermometer decoder. Each current source is connected to a differential pair of the switches. It is necessary that the switches connected to a single current source never simultaneously be in the off state [80]. Here switches are nMOS transistors so a differential controlling signal with high crossing point is demanded [80]. In the latch shown in Fig. 2.12, the intrinsic delay between the two complementary outputs is used to lower the crossing point of the controlling signals [86]. Then an inverter is placed to invert the crossing point from low to a high value [68]. Fig. 2.12 also shows that switches are connected to the bottom of the stacked-FET current buffer and they lead the current of each current source to the left or right branch depending on the controlling signals. Current bleeders are attached to the bottom of the buffer to improve the linearity, as discussed in section 2.3. Fig.

![Figure 2.13: Output impedance of the thermometer unit current cell.](image)

2.14 shows the current source array of this design. The array is divided into 16 sub-array. In each sub-array there are 32 units of 2-LSB current source, where 31 of them are related to thermometer codes. Another unit in eight of the sub-arrays represents the 5th binary bit (16 LSB), in four of the sub-arrays are related to the
4th binary bit (8 LSB) and in the other four sub-arrays are dummy transistors. The three other binary bits (4 LSB, 2 LSB and 1 LSB) are in the center of the array. There are also dummy transistors around the current array to provide a better matching. In Fig. 2.14, 16 units, each one in a sub-array are highlighted.

Figure 2.14: Layout for current source array to minimize layout variations.

These 16 units are tied together and represent a thermometer code (32 LSB). While the placement of the units in each sub-array is identical, the sub-arrays are rotated with respect to one another in a certain way that cancels both linear and parabolic process gradients [87].

2.4 Measurement Results

The DAC is implemented in 45-nm CMOS SOI technology and occupies 1.5 mm × 1.5 mm. Fig. 2.15 shows the chip microphotograph. The stacked-FET current buffer on top of the current sources requires a 4-V supply and consumes 84 mA for a power consumption of 336 mW. The local negative feedback in the current cells consume 102 mW from a 1.5-V supply. The de-serializer and digital
circuitry of the DAC consume 38 mW from a 1-V supply. Therefore the total power consumption of the chip is 476 mW. All the measurements have been done at the full-scale output current of 60 mA and a 100-Ω differential load. For INL

![Chip photograph of the power DAC.](image)

**Figure 2.15**: Chip photograph of the power DAC.

and DNL, three parts are measured. The first chip has INL \( \leq 0.6 \) LSB, DNL \( \leq 0.44 \) LSB, the second chip has INL \( \leq 0.53 \) LSB, DNL \( \leq 0.44 \) LSB, and the third one has INL \( \leq 0.56 \) LSB, DNL \( \leq 0.44 \) LSB. Fig. 2.16 shows the measured DNL profile versus the input code and Fig. 2.17 shows the measured INL profile for the worst case of the power DAC. The LSB voltage is 6 mV and DNL and INL measurements are done with 1 mV accuracy (1/6 of the LSB). Fig. 2.18 demonstrates the dynamic measurement setup. An Agilent N9403B signal generator generates the clock and also provides external clock for Agilent 81134A. Additionally, an Agilent 81134A dual channel pulse pattern generator (PPG) provides the synchronous serial data and reset signal. The time-domain output swing of the power DAC is captured
Figure 2.16: Measured DNL versus input code.

Figure 2.17: Measured INL versus input code.
with an Agilent DSO80604B oscilloscope. For linearity measurements, an Agilent E4448A spectrum analyzer is used. Since the maximum data rate of the PPG is 3 GS/s, the on-chip 1:10 deserializer limits the DAC measurement to a Nyquist rate of 300 MS/s. Fig. 2.19 shows the measured output voltage of the power DAC for an input code related to a sinusoid full swing at 150 kHz. As Fig. 2.19 demonstrates, the power DAC generates a $6.3 \, V_{PP}$ differential output swing. This swing is achieved without subjecting the device to breakdown swings. The circuit is subjected to breakdown by increasing the current and simultaneously increasing the supply voltage. Measurement shows that the power DAC is can generate up to $9.5 \, V_{PP}$ before reaching destructive breakdown. This break-down voltage swing is 60% higher than the specified swing. From (1) this is equivalent to 50% deviation from nominal value for the smallest capacitor used in the buffer. Fig. 2.20 shows the measured output power of the DAC from DC to the Nyquist frequency over a 100 $\Omega$ differential load. The 3-dB bandwidth of the output power is more than 100 MHz. To determine the linearity, both SFDR and IM3 are measured at different frequencies. For these measurements, the chip is tested with a full swing signal at the output and sampling rate is 300 MHz. Fig. 2.21 shows the SFDR at low frequency. While the main tone is at 375 kHz and the major spur is the third order harmonic, the SFDR is 73 dB. The SFDR is recorded as a function of signal frequency in Fig. 2.22 and shows 57 dB SFDR at Nyquist rate. Fig. 2.23 shows the measured output for a two-tone test at low frequency. In the two-tone test, each tone is at 6 dB back off with respect to full swing. Therefore, the peak envelope reaches the full swing signal. The power DAC achieves -69 dBc IM3 at 4 MHz. The IM3 power under these conditions are plotted versus signal frequency in Fig. 2.24 and shows -58 dBc IM3 at Nyquist rate. Fig. 2.24 also indicates that beyond 50 MHz the measured IM3 degrades from -62 dBc. This agrees with the theory and simulation results presented in Fig. 2.13. Improvements compared to the measurement results presented in [88] were yield from using the spectrum analyzer rather than oscilloscope. Table 3.1 compares this DAC with published current steering DACs [68], [78], [80], [85], [89]. As it can be seen the maximum voltage swing varies significantly from $0.75 \, V_{PPd}$ in [89] to $6.3 \, V_{PPd}$ (this work). When
Figure 2.18: Dynamic measurement setup.

Figure 2.19: 6.3 \( V_{PPd} \) measured differential output swing at 150 kHz.
Figure 2.20: Measured output power over 100 Ω differential load.

Figure 2.21: Measured SFDR at 375 kHz.
Figure 2.22: Measured SFDR, DC to Nyquist. One-tone test at full swing.

Figure 2.23: Measured IM3 at 4 MHz.
the power consumption is being compared, the available power for the load also should be considered. Therefore, the normalized power efficiency (NPE) proposed in earlier work is adopted here [68]. The NPE is defined as

\[ NPE = \frac{P_{\text{peak}}(R_{\text{load}})}{0.25P_{\text{supply}}} \]

where \( P_{\text{peak}}(R_{\text{load}}) \) is the peak available power for the load.

As table 3.1 shows, this work demonstrates the highest power efficiency and the largest output voltage swing.

## 2.5 Conclusion

A 10-bit, 300-MS/s current-steering power DAC is demonstrated in 45-nm CMOS SOI and generates a 6-\( V_{pp} \) differential output swing into a 100-\( \Omega \) differential load. A stacked-FET current buffer is used to produce the high voltage swing and avoid transistor breakdown. Using a Volterra series analysis, the linearity of the stacked-FET buffer is described to present fundamental trade-offs in the number of stacked stages and HD3. The results demonstrate a 3-stage stacked-FET current buffer.
Table 2.1: Comparison With Published Data

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<th>[78]</th>
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buffer to provide sufficient HD3 for 10-b operation. Additionally, the local negative feedback is used to increase the output impedance of the DAC current cells.

Appendix A

Substituting (2.2) into (2.5a), the gate-source voltage becomes

$$v_{gs} = -\alpha \left[ Z_1(s) \circ i_s + Z_2(s_1, s_2) \circ i_s^2 + Z_3(s_1, s_2, s_3) \circ i_s^3 \right]. \quad (2.12)$$

Applying this to (2.4) and substituting the $v_{gs}$ from (2.12), the Volterra series of $i_{ds}$ is derived as

$$i_{d,1}(s) = \left[-g_m\alpha Z_1(s)\right] \circ i_s \quad (2.13a)$$

$$i_{d,2}(s_1, s_2) = \left[ -g_m\alpha Z_2(s_1, s_2) + \frac{1}{2}g_m'\alpha^2 Z_1(s_1) Z_1(s_2) \right] \circ i_s^2 \quad (2.13b)$$

$$i_{d,3}(s_1, s_2, s_3) = \left[ -g_m\alpha Z_3(s_1, s_2, s_3) + g_m'\alpha^2 Z_1(s_1) Z_2(s_2, s_3) - \frac{1}{6}g_m''\alpha^3 \prod_{i=1}^{3} Z_1(s_i) \right] \circ i_s^3. \quad (2.13c)$$
Solving for $v_d$ using KCL, the relationship between $i_{ds}$, $v_s$ and $i_s$ can be derived.

$$\left(\frac{r_o}{r_o + Z_L(s)}\right) \times i_{ds} + i_s = \left(\frac{1}{Z_S(s)} + \frac{1}{Z_{gs}(s) + Z_g(s)} + \frac{1}{r_o + Z_L(s)}\right) \times v_s \quad (2.14)$$

Now, the linear term of the $v_s$ from (2.5a) ($Z_1(s) \circ i_s$) and the linear term of the $i_{ds}$ from (2.13a) are substituted into (2.14) to find the first order Volterra kernel in (2.5b). To find $Z_2(s_1, s_2)$ and $Z_3(s_1, s_2, s_3)$, the second and third order terms of the the $v_s$ and also $i_{ds,2}$ from (2.13b) and $i_{ds,3}$ from (2.13c) are substituted in (2.14) to give (2.5c) and (2.5d), respectively.

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Chapter 3

Wideband Outphasing modulator

3.1 Outphasing versus Envelope Tracking

Wideband, high-data rate wireless systems generally suffer from low-efficiency or poor linearity. To realize both a linear response and high-efficiency, a variety of linearization approaches have been proposed. Polar transmitters separate the signal into amplitude and phase components [13], [14], [15]. The phase component drives a high-efficiency power amplifier (PA) while the amplitude component drives the power supply. While this improves the efficiency of the PA, the amplitude modulator requires much higher bandwidth compared to the input signal [19]. Envelope tracking systems generally struggle to reach bandwidths exceeding 100 MHz due to the difficulty to realize supply modulators that remain efficient over wide bandwidth [20], [21], [22].

An alternative to envelope tracking is linear amplification with nonlinear components (LINC) also called outphasing [44] (Fig. 3.1). In an outphasing transmitter, an input signal is separated into amplitude and phase components that are used to construct two constant-envelope phase-modulated signals. Therefore, high-efficiency PAs amplify the constant envelope signals and this improves the efficiency without degrading the linearity [58], [59]. The amplified signals are combined together to restore the amplitude and phase components of the output signal. Although, in theory, for an outphasing system combining two outphased signals would restore the original signal, any imbalance results in error. For example a
phase mismatch between the two signals translates into phase and amplitude error in the combined signal which limits the control over the output power dynamic range.

This work demonstrates a fully-integrated outphasing modulator that operates at 10 GHz in 45-nm CMOS SOI. The chip includes digital, baseband and RF circuitry and is intended as a driver for GaAs or GaN final stage PAs. Integrating high-linearity, high-speed, 10-bit digital to analog converters (DACs) provides a fine control on the amplitude and phase of each signal. Therefore, our approach demonstrates high dynamic range and excellent linearity required for wideband complex modulation. The output of the CMOS chip uses stacked-FET buffers to deliver 23 dBm to the differential 100-Ω loads [90]. As a result this modulator can drive off-chip PAs with no need for pre amplification.

Section 3.2 overviews the theory of the outphasing and also introduces the system level of the proposed wideband outphasing modulator. Circuit design of the key building blocks is discussed in section 3.3. Section 3.4 presents the measured results and compares this chip to the state-of-the-art. Finally, section 4.4 concludes the paper.

Figure 3.1: Representations of signals in an outphasing modulator.
3.2 Outphasing Modulator Architecture

3.2.1 Outphasing Description

Fig. 3.1 illustrates the signals produced by an outphasing modulator. The desired complex waveform can be represented as $S(t) = A(t)\cos(\omega t + \theta(t))$, where the amplitude $A(t)$ and phase $\theta(t)$ are modulated. The signal $S(t)$ can be decomposed into two constant-envelope phase-modulated signals

$$S_1(t) = \frac{A_{max}}{2} \cos(\omega t + \theta(t) + \phi(t))$$  \hspace{1cm} (3.1a)

$$S_2(t) = \frac{A_{max}}{2} \cos(\omega t + \theta(t) - \phi(t))$$  \hspace{1cm} (3.1b)

where the amplitude of $S_1(t)$ and $S_2(t)$ is constant and $\phi(t)$ is the outphasing angle between the two signals. The outphasing angle is a function of the $A(t)$ and the maximum value of $A_{max} = \max\{A(t)\}$.

$$\phi(t) = \arccos \left( \frac{A(t)}{A_{max}} \right).$$  \hspace{1cm} (3.1c)

Since signal power is proportional to $A^2(t)$, it is a linear function of $\cos^2(\phi)$. At the maximum amplitude of the input signal, the outphasing angle is zero and $S_1$ and $S_2$ sum in-phase. As the amplitude reduces, the outphasing angle increases and if the amplitude of the input signal is zero, $\phi$ is $90^\circ$ which results in complete cancellation of $S_1$ and $S_2$. The cancellation of the signals is sensitive to the ability of the circuitry to generate accurate phase shift between the two signals. This is explained in the next two sections in details.

3.2.2 Outphasing Accuracy for High-Dynamic Range

Unfortunately, outphasing angle errors exist that impact the ability of the modulator to perfectly cancel the two signals. Imperfect cancellation results in a floor on the output power of the modulator and defines a dynamic range between the maximum output power and minimum achievable output power. Consider a phase error between the signals of $\delta$, ((3.1a)) and ((3.1b)) can be rewritten as
When the signals are ideally combined, the output signal is

\[ S_{\text{out}}(t) \approx A(t) \cos(\omega t + \theta(t)) + S_{\text{err}}(t) \]  

(3.3)

where

\[ S_{\text{err}}(t) \approx \frac{\delta}{2} \left( \sqrt{A_{\text{max}}^2 - A^2(t)} \cos(\omega t + \theta(t)) - A(t) \sin(\omega t + \theta(t)) \right) \]  

(3.4)

From (3.3), \( S_{\text{out}}(t) \) is approximated by \( A_{\text{max}} \cos(\omega t + \theta(t)) \) when \( A(t) \approx A_{\text{max}} \) but when \( A(t) \to 0 \), \( S_{\text{out}}(t) \approx S_{\text{err}}(t) \approx (1/2)\delta A_{\text{max}} \cos(\omega t + \theta(t)) \). Thus, the dynamic range (DR) is calculated from the ratio of maximum power over minimum power.

\[ DR = 10 \log_{10} \left( \frac{A_{\text{max}}^2}{(1/4)\delta^2 A_{\text{max}}^2} \right) = 10 \log_{10} \frac{4}{\delta^2}. \]  

(3.5)

Fig. 3.2 presents the dynamic range as a function of phase error. If the outphasing modulator should be accurate over a dynamic range of 60 dB, then the phase errors should be controlled on the order of 0.1 degree.

### 3.2.3 Outphasing Architecture

Fig. 3.3 demonstrates the architecture of the proposed outphasing modulator. Deserializers are used to convert the serial input data to parallel data. There are two channels that generate separate I/Q modulation through quadrature mixers to implement \( S_1 = I_1 + jQ_1 \) and \( S_2 = I_2 + jQ_2 \). The use of current buffers at the output protects the modulator from breakdown due to the large output voltage swing. The output of this chip has an open-drain structure and the voltage bias is provided with off-chip bias-T networks.

The \( I \) and \( Q \) data on each of the two channels can be derived from (3.1a) and (3.1b). For instance,
Figure 3.2: Dynamic range as a function of the error in the outphasing angle.

Figure 3.3: Block diagram of the implemented outphasing modulator.
\[ S_1(t) = \frac{A_{\text{max}}}{2} \left( \cos(\omega t) \cos (\theta(t) + \phi(t)) - \sin(\omega t) \sin (\theta(t) + \phi(t)) \right) \]  

(3.6)

\[ S_1(t) = I_1 \cos(\omega t) + Q_1 \sin(\omega t) \]  

(3.7)

where \( I_1 = (1/2)A_{\text{max}} \cos (\theta(t) + \phi(t)) \) and \( Q_1 = -(1/2)A_{\text{max}} \sin (\theta(t) + \phi(t)) \). The second channel has the opposite sign for \( \phi(t) \). Each channel has two current steering digital-to-analog converters (DACs) to convert digital \( I \) and \( Q \) data to analog currents. The DAC resolution determines the phase accuracy of this architecture. To determine the minimum number of bits for a given phase accuracy, it should be considered that from (3.1c) \( \phi(t) \) is not a linear function of amplitude \( A(t) \). Therefore, the phase resolution is not constant over the 0° to 90° range of \( \phi(t) \), and for an \( N \)-bit DAC it cannot be calculated with a simple equation such as \( 360/2^N \). Fig. 3.4 presents the phase resolution versus outphasing angle in an outphasing system for DACs with different number of bits. For a signal in the form of \( I + jQ \), \( I \) and \( Q \) are quantized to \( N \) bits and swept over the full range of 0 to \( 2^N - 1 \). Then, the outphasing angle \( \phi(t) \) is calculated from (3.1c) where \( A(t) = \sqrt{I^2 + Q^2} \). To find the phase resolution, the difference between the outphasing angles for each of the two adjacent codes are calculated. One observation is that for a given DAC number of bits, the phase resolution increases as \( \phi \) increases and the finest resolution is achieved near \( \phi = 90^\circ \). Since (3.5) shows that the phase error at \( \phi \) close to \( 90^\circ \) determines the dynamic range, this is an advantage in an outphasing system for improving the dynamic range. This conclusion can also be explained intuitively: the output power is not very sensitive to phase variation at small outphasing angles. For instance, a phase step of 5° at \( \phi = 0 \) only results in 0.03 dB power variation or changing the outphasing angle from 0° to 45° only changes the power for 3 dB. Whereas at outphasing angles close to 90° power changes dramatically with phase variations.

From the previous section, the phase at low output power (\( \phi \) near 90°) needs to be controlled to within 0.1° accuracy for 60-dB dynamic range. Fig. 3.4 indicates that 9-bit DACs will result in 0.11° phase resolution, marginally
failing the 0.1° requirement. This work has therefore implemented 10-bit DACs to satisfy the phase control requirement for a 60-dB dynamic range while providing some margin for calibration of I/Q mismatch. While the phase resolution of the $\phi$ determines the amplitude accuracy of the signal, the resolution of the $\theta$ impacts the phase accuracy of the signal. Unlike $\phi$, $\theta$ is not a function of the $A(t)$ and it can be related to the number of bits using $360/2^N$.

### 3.3 Circuit Implementation of the Outphasing Modulator

The architecture includes both baseband and RF blocks that can be optimized to improve the performance of the overall modulator. The baseband section includes deserializers and current steering DACs while the RF section includes quadrature mixers, stacked-FET current buffers and LO routing.
3.3.1 RF

Fig. 3.5 presents the double-balanced upconversion quadrature mixer and the stacked-FET current buffer for one of the two channels. Placing a current-to-voltage, e.g. transimpedance, conversion before the load potentially degrades the linearity and is avoided. The baseband current swing from I and Q DACs are fed to the bottom of a differential mixer. Then, the baseband current is upconverted to RF through the switch-mode mixer driven by differential quadrature LO. Each of the two channels are designed to deliver 20 dBm output power to an external 100-Ω load. Consequently, the current swing at the mixer is high and generates a large voltage swing across a 100-Ω differential load. Connecting the mixer directly to the load would result in a large voltage swing across the mixer and potentially limits the linearity of the upconverter. Also, it would put the devices under breakdown stress.

![Figure 3.5: Quadrature double-balanced upconversion mixer.](image)

To produce a highly linear upconversion, a stacked-FET current buffer is added on top of the mixer. Unlike the cascode structure where the gate is ac
grounded, the stacked-FET attaches capacitors to the gate to generate a voltage swing at the gate which is in-phase with the voltage swing at the source and drain to reduce the gate-source and drain-gate voltage swing [90]. The larger the ratio of the gate-source capacitance \( C_{gs,i} \) to the gate capacitance \( C_i \), the higher the impedance at the source. Therefore, \( C_{gs,3}/C_3 \) is designed to be larger than \( C_{gs,2}/C_2 \) to increase the voltage swing gradually as the current signal travels through the buffer. The resulting output voltage swing is much higher than the breakdown voltage of a single device while no transistor is under breakdown stress [90]. The top device of the stacked-FET buffer is a thick-oxide transistor which tolerates a DC voltage of 1.65 V and a voltage swing of 3.3 \( V_{pp} \).

Fig. 3.5 also indicates two current bleeders attached to the bottom of the mixer. These are 10-mA dc current sources to provide dc current for both sides of the differential structure even if all the 60-mA baseband current is switched to one side [90]. This will improve the linearity by keeping the devices always on [91]. To evaluate the linearity of the mixer and stacked-FET buffer, the OIP3 is simulated by performing a two-tone test. For this simulation, two ideal current sources are attached to the bottom of the quadrature mixer and represent the I and Q DACs and a quadrature 10-GHz rail-to-rail LO is applied to the mixer. Fig. 3.6(a) shows the simulated OIP3 is 34.2 dBm for a baseband two tone at 10 MHz and 11 MHz.

To study the power handling, \( P_{1dB} \) is simulated with single-tone input at 10 MHz. Fig. 3.6(b) depicts a \( P_{1dB} \) of 21.8 dBm. In both Fig. 3.6(a) and Fig. 3.6(b), the x-axis is the current swing normalized to the current that results in a 20-dBm output power.

Two quadrature double-balanced mixers on both output channels are driven with differential quadrature LO signals. The modulator is designed to work with a single-ended external LO, and the LO chain is designed to minimize the phase imbalance (Fig. 3.7). First, a passive balun is used to generate a differential LO. Then, an active power divider splits the differential LO and routes each signal to the two outphasing channels. After the divider, one current mode logic (CML) buffer in each channel boosts the signal before reaching the polyphase filter (PPF). PPFs are located after the power divider to generate quadrature LO for the quadrature
Figure 3.6: (a) Simulated OIP3. (b) Simulated $P_{1dB}$ compression point.
mixers of the two channels. This type-1 PPF provides quadrature signals. There is, however, an intrinsic amplitude mismatch associated with the type-1 PPF at an offset from the center frequency, and that limits the center frequency bandwidth. By adding CML buffers after the PPF, this amplitude mismatch is minimized over the modulation bandwidth. These buffers have a gain of 10 dB at 10 GHz and drive the signals across a 1-mm routing distances.

Figure 3.7: LO signal chain.

### 3.3.2 Serial Deserializer

A 1-to-10 bit deserializer is designed for each of the high-speed DACs in order to reduce the number of pins and avoid running multiple parallel high-speed digital signal paths on the PCB board. Fig. 3.8 presents the implemented deserializer. A shift register based on positive edge-triggered D flip-flops is put into a known state by a reset signal. The output of the flip-flops are zero when the
reset is active except for the one at the bottom of the first column shown in Fig. 3.8 which is set when reset is active. Once reset is false, clock (clk) and data (D) dictate the state of the output of each flip-flop.

Figure 3.8: Circuit schematic of the 1-to-10 bit deserializer.

At the first column, the input clock is connected to the clk of all the flip-flops and Q of each flip-flop is connected to the D of the next element in the shift register. As Fig. 3.8 shows the Q of the final register feeds back to the first element in the shift register. Consequently, the high state in the final register travels through the first column at the clock rate. Since first column consists of 10 registers the period of the clock is 10 periods of the serial clock.
The Q of the flip-flops of the first column are connected to the clock of the second column while the input serial data drives the port D of the second column. Therefore, at the Q of the second column the parallel data is available. However, since each of the flip-flops is triggered with the signal provided from the first column, the parallel data is not aligned to a single clock edge of the clk/10. In order to synchronize the parallel data, a third 10-b register is triggered with a common bus-rate clock (clk/10). The rising edge of the clk/10 happens once all 10 parallel bits are triggered. Therefore, the output of the fifth and tenth flip-flops of the first column are connected to an OR gate. The output of the OR gate triggers a D flip-flop while the $Q$ is connected to the D to implement a frequency divider that generates a 50% duty cycle clock. To avoid timing skew errors, a buffer is added after the D flip-flop to make sure that the rising edge of the clk/10 gets to the third column of the flip-flops with a delay compared to the data. However, this delay should not be too long to make sure that the rising edge occurs within the desired packet of the 10-bit serial data and not within the next packet. In this design, 11 inverters are connected in series to provide the delay. The number of the inverters should be odd to generate a correct rising edge.

### 3.3.3 Digital-to-Analog Conversion

Fig. 3.9 shows the 10-bit current-steering DAC, and is implemented with a combination of unary and binary bits. There is an intrinsic trade-off between linearity and speed such that the higher the number of the unary bits, the higher the linearity and the lower the speed [92], [93]. To implement a modulator capable of supporting data rates higher than 1 Gbit/s, given that the modulation is 256-QAM, DACs should be able to operate above 125 MS/s. The implemented DAC is segmented into 5 unary MSBs and 5 binary LSBs to achieve a high linearity while allow for the required data conversion rate. This DAC is measured separately and achieved an SFDR and IM3 better than 57 dB and -58 dBC, respectively, up to 300-MS/s data rate [90].

A binary-to-thermometer decoder converts the 5-bit MSBs to 31-bit thermometer code and a delay block in front of the 5-bit LSBs synchronizes the data.
at the DAC. The delay block is implemented using a chain of inverters on each data path and latches on the data path synchronize the data. Each current source is connected to a differential switch pair which is controlled by the signal from the latch.

![Circuit schematic of the 10-bit current steering DAC.](image)

Figure 3.9: Circuit schematic of the 10-bit current steering DAC.

In a current-steering DAC, the size of the unit current cell ($W \times L$) needs to be designed carefully since it determines the matching between the current sources which effects the linearity at low data rates. On the other hand, the ratio of ($W/L$) is determined by the LSB current. In this 10-bit DAC, a 60-mA peak-to-peak current swing is required which results in a 59-uA LSB current. To achieve the required LSB current with enough matching between current sources for a 10-bit linearity, the unit current cell is designed with $W = 30\mu m$ and $L = 4\mu m$.

Another key factor is the output impedance of the current sources. This is another limiting factor of the system linearity. To increase the output impedance and satisfy the requirement for a 10-bit linearity, cascode devices and also $g_m$ boosting are used in the current sources. More details on the implemented current steering DAC is available in [90]. In the proposed current mode up conversion, no anti-aliasing filter is incorporated between the DAC and the mixer. Since the
architecture relies on current mode operation, a conventional gm-C filter cannot be placed between the DAC and the mixer. This is a drawback of this approach. To compensate, the DAC sampling frequency can be increased to push the aliases to a higher offset frequency.

### 3.4 Measurement Results

![Die photograph of the outphasing modulator.](image)

**Figure 3.10:** Die photograph of the outphasing modulator.

The outphasing modulator is implemented in a 45-nm CMOS SOI technology and occupies $3 \text{ mm} \times 3 \text{ mm}$. Fig. 3.10 shows the chip micrograph. To maintain the layout symmetry, four input digital data lines are located at the corners while the RF outputs are routed from the left and right sides. The stacked-FET output buffers and quadrature mixers on top of the DACs require a 4-V DC supply and
consume 280-mA current. The DACs also consume 232 mA from a 1.5-V supply. The LO distribution circuitry including the active power divider and CML buffers consume 78 mA from a 1.5-V supply. Finally, the digital circuitry consumes 135 mA from a 1-V supply. The total chip power consumption is 1.72 W.

Fig. 3.11 presents the measurement setup. The chip is wire-bonded to an FR-4 PCB. Coplanar waveguide (CPW) transmission lines carry the differential input serial data \((I_1, I_2, Q_1, Q_2)\) at rates as high as 4 GS/s along with a 4-GHz differential clock and a reset pulse with sharp rise edge. The LO frequency is nominally 10 GHz as well as the output signal \((S_1, S_2)\) which are at the LO frequency. A Picosecond 12070 serial data generator (SDG) provides the serial data and also trigger signal for an Agilent 81134A pulse pattern generator (PPG) which provides the reset signal for the chip. A Hittite 1-to-4 demultiplexer (DEMUX) is located between the SDG and the outphasing modulator to feed the serial data into four DACs of the modulator and operates to 16 GHz, limiting the maximum clock rate to 4 GHz. The 10-bit deserializer converts the serial data to 10 parallel data and the maximum clock rate at the DACs is 400 MHz. An Agilent E8257D PSG analog signal generator provides a 10-GHz LO for the upconverter mixers.

DC bias is provided through Picosecond 5542 Bias-Tees and a SigaTek SP64205 two-way Wilkinson power combiner sums the outphasing channels \((S_1, S_2)\) to reproduce the desired waveform. To capture the spectrum, Agilent E4448A PSA spectrum analyzer is used. For time domain measurements, a Tektronix 72004C oscilloscope is used. This is a 100-GS/s oscilloscope with 20 GHz analog bandwidth and 8 bit resolution which is sufficient to measure EVMs as low as 0.3\% [94]. Fig. 3.11 illustrates how the outputs are connected to the oscilloscope and PSA. For certain tests, the output of the power combiner is connected to the oscilloscope and each of the channels are connected to the PSA.

### 3.4.1 Channel Measurements

Each I/Q channel has been measured separately. To evaluate each of the channels, the SDG provides I and Q baseband digital data representing either a single or dual tone signal. The two PSAs capture the output spectrum of each
channel in single-ended mode while the other output of each channel is terminated to 50 Ω. Fig. 3.12(a) shows the measured output spectrum centered at 10 GHz while the baseband data is a 10-MHz single tone sine wave. This channel has -33 dB of LO leakage and 41 dB of sideband suppression. This is a single ended measurement and each channel generates 17 dBm single-ended output power which is equivalent to a 20-dBm differential output power. Adjusting the dc level of I and Q through the LSBs of each DAC improves the LO leakage and equalizing the swing of I and Q improves sideband suppression. These calibrations are performed initially and then used to compensate the baseband data. Fig. 3.12(b) demonstrates the measured spectrum at the output and shows that the calibration improves the LO leakage and sideband suppression to -63 dB and -52 dB, respectively. The performance of both channels are similar to within 1 dB.

Fig. 3.13(a) presents the measured output power as a function of the DAC current swing. For this measurement, the input digital signal represents a single-tone sine at 10 MHz. At high output powers, the $P_{1dB}$ is slightly more than 20 dBm, however, it is not possible to measure $P_{1dB}$ exactly since the maximum DAC current swing is reached and the output power does not exceed 20 dBm. Measurements for the two tone test is shown in Fig. 3.13(b). To measure $OIP3$, the baseband
Figure 3.12: (a) before calibration. (b) After calibration.
Figure 3.13: (a) Measured $P_{1dB}$ compression point (b) Measured $OIP3$. 
signal is the sum of two sine waves at 10 MHz and 11 MHz. \( OIP3 \) is 31 dBm for one of the channels and is 32 dBm for the other channel. This represents exceptional linearity performance for RF-CMOS at microwave frequencies. The measured \( OIP3 \) and \( P_{1dB} \) are in-line with the simulated results of the quadrature mixer and stack-FET presented in Fig. 3.6(a) and Fig. 3.6(b), respectively.

### 3.4.2 Outphasing Measurements

![Figure 3.14](image)

**Figure 3.14:** Measured power versus outphasing angle \( \phi \).

Fig. 3.14 presents the measured output power of the outphasing modulator \((S_1 + S_2)\) versus the outphasing angle \((\phi)\) as well as the power of each of the channels. For this measurement, the digital input data represents two outphased sine waves at 10-MHz with maximum swing. Fig. 3.14 shows a 60.3 dB dynamic range for the outphasing output while both outphased signals are at maximum power. For a given phase variation, as \( \phi \) gets closer to 90 degree, the power variation increases. Therefore, the measurement is done with higher phase resolution for outphasing angles close to 90 degree to demonstrate that the modulator is capable of covering 60.3 dB dynamic range with power steps smaller than 1 dB.
Fig. 3.15 plots the measured output power of the outphasing modulator as a function of $\cos^2 \phi$, which is a linear function described in Section 3.2. Fig. 3.15 also depicts the measured output power deviation from the theory. The least significant bit (LSB) is defined as maximum output power (200 mW) divided by 1024 since 10-bit DACs are used. At low and high output powers DNL is less than one LSB but at moderate power levels it degrades and increases to three LSB. This occurs because calibration is applied to correct the phase and amplitude only at minimum and maximum power ($\phi = 0$ and $\phi = 90$). Digital pre-distortion (DPD) could be applied to correct for power errors based on an arbitrary outphasing angles.

The sum of the two constant envelope outphasing signals reproduce the desired complex signal with phase and amplitude modulation. To demonstrate this behavior, a 10-MHz 256-QAM waveform is created at 10 GHz and each of the channels is observed in Fig. 3.16. One output of each channel is connected to a port of the oscilloscope while the other output is combined through the Wilkinson combiner to the other channel and monitored on the oscilloscope. While the envelope of $S_1 + S_2$ is varying, $S_1$ and $S_2$ are constant envelope. The 256-QAM
Figure 3.16: Measured output swings.

input digital data is not filtered to demonstrate the sharp rising and falling edges of $S_1 + S_2$ envelope.

To evaluate the waveform quality of the outphasing modulator, different quadrature amplitude modulation (16-QAM, 64-QAM and 256-QAM) at low (10 MHz) and high (135 MHz) data rates as well as a 100-MHz LTE-Advanced carrier aggregation were measured. Since the maximum available clock rate was 400 MHz, the maximum data rate was limited to 133 MHz to be able to perform effective digital filtering on the input data.

Fig. 3.17 shows the measured output spectrum and constellation for a 16-QAM waveform at the low and high data rate. For the 10 MHz modulation with 6.1 dB peak-to-average power ratio (PAPR), the EVM is 2.1%. Also, from the spectrum the lower and upper ACLR is 37.1 dBc and 37.0 dBc, respectively. For calculating the ACLR for all the QAM waveforms, a guard band of 20% of the bandwidth is considered between the main channel and adjacent channel. Fig. 3.17 also shows that for 133 MHz modulation with 6.6 dB PAPR, the EVM is 3.4%. The lower and upper ACLR is -35.1 dBc and -35.4 dBc, respectively.

Fig. 3.18 shows the measured constellation and output spectrum for a 64-
Figure 3.17: Measured constellation and spectrum for a 16-QAM modulation.

Figure 3.18: Measured constellation and spectrum for a 64-QAM modulation.
Figure 3.19: Measured constellation and spectrum for a 256-QAM modulation.

QAM waveform. At 10 MHz with 6.6 dB PAPR, the EVM is 2.2% and the lower and upper ACLR are -37.2 dBc and -36.9 dBc, respectively. At 133 MHz with 7.1 dB PAPR the EVM is 3.5% and the lower and upper ACLR are -35.2 dBc and -35.6 dBc, respectively.

A 256-QAM waveform is also measured at low and high data rates and the results are shown in Fig. 3.19. At 10 MHz with 6.3 dB PAPR, the EVM is 2.2% and the lower and upper ACLR are -37.0 dBc and -37.5 dBc, respectively. At 133 MHz with 7.2 dB PAPR, the EVM is 3.5% and the lower and upper ACLR are -35.2 dBc and -35.6 dBc, respectively. Therefore, the implemented outphasing modulator is capable of 1.1 Gbit/s data transmission. This is the highest data rate published for outphasing modulators. Note that the 4-to-1 Demux is the limitation on the maximum measured data rate. The low measured EVM and ACLR at 133 MS/s indicates the outphasing modulator could support data rates higher than 1.1 Gbit/s.

One observation from comparing measured results for 16 QAM, 64 QAM and 256 QAM is that the EVM is not a function of the number of symbols in the constellation. For an I/Q modulator, nonlinearity (AM-AM and AM-PM of the current buffer) would degrade the EVM for higher number of symbols in QAM [94]. An advantage of the outphasing modulator is that each of the two I/Q channels
operate with constant envelope signals and the EVM is not influenced by strong AM-AM and AM-PM compression.

A 100-MHz LTE-Advanced carrier aggregation signal (which is the maximum aggregated bandwidth) with 8.3 dB PAPR is also measured. Fig. 3.20 shows the output spectrum. The lower and upper ACLR is -35.9 dBc and -36.4 dBc, respectively. For the LTE waveform, 90% of the channel bandwidth is signal. This measurement suggests that our outphasing modulator can support wideband complex modulations.

Table 3.1 compares this work with published state-of-the-art outphasing modulators. This work is the first published microwave outphasing modulator and also one of the few published outphasing modulators including the digital, baseband and RF blocks on-chip. One should consider that manuscript presents the modulator and since the PA is not included, efficiency is not discussed. The system operates at a 1.1-Gbit/s data rate to offer the highest modulation rate among the published RF and microwave outphasing modulators. To our knowledge, this is also the first demonstration of 256-QAM modulation using outphasing.

3.5 Conclusion

A 10-GHz outphasing modulator with more than 60 dBc dynamic range and capable of supporting 100-MHz LTE-Advanced carrier aggregation and 1.1-Gbit/s 256-QAM is implemented in 45-nm CMOS SOI. Analysis shows that to
Table 3.1: Comparison With Published Data

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*PA Only.

achieve 60 dB dynamic range as well as performing calibration, a 10-bit DAC is required. Therefore, four 10-bit power DACs are integrated on-chip to convert the baseband I and Q digital data to analog current swing. Quadrature double-balanced switching mode mixers upconvert this current signals to 10 GHz, and the modulated microwave current signals flow into the stacked-FET buffers which protect the mixers and DACs from breakdown. Each channel of this outphasing modulator delivers 20 dBm power which is sufficient to drive high-power off-chip PAs without need for any pre-amplification.

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Program (FA8650-11-C-7184). The dissertation author was the primary author of this material.
Chapter 4

Polar Modulator Based on Coupled-Oscillators

This chapter describes a proposed analog technique to drastically reduce the power consumption of an outphasing polar modulator. The outphasing modulator is based on the dynamics of coupled oscillators. The analysis of this coupled oscillator system will be discussed in the following sections accompanied with discussion of the circuitry required to implement this circuit. Measurements of an RFIC using a 45-nm CMOS SOI process is demonstrated that operates at X-band.

4.1 Proposed Outphasing Concept and Architecture

The polar representation of a signal \( s(t) = A(t)e^{j\theta(t)} \) can be extended to an outphasing representation based on \( s_1(t) = \frac{1}{2}A_{\text{max}}e^{j(\theta(t)+\phi(t))} \) and \( s_2(t) = \frac{1}{2}A_{\text{max}}e^{j(\theta(t)-\phi(t))} \) as shown in Fig. 4.1 and discussed in the previous chapter. The outphasing angle is

\[
\phi(t) = \arccos \left( \frac{A(t)}{A_{\text{MAX}}} \right),
\]

where \( A_{\text{MAX}} = \max(A(t)) \). When the two outphasing signals are added with an ideal power combiner, the output power is
\[ P_O = P_{MAX} \frac{1 + \cos 2\phi}{2}, \]  

(4.2)

where \( P_{MAX} \) is the maximum power. As the outphasing angle changes from 0 degrees to 90 degrees, the output drops from the maximum power to 0.

Figure 4.1: Amplitude to phase modulation

4.1.1 Injection Locked Oscillators

Rather than rely on a digital circuit to compute the outphasing angle from the amplitude as demonstrated in the previous chapter, this chapter presents the use of injection-locked oscillators to implement the \( A \) to \( \phi \) transformation. In an injection locked oscillator, frequency detuning can be used to produce a phase shift between the injected signal and the oscillator output phase. The injected frequency \( \omega_i \) is detuned from the natural frequency \( \omega_o \). Within the locking range \( \omega_L \) of the oscillator, the oscillator frequency will lock to the injected frequency but produce a phase shift of

\[ \phi = \arcsin \left( \frac{\omega_o - \omega_i}{\omega_L} \right). \]  

(4.3)

The locking range has been demonstrated to be related to the circuit parameters, e.g. \( \omega_L = \frac{2}{Q} \frac{I_{inj}}{I_{osc}} \omega_o \), where \( Q \) is the quality factor of the resonator, \( I_{inj} \) is the injected current, and \( I_{osc} \) is the oscillator current swing [97–99]. As the injected current increases, the locking range is also increased. Additionally, the natural frequency in a VCO can be controlled through an external control voltage \( V_{tune} \). Each VCO has MOS varactors. Fig. 4.2 shows the cross-section of a conventional p-n junction MOS varactor alongside the capacitance variation. Considering Fig. 4.2 and given
that $\omega_o = 1/\sqrt{LC}$ it is expected that frequency versus detuning voltage has a compression behavior. This is shown in previous published works [100]. On the other side from 4.3 the phase is related to frequency with an arcsine function which has expansion behavior. Therefore, phase versus detuning voltage is expected to have a linear behavior and can be calculated from

$$\phi = \frac{1}{2} \left( \frac{V_{tune}}{V_{MAX}} \right) \pi$$

(4.4)

Figure 4.2: Capacitance of a MOS varactor versus bias voltage.

### 4.1.2 Bilateral Coupled Oscillators

A coupled oscillator system is constructed from the bilateral injection between two oscillators. As shown in Fig. 4.3, a resistor is used to produce the bilateral coupling between the two oscillators by means of allowing current to flow through the resistor between the resonators of each oscillator. As (4.4) shows, by detuning two oscillator differentially ($+V_{tune}$ and $-V_{tune}$) the phase at outputs of the two oscillators are $+\phi$ and $-\phi$.

However, the circuit-level simulations are used to plot the outphasing angle with respect to the applied tuning signal in Fig. 4.4. The phase shift changes essentially linearly with the applied voltage up to a phase shift of 74°. This linear behavior is compatible with (4.4). Above the amplitude of 0.34 V, the frequency detuning exceeds the locking range and the oscillator begins to pull away from the injected frequency.
Figure 4.3: Amplitude-to-phase modulation with coupled-oscillator.

Figure 4.4: Outphasing angle as a function of the signal amplitude.
At this point, the analysis and the simulation deviate for two substantial reasons. First, the outphasing angle does not reach ±90°. This occurs only when the argument of (4.3) reaches one. At this boundary, the circuit may be perturbed out of the locking range resulting in cycle slipping which is highly undesirable. Second, the tuning control on the oscillator does not fix the output frequency as a function of the amplitude. As shown in Fig. 4.5, the oscillation frequency drifts over a range of 124 MHz with different signal amplitudes.

![Oscillation frequency for different signal amplitudes.](image)

**Figure 4.5**: Oscillation frequency for different signal amplitudes.

### 4.1.3 Bilateral Master-Slave Coupled Oscillators

To fix the problems associated with bilateral injection locking, I propose to modify the previous coupled oscillator approach. First, the bilateral coupling between the two coupled oscillators is substituted with bilateral coupling from a central “master” oscillator to two “slave” oscillators as shown in Fig. 4.6. In theory, bilateral injection between three oscillators should double the achievable the phase range compared with two bilateral coupled oscillators. Circuit-level simulations are plotted in Fig. 4.7 and confirm that the phase shift reaches 105° rather than 74° before becoming unstable.

Still, the phase shift does not meet the requirement of an outphasing mod-
Figure 4.6: Amplitude-to-phase modulation with three coupled-oscillator.

Figure 4.7: Outphasing angle for three coupled-oscillators.
ulator (\(\Delta \phi = 180^\circ\)). Fig. 4.8 shows a frequency variation of 253 MHz over various signal amplitudes. Not surprisingly, the frequency variation is nearly twice the frequency variation demonstrated with the bilateral coupled oscillators.

![Graph showing oscillation frequency for different signal amplitudes.](image)

**Figure 4.8:** Oscillation frequency for different signal amplitudes.

To solve the frequency drift issue, the master oscillator is locked to an external reference oscillator as shown in Fig. 4.9. Since the master oscillator is unilaterally locked to the external reference, its frequency and consequently the frequency of the outphasing slave oscillators are fixed. Fig. 4.10 shows that after locking the master oscillator to an external oscillator the phase range is still far from 180°. Also locking to the external oscillator increases the detuning voltage corresponding to a 90° phase shift. Fig. 4.10 shows that the phase versus detuning voltage has a linear range and after that it is nonlinear. The linear part can be explained from (4.4). However, not surprisingly, the expansion behavior of the phase versus frequency cannot cancel out the compression behavior of the frequency versus detuning voltage for all the detuning voltages and as Fig. 4.10 shows eventually for very high detuning voltages it becomes nonlinear. It is simply because the frequency versus detuning voltage is not perfectly a sine wave and it can only be approximated with a sine wave on a limited range.
Figure 4.9: Locking the center oscillator to an external oscillator.

Figure 4.10: Outphasing angle with an external oscillator.
4.1.4 Proposed Bilateral Injection Locked Oscillator Outphasing Modulator

Fig. 4.10 shows that even though increasing the detuning voltage will increase the phase shift, beyond 90° it is not linear. Therefore, another approach other than increasing the detuning voltage should be taken. Previous work on coupled oscillators for phased array antennas encountered the limited stable range within the locking range and suggested the use of multipliers to double the phase variations [101]. Now the outphasing angle is expressed as

\[ \phi = M \arcsin \left( \frac{\omega_o - \omega_i}{\omega_L} \right), \]  

(4.5)

where \( M \) is the frequency multiplication. Fig. 4.11 illustrates how a frequency multiplier increases the phase range by the multiplication factor to satisfy the 180° outphasing angle. A factor of \( M = 2 \) is sufficient to provide the required margin for our outphasing modulator. However, higher frequency multiplication factors have the added benefit of improving the linearity of the transformation from amplitude \( A \) to \( \phi \). The disadvantage of using higher frequency multiplier factors is that any phase noise from the master and slave oscillators is also multiplied. However, this can be mitigated through the use of a low phase noise external reference [102].

Fig. 4.12 shows a general block diagram illustrating the external injected bilateral coupled oscillator outphaser with the frequency doubler and output amplifier. Since the frequency doublers are lossy, (power) amplifiers are placed after the doubler to amplify the RF signal. Circuit-level simulations are presented in Fig. 4.13 to indicate how adding the frequency doubler results in twice the phase shift for the same voltage detuning as in Fig. 4.10. Fig. 4.13 illustrates that a 180 degree phase shift is possible with an amplitude of 230 mV using \( M = 2 \). The effect of the \( M \) on the \( \phi \) in (4.4) can be described as the higher the \( M \) the smaller the \( V_{MAX} \). This is shown in the following equation:

\[ \phi = M \frac{1}{2} \left( \frac{V_{tune}}{V_{MAX}} \right) \pi = \frac{1}{2} \left( \frac{V_{tune}}{V_{MAX,M}} \right) \pi \]  

(4.6)
Figure 4.11: Stable progressive phase enhancement using frequency multiplier [4].

Figure 4.12: Adding doubler and amplifier after coupled-oscillators.
Polar modulation is implemented through differential tuning signals \( A(t) \) and \(-A(t)\) applied to each oscillator with constant envelope such that the phase difference between the oscillators is a function of the amplitude of the input signal. To produce the phase modulation, the phase modulation is produced through from the external oscillator. Since the other two oscillators are injection locked to the central oscillator, it rotates with phase \( \theta \) producing a common mode signal and the other two oscillators will also rotate with \( \theta \). Fig. 4.14 shows the block diagram of the proposed modulator. A chain of CML buffers following by CMOS buffers deliver a rail-to-rail signal to \( 50 - \Omega \) load.

Substituting the (4.4) into the (4.2), the output power of the proposed outphasing modulator is

\[
P_O = P_{MAX} \frac{1 + \cos \left( \left( \frac{V_{tune}}{V_{MAX}} \right) \pi \right)}{2}.
\]  

(4.7)

From (4.7), the normalized power can be plotted as a function of the tuning voltage in Fig. 4.15. The bilaterally coupled oscillator outphasing modulator produces an output power that behaves similarly to the ideal outphasing modulator but the argument of the outphasing response depends on the amplitude at the tuning port of the injection locked oscillator rather than through the phase produced at this
Finally, the linearity of the amplitude to power transfer function can be investigated. If we consider $V_{tune} = \frac{A}{2}(1 + \sin(\omega_m t))$, as it is shown in Fig. 4.15, and substitute this into 4.7, HD2 and HD3 can be calculated. Fig. 4.16 shows that as $A$ increases, HD2 improves and HD3 degrades. The improvement in HD2 can be explained considering the fact that $P_{out}$ is a symmetric function. Therefore, the more that $V_{tune}$ covers the $A_{MAX}$ the better the HD2.

### 4.2 Integrated Circuit Implementation

The proposed coupled oscillator outphasing system is designed in 45 nm SOI CMOS. Block level designs are presented in the following sections. Portions of the circuits used in this design were adopted from [4] and parts of the following sub-sections have been reprinted from [103].
Figure 4.15: Detuning the coupled oscillators with sine wave signal.

Figure 4.16: Calculated HD2 and HD3.
4.2.1 Oscillator & Coupling Network

A cross-coupled LC oscillator is designed as shown in Fig. 4.17. A pMOS cascode current source is used for low 1/f noise. Typically, metal-on-metal (MOM) capacitors are used for high quality factor $Q$ with discrete tuning steps. However, the analog nature of the phase modulation requires the use of the analog varactors. Therefore, MOS capacitors are used as varactors to tune the oscillator.

With improved metalization the MOS capacitor exhibits the quality factor equal to 20. A differential spiral inductor with lowest metal shield is designed and simulated using Sonnet EM Solver [104]. Grounded metal shield reduces the substrate coupling and eddy-current losses. To improve the $Q$, the inductor turns are composed of parallel connection of top three metals available in the process. Any further parallel metalization does not improve the quality factor due to reduced lower metal thickness. The simulated 1 nH inductor has a quality factor equal to 13 at 5 GHz center design frequency. A relatively large aspect ratio of cross-coupled pair improves swing at the given power consumption. The simulated tuning range for the stand-alone oscillator is 4.3 GHz to 5.5 GHz. The simulated differential voltage swing is 1.2 V with typical 4.5 mW power [103]. Three oscillators are coupled through resistive network.

Figure 4.17: Cross-coupled LC oscillator.
4.2.2 Frequency Doubler

The oscillator is followed by the frequency doubler shown in Fig. 4.18. The doubling pair is biased in class C to maximize the second harmonic for a given transistor size [105]. Cascode device reduces the effect of miller capacitance and improves input to output isolation. An LC resonant load with 10 GHz resonant frequency is used to filter the higher harmonics at the output of doubler. However, narrow-band nature of LC load causes swing variation with the oscillator tuning. A parallel 200 ohm resistor is used to reduce the quality factor of the LC load to broaden the bandwidth and thereby minimizing the swing variation. The simulated doubler loss is 8 dB with typical 1.0 V input swing at 5 GHz input frequency. The power consumption is 4.5 mW [103].

Figure 4.18: Schematic of frequency doubler in 45-nm CMOS SOI.

4.2.3 Active Balun

An active balun amplifies the 10 GHz doubler output while converting it to differential signal. No matching inductors are used to save the area. The first stage of active balun is resistively loaded NMOS differential pair. A push-pull type second stage is added to improve the amplification. The active balun amplifies the signal by 9 dB while consuming 7.5 mW power [103].
4.3 Measurement Results

The die photograph for the prototype bilateral injection locked oscillator outphasing modulator is shown in Fig. 4.19. The circuit is implemented in 45-nm CMOS SOI and consumes 140 mW from 1.5-V supply.

Figure 4.19: Chip microphotograph of the 45-nm CMOS SOI prototype.

To test the outphasing modulator, we demonstrate the static and dynamic performance separately. Fig. 4.20 illustrates the proposed test setup for the static and dynamic measurements. First, the individual oscillator performance is characterized through the use of frequency-tuning curves. Then the injection locking of the oscillators is characterized to show the locking range and the phase shift that is produced. The static outphasing response is demonstrated to show that a full 180 degree tuning range is possible with the use of the frequency doublers. Finally, we investigate dynamic performance of the outphasing modulator in terms of the generation of harmonic distortion and the bandwidth dependence of the outphasing modulator.
4.3.1 Oscillator Characterization

First, the tuning range of the slave oscillators is characterized by sweeping DC tuning voltage and measuring the oscillator output. In this case, the oscillator output is measured at the output of the doubler and therefore the frequency is twice of the actually oscillator frequency. Fig. 4.21 shows the tuning range and that the oscillator has a relatively wide tuning range of 2.3 GHz when the tuning voltage is swept over 1 V. Fig. 4.21 shows the compression behavior as it was predicted and discussed in the previous section. A sample spectrum is illustrated in Fig. 4.22 for single channel. The output power of the doubler is 1.5 dBm at 8 GHz. Also present is the 3rd harmonic at 24 GHz which is -20 dBc relative to the carrier and the 2nd harmonic at 16 GHz which is -40 dBc relative to the carrier.

4.3.2 Injection Locking Characterization

The locking range of the oscillator should be a function of the injected power as shown in 4.3. By tuning the natural frequency of each oscillator to 8 GHz, the external reference frequency was swept to determine the locking range of the oscil-
Figure 4.21: Free-running frequency versus tuning voltage.

Figure 4.22: Single-ended output spectrum of each channel.
Table 4.1: Locking range of the coupled oscillator versus injection power.

<table>
<thead>
<tr>
<th>$P_{\text{inj}}$</th>
<th>$f_{o,\text{min}}$</th>
<th>$f_{o,\text{max}}$</th>
<th>Locking Range</th>
</tr>
</thead>
<tbody>
<tr>
<td>-15dBm</td>
<td>7.957GHz</td>
<td>8.047GHz</td>
<td>90MHz</td>
</tr>
<tr>
<td>-5dBm</td>
<td>7.860GHz</td>
<td>8.160GHz</td>
<td>300MHz</td>
</tr>
<tr>
<td>-2dBm</td>
<td>7.743GHz</td>
<td>8.223GHz</td>
<td>480MHz</td>
</tr>
<tr>
<td>0dBm</td>
<td>7.667GHz</td>
<td>8.277GHz</td>
<td>610MHz</td>
</tr>
</tbody>
</table>

lator. Over the locking range, the natural frequency tracks the injected frequency. The locking range should be large enough to track the amplitude variations and therefore an injected power is chosen based on the desired locking range.

4.3.3 Static Outphasing Characterization

The difference of the phase between the two slave oscillators is measured using a sampling oscilloscope. As the differential tuning signal is applied on the oscillators, the phase difference is recorded for a fixed injected power of -4 dBm at different injected frequencies. The measurement shows that the phase shift of 180 degrees necessary for outphasing can be achieved for frequencies from 7.5 GHz to 9 GHz. Additionally, the outphasing angle is demonstrated to be approximately linear over the amplitude range as predicted from (4.6). Furthermore, the measurement can be corroborated against circuit level simulations in Fig. 4.13 that demonstrated that a 180 degree phase shift was reached for a detuning voltage of 230 mV.

Furthermore, the outphasing angle can be measured against a change in the injected frequency for a fixed amplitude. In Fig. 4.24, the phase angle changes from 38 degrees to 50 degrees as the frequency changes from 7.85 to 8.15 GHz. This variation is not unexpected since the change in the $Q$ of the oscillator resonator changes across frequency causing variations in the locking range.

The outphasing signals are power combined and measured simultaneously in the oscilloscope and the spectrum analyzer under different static outphasing conditions in Fig. 4.25. The maximum power is 4.17 dBm when the two signals
Figure 4.23: Phase of the coupled oscillator versus detuning voltage.

Figure 4.24: Phase of the coupled oscillator versus injection frequency.
are in phase and reduces to -25.32 dBm when the signals are completely out of phase. The incomplete cancellation of the signals arises from slight amplitude variations which occur in the two outphasing channels.

Figure 4.25: Output power from the combined outphasing.

The measured power combined outphasing signals are plotted in 4.26 and illustrate excellent agreement with the predicted power variation from 4.7. In this plot the 2 dB measured loss in the cables, connectors and power combiner is included. Also, since the single-ended power is measured, 3 dB is added for single ended to differential conversion.

4.3.4 Dynamic Outphasing Characterization

The dynamic characterization is also a relevant investigation for the use of the outphasing modulator with modulated signals. To investigate this topic, we
explore large perturbations in the coupled oscillator circuit to verify that the circuit remains stable in response to a step change in the amplitude as well as to verify the time constant of the step change. In Fig. 4.27, the step response from maximum to minimum output power is plotted on a time scale. The tuning voltage is stepped periodically between the amplitude corresponding to the maximum and minimum power. Notably, the phase shift follows the step response and does not show any indication of ringing or loss of lock. Additionally, the transition from maximum to minimum and minimum to maximum power indicates a 14 ns rise time for a 0 to 100% change in the power. A traditional 20%-80% variation can also be measured from Fig. 4.27 and indicates a rise time of 2 ns. This corresponds to a bandwidth of 200 MHz and agrees with the predicted locking range of the oscillators.

The harmonic distortion of the power combined outphasing signals was also measured. In Fig. 4.28, the contributions of HD2 and HD3 are measured as a function of the signal swing. The sine wave amplitudes are generated as discussed in Fig. 4.15. As the amplitude is swept, the DC offset is adjusted to keep the maximum power constant. As predicted the contribution of HD3 increases with larger amplitude while the contribution of HD2 decreases. Measurements of the HD2 and HD3 are compared to predictions based on the ideal sine wave modulation and demonstrate excellent agreement for both HD2 and HD3.

Finally, we investigated the HD2 and HD3 as a function of modulation fre-
Figure 4.27: Step function of the outphasing modulator.

Figure 4.28: Measured and calculated HD2 and HD3 versus amplitude.
quency for a full scale signal. Over the scan range allow by our frequency synthe-
sizer, the harmonic distortion contributions were constant. This corroborates the
large signal step response prediction that the locking bandwidth is greater than
200 MHz. Note that this bandwidth exceeds most commercial cellular channel
bandwidths in use today.

Figure 4.29: Measured HD2 and HD3 versus frequency for sine-wave detuning.

4.4 Conclusion

In this chapter, the use of coupled oscillators was demonstrated for the first
time as a viable way to produce outphasing signals. Injection locked oscillators
were shown to offer a low-power method to produce the amplitude to phase varia-
tion required from ideal outphasing modulators. An analysis of the injection locked
behavior of oscillators illustrated that a master-slave scheme with frequency dou-
bler produces an adequate phase shifting range to allow for 180 degree phase shift
between the oscillators. The proposed unilateral injection locked outphasing mod-
ulator was demonstrated with a 45-nm CMOS SOI process and measurements ver-
ified the static outphasing characteristics as well as the dynamic ability to change
the step response and the harmonic distortion of the power combined outphasing
signals.
Acknowledgment

Some of the blocks that are used in this modulator are adopted from [4] and some parts of this chapter are a reprint of the [103].
Chapter 5

Conclusions

This dissertation presents the analysis, design and measurement results in the area of microwave-wave integrated circuits for wireless communication. First, a 10-bit, 300-MS/s current-steering power DAC is demonstrated in 45-nm CMOS SOI and generates a 6-$V_{pp}$ differential output swing into a 100-Ω differential load. A stacked-FET current buffer is used to produce the high voltage swing and avoid transistor breakdown. Using a Volterra series analysis, the linearity of the stacked-FET buffer is described to present fundamental trade-offs in the number of stacked stages and HD3. The results demonstrate a 3-stage stacked-FET current buffer to provide sufficient HD3 for 10-b operation. Additionally, the local negative feedback is used to increase the output impedance of the DAC current cells.

Second, a 10-GHz outphasing modulator with more than 60 dBc dynamic range and capable of supporting 100-MHz LTE-Advanced carrier aggregation and 1.1-Gbit/s 256-QAM is implemented in 45-nm CMOS SOI. Analysis shows that to achieve 60 dB dynamic range as well as performing calibration, a 10-bit DAC is required. Therefore, four 10-bit power DACs are integrated on-chip to convert the baseband I and Q digital data to analog current swing. Quadrature double-balanced switching mode mixers upconvert this current signals to 10 GHz, and the modulated microwave current signals flow into the stacked-FET buffers which protect the mixers and DACs from breakdown. Each channel of this outphasing modulator delivers 20 dBm power which is sufficient to drive high-power off-chip PAs without need for any pre-amplification.
Finally, a new technique to implement polar modulator is proposed which is based on using coupled-oscillator. Three oscillators are coupled to implement the amplitude to phase modulation. Frequency doubler relaxes the requirements for the coupled-oscillators. To the best of author’s knowledge, this work is the first demonstration of polar modulator based on coupled oscillators.
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