High Power and High Efficiency Doherty Power Amplifier Design at 8GHz for Drone Application

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UNIVERSITY OF CALIFORNIA, IRVINE

High Power and High Efficiency Doherty Power Amplifier Design at 8GHz for Drone Application

THESIS

submitted in partial satisfaction of the requirements for the degree of

MASTER OF SCIENCE

in Electrical Engineering

by

Anupama Bhat

Thesis Committee
Professor Payam Heydari, Chair
Professor Ondal Boyraz
Professor Ender Ayanoglu

2016
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I would like to thank Cree Inc for providing the GaN transistors for this design.

I would like to thank my family and friends who have been supportive with me during this entire journey.
LIST OF SYMBOLS

DPA- Doherty Power Amplifier

PA- Power Amplifier

PAE – Power Added Efficiency

BOM – Bill Of Materials

Pout- Output Power of PA

GaN – Galium Nitride

GaAs- Galium Arsanide

IP – Input Network
ABSTRACT OF THE THESIS

High power and High Efficiency Doherty Power Amplifier Design
at 8GHz for Drone Application

By
Anupama Bhat
Master of Science
in Electrical Engineering
University of California, Irvine, 2016
Professor Payam Heydari, Chair

New generation Drone transceiver systems require high linearity and high efficiency power amplifiers. Consumers need more transmitter range, hence more output power from a Power Amplifier. Doherty Power amplifier has been chosen for this application as it provides both high linearity and high efficiency. In this thesis DPA is designed for greater than 4W output power at 8GHz frequency, to be used as Phased array elements so as to provide a power combined output power of 40W for long range Drone transmission. The range of the Drone can be increased significantly with this approach.

A high power and high efficiency, linear Doherty Power Amplifier is designed at 8GHz X band frequency using Cree’s 0.25um Discrete GaN HEMT DFN packaged power amplifiers. An output power of 38dBm is to be achieved and a gain of 12dB.

The Doherty PA is housed on a Roger 4350B PCB. 50V supply voltages are used. The DC current is 40mA per PA. The target drain efficiency of 60% to be achieved. The PA was fabricated and performance issues has been discussed.
CHAPTER 1

1.1 INTRODUCTION

Project motivation and objectives:

The choice of the type of Power Amplifier is crucial for drone application in deciding the linearity, output power and efficiency specifications to meet our project objective. High power and linearity with good efficiency is the need for Drones.

I chose Doherty Power Amplifier Design for this project due to its inherently high linearity and efficiency it can provide for the specified output power compared to other types of Power Amplifiers. COFDM Modulation is used for Drone Application.

The type of device chosen was GaN HEMT discrete devices provided by Cree. For high range of output power >1W III-V devices have been preferred. For this project we aim for output power of greater than 4W.
1.2 DOHERTY POWER AMPLIFIER OPERATION:

The Doherty Power Amplifier comprises of a Main Power Amplifier and a Peaking Power Amplifier.

Class B Power Amplifier was used for the main PA and a Class C for the Peaking Power Amplifier.

For GaN HEMT process the bias chosen for the class B is -2.95V. The classical Class B has its harmonics shorted, however at 8GHz frequency adding additional elements to short harmonics does not help. For the Class C power amplifier, the bias chosen was -4V.
1.3 DYNAMIC LOADLINE MODULATION:

Dynamic Load Modulation or Active Load Pulling is used in Doherty PA to achieve high power and linearity. At low power - only Main Amp is on operates into high RL (good efficiency). When Main Amp begins to saturate, peaking amp turns on (class C bias). Changes load seen by Main Amp to keep it out of hard saturation.

![Diagram of dynamic load line]

**Figure 2 : Dynamic Load Line**

The dynamic loadline can be used to determine low/high power operation.
Figure 3: Efficiency vs Pout

1.4 COMPARISON BETWEEN CMOS, GaAs and GaN DEVICES:

<table>
<thead>
<tr>
<th>Type of Device</th>
<th>CMOS</th>
<th>GaAs</th>
<th>GaN HEMT on SiC</th>
</tr>
</thead>
<tbody>
<tr>
<td>High Power Application</td>
<td>Not good</td>
<td>Good</td>
<td>Very Good</td>
</tr>
<tr>
<td>&gt;2 Watts output</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Operating Voltage</td>
<td>Upto 5V</td>
<td>5-20V</td>
<td>28-50V</td>
</tr>
<tr>
<td>Breakdown voltage</td>
<td>Very low</td>
<td>20-40V</td>
<td>100V &gt;</td>
</tr>
<tr>
<td>Energy Gap (eV)</td>
<td>1.11</td>
<td>1.43</td>
<td>3.4</td>
</tr>
<tr>
<td>Breakdown E-field (V/cm)</td>
<td>6x10^5</td>
<td>6.5x10^5</td>
<td>3.5x10^6</td>
</tr>
<tr>
<td>Saturation Velocity (cm/s)</td>
<td>1.0x10^7</td>
<td>2x10^7</td>
<td>2.5x 10^7</td>
</tr>
<tr>
<td>Electron Mobility (sq cm/V-s)</td>
<td>1350</td>
<td>6000</td>
<td>1600</td>
</tr>
<tr>
<td>Thermal Conductivity (W/cm-K)</td>
<td>1.5</td>
<td>0.46</td>
<td>3.5</td>
</tr>
<tr>
<td>Maximum Temperature (deg C)</td>
<td>300</td>
<td>300</td>
<td>700</td>
</tr>
<tr>
<td>Cost</td>
<td>Cheap</td>
<td>Expensive</td>
<td>More Expensive</td>
</tr>
</tbody>
</table>

Table 1: CMOS, GaAs, GaAN Device Comparison

GaN HEMT on SiC has excellent thermal performance, higher breakdown voltage.
1.5 ADVANTAGES OF GaN

This excellent performance is attributed to the following advantages it has:

1. The room temperature energy gap of 3.4 eV enables GaN devices to support internal electric fields about five times higher than Si or GaAs, which means GaN has a higher breakdown voltage, a desirable attribute of power devices.

2. As a member of HEMT family, the GaN device also inherits the feature of HEMT—high electron mobility. In the RF/Microwave domain, high electron speeds are required to minimize internal device delays.

3. Benefiting from the excellent thermal conductivity of its SiC substrate, the GaN HEMT is very suitable for high power devices with reduced cooling requirements.
1.6 DESIGN CONSIDERATIONS;

From the different Discrete GaN PA provided Figure of Merit (FOM) was determined based on the maximum drain efficiency for the given frequency, gain and output power

Choice of GaN Device and FOM:

The FOM is calculated as the frequency into the Power Added Efficiency.

Discrete PA pose limitation on their performance and hence it is important to determine the maximum possible performance achievable from the device and the frequency of operation for this.

The various X band Frequency devices available from Cree were:

CGH40010
CGH55015F2
CGH60015D
CGH60008D
CGHV1F006S

For each device the FOM was calculated and CGHV1F006S was the one providing the best FOM for the required specifications.

Table 2: FOM calculation

<table>
<thead>
<tr>
<th>CGHV1F006S</th>
<th>VDD</th>
<th>VSWING-VMAX-VMIN</th>
<th>VMAX</th>
<th>VMAX+VMIN</th>
<th>CLASS A EFF</th>
<th>I_MAX</th>
<th>BV</th>
<th>VKNEE</th>
<th>POUTMAX</th>
<th>POUT</th>
<th>CLASS B EFF</th>
<th>PIN(dBm)</th>
<th>POUT(dBm)</th>
<th>GAIN</th>
<th>FOM</th>
<th>FREQ</th>
<th>I_MAX</th>
</tr>
</thead>
<tbody>
<tr>
<td>6W device</td>
<td>40</td>
<td>72</td>
<td>76</td>
<td>80</td>
<td>45</td>
<td>0.63</td>
<td>100</td>
<td>7.56</td>
<td>5.67</td>
<td>7.56</td>
<td>61.18469478</td>
<td>37.53583</td>
<td>12.53583</td>
<td>102.9</td>
<td>8</td>
<td>0.127</td>
<td></td>
</tr>
</tbody>
</table>
1.7 ANALYSIS OF 2 WAY DOHERTY PA STRUCTURE

This shows the analysis of a Doherty Power Amplifier.
CHAPTER 2

2.1 DYNAMIC LOADLINE ANALYSIS FOR GaN PA

Below are the results obtained for the ClassB/Depp class AB PA

![Dynamic Loadline Analysis of GaN PA](image)

Figure 4: Dynamic Loadline Analysis of GaN PA
2.2 LOADPULL SIMULATION

Preliminary Load pull simulation helps determine the optimum load for power added efficiency.

Schematic Setup:

Figure 5: Loadpull Schematic Setup
PAE Contours from Loadpull:

Figure 6: PAE Contours for specified output power

A load of 12 ohms was chosen for this design based on Loadpull simulations.

At high frequency the load tends to get smaller than 50 ohms.
2.3 SCHEMATIC OF THE CLASS AB DESIGN:

The main PA is a deep class AB power amplifier.

It is biased at -2.95V.

Figure 7: Schematic of deep Class AB PA

The efficiency obtained from this was about 55%

2.4 SCHEMATIC OF THE CLASS C DESIGN:

The Peaking Power Amplifier is a Class C Power amplifier biased at -4V. The efficiency obtained was 57%

Figure 8: Schematic Of Class C PA
2.5 SCHEMATIC OF THE COMBINED DPA:

![Combined DPA Schematic](image)

Uneven power splitter with the ratio 1:4 gives optimum results with the peaking amplifier.

A Z transformation power splitter is used at the input side. The power splitter used is an asymmetrical power splitter with 1:4 ratio. This provides optimum performance.

The output side quarter wave transformers are used as power combiners.
2.6 SUSTRATE MODELING OF GROUND AND SIGNAL LAYERS

Microstrip Design for Roger 4350B. This PCB material has good thermal coefficient for high power and high frequency application. 2oz copper thickness was chosen for better performance compared to thinner microstrip, however during fabrication this turned out to be more expensive.

Schematic of the DPA with microstrip modeled along with T junctions and taper bends of layout

Dcaps of 43pF have been added near Voltage sources

Radial stubs are used at the input side for more broadband input matching.
2.7 STABILITY CIRCUIT:

![Stability Circuit Diagram]

Figure 12: Stability Circuit with RC series in parallel with IP network
RC series stability circuit added at the input of the DPA.
2.8 MODELING OF PROBE INDUCTANCES:

Extra transmission lines have been added to model the probe inductance effects.

Figure 13: Dcap with long transmission line inductance modeled
CHAPTER 3

3.1 SIMULATION RESULTS

Power Gain of the DPA using Harmonic Balance

Figure 14: Power Gain of The DPA
3.2 POWER ADDED EFFICIENCY AT FUNDAMENTAL FREQUENCY USING HARMONIC BALANCE

\[ \text{PAE} = \frac{P_{\text{out}} - P_{\text{in}}}{P_{\text{dc}}} \]

Figure 15: PAE of the DPA
3.3 DRAIN EFFICIENCY AT FUNDAMENTAL FREQUENCY

Equation: $\text{Drain Eff} = \frac{(P_{fc1})}{(Pt1)} \times 100$

Figure 16: Drain Efficiency of DPA

By decreasing the supply voltage, at backoff the efficiency is slightly more.
3.4 **LAYOUT FEM SIMULATION:**

The layout needs to be FEM simulated to be able to see the effects of the bends of the microstrips. The pads of the capacitors, resistors needs to be included in the FEM simulations as it changes the impedance.

The sp file generated from the FEM simulation can be used in the schematic to help improve the performance degradations caused after layout.

3.5 **EM COSIMULATION**

EM Cosimulations helps determine the realistic effects of any bends, coupling from adjacent traces post layout. Tuning and optimization techniques were used to improve the design.

![Figure 17: EM Cosimulation Setup](image)

3.6 **HEAT SINK**

A good heat sink is required with fins under the substrate.

Aluminium housing can be used or adhesive method can be used to attach the heat sink.
CHAPTER 4

4.1 FOUR LAYER PCB DESIGN LAYOUT WITH THROUGH HOLE VIAS

Substrate Modeling of 4 Layer PCB:

Figure 18: Four Layer PCB Substrate Setup

Pc1 is the top signal layer
Ref_gnd is the 2nd layer ground plane
Pc2 is the power plane
Pc3 is the gnd plane
Pcb_via is the through hole via. It is best for high power applications to use through hole vias instead of blind or microvias.

The layout needs to have appropriate holes so as to be connected to the right plane.
4.2 COMPLETED 4 LAYER PCB LAYOUT

Figure 19: Four Layer PCB Layout
4.3 FABRICATED CHIP

Figure 20: Fabricated Chip
4.4 MEASUREMENT RESULTS AND FAILURE ANALYSIS:

The measurement could not be completed due to assembly short due to the very small dimensions of the components chosen (microscope required for hand soldering) and made it hard.

The Roger 4350B material chosen was with 2 oz (70um) Electrodeposited Copper Foil – ED. The surface roughness of the ED copper causes loss at high frequency, high power application. One way to improve this would be to use a smoother Copper called Rolled Copper which is much more favorable for high frequency, high power application.

Modeling of the SMA connectors as they have big footprint, this needs to be included in the EM simulations of the layout.

4.5 CONCLUSION AND FUTURE WORK:

The discrete PA poses limitation on the frequency for the best possible performance. Careful inspection is required while choosing the components and extra space for any solder overflow to avoid any potential shorts.
##CHAPTER 5

###5.1 Bill of Materials (BOM) for PCB Fabrication and Assembly

<table>
<thead>
<tr>
<th>Item Number</th>
<th>Quantity</th>
<th>Description</th>
<th>Part Reference</th>
<th>Value</th>
<th>PCB Footprint</th>
<th>CIS : Manufacturer</th>
<th>CIS Manufacturer PN</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>2</td>
<td>Thick Film Resistors - SMD 1ohms 2W 1% TCR200 RES</td>
<td>R1,R3</td>
<td>1 ohm</td>
<td>Bourns</td>
<td>CRS2512-FW-1R00ELF</td>
<td></td>
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<tr>
<td>2</td>
<td>3</td>
<td>Multilayer Ceramic Capacitors MLCC - SMD/SM T 0603 43pF 50volts C0G 5%</td>
<td>C16,C17,C18</td>
<td>43pF</td>
<td>Murata</td>
<td>GRM1885C1H430JA01D</td>
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<td>3</td>
<td>1</td>
<td>Multilayer Ceramic Capacitors MLCC - SMD/SM T 50V .70pF 30ppm</td>
<td>C2</td>
<td>0.7pF</td>
<td>AVX</td>
<td>02015J0R7PBSTR500</td>
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<tr>
<td>4</td>
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<td>Multilayer Ceramic Capacitors MLCC - SMD/SM T 0402 7.2pF 50volts C0G +/- 0.1pF</td>
<td>C15</td>
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<td>Murata</td>
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<td>7</td>
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<td>Thin Film Resistors - SMD</td>
<td>2.8ohms</td>
<td>Patent051L2R80FG</td>
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<tr>
<td></td>
<td></td>
<td>0.2 watt</td>
<td>Vishay</td>
<td>T1</td>
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<tr>
<td></td>
<td></td>
<td>2% 200ppm</td>
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<td>8</td>
<td>1</td>
<td>Multilayer Ceramic Capacitors MLCC - SMD</td>
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<td>GJM1555C1H2R5W</td>
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<tr>
<td></td>
<td></td>
<td>T0201</td>
<td>50volts</td>
<td>B01D</td>
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<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>C0G +/- 0.1pF</td>
<td></td>
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<td></td>
<td></td>
</tr>
</tbody>
</table>

**RFin, RFout**

SMA connectors

**VDD, Vbias**

Banana plugs

**Heat sink below**

[2] Peter Asbeck UCSD Power Amplifier Lecture Notes


http://www.wolfspeed.com/cghv1f006s