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Integration of III-V Materials with Silicon for Optoelectronic Integrated Circuit Applications

A dissertation submitted in partial satisfaction of the requirements for the degree of Doctor of Philosophy in Electrical Engineering (Applied Physics) by Peng Chen

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2008
The dissertation of Peng Chen is approved, and it is acceptable in quality and form for publication on microfilm:

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Chair

University of California, San Diego

2008
To my parents
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<tr>
<td>OEIC</td>
<td>OptoElectronic Integrated Circuit</td>
</tr>
<tr>
<td>AFM</td>
<td>Atomic Force Microscopy</td>
</tr>
<tr>
<td>TEM</td>
<td>Transmission Electron Microscopy</td>
</tr>
<tr>
<td>SEM</td>
<td>Scanning Electron Microscope</td>
</tr>
<tr>
<td>RBS</td>
<td>Rutherford Backscattering Spectrometry</td>
</tr>
<tr>
<td>ERD</td>
<td>Elastic Recoil Detection</td>
</tr>
<tr>
<td>XRD</td>
<td>X-Ray Diffraction</td>
</tr>
<tr>
<td>FTIR</td>
<td>Fourier transmission infrared</td>
</tr>
<tr>
<td>FWHM</td>
<td>Full Width at Half Maximum</td>
</tr>
<tr>
<td>CMP</td>
<td>Chemical Mechanical Polishing</td>
</tr>
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The dissertation author is the first author of these papers.

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Journal Publications


**Conference Presentations**


Integration of III-V materials with Silicon for Optoelectronic Integrated Circuit
Applications

by

Peng Chen
Doctor of Philosophy in Electrical Engineering (Applied Physics)
University of California, San Diego, 2008
Professor Silvanus S. Lau, Chair

Integration of III-V materials with Si substrates has been studied extensively in recent years since it has a wide range of applications on optoelectronic integrated circuits (OEIC). It enables the combinations of III-V based optoelectronic devices with Si-based microelectronic devices and circuits.

The conventional approach for III-V integration with Si is based on wafer bonding and etch-back. Although it provides III-V materials transferred on Si with relatively high crystalline quality, the etch-back process in this approach etches off the initial III-V growth substrate thus it gives low yield and increases the cost. Recently, another III-V layer transfer approach using the ion-cut (smart-cut®) process has been demonstrated, based on hydrogen ion implantation and wafer bonding. This approach
has the advantage of saving the initial III-V substrate for reuse, but the transferred structure usually suffers from the hydrogen implantation induced damage.

This dissertation demonstrates a new approach that combines ion-cut and selective chemical etch for InP-based III-V layer transfer. This layer transfer scheme takes advantage of conventional ion-cutting process by conserving III-V substrates for reuse, and simultaneously improving the transferred layer quality and surface condition without using chemical and mechanical polishing. The effects of hydrogen ion implantation conditions (temperature, dose rate, and energy) on III-V ion-cut process have been investigated and the physical mechanism behind these effects was examined. Based on these findings, the hydrogen implantation conditions were optimized in our study that led to successful III-V layer transfers.

Based on our layer transfer scheme, two approaches have been explored for integrating an III-V based device on Si. One way is to transfer an InP layer onto Si and use this transferred structure as a growth template. Instead of growing complicated III-V device structures which are out of the growth capacity in our laboratory, we focused on the fundamental issues with the transferred structure that must be solved for the growth template purpose. Particularly there is a bubble issue that always shows up when the transferred structures are heated up in the growth chamber. We studied the origin of these bubbles and implemented a simple and effective approach that can constantly solve the bubble problem. Another way is to grow an III-V device on III-V substrate and transfer the whole device structure onto Si. InP/InGaAs/InP $p-i-n$ photodiodes were transferred onto Si substrate and the effects of the hydrogen implantation on the device performance have been discussed.
Chapter 1

Introduction

1.1 Integration of III-V semiconductor materials with Silicon

Integration of III-V materials with Si substrates has been studied extensively in recent years, due to the increasing interests in combining III-V based optoelectronic devices with Si-based microelectronic circuits [1-8]. Among various applications, there are two major applications for the III-V to Si integration.

The first application of is to prepare III-V-on-Si structures that can be used as templates for subsequent epitaxial growth. Wafers of III-V materials are generally mechanically fragile, expensive and not commercially available in large size. For instance, currently the largest InP wafer widely available on the market is 4-inch in diameter, while the growth technology for 12-inch Si wafers is mature. Compared with III-Vs, Si wafer, as the most common substrate used in semiconductor industry, has superior mechanical strength, high thermal conductivity and relatively low cost [9]. Therefore, it is ideal to use Si as a robust and cheap handle substrate to achieve large-scale III-V growth. However, it is rather difficult for epitaxial growth of III-V layers directly on Si due to the considerable lattice mismatch between III-V material and Si. For example, InP and Si have a lattice mismatch of \(~8\%\) that leads to significant dislocations and defects during epitaxial growth beyond the critical thickness [10]. If a high-quality III-V thin layer could be transferred onto a Si substrate by wafer bonding, this III-V layer becomes a suitable template for further high-crystalline quality epitaxial
growth of III-V layers on Si substrate [11-13]. This leads to the first important application of III-V integration with Si.

The second important application of III-V integration with Si is to enable optoelectronic integrated circuits (OEIC), including optical interconnections between Si chips, optical transmitters/receivers, optical switching chips [5-7, 14-16]. For example, InP-based III-V materials are attractive candidates for fabricating lasers and detectors for telecommunication applications on Si chips, since their optical spectra can cover the low dispersion and minimum loss wavelength for optical fibers communications at 1.3 μm and 1.5 μm. The integration of III-V materials with Si also encourages a wide range of novel device designs that take advantages of both III-V materials and Si substrates. An optically controlled MOSFET has been demonstrated by Shimomura et al. [14]. More recently Intel and UC Santa Barbara developed a hybrid silicon laser in which an III-V laser structure is integrated with a Si waveguide [15, 16]. As the scaling of conventional CMOS technology approaches fundamental quantum limits, III-V integration with Si can provide an effective and practical solution for high-speed and high density circuit applications.

1.2 Semiconductor Wafer bonding

In this dissertation, semiconductor wafer bonding is used for integration of InP-based III-V materials with Si substrates. A brief introduction to wafer bonding is presented here, with a focus on the type of bonding method we used in this study.

In general, wafer bonding technology refers to the process by which two polished, flat, and clean wafers adhere to each other by forming bonds. In the 17th century,
bonding was already observed by Sir Isaac Newton (1642-1727), as testified by his famous central black spot surrounded by 'Newton rings,' established between an optical contact of a flat and a convex optical surface. The phenomenon that two polished pieces can bond to each other was studied by Rayleigh in 1936 for quartz glass [17]. In the 1960's, Nakamura et. al at RCA proposed the wafer bonding concept by a series of patents [18]. However, the poor conditions of wafer surface at that time prevented any commercial applications. This technology was then re-evaluated in the 1980's. In 1985 the room temperature adhesion phenomenon coupled with appropriate annealing steps was utilized for silicon wafers to replace the epitaxial growth of thick silicon wafers [19], and to fabricate silicon-on-insulator (SOI) structures [20]. The generic nature of wafer bonding was theoretically recognized in the early 90’s [21]. In 1995, Bruel et. al developed an novel procedure combining wafer bonding technology and hydrogen implantation induced layer delamination to fabricate SOI [22, 23]. Due to many advantages of the SOI structure over conventional bulk silicon substrates in device performance, SOI market increased rapidly in recent years thus the wafer bonding technology also developed significantly. In 1999, the first reference book on wafer bonding technology was published with a relatively comprehensive understanding of wafer bonding at the time [24].

In general, wafer bonding relies on attractive forces between two sufficiently smooth and clean surfaces. The most important surface interaction in wafer bonding is the van der Waals forces, which originate from atomic and molecular electric dipoles [25]. Besides the van der Waals forces, there are also some other important forces such as the
electrostatic (Coulombic) forces, which will be involved if the surfaces become macroscopically charged by either adsorbing or desorbing electrons or ions [26].

Semiconductor wafer bonding can be roughly placed in two categories. The first type is direct bonding in which bonding is performed without interlayer in between. It has the merit of relatively good thermal and electrical conductance through the bonding interface. It also has strict requirements on the flatness and cleanliness for both surfaces. The second type is indirect bonding which is performed using an interlayer that can be dielectric, metal, or polymer. The requirements on the flatness and cleanliness are not as restrictive as for the direct bonding. However, the use of interlayer may change the electrical resistance and thermal conductance of the bonded structure. Indirect bonding is used in our study where an InP sample is bonded to a Si sample coated with a thin SiO₂ layer. The cleaning and plasma activation processes on the InP sample also generate a thin layer of oxide on the InP piece. Therefore in our case it is essentially an oxide-to-oxide bonding. A brief review of SiO₂-to-SiO₂ hydrophilic bonding is presented as below.

It is well known that silicon wafers usually have a 1-2 nm thick native oxide layer, especially after the usual cleaning steps in highly oxidizing solutions [27]. This native oxide layer is terminated by Si-OH groups, so-called silanol groups, which cause wafer surfaces to be hydrophilic. Hydrophilic surfaces are usually covered with water molecules which interact with the surface silanol groups through the formation of hydrogen bonds. The number of hydrogen bonds depends on the humidity and temperature to which the wafers are exposed [28]. The bonding at room temperature is
caused by hydrogen bonds between chemisorbed water molecules located on opposing wafer surfaces (as shown in Fig. 1.1).

\[
\gamma = \frac{1}{2} (2d_{OH}E_{bi} + d_{OHH}E_{hH})
\]

where \(d_{OH}\), \(d_{OHH}\) are the surface density of silanol groups, respectively. \(E_{bi}\), \(E_{hH}\) are the hydrogen bond energy of the isolated and the associated silanol groups, respectively.

However, the energy of hydrogen bonds depends on the distance and orientation of the species involved. An exact calculation of the bonding energy is therefore difficult. If each OH-group is covered by one water molecule and each water molecule forms one hydrogen bond to an opposing water molecule, a bonding energy of 80-160 mJ/m² should be obtained. Figures 1.2 and 1.3 are the typical infrared and TEM images on the bonded hydrophilic Si wafers, respectively.

**Figure 1.1:** Schematic drawing of the bonding of two hydrophilic silicon surfaces at room temperature. (After Ref [29])

Assuming all surface silanol groups adsorb water molecules and all interface water molecules are connected by hydrogen bonds across two surfaces, the specific bonding strength (also called surface energy) \(\gamma\) of the room temperature bonded hydrophilic Si/Si pair may be estimated as follows [24]:
Figure 1.2: Typical infrared spectrum of two hydrophilic Si (111) wafers, bonded at room temperature. Schematic representations of the vibrational modes associated with each absorbance band are shown, for reference. (after Ref [30])

Figure 1.3: Cross-sectional high resolution transmission electron micrograph of the interface of a bonded hydrophilic silicon wafer pair. The amorphous interlayer represents the combined native silicon dioxide layers of both wafers (after Ref [29])

The intermediate-layer bonding is also widely used when direct bonding is almost impossible. The intermediate layer could be a thin oxide or nitride layer like a SiO₂ layer as used in our study. It could also be various kinds of glue layers like photo resists and wax. The intermediate layer usually facilitates the bonding and sometimes itself plays an important function in the bonded structure. For instance, the SiO₂ layer used in our study can provide the advantage of electrical isolation.

A typically direct wafer bonding process consists of three basic steps: surface preparation, contacting, and annealing. The starting wafers must be smooth and flat.
Some studies indicated that the wafers should have a roughness of no greater than 1nm and a bow of less than 5 μm for wafer bonding [31, 32]. Different chemical solutions have been developed to clean different surfaces. Following the preparation, the wafers are contacted in a clean environment by gently pressing the two surfaces together at one central point. The surfaces come into contact at this point and are bound by a surface attraction of the two hydrated surfaces. The contacting process is critical to prevent trapping of particulate or air between the surfaces. The final step is an annealing of the contacted pair at high temperatures to increases the bonding strength.

1.3 Two approaches for III-V layer transfer based on wafer bonding

As discussed above, wafer bonding enables integration of an III-V wafer (normally ~ 350 μm or thicker) with a Si wafer. However, in most cases only a thin layer of III-V (usually a few hundred nms to a few μms) is needed for subsequent growth or for device fabrication. Therefore it is necessary to thin the bonded III-V piece down to a suitable thickness after wafer bonding. Based on the methods used for the thinning, there are two approaches for thin III-V layer transfer.

1.3.1 Wafer bonding and etch back

Wafer bonding and etch-back process is one of the two generally used methods for III-V layer transfer. As an example, Fig.1.4 shows an illustration of the process flow for transferring a thin InP layer onto Si with an oxide in between. This process begins with a heterostructure grown by CVD or MBE, placing an epitaxial InP layer on top of an etch-stop layer of InGaAs. The heterostructure is flipped over and bonded to a Si piece,
coated with a thin oxide. After subsequent thermal annealing to increase the bonding strength, the bonded structure is then chemically etched from the backside of the InP wafer until the etching reaches the InGaAs layer. The InGaAs layer can be etched away using another etchant that does not attack InP. Finally an Epi InP layer is transferred onto Si.

**Figure 1.4:** Schematic of wafer bonding and etch back approach for a InP layer transfer.

This approach has been widely used to transfer various semiconductor layers onto different substrates. The advantage is the relatively high crystalline quality of the transferred Epi layers. However, this process requires the entire substrate to be etched and thus it has relatively low yield and high cost, especially in the case of III-V layer transfer with expensive III-V materials.

1.3.2 Ion-cut (or Smart Cut®)

This layer transfer process is based on hydrogen ion-implantation and wafer bonding. This innovative approach provides an effective, versatile, and relatively low-cost method of transferring thin surface layers from bulk substrates onto another host substrate [22, 23]. This process is known as ion-cut or Smart Cut®. Smart Cut® is a
trademark of SOITEC Corporation in France. The essence of the Ion-Cut process is to implant the donor wafer with hydrogen or helium atoms at a well defined depth before bonding to a handle wafer. The bonded structure is then annealed at relatively low temperatures (typically ~ 100 °C) to increase the bonding strength and eventually heated to a higher temperature to induce layer exfoliation. As a result, a thin film of donor piece is transferred onto the host piece. Figure 1.5 shows an example of using ion-cut to transfer a thin InP layer onto Si substrate. One of the main advantages of ion-cut process is that the remaining donor piece can be reused, thus lowering the total fabrication cost.

![Figure 1.5: Schematic of ion-cut approach for an InP layer transfer.](image)

Hydrogen plays a crucial role in the ion-cut process. After hydrogen implantation with sufficient dose (typically ~ 5×10^{16} cm^{-2} or higher), a subsequent annealing would induce surface blistering on the implanted piece if it is not bonded to another substrate, as shown in Figure 1.6. Surface blistering study is thus a convenient method to examine the efficiency of hydrogen implantation. In Chapter 2 we used this method to study the effects of hydrogen implantation conditions on the InP ion-cut process.
Figure 1.6: Hydrogen micro-bubble evolution without wafer bonding.

If after an appropriate hydrogen implantation, the implanted sample is bonded to a solid handle piece, the hydrogen micro-bubbles around the projected range of hydrogen would propagate in a direction parallel to the surface and eventually connect to each other, leading to layer exfoliation, as shown Figure 1.7.

Figure 1.7: Hydrogen micro-bubble evolution with wafer bonding.

The ion-cut process has been commercially used to transfer thin Si layers onto insulators to form silicon-on-insulator (SOI) substrates. Recently, it has also been demonstrated for III-V layer transfers [7, 11-13, 24].

There are some disadvantages of ion-cut that prevent it from more wide applications. The surface region of the transferred layer always suffers from the implantation induced damage, which can not be easily recovered by thermal annealing.
Moreover, the as-transferred III-V layer surface is usually rough with a typical root-mean-square (RMS) surface roughness of ~10nm or higher, causing great difficulties for subsequent epitaxial growth or device fabrication. Chapter 3 of this dissertation discusses a new method to address these two issues in ion-cut process.

### 1.4 Scope of this dissertation

The scope of this dissertation is as follows:

Chapter 2 discusses the effects of hydrogen ion implantation conditions (temperature, dose rate, and energy) on III-V ion-cut process. It was found that both the point defects induced by the hydrogen implantation and the in-plane compressive stress were necessary for hydrogen trapping and H-platelet nucleation and growth. An empirical formula based on the Morehead-Crowder model was used to rationalize the implantation condition dependence. A critical implantation temperature ($T_c$) above which hydrogen implantation would not cause surface blistering or layer exfoliation was estimated. Based on these understandings on the effects of hydrogen implantation conditions on ion-cut process, we found the optimized hydrogen implantation conditions in our study that led to successful III-V layer transfer as described in the following chapters.

Chapter 3 describes a new approach that combines ion-cut and selective chemical etch for InP-based III-V layer transfer. This layer transfer scheme takes advantage of the ion-cutting process by conserving III-V substrates for reuse, and simultaneously improving the transferred layer quality and surface condition without using chemical and mechanical polishing.
Chapter 4 discusses the feasibility of using our transferred structure as a growth template. A high-crystalline quality InP layer was transferred onto Si using the method described in chapter 3. The transferred structure is subsequently used as a growth template for epitaxial growth. Instead of growing complicated III-V device structure which is out of the growth capacity in our laboratory, we focused on the fundamental issues with the transferred structure (such as InP/SiO$_2$/Si) that must be solved for any kind of growth template purpose. Particularly there is a bubble issue that always shows up when the transferred structures are heated up in the growth chamber thus significantly degrades the transferred film quality. We studied the origin of these bubbles and implemented a simple and effective approach that can constantly solve the bubble problem. Some preliminary results from our re-growth are also shown to prove the feasibility of using our transferred structure as a growth template.

Chapter 5 presents, for the first time to the best of our knowledge, the transfer of InP/InGaAs/InP $p$-$i$-$n$ photodiodes onto Si substrate based on the ion-cut process and selective etch. The feasibility of using the layer transfer approach described in chapter 3 for an optoelectronic devices transfer onto Si was demonstrated. X-ray diffraction and I-V characteristics were used to study the effects of hydrogen implantation on the performance of the device after transfer.

Chapter 6 presents a summary of this dissertation and future work.
References


The process of Ion-cut (or Smart Cut®) is based on a combination of hydrogen implantation and wafer bonding. The success of the ion-cut process directly depends on the control of hydrogen implantation conditions. For a typical hydrogen ion implantation, there are four important parameters: energy, dose, temperature, and dose rate. It has been found that the ion-cut process for III-Vs strongly depends on hydrogen implantation conditions [1, 2]. As a first step of our investigation of III-V integration to Si by ion-cut, we examined the effects of implantation parameters (the implant temperature in particular) on the ion-cut process, and conducted detailed implantation experiments to ascertain the physical mechanisms behind the process dependence.

2.1 H implantation energy

Implant energy determines the projected range ($R_p$), where the hydrogen concentration is at a maximum. Since the thickness of the transferred layer generally scales with the projected range, the implantation energy is used to control the transferred thickness. In our study, we used 45 keV, 60 keV, 80 keV, 100 keV, and 160 keV for various purposes. Figure 2.1 shows the simulated hydrogen depth distribution at two typical implant energies, 80keV and 160 keV, respectively. The implantation of hydrogen into InP substrate was simulated using the Stopping and Range of Ions in
Matter (SRIM) 2006 computer code [3]. Table 2.1 summaries projected range and longitudinal straggling for different hydrogen implant energies.

Figure 2.1: SRIM2006 simulation of the implanted hydrogen ion distribution in InP at two different energies: (a) 80 keV, (b) 160 keV.
Table 2.1: SRIM2006 simulations of projected range, longitudinal straggling for various hydrogen implant energies.

<table>
<thead>
<tr>
<th>Implant Energy (keV)</th>
<th>Projected Range (Å)</th>
<th>Longitudinal Straggle (Å)</th>
</tr>
</thead>
<tbody>
<tr>
<td>10</td>
<td>1063</td>
<td>361</td>
</tr>
<tr>
<td>25</td>
<td>2310</td>
<td>700</td>
</tr>
<tr>
<td>45</td>
<td>3745</td>
<td>929</td>
</tr>
<tr>
<td>80</td>
<td>6050</td>
<td>1195</td>
</tr>
<tr>
<td>100</td>
<td>7549</td>
<td>1322</td>
</tr>
<tr>
<td>120</td>
<td>8997</td>
<td>1436</td>
</tr>
<tr>
<td>160</td>
<td>12000</td>
<td>1653</td>
</tr>
</tbody>
</table>

**2.2 H implantation dose**

The hydrogen dose is a critical factor that significantly affects the ion-cut process. It should be noted that there is a minimum dose of hydrogen to induce sufficient H-related platelets formation and subsequent coalescence to form microcracks for layer exfoliation. However, if the hydrogen dose is too high, the implanted sample blisters directly after implantation, thus disabling the subsequent wafer bonding or layer transfer process. Therefore, there is only a relatively narrow window for hydrogen dose in the III-V ion-cut process.

Furthermore, for III-V layer transfers, the required hydrogen dose for ion-cutting is a function of implant energy. At 80 keV, \( \sim 6 \times 10^{16} \text{ cm}^{-2} \) is needed for InP ion-cut, while at 160keV with all other implantation parameters the same, \( \sim 8.5 \times 10^{16} \text{ cm}^{-2} \) is the lowest dose to induce successful InP layer transfer in our study. For an effective hydrogen implantation for ion-cutting, the peak concentration of hydrogen at the projected range
needs to reach a critical concentration. Implantation at 160 keV (Fig. 2.4 (b)) has a hydrogen distribution longitudinal straggling of 1653 Å, ~ 13.8% broader than that for the 80 keV implantation (1195 Å). Therefore, to reach the same level of peak hydrogen concentration, higher hydrogen dose is needed for the 160 keV implantation than for the 80 keV implant. This correlates the implant energy to the dose of hydrogen.

2.3 H implantation temperature

2.3.1 Introduction

The temperature windows for H implantations and subsequent thermal treatments to induce surface blistering and/or layer exfoliation appear to be relatively wide for Si substrates, but rather narrow for III-V compounds.

Table 2.2: different implantation temperature windows for various materials as reported in literature.

<table>
<thead>
<tr>
<th>Material</th>
<th>H Implantation Temperature Window (°C)</th>
<th>References</th>
</tr>
</thead>
<tbody>
<tr>
<td>Si</td>
<td>-175-450</td>
<td>[4], and our results</td>
</tr>
<tr>
<td>SiC</td>
<td>50-900</td>
<td>[4]</td>
</tr>
</tbody>
</table>
Table 2.2 summarizes different implantation temperature windows for various materials as reported in literature. In the case of InP, various hydrogen implantation temperature windows have been reported. Tong et al. pointed out a temperature window of 150-250 °C [4], Hayashi et. al. demonstrated that a hydrogen implantation temperature of -20 °C would induce InP surface blistering upon subsequent annealing but a room temperature implantation without controlled cooling prevented any blistering [2]. These discrepancies in the literature could be due to other differences in other implantation parameters and process conditions that were used by different groups. Furthermore, in the -20 °C implantation case, a low temperature annealing at 150 °C followed by a higher temperature 300 °C annealing was found to be more effective to induce surface blistering than annealing directly at a high temperature of 300 °C [2].

It has been reported that the ion-cut process in Si is directly related to the trapping of H by ion implantation induced damage [8-10], and ion-induced stress in enhancing vacancies motion and producing favorable conditions for platelet nucleation in the plane of the stress [11]. However, the relation of hydrogen implantation condition to the resulting damage and strain profiles in the case of III-V ion-cut have not been clarified in the literature. In this study, we examined the effects of implant temperature in relation to the necessary conditions for surface blistering and eventual layer delamination in InP. The results were rationalized in term of an empirical model for damage formation that relates implantation temperature, dose rate and energy.
2.3.2 Experimental details

N-type <100> InP wafers with a resistivity of 0.0022 Ω⋅cm (~ 1.7x10^{18} cm^{-3}) were used in this study. To study the influence of implantation temperature, a set of two samples was implanted with H^{+} at 100 keV with a dose of 5x10^{16} cm^{-2} at a dose rate of 3.13x10^{13} cm^{2}s^{-1} and at two temperatures (room temperature (RT) and 200 °C, respectively). A second set of two samples was implanted with H^{+} at 45 keV with a dose of 4.5x10^{16} cm^{-2} at a dose rate of 8.3x10^{12} cm^{2}s^{-1} and at two temperatures (RT and 200 °C). To pre-engineer extrinsic trapping sites for hydrogen atoms at elevated implantation temperatures, a third set of samples was first implanted with Ne^{+} ions at 250 keV with a dose of 1x10^{14} cm^{-2} at a dose rate of 3.76 x 10^{11} cm^{2}s^{-1} and at room temperature, followed by hydrogen implantation with the same conditions as in set #2. During implantation the samples were attached to a massive metal sample holder with carbon tape. The temperature was monitored by a thermocouple directly connected to the sample holder and placed close to the samples. The implantation at room temperature was done with air cooling of the sample holder and the one at 200 °C was done with a heating element placed inside the holder. The temperature during implantation was carefully maintained to within ± 10 °C from the temperature setting.

Optical microscopy with Nomarski lenses was used to examine bubble formation on the sample surface up to a magnification of 1000 X. Rutherford backscattering spectrometry (RBS) in the channeling mode with a 2.0 MeV $^4$He^{+} beam was utilized to study the H-induced damage profile after different implantations. The detector was placed 167° from the incident beam. The H distribution profiles were examined using elastic recoil detection (ERD) with a 3.0 MeV $^4$He^{+} beam. Double crystal X-ray
diffraction (XRD) in (004) double axis $\omega/2\theta$ scan mode was used to characterize the strain involved in various implantation conditions.

2.3.3 Surface blistering results

To investigate the surface blistering phenomenon, all the hydrogen implanted samples were annealed at 200 °C or higher in a flowing N$_2$ ambient. Surface blistering is an indication of the platelet formation and nucleation of micro-bubbles with internal pressure around the implanted region, a necessary condition for the thermal exfoliation of surface layers. The sample implanted at 100 keV and at RT showed obvious surface blisters with microscopic inspection after annealing at 200 °C for 10 minutes as shown in Fig. 2.2(a), or after annealing at 400 °C for 10 minutes. However, for the sample implanted at 100 keV and at 200 °C, blisters were not observed at a magnification as high as 1000 X after annealing at 200 °C or any other temperatures up to 500 °C for 2 h (Fig. 2.2(b)). The samples implanted at 45 keV also exhibited the same trend that only RT implantation induced subsequent blistering. The samples pre-implanted with Neon in set #3 did not show blistering after subsequent hydrogen implantation at 200 °C. These observations suggest that implantation at RT, but not at 200 °C, should be used for InP ion-cutting, given the implantation energy and dose rate used in this study.
2.3.4 Effect of hydrogen implantation temperature on damage

RBS data shown in figure 2.3 indicate the damage distributions in InP samples at different implantation conditions. For the sample implanted with hydrogen only at 200 °C, a significant damage peak was observed in Fig. 2.3(c) around 1.54 MeV. For the RT implanted sample (Fig. 2.3(b)), a broad damage region was present, extending from the near-surface region to a depth around the projected range (Rₚ) of hydrogen. The RBS data from samples implanted at 100 keV (not shown here) also showed the same trend, i.e., high temperature implantation created a concentrated damage peak while RT implantation showed a lower and broader damage distribution. A similar phenomenon termed “reverse annealing” has been observed in hydrogen implanted Si substrates in which the RBS dechanneling yield increases with the annealing temperature due to defect cluster formation and localized deformation of the lattice [12-15]. Implantations at room temperature generally create point defects such as vacancies, interstitials and complexes.
due to the active interaction of H\(^+\) ions with InP substrate [16]. At elevated implant temperatures, since dynamic annealing occurs, these point defects agglomerate and form defect clusters and/or other localized deformation of lattice which give rise to dechanneling yield [1, 15-17]. The presence of these defect clusters around R\(_p\) is confirmed by cross-section transmission electron microscopy, shown in the Fig. 2.4 (b).

**Figure 2.3:** RBS channeling spectra obtained from InP samples: (a) virgin InP, (b) implanted with 4.5x10\(^{16}\) cm\(^{-2}\) H\(^+\) at 45 keV at RT, (c) implanted with 4.5x10\(^{16}\) cm\(^{-2}\) H\(^+\) at 45 keV at 200 °C, (d) implanted with 1x10\(^{14}\) cm\(^{-2}\) Ne\(^+\) at RT then implanted with 4.5x10\(^{16}\) cm\(^{-2}\) H\(^+\) at 200 °C, (e) implanted with 1x10\(^{14}\) cm\(^{-2}\) Ne\(^+\) at 250 keV at RT then annealed at 200 °C for 1.5 hours, and (f) a random spectrum from virgin InP.
Figure 2.4: Cross-section transmission electron micrograph obtained from InP samples implanted at: (a) room temperature, and (b) 200°C. Bright-field images, with 220 Bragg condition satisfied. Black dots in both images are indium dots due to ion milling during the TEM sample preparations.
Different hydrogen distribution profiles for these two implants are shown in Fig. 2.5, extracted from ERD data [18]. For the RT implanted sample (Fig. 2.5(b)), a hydrogen concentration peak located around the projected range of hydrogen was observed. The concentration peak from sample implanted at 200 °C shown in Fig. 2.5 (c) was closer to the surface and much lower in the integrated hydrogen dose with only ~36% of that from a RT implantation. The implantation at 200 °C created defect clusters which became less effective H trapping sites, thus H atoms can diffuse out toward the surface at elevated temperatures. As a result of much less H trapping, surface blistering was not observed for samples implanted at 200 °C upon subsequent annealing.

![Figure 2.5](image_url)

**Figure 2.5**: Depth profiles of hydrogen concentration extracted from Elastic recoil detection (ERD) spectra from InP samples: (a) virgin InP, (b) implanted with $4.5 \times 10^{16}$ cm$^{-2}$ H$^+$ at 45 keV at RT, (c) implanted with $4.5 \times 10^{16}$ cm$^{-2}$ H$^+$ at 45 keV at 200 °C, (d) implanted with $1 \times 10^{14}$ cm$^{-2}$ Ne$^+$ at RT then implanted with $4.5 \times 10^{16}$ cm$^{-2}$ H$^+$ at 200 °C.
If effective hydrogen trapping sites such as point defects are pre-engineered into the sample before hydrogen implantation at elevated temperatures, more hydrogen atoms are expected to be trapped in spite of the relatively high diffusivity of H atoms. To demonstrate this point, a Neon implantation at 250 keV with a dose of $1 \times 10^{14}$ cm$^{-2}$ at RT was conducted with a $R_p$ of ~385 nm that was similar to that of the H implant at 45 keV (~375 nm). The RBS spectrum shown in Fig. 2.3(e) was taken on the Ne$^+$ implanted sample after annealing at 200 °C for 1.5 hours, which was similar to the time for the hydrogen implantation at 200 °C. It is obvious that there was substantial damage remaining in this Ne$^+$ pre-implanted substrate as hydrogen trapping sites during the second H$^+$ implantation at 200 °C. The ERD spectra shown in Fig. 2.5(d) showed that the amount of H detected in the sample pre-implanted with Ne$^+$, followed by H implantation at 200 °C was ~ 90% of that in the sample with a single H$^+$ implantation at RT. These observations suggested that H ions implanted at 200 °C were trapped in the sample when active trapping sites were engineered in the sample prior to the hydrogen implantation at elevated temperatures. However, despite the abundance of H trapped in the substrate pre-implanted with Ne, surface blistering was not observed on any samples implanted at 200 °C. The presence of a sufficient amount of H trapped in the samples alone does not necessarily lead to surface blistering or layer delamination.

2.3.5 Effect of hydrogen implantation temperature on stress

Figure 2.6 summaries the X-ray diffraction data obtained from InP samples at various implant conditions. A series of interference peaks, as shown in Fig. 2.6(b), indicate that implantations at RT created significant out-of-plane tensile strain, indicative
of a corresponding in-plane compress stress. The maximum strain, measured by the separation of the left-most peak and the unstrained InP substrate peak, is proportional to the implanted hydrogen dose. The absence of those interference fringes in Fig. 2.6(c) indicated that hydrogen implantation at 200 °C introduced much less out-of-plane strain and corresponding in-plane compressive stress than in the case of RT implantation.

![X-Ray diffraction data on InP samples](image)

**Figure 2.6:** X-Ray diffraction data on InP samples: (a) virgin InP, (b) implanted with $4.5 \times 10^{16} \text{ cm}^{-2} \text{ H}^+$ at 45 keV at RT, (c) implanted with $4.5 \times 10^{16} \text{ cm}^{-2} \text{ H}^+$ at 45 keV at 200 °C, (d) implanted with $1 \times 10^{14} \text{ cm}^{-2} \text{ Ne}^+$ at 250 keV at RT, and (e) implanted with $1 \times 10^{14} \text{ cm}^{-2} \text{ Ne}^+$ at RT then implanted with $4.5 \times 10^{16} \text{ cm}^{-2} \text{ H}^+$ at 200 °C.

The observation of ion implantation induced out-of-plane tensile strain and corresponding in-plane stress in semiconductor materials is well documented and has
been shown to be correlated with implantation induced defects [19-21]. The origin of this hydrogen implantation-induced stress has been suggested to be related to the tetragonal distortion of lattice and volume expansion in the implanted region [2, 14, 19]. In the case of hydrogen implantation at RT, the point defects with a Gaussian-like distribution generated significant in-plane compressive stress and contributed to a series of interference diffraction peaks [2, 22, 23]. In the hydrogen implanted sample with relatively high dose, the hydrogen atoms have a Gaussian-like distribution, thus the point defect-induced corresponding strain also has a Gaussian-like distribution profile in the implanted region. The maximum strain is at the depth around the projected range of hydrogen, represented by the leftmost diffraction peak on XRD. The strain at the depths on either side of the maximum strained depth is less than the maximum stain, contributing to interference peaks to the right of the "leftmost diffraction peak" on the XRD data. At an elevated temperature of 200 °C in this work, the implantation induced defect clusters gave rise to the dechanneling yield on the RBS spectrum (Fig. 2.3(c)). These localized clusters apparently did not generate much stress in the implanted region.

For the Ne⁺ pre-implantation at RT, a slight increase in the width of InP substrate diffraction peak compared to that for the bulk InP was observed in Fig. 2.6(d). Although the Ne⁺ implantation created sufficient amount of defects to trap hydrogen, the stress generated by the Ne⁺ implantation was much smaller and very different from that generated by the H⁺ implantations (see Fig. 2.6 (b) and Fig. 2.6 (d)). Ne is an inert element, the chemical interaction of Ne⁺ ions with InP substrate is likely to be very different from that between H⁺ ions and InP [16], and that tetragonal distortion of lattice does not seem to take place. The stress observed for the Ne⁺ and H⁺ co-implantation
(Fig. 2.6 (e)) was similar to that of a single H\(^+\) implantation at 200 °C, and much less than that of a single H\(^+\) implantation at RT. Hydrogen implantation induced in-plane compressive stress has been reported to play a significant role in the blistering of Si [11]. For the RT implanted case, during subsequent annealing the significant in-plane compressive stress facilitated the diffusion of vacancies toward the maximum damage depth and produces favorable conditions for platelet nucleation and growth in the plane of the stress due to the presence of a Peach-Koehler force [11, 24, 25]. A detail description of platelet nucleation in the presence of an in-plane compressive stress can be found in references 11 and 25. The growth of H-platelets ultimately led to surface blistering or layer exfoliation. In contrast, in the Ne\(^+\) and H\(^+\) co-implanted sample, the stress was insufficient to drive to H-platelets nucleation and growth, thus the sample did not show any surface blistering even though the H contents were at a similar level to that implanted with H\(^+\) at room temperature.

**2.4 Effect of implantation dose rate**

To study the effects of implantation dose rate, a set of samples was implanted with H\(^+\) at 60keV with a dose of 5x10\(^{16}\) cm\(^{-2}\) at room temperature, but with three different dose rates (8.2 μA/cm\(^2\), 25 μA/cm\(^2\), and 75 μA/cm\(^2\), respectively).
Figure 2.7: Optical micrographs obtained using 400X magnification from InP samples implanted with the same dose \((5 \times 10^{16} \text{ cm}^{-2})\), same energy \((60 \text{keV})\), same temperatures (room temperature) but three different dose rates: (a) \(8.2 \mu \text{A/cm}^2\), (b) \(25 \mu \text{A/cm}^2\), and (c) \(75 \mu \text{A/cm}^2\). All samples were annealed at 250 °C for 2 hours after implantation.

Optical micrographs shown in figures 2.7(a)-3(c) demonstrate the effects of dose rate on surface blistering. With an increase of implantation dose rate, the surface blistering after subsequent annealing becomes more significant.

In general, at a given temperature and a fixed total dose, implantation at higher dose rate creates more damage in the substrate. Compared with the effect of implantation temperature on InP surface blistering, the effect of dose rate is less obvious. The relation between dose rate and damage is included in the empirical formula as discussed below.

2.5 Critical temperature concept and an empirical formula

To evaluate the dependence of damage formation on H implantation conditions, a formula based on Morehead-Crowder (MC) model [26-28] was used in this study. The MC model basically explains the “dynamic annealing” phenomenon during ion implantation. According to the model, each incoming ion produces a cylindrical cascade volume with a high density of primary defects inside. The simple primary defects may
diffuse out of this volume within a finite time interval before the cascade relaxes. The out-diffusion of defects produces a low-density defect region at the boundary of the original cascade volume, with a high-density defected core. Damage results from the collapse of the core to an amorphous state, while the sheath relaxes to a defect-free crystalline state. This model predicts a critical temperature \( T_c \), above which little or no damage would be created. More recently modeling led to an empirical equation that correlates \( T_c \) with implantation parameters \([1, 27-29]\):

\[ T_c = \frac{A}{B - \ln[(N_{\text{displ}}^*)^2 j]} , \quad (1) \]

where \( A \) and \( B \) are material constants, \( j \) is the dose rate and \( N_{\text{displ}}^* \) is the number of displaced target atoms per ion per angstrom, as a function of implant ion mass and energy. The value of \( N_{\text{displ}}^* \) can be extracted from SRIM 2006 simulations \([2]\). This empirical formula has been shown to be reasonably accurate for the prediction of \( T_c \) in Si, Ge, GaAs and other substrates implanted with various ions \([30, 31]\).

Table 2.3: Material constants \( A \) and \( B \) for different semiconductor materials

<table>
<thead>
<tr>
<th>Material</th>
<th>A</th>
<th>B</th>
<th>Reference</th>
</tr>
</thead>
<tbody>
<tr>
<td>InP</td>
<td>9640</td>
<td>52.5</td>
<td>[1]</td>
</tr>
<tr>
<td>GaAs</td>
<td>12651</td>
<td>70.0</td>
<td>[1]</td>
</tr>
<tr>
<td>InAs</td>
<td>9060</td>
<td>59.1</td>
<td>[28]</td>
</tr>
<tr>
<td>Si</td>
<td>13400</td>
<td>57.5</td>
<td>[29]</td>
</tr>
</tbody>
</table>
Table 2.3 shows material constants A and B for different materials. For InP, A and B have been reported in the literature to be 9640 and 52.5, respectively.

The value of $N^*_{\text{displ}}$ was extracted from TRIM to be 0.0072/ion/Å for implantation of 100keV H$^+$ ions into InP. Dose rate $j$ was $3.13 \times 10^{14}$ cm$^2$s$^{-1}$ (corresponding to 50µA/cm$^2$). We estimated the critical implant temperature to be ~60 °C, based on equation (1). In the present study, we found that samples implanted at 200 °C did not blister while those implanted at RT did. These observations were in agreement with a $T_c$ value of ~60 °C. Furthermore, this critical $T_c$ concept is consistent with the results reported in reference [2], where InP surface blistering was observed upon subsequent annealing only on samples implanted at -20 °C and not on the uncontrolled “room temperature” implanted sample. The uncontrolled temperature was estimated to be ~300 °C due to beam-heating.

Table 2.4: Calculated critical temperatures in InP substrate for different implant energies and dose rates.

<table>
<thead>
<tr>
<th>Implant energy (keV)</th>
<th>$N^*_{\text{displ}}$ (ion/Å)</th>
<th>Dose rate (/cm$^2$/s)</th>
<th>$T_c$ (°C)</th>
</tr>
</thead>
<tbody>
<tr>
<td>45</td>
<td>0.0081</td>
<td>$3.13 \times 10^{13}$</td>
<td>37</td>
</tr>
<tr>
<td>45</td>
<td>0.0081</td>
<td>$3.13 \times 10^{14}$</td>
<td>62</td>
</tr>
<tr>
<td>100</td>
<td>0.0072</td>
<td>$3.13 \times 10^{13}$</td>
<td>35</td>
</tr>
<tr>
<td>100</td>
<td>0.0072</td>
<td>$3.13 \times 10^{14}$</td>
<td>60</td>
</tr>
</tbody>
</table>

Table 2.4 presents more calculated critical temperatures at different implant
energies and dose rates. It is obvious that $T_c$ is a weak function of implant energy and dose rate. At a given implant energy, $T_c$ only increases by 25 °C with one order increase of the dose rate. It should be pointed out that the H implant temperature above which little or no damage would be created should be higher than these estimated $T_c$ since the active chemical interactions of H with lattice defects were not included in the MC model.

This critical temperature concept is also in agreement with our data on stress at different implant temperatures. Since the implantation induced in-plane stress is correlated with implantation induced defects [19-21], significant stress was observed when the temperature is below the estimated $T_c$ in our study. When the implant temperature was 200 °C, much higher than the estimated $T_c$, little stress was generated in the sample due to the lack of point defects (Fig.2.6).

2.6 Conclusion

In summary, the effects of hydrogen implantation conditions (energy, dose, temperature, and dose rate) on the ion-cut process of InP have been studied. Implant energy is used to control the thickness of transferred layers. Hydrogen dose was found to have a relatively narrow window for a successful III-V ion-cutting. And the required hydrogen dose for ion-cutting is a function of implant energy. We found that H trapping sites created by ion implantation and the in-plane compressive stress are both necessary for platelet nucleation, growth, and ultimately surface blistering or layer delamination. A sufficiently low implantation temperature is required for the ion-cut process of InP. The results were rationalized in terms of an empirical equation based on MC model, which can be used to guide the selection of implantation parameters in ion-cut process. Based
on these understandings on hydrogen implantation conditions, we optimized hydrogen implantation parameters for InP ion-cut in our study as presented in the following chapters.

Reference


Chapter 3

High crystalline-quality III-V layer transfer onto Si

3.1 Issues with conventional III-V layer transfer approaches

3.1.1 Ion-induced damage with conventional ion-cut

The ion-cut (or smart-cut®) process [1], commercially used to transfer thin Si layers onto insulators to form silicon-on-insulator (SOI) substrates, has been recently demonstrated for III-V layer transfers [2-7]. As introduced in Chapter 1, the ion-cut process typically utilizes hydrogen ion implantation to induce layer exfoliation. As a result, there are two major issues with the conventional ion-cut, discussed as follows:

(1) Since the layer exfoliation occurs around the projected range of hydrogen ions, part of the implanted region gets transferred and becomes the surface region of the transferred structure. Therefore the top portion of the transferred layer always suffers from the implantation-induced damage, which can not be easily recovered by thermal annealing [5-7]. Figure 3.1 shows a typical cross-section TEM image on an as-transferred InP on GaAs structure with SiNx in between as the bonding layers [7]. It is obvious that in the as-transferred structure, ~100nm thick surface region is heavily damaged by hydrogen ion implantation.
(2) The as-transferred surface is usually rough with a typical root-mean-square (RMS) surface roughness of $\sim 10\text{nm}$ or higher as reported for the transferred III-V layers [3, 7]. For example, Figure 3.2 shows 2D and 3D Atomic Force Microscope (AFM) views on the as-transferred InP surface with a RMS roughness of 8.5nm [7].
For subsequent epitaxial growth or device fabrication, typically the surface needs to be smoothed to a level with a RMS less than 1nm. Although a chemical mechanical polishing (CMP) [7], or a plasma etch [3] has been utilized to improve the as-transferred rough surface, these polishing processes have not been well developed for III-V materials. Without the presence of an etch-stop layer in the transferred structure, it is rather difficult to control these polishing processes.

3.1.2 Processing issues with conventional wafer bonding and etch-back

Another approach based on wafer bonding and etch-back is widely used for III-V layer transfer [8, 9], as shown in Fig1.4 in Chapter 1. In this case, an etch-stop layer is pre-engineered into III-V materials before wafer bonding, thus the bonded structure can be etched from the backside of the III-V material until the etching reaches the etch-stop. This approach provides relatively high quality layer transfer compared with the conventional ion-cut process, since there is no hydrogen ion implantation involved. However, it also increases the cost because the whole substrate is etched, especially in the case of III-V layer transfer since the III-V wafers are relatively expensive. The yield of the wafer bonding and etch back method can be an issue as well.

3.2 Our new approach of combining ion-cut and selective etch for III-V layer transfer

Our approach to reduce ion-induced damage is to combine ion-cutting together with selective chemical etch. This approach can also improve the transferred surface flatness.
Figure 3.3: Process flow of our scheme for InP layer transfer: (a) heterostructure growth using MOCVD; (b) H⁺ ion implantation (dotted line indicates the projected range of the hydrogen implant); (c) wafer bonding of implanted heterostructure with a SiO₂/Si piece; (d) layer exfoliation induced by a thermal annealing; (e) selective etching on both sides.

Figure 3.3 shows a schematic diagram of our process flow for III-V layer transfer. An InP (200 nm)/InGaAs(500 nm)/InP(150 nm)/InGaAs(500 nm)/InP substrate structure was grown by Metal Organic Chemical Vapor Deposition (MOCVD). To illustrate the feasibility of using ion-cut for multiple III-V layers transfer, the top double-heterostructure (DH) of InP/InGaAs/InP was chosen as an example for the layer transfer
in our study. The 500nm-thick InGaAs layer below the DH was used as an etch-stop layer. The as-grown sample was coated with a 65nm-thick SiNx film using plasma enhanced chemical vapor deposition (PECVD) to protect the surface during ion implantation. H\(^+\) ions were implanted at 160 keV with a dose of \(8 \times 10^{16} \text{ cm}^{-2}\), nominally at room temperature. The hydrogen dose of \(8 \times 10^{16} \text{ cm}^{-2}\) at 160keV was found to be the minimum dose required to induce the layer transfer in this study. After implantation, the protective SiN\(_x\) layer was etched off and the sample was cleaved into pieces with 1 cm\(\times\)1 cm in dimensions. A piece of implanted heterostructure sample and a piece of Si substrate coated with a 68 nm-thick thermal SiO\(_2\) layer were cleaned with organic solutions. The SiO\(_2\)/Si piece was then cleaned by RCA1 solution (NH\(_4\)OH:H\(_2\)O\(_2\):H\(_2\)O=1:2:10) and the heterostructure was cleaned by 1% hydrofluoric acid. After an oxygen plasma activation process on both pieces, they were placed in contact at room temperature in air, followed by a thermal anneal at 100 °C for 10 hours to increase the bonding strength. Upon a subsequent anneal at 180 °C, the bonded structure exfoliated and resulted in a structure of InGaAs(350 nm)/ InP(150 nm)/ InGaAs(500 nm)/ InP(200 nm)/ SiO\(_2\)(68 nm)/ Si sub. The top InGaAs layer was then selectively etched using a solution of phosphoric acid and hydrogen peroxide, yielding a double-heterostructure of InP/InGaAs/InP on a SiO\(_2\)/Si substrate. The top InP and InGaAs layers can be further etched off for different purposes.

3.3 Surface roughness study

This layer transfer scheme provides an effective way to improve the surface flatness. Digital camera, Optical microscope with Nomarski lens, Scanning Electron
Microscope (SEM), and Atomic Force Microscope (AFM) were utilized to examine the surface conditions.

Figure 3.4 presents a typical digital photo on the as-transferred surface taken by a digital camera. In this example, an implanted heterostructure donor piece with ~ 1cm × 1 cm in dimensions was bonded to a bigger SiO$_2$/Si acceptor piece. It is obvious that almost all the bonded donor piece (~ 1cm × 1 cm) was transferred onto the SiO$_2$/Si piece, as shown in the middle area of Fig. 3.4. The surrounding blue area is the exposed SiO$_2$ surface that was not bonded.

![Image of bonded donor piece](image)

**Figure 3.4:** Digital image on the as-transferred InGaAs/InP/InGaAs/InP/SiO$_2$/Si sample.

Optical microscopic images shown in Figure 3.5 and Figure 3.6 were taken on the surface before and after etching, at 50 X and 400 X magnification, respectively. It is clear that after etching the surface is much smoother.
Figure 3.5: Optical microscope images taken at 50X magnification on sample surfaces: (a) one corner of the as-transferred InGaAs surface, (b) after etching with $\text{H}_3\text{PO}_4:\text{H}_2\text{O}_2:\text{H}_2\text{O}=1:1:30$ for 3 minutes, top InGaAs layer was removed.

Figure 3.6: Optical microscope images taken at 400X magnification on sample surfaces: (a) one corner of the as-transferred InGaAs surface, (b) after etching with $\text{H}_3\text{PO}_4:\text{H}_2\text{O}_2:\text{H}_2\text{O}=1:1:30$ for 3 minutes, top InGaAs layer was removed.
Figures 3.7 and 3.8 are SEM images taken from another set of samples in our study. The initial MOCVD grown sample had a structure of InP(200nm)/InGaAs(300nm)/InP substrate. After a hydrogen implantation at 80 keV and layer transfer process, the as-transferred layer structure was InP(110nm)/InGaAs(300nm)/InP(200nm)/SiO$_2$/Si sub, as shown in Figure 3.7.

**Figure 3.7:** SEM images on the as-transferred InP/InGaAs/InP/SiO$_2$/Si sub sample: (a) 45° View, (b) 85° view (cross-section). A few nanometer thick Au film was deposited prior to SEM analyses to reduce charging problem.
Figure 3.8: SEM images on the transferred and etched sample with a structure of after etching with a structure of InGaAs/InP/SiO$_2$/Si sub: (a) 45° View, (b) 85° view (cross-section). A few nanometer thick Au film was deposited prior to SEM analyses to reduce charging problem.

After etching, the resulting structure was InGaAs(300nm)/InP(200nm)/SiO$_2$/Si sub, as shown in Fig. 3.7(b) and Fig. 3.8(b). It should be pointed out that the surface shown in Figure 3.7 and Figure 3.8 were covered by a thin Au layer (a few nanometers) that was deposited on the top surface to reduce the charging problem. However, by
comparing the samples before and after etching, it is obvious that the etching significantly smoothed the as-transferred surface.

In our study, AFM was used to monitor the surface roughness after each step. Each AFM scan covered an area of $5\, \text{um} \times 5\, \text{um}$ in dimensions. The as-grown InP/InGaAs/InP/InGaAs/InP sub heterostructure had a surface roughness RMS 0.57 nm, as shown in Fig. 3.9 (a).

![AFM Image](image)

(a) RMS=0.57 nm

(b) RMS=0.267 nm

Figure 3.9: 3D-view AFM image of: (a) as-grown top InP surface of heterostructure (see the structure in Fig.3.3 (a)); (b) SiO$_2$/Si surface.
The other bonding side, the SiO$_2$ (68nm)/Si sample had a surface RMS of 0.267 nm, as shown in Figure 3.9(b). Both sides were sufficiently flat for our bonding purpose.

The as-transferred InGaAs surface had a surface roughness of 72.3 nm (Fig. 3.10). It is much rougher than a typical as-transferred InP surface which has a roughness RMS of 10-20 nm [3, 7]. This is possibly due to different fracture properties of different materials, such as fracture toughness.

**Figure 3.10:** 3D-view AFM image of the as-transferred InGaAs surface (see the structure in Fig.3.3 (d)).

This top InGaAs layer was then selectively etched and the newly exposed surfaces roughness was examined by AFM. In our study, a solution with Hcl: H$_2$O=1:1 was used to etch InP layers from InGaAs, which is a commonly used chemical for this kind of
selective etch. There are a few etchants reported in the literature that can selectively etch InGaAs from InP [14-17]. In our study, it has been observed that various etchants created different surface roughness, as shown in Table 3.1. The smoothest surface was obtained after etching with a solution of $\text{H}_3\text{PO}_4:\text{H}_2\text{O}_2:\text{H}_2\text{O}=1:1:30$.

Table 3.1: Surface roughness after different etch solutions.

<table>
<thead>
<tr>
<th>Solution</th>
<th>Etch time (min)</th>
<th>RMS after etch (nm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Citric acid ($\text{C}_6\text{H}_8\text{O}_7$):$\text{H}_2\text{O}_2$:H$_2$O</td>
<td>5</td>
<td>1.715</td>
</tr>
<tr>
<td></td>
<td>$=15\text{g}:4\text{ml}:15\text{ml}$</td>
<td></td>
</tr>
<tr>
<td>H$_2$SO$_4$:H$_2$O$_2$:H$_2$O=1:1:30</td>
<td>5</td>
<td>1.951</td>
</tr>
<tr>
<td>H$_3$PO$_4$:H$_2$O$_2$:H$_2$O=1:1:30</td>
<td>5</td>
<td>0.83</td>
</tr>
</tbody>
</table>

The surface roughness on the new InP surface decreased to 0.83 nm (Fig. 3.11), sufficiently smooth for subsequent epitaxial growth.

Figure 3.11: 3D-view AFM image of transferred and etched sample with a structure of InP/InGaAs/InP/SiO$_2$/Si sub, etched by $\text{H}_3\text{PO}_4:\text{H}_2\text{O}_2:\text{H}_2\text{O}=1:1:30$. 

RMS=0.83 nm
3.4 Damage distribution study

The hydrogen ion implantation profile has a Gaussian-like distribution [10, 11]. The damaged peak is located near the projected range of hydrogen, but extends to a deeper depth to the end-of-range of the ions [7, 12]. To reduce the implantation damage when using this combined ion-cutting and selective etch scheme, it is crucial to place the hydrogen ions sufficiently deep into the substrate and transfer a relatively thick structure. By doing this, the primary implantation damage is located below and away from those top layers of interest (e.g., the double-heterostructure in this study). A portion of heavily damaged region is transferred and is located on top of the transferred structure, which can be selectively etched off. In this study, the hydrogen implant energy of 160 keV defined a projected range of 1.2 µm below the surface, thus it induced the layer split in the InGaAs layer right above the InP substrate. A cross-section transmission electron microscopy (TEM) image shown in Fig. 3.12(a) indicates that there are no noticeable defects in the as-grown heterostructure. To examine the implantation damage distribution and the location of H-related microcracks, an implanted sample was annealed at 200 °C to induce surface blistering without wafer bonding and the corresponding TEM image is shown in Fig. 3.12(b). It is obvious that the hydrogen implantation induced cracks in the InGaAs layer above the InP substrate. The implantation damage was located in the InP substrate and in the InGaAs layer directly above it, leaving the top InP and InGaAs epitaxial layers relatively damage-free.
Figure 3.12: Cross-section TEM images of: (a) as-grown sample; (b) hydrogen implanted and annealed sample.
Based on a SRIM ion-range simulation (shown in Fig. 3.13) [13], the hydrogen concentration in the double-heterostructure of InP/InGaAs/InP is neglectable compared to the total hydrogen dose. Although the hydrogen implantation is used to induce the layer transfer, the effects of implantation on the final transferred and etched structure have been minimized.

Figure 3.13: A SRIM simulated hydrogen ion distribution profile for the implant energy of 160 keV.
3.5 Stress study

Figure 3.14 presents the X-ray diffraction (XRD) studies along with our process. For all the strain analyses, the (004) diffraction peak from InP substrate in the as-grown sample was used as a reference with no or little stain. In Fig. 3.14 (a), the diffraction peak from as-grown InGaAs layers was 692 arcseconds away from the InP substrate peak, indicating the out-of-plane compressive strain in the InGaAs layers. After hydrogen implantation, a series of peaks was observed to the left of InP substrate diffraction peak with the maximum strain of 864 arcseconds as shown in Fig. 3.14(b). The InGaAs peak also shifted to the left of its original position (Fig. 3.14 (b)). These results revealed the out-of-plane tensile strain induced by the hydrogen implantation with a Gaussian-like distribution. After the wafer bonding and layer transfer process at 180 °C, the transferred InP layers had the out-of-stain tensile strain of 392 arcseconds and the InGaAs layers had the out-of-plane compressive strain of 494 arcseconds. Upon subsequent annealing at 400 °C for 1 hour, the strain in both InP and InGaAs layers was reduced due to the partial recovery of the implantation induced damage (Fig. 3.14 (d)). With the top InGaAs layer, which contained most of the implantation damage in the transferred structure, selectively etched off, the strain of the remaining InGaAs layer was further reduced to 439 arcseconds (Fig. 3.14 (e)). The top two layers of InP and InGaAs were further etched off, resulting in a simple structure of InP/SiO₂/Si with a full width at half maximum (FWHM) of ~ 130 arcseconds as shown in Fig. 3.14 (f). These results demonstrate that thermal annealing and selective etching can effectively minimize the effects of hydrogen implantation on the strain of transferred layers.
Figure 3.14: X-ray diffraction data from: (a) as-grown InP/InGaAs/InP/InGaAs/InP sub; (b) H⁺ as-implanted InP/InGaAs/InP/InGaAs/InP sub; (c) as-transferred InGaAs/InP/InGaAs/InP/SiO₂/Si sub; (d) annealed InGaAs/InP/InGaAs/InP/SiO₂/Si sub; (e) after first etch, InP/InGaAs/InP/SiO₂/Si sub; (f) after further etch, InP/SiO₂/Si sub.
3.6 Conclusion

The feasibility of III-V layer transfer using the ion-cutting process and selective chemical etching has been demonstrated. A double-heterostructure of InP/InGaAs/InP has been transferred onto a SiO$_2$/Si substrate. Advantages of this approach include a reduction in implantation induced damage, as well as an improvement in the surface quality of the transferred surface without CMP.


Reference


Chapter 4

Using transferred InP/SiO$_2$/Si as a regrowth template

4.1 Introduction

As discussed in previous chapters, the ion-cut process has been recently utilized for III-V layer transfers. In particular, a few preliminary investigations have demonstrated the feasibility of using III-V-on-Si structures obtained by ion-cutting for regrowth of III-V device structures [1-3]. A germanium-on-insulator structure obtained by ion-cutting has been reported in the literature. GaInP/GaAs dual junction solar cell was then epitaxially grown on the ion-cut substrate [4].

Due to the nature of ion-cutting, an ion-damaged region near the top of transferred structure is always present, and the as-transferred surface is usually rough, as shown in Fig 3.1 and Fig 3.2 in Chapter 3. To use the transferred III-V layer as a growth template, it is crucial to remove the top damaged portion to improve the crystalline quality of regrowth. Figure 4.1 compares the Ge epitaxial growth on transferred Ge/Si structure, with or without the damage removal [4]. It is clear that in the case without damage removal, the damage in the as-transferred structure resulted in defect propagation into the re-grown epitaxial layers (Fig. 4.1(a)). The removal of the ion damage in the transferred structure thus provides viable substrates for high quality epitaxial growth (Fig. 4.1 (b).)
Figure 4.1: Cross-sectional transmission electron microscopy images of Ge homoepitaxy on a Ge/ Si template (a) directly grown the as-transferred surface without damage removal, (b) with damage removal. The white line is at the interface of the substrate and the homoepitaxy. (after reference [4])

General approaches have also been demonstrated to remove the damaged region and to improve the surface flatness. For the case shown in Figure 4.1, the RMS roughness after layer transfer was approximately 25 nm and the ion implantation induced damaged layer extended approximately 200 nm into the film. A dilute CP-4 (HF:HNO$_3$:CH$_3$COOH) wet etch was first used to remove the damaged layer. A touch polish process was then used to further polish the surface until it achieved a final RMS roughness of ~0.5 nm [4]. A chemical mechanical polishing (CMP) process [2, 5], and a plasma etch [1] have also been utilized to prepare a suitable surface for subsequent regrowth. These etching and polishing processes, however, have not been fully developed for III-V materials and the yield is often low.

In Chapter 3, we have demonstrated a high quality III-V layer transfer scheme that reduces the ion-implantation induced damage and improves the transferred surface
flatness. The top portion containing most of the implant damage in the as-transferred structure is etched by a simple selective chemical etch and the resulting surface has a surface roughness RMS of only 0.87 nm. This chapter discusses the feasibility of using this improved transferred structure as a template for further epitaxial growth of InP.

4.2 Surface bubble issue

A typical III-V epitaxial growth is conducted in the temperature range of ~500-650 °C, thus it is required that the transferred III-V-on-Si samples must survive such a high temperature without any surface degradation. In this study, H-induced layer exfoliation occurs at a relatively low temperature of ~120-180 °C. The as-transferred sample usually had a uniform surface, free of bubbles, as shown in Fig. 4.2 (a). Temperature-dependent bubbles were observed when the transferred samples were heated to an elevated temperature range of ~300-400 °C as shown in figures 4.2 (b) and (c). It should be noted that the samples shown in Fig 4.2 were obtained by ion-cutting a bulk InP wafer, with a final transferred structure of InP/SiO₂/Si as shown in Fig. 4.3. The bubble issue is a common problem that occurred on all our transferred samples, including the simple structure of InP/SiO₂/Si and more complicated structure of InP/InGaAs/InP/SiO₂/Si. The transfer of a single InP layer onto Si with a resulting structure of InP/SiO₂/Si was used to study the origin of the surface bubbles. A few extra processing steps were then developed to reduce/prevent the bubble formation. The established procedure was then applied to more complicated structures, and found effective as well.
Figure 4.2: Optical microscopic images on the surface of: (a) as-transferred InP/SiO$_2$/Si (transfer temperature was 180 °C); (b) after annealing at 300 °C for 1hr; (c) after further annealing at 400 °C for 1hr.

Figure 4.3: A schematic diagram of the process flow for a single InP layer transfer. The bubble issue with the resulting InP/SiO$_2$/Si is shown in Figure 4.2.
To investigate the origin of the surface bubbles, Fourier transmission infrared (FTIR), an effective method for chemical composition analyses at surfaces/interfaces [6-8], was used in this study to detect the compositions of the chemicals at the bonding interface.

**Figure 4.4:** Fourier transmission infrared (FTIR) on a transferred sample InP/SiO$_2$/Si after annealing at 400 °C for 1hr. A few bubbles were present on the surface. (FTIR measurement was in collaboration with Prof. T. F. Kuech’s group at University of Wisconsin, Madison)

Figure 4.4 shows FTIR data on a transferred InP/SiO$_2$/Si sample after annealing to 400 °C, and with a few bubbles on the surface. On the transmission spectrum, two peaks at wave number ~ 440 cm$^{-1}$ and 600 cm$^{-1}$ are vibrational modes from the InP layer. The peak around 1092 cm$^{-1}$ indicates the presence of InPO$_4$ at the bonding interface. There is a broad peak centered at ~ 2727 cm$^{-1}$, which is generally attributed to a mixture of In and
P hydrides and hydroxides at the interface. Signals from hydrocarbon related contaminations may also be buried in this broad peak since they have been reported to be present in the range of 2800-3000 cm$^{-1}$ [6].

There are many sources for hydrocarbon contamination. It is difficult to avoid during wafer cleaning processes [6]. Ion implantation also introduces hydrocarbons to the surface. To minimize the hydrocarbons generated on the surface during hydrogen implantation, a 70nm-thick SiNx protecting film was deposited on the InP surface using Plasma Enhanced Chemical Vapor Deposition (PECVD) at 350 °C, before implantation. This SiNx was then etched off after hydrogen implantation and before wafer bonding process. Figure 4.5 shows a schematic diagram of the process flow with the use of a SiNx layer.

![Figure 4.5](image)

**Figure 4.5:** A schematic diagram of InP layer transfer, with the use of a protecting SiNx layer.

After layer transfer at ~ 180 °C, the transferred structure was annealed to elevated temperatures to examine the bubble issue, as shown in Figure 4.6. At 400 °C, the surface was still free of bubbles (Figure 4.6 (b)), while the sample prepared without using a SiNx layer showed significant bubbles at 400 °C (Figure 4.2 (c)). At an annealing temperature of 500 °C, the surface degraded significantly due to the presence of surface bubbles.
Figure 4.6: Optical microscopic images on the sample transferred with SiN\textsubscript{x} protecting layer. (a) as-transferred InP/\textit{SiO}_2/Si (transferred at 180 °C); (b) after annealing at 400 °C for 1hr; (c) after further annealing at 500 °C for 1hr.
Therefore, the use of SiN\textsubscript{x} protecting layer during implantation delayed the on-set of bubble formation, but did not eliminate the bubble issue.

Surface bubble formation is a function of annealing temperature, simple calculations were used to estimate the vapor pressure from the vaporized hydrides, hydroxides, and/or hydrocarbons at the bonding interface. Assuming a volatilized monolayer of hydrides, or hydroxides, or hydrocarbons at the interface with an areal density of 1 \times 10^{15}/cm\textsuperscript{2} and confined within 0.1um (1 \times 10^{-5} cm) in between the bonding interface, e.g. n=1 \times 10^{20}/cm\textsuperscript{3}=1 \times 10^{26}/m\textsuperscript{3}. According to the ideal gas law:

\[ P=nK_B T \quad (1) \]

Where \( P \) is the absolute pressure of the gas, \( n \) is the volume density of molecules, \( K_B \) is the Boltzmann’s constant that is 1.38 \times 10^{-23} J/K, and \( T \) is the absolute temperature.

At 500 °C, \( n=1 \times 10^{26}/m^3 \), \( P = 1.07 \times 10^6 \) Pa = ~ 10 atm. This rough calculation suggests that even a monolayer at the bonding interface can induce a pressure as high as ~ 10 atm at 500 °C. If the force associated with this level of pressure is higher than the bonding strength in a local area, it can separate the bonding in that area to form interfacial bubbles. As a result of pressure built-up, these interfacial bubbles developed into surface bubbles. It should be noted that the calculation is based on an assumption that the areal density of some form of contamination at the bonding interface is 1 \times 10^{15}/cm\textsuperscript{2}. The calculated pressure is a linear function of the assumed areal density.
Based on the estimated pressure at the bonding interface, an external pressure was introduced in our layer transfer and subsequent annealing processes, to suppress the vapor pressure at the bonding interface. The process flow is still the same as shown in Fig.4.5. The InP wafer and the SiO$_2$/Si piece were put into contact at room temperature, and the bonded pair was annealed on a hot plate. A heavy weight was then put directly on the bonded pair applying a pressure of ~10 atm. The bonded pair exfoliated when the temperature reached ~ 180 °C, under applied external pressure. Without removing the heavy weight, the transferred structure was further annealed sequentially with an increase of 100 °C per step with 1hr at each step. It was found the transferred piece was completely free of surface bubbles after annealing up to 500 °C for 1 hr. Since 500 °C is the maximum temperature for the hot plate used in our study, we subsequently annealed this piece at 650 °C for 1 hr in a furnace with a N$_2$ gas flow. As shown in Figure 4.7 (b), the surface is still free of surface bubbles after annealing at 650 °C.

In this study, the prevention of surface bubbles at high temperatures by applying an external pressure was constantly successful for multiple samples. The 10 atm external pressure applied during layer transfer and subsequent annealing effectively suppressed the development of the vapor pressure at the interface toward the direction perpendicular to the surface. Also, this external pressure during wafer bonding could increase the bonding strength and thus provided higher energy barrier for the interfacial bubbles to form.
Figure 4.7: Optical microscopic images on the sample transferred with SiN$_x$ protecting layer and external pressure. (a) as-transferred InP/SiO$_2$/Si (transferred at 180 °C); (b) after further annealing at 650 °C for 1hr.

The combination of the “SiN$_x$ protecting layer” and the “external pressure” was also found useful when applied to more complicated structures for regrowth at ~ 650 °C without any surface degradation.

4.3 Regrowth of InP epitaxial layer

Figure 4.8 shows a schematic diagram of our process flow that was used to prepare an InP/SiO$_2$/Si structure as a growth template. An InP (200 nm)/InGaAs(400 nm)/InP substrate structure was grown by Metal Organic Chemical Vapor Deposition (MOCVD). The as-grown sample was coated with a 70nm thick SiN$_x$ film using
PECVD to protect the surface from hydrocarbon contaminations during ion implantation.

H$^+$ ions were implanted at 160 keV at -15 °C with a dose of $8 \times 10^{16}$ cm$^{-2}$.

**Figure 4.8**: Process flow of InP layer transfer for regrowth purpose: (a) heterostructure growth using MOCVD and a SiN$_x$ deposition by PECVD; (b) H$^+$ ion implantation (dotted line indicates the projected range of the hydrogen implant); (c) wafer bonding of implanted heterostructure with a SiO$_2$/Si piece; (d) layer exfoliation induced by a thermal annealing; (e) selective etching.
After implantation, the protective SiN$_x$ layer was etched off and the sample was cleaved into pieces with 1 cm×1 cm in dimensions. A piece of implanted heterostructure sample and a piece of Si substrate coated with a 68 nm-thick thermal SiO$_2$ layer were cleaned with organic solutions. The SiO$_2$/Si piece was then cleaned by RCA1 solution (NH$_4$OH:H$_2$O$_2$:H$_2$O=1:2:10) and the heterostructure was cleaned by 1% hydrofluoric acid. After an oxygen plasma activation process on both pieces, they were placed in contact at room temperature in air, followed by a thermal anneal at 100 °C for 10 hours under an external pressure of 10 atm. Upon a subsequent anneal at ~ 180 °C under the external pressure, the bonded structure exfoliated and resulted in a structure of InP(600 nm)/InGaAs(40 nm)/ InP(200 nm)/ SiO$_2$(68 nm)/ Si sub, as in Figure 4.8(d).

**Figure 4.9:** Optical microscopic images on (a) as-transferred surface after annealing at 650 °C for 1 hr, (b) after a regrowth of 300nm thick InP layer directly on the as-transferred structure (see Fig 4.8 (d))

The transferred piece then went through sequential annealing under the 10 atm pressure up to 500 °C, and a final annealing at 650 °C in N$_2$ for 1hr without the applied
pressure. A 300nm-thick InP layer was grown on the transferred structure, with or without the removal of the top two layers of InP (600nm) and InGaAs (400nm). The regrowth was done at 650 °C using MOCVD, by Winnie Chen, our collaborator in Prof. Paul Yu’s group.

Figure 4.9 (a) shows an optical microscopic image taken on the transferred and annealed sample, i.e. InP(600nm)/InGaAs(400nm)/InP(200nm)/SiO₂(68nm)/Si sub as shown in figure 4.8(d). The surface roughness RMS was ~ 15 nm. Figure 4.9(b) presents the surface after the regrowth directly on the as-transferred surface. It is obvious that the new regrown InP surface was quite rough with many particles on it.
Figure 4.10: X-Ray diffraction (XRD) data on: (a) as-grown sample before ion-cutting, (b) transferred and annealed sample, (c) after further regrowth of a 300nm thick InP layer.

Figure 4.10 presents X-Ray diffraction (XRD) data at different processing stages. No significant diffraction peak was observed other than the main peak from InP substrate in the as-grown sample, indicating the InP and InGaAs layers were relatively lattice matched to the InP substrate. For the transferred and annealed sample (Fig.4.10(b)), there were two diffraction peaks. The peak with higher intensity was from InP layer and the shoulder peak was believed to be from the remaining implantation damage that could...
not be completely removed by annealing. After regrowth, the two peaks in 4.10 (b) developed into a broad peak with a full width at half maximum (FWHM) of 230 arcsec. The regrowth of InP layer directly on the transferred surface without selective etch did not achieve high-quality epitaxial layer.

The regrowth of an InP layer was then conducted on transferred and etched sample. Figure 4.11(a) shows the surface of the structure after etching, i.e. InP(200nm)/SiO$_2$(68nm)/Si as shown in Figure 4.8 (e). The sample was then etched by 1% HF for 1 min before regrowth. After the regrowth of a 300 nm thick InP layer, the surface was still smooth and clean, as shown in Figure 4.11 (b).

![Figure 4.11](image-url)

**Figure 4.11:** Optical microscopic images on (a) transferred, annealed and etched structure of InP/SiO2/Si (b) after a regrowth of 300 nm thick InP layer at 650 °C.

Figure 4.12 summarizes the XRD data on the samples with selective etch before regrowth. It is obvious that after selective etch, only one diffraction peak was present in
Figure 4.12 (c), with a FWHM of 137 arcsec. The regrowth of a 300nm InP layer did not create any extra peak, with only a slight increase on the peak width, resulting in a diffraction peak with a FWHM of 160 arcsec.

**Figure 4.12:** X-Ray diffraction (XRD) data on: (a) as-grown sample, (b) transferred and annealed sample, (c) selectively etched to InP/SiO₂/Si, (d) after further regrowth of a 300nm thick InP layer at 650 °C.
4.4 Surface cleaning for regrowth

The surface treatment before regrowth has a strong influence on the crystalline quality of the epitaxial layer. In general, growth on a bulk Epi-ready wafer is straightforward without any special surface cleaning or treatment needed. In our study, we found the most effective way to prepare a bulk InP wafer for MOCVD growth is rinsing in deionized (DI) water followed by a N\textsubscript{2} blow dry. However, the regrowth on a transferred and etched surface is much more difficult, since the etched surface is different from an Epi-ready surface in terms of the surface roughness, cleanliness, surface recombination velocity [9], and chemical properties. It has been reported that the surface preparation dominates the performance of the devices obtained by a re-grow on a transferred Ge/Si template [10]. There are several studies on the surface preparations for regrowth on InP and InGaAs surfaces [9, 11, 12]. For example, reference 9 showed that dilute bromine-based solution treatment on InGaAs surface before InP regrowth yielded low surface recombination velocity.

In this study, we investigated surface treatment on the transferred and etched samples for regrowth. In Fig. 4.8 (e), the last chemical used to selectively etch InGaAs from InP was H\textsubscript{3}PO\textsubscript{4}:H\textsubscript{2}O\textsubscript{2}:H\textsubscript{2}O=1:1:30. After this etching step followed by a DI water rinsing, the obtained InP(200nm)/SiO\textsubscript{2}(68nm)/Si sample was cut into three pieces, for different surface treatments before the regrowth. The first set of samples was used directly for regrowth, without any further treatment after the etching. The second set of samples was cleaned using 1% HF for 1 min followed by a DI water rinsing. The third set of samples was cleaned by a solution of H\textsubscript{2}SO\textsubscript{4}:H\textsubscript{2}O\textsubscript{2}:H\textsubscript{2}O=1:1:30 for 2min followed by DI water rinsing.
Figure 4.13: Optical microscopic images on the surfaces after regrowth of a 300nm thick InP layer. Different surface treatments were conducted before the regrowth: (a) 1% HF for 1 min, (b) no treatment, (c) H_2SO_4:H_2O_2:H_2O=1:1:30 for 2 min.
Optical microscopic images were taken on the surface after the regrowth on each sample, as shown in Fig. 4.13. The best surface after regrowth was obtained from the HF cleaned sample. For the samples with a H$_2$SO$_4$ based treatment or without any treatment, the surfaces were not as flat or as clean as the HF treated one.

Fig. 4.14 shows the corresponding AFM data from each surface shown in figure 4.13. The transferred and etched InP surface had a surface roughness RMS of ~0.80 nm. After HF treatment and regrowth of a 300nm thick InP layer, the surface roughness RMS slightly dropped to 0.69nm, as shown in Figure 4.14 (a). For the sample without any treatment, the new surface had a roughness RMS of 0.87nm, and the one with the H$_2$SO$_4$ based treatment had a surface roughness RMS of 1.25nm after the regrowth.

Figure 4. 14: AFM 3D view on the surfaces after regrowth of a 300nm thick InP layer. Different surface treatments were conducted before the regrowth: (a) 1% HF for 1 min.
Figure 4.14 (continued): AFM 3D view on the surfaces after regrowth of a 300nm thick InP layer. Different surface treatments were conducted before the regrowth: (b) no treatment, (c) $\text{H}_2\text{SO}_4:\text{H}_2\text{O}_2:\text{H}_2\text{O}=1:1:30$ for 2 min.

Based on these observations, it is likely that the etching with $\text{H}_3\text{PO}_4:\text{H}_2\text{O}_2:\text{H}_2\text{O}=1:1:30$ created a thin layer of oxide that affects the regrowth. Etching
with HF was able to prepare a hydrophobic InP surface that was more suitable for the InP regrowth, compared with other surfaces.

4.5 Conclusion

The feasibility of using the transferred and etched InP/SiO2/Si structure as a template for InP epitaxial regrowth has been demonstrated. Hydrocarbon contaminations and vapor pressure at the bonding interface have been found to cause the temperature-dependent surface bubbles on the transferred surface. The “SiNₓ protecting layer” and the “external pressure” method developed in our process can effectively suppress the surface bubbles and thus provide transferred structures that can stand 650 °C for regrowth. InP epitaxial layer was grown on the transferred and etched InP/SiO₂/Si structure with only a slight increase on the FWHM of the XRD diffraction peak. Cleaning with 1% HF on the transferred and etched sample resulted in the cleanest and smoothest surface after regrowth of InP.
Reference


Chapter 5

Transfer of InP/InGaAs/InP p-i-n photodiodes onto Si

5.1 Introduction

The goal for III-V integration with Si is to enable optoelectronic integrated circuits (OEIC) that combine III-V based optoelectronic devices with Si-based microelectronic circuits. Optical interconnections on Si chips have been considered to be one of the most promising solutions to overcome the communication bottlenecks in electrical interconnections of VLSI circuits or systems [1-4]. InP-based photodetectors and lasers on Si substrates are of particular interest for the optical interconnection purpose, since their optical spectra can cover the low dispersion and minimum loss wavelength for optical fibers communications at 1.35 \( \mu \text{m} \) and 1.55 \( \mu \text{m} \) [5]. In addition, the Si substrate is transparent at the emission and absorption wavelengths most often used in InP-based optoelectronics [4].

Wafer bonding and etch back approach has been widely used to transfer III-V devices onto Si. For instance, InP based edge-emitting laser and LED have been integrated to Si substrate by InP-to-Si wafer bonding and etch of the original growth substrate [6].

In the case of III-V to Si integration using ion-cutting, it is common to transfer III-V layers onto Si and use the transferred structure as a template for subsequent epitaxial growth of devices [5, 7, 8]. Due to the rough as-transferred surface and considerable implantation-induced radiation damage near the surface region of transferred structure, a
chemical mechanical polishing (CMP) process and/or other surface treatments are required before re-growth of epitaxial layers [7-9]. Without the complete damage removal, the re-grown III-V device structures always suffer from the propagation of remaining radiation damage in the transferred layers.

Chapter 3 presents a high crystalline quality III-V layer transfer scheme that combines ion-cutting and selective chemical etch. This method reduces the implantation-induced damage and improves the transferred surface flatness, thus is able to provide relatively high crystalline quality template for subsequent regrowth of device structures. In this chapter, we demonstrate the use of this method to transfer a III-V device layer structure onto Si, instead of the epitaxial growth of the device structure on the transferred layer serving as a template. This study presents an alternative approach to such device integration on Si and also provides direct evidence of the effects of hydrogen ion implantation-induced damage on the device performance.

5.2 Characterizations of p-i-n photodetector before transfer

An $n$-type InP (100) wafer was used as an initial growth substrate. A $p$-InP (140 nm)/$i$-InGaAs(260 nm)/$n$-InP(150 nm)/InGaAs(300 nm)/InP heterostructure was grown by metal organic chemical vapor deposition (MOCVD), as shown in Figure 5.1(a). The top $p$-InP layer was doped in-situ with Zn to a concentration of $2 \times 10^{18}$ cm$^{-3}$ and the $n$-InP layer was doped with Si to $3 \times 10^{18}$ cm$^{-3}$. The primary purpose of our study is the comparison of the electrical properties of this test device structure before and after layer transfer. The 300 nm-thick undoped InGaAs layer below the $p-i-n$ structure served as an etch-stop layer after layer transfer.
Figure 5.1: Schematic diagram of p-i-n photodiode fabrication before transfer: (a) MOCVD as-grown layer structure; (b) device structure with metal contacts.

*p-i-n* photodiodes were fabricated on the as-grown sample (see Figure 1(b)) as a control sample. The active area for each photodiode was $\sim 0.7 \text{ mm}^2$. Ti(10 nm)/Pd(10 nm)/Au (100nm) $p$-type metal contacts were deposited on the top InP surface. Ti (10nm)/Au (100nm) were deposited on the $n$-InP surface as side $n$-type metal contacts, as shown in Figure 5.2.
Figure 5.2: (a) Digital image on the top view of final device structure of a \( p-i-n \) photodiode fabricated on as-grown sample; (b) Optical microscopic image on a local area, showing the \( p \)-type metal rings on mesa structure.
The diameter of the p-metal rings is 680 µm. Then during the second photolithography, these metal rings were protected by photo resist and the rest area was etched down to the n-InP surface. A common n-type side contact of Ti (10nm)/Au (100nm) was deposited by sputtering at the corner of the sample, as shown in Figure 5.2 (a). The sample was annealed at 350 °C in forming gas for 2 minutes to facilitate the ohmic contacts formation.

I-V curves from the obtained photodiode were presented in Figure 5.2. The current limit was set as 0.01 A during the measurements. The photo current was measured with an infrared light source at a wavelength of 1.55 µm and a power of 2 mw.

Figure 5.3: I-V characteristics of the p-i-n photodiode (a) dark current in both forward and reverse bias regions; (b) dark current (blue line) and photo current (pink line) in the reverse biased region.
The photodiode shows a typical p-n junction behavior in Figure 5.3 (a), with a turn-on voltage of \( \sim 0.85 \) V and a breakdown voltage of \( \sim 3.7 \) V. The breakdown voltage is relatively low since the light absorbing InGaAs layer is only 260 nm thick, much thinner than a standard absorbing layer thickness of \( \sim 1 \) \( \mu \)m [10]. The estimated theoretical breakdown voltage was 5.2 V for the \( p-i-n \) photodiode in this study, assuming the breakdown field for In\(_{0.53}\)Ga\(_{0.47}\)As is \( 2 \times 10^5 \) V/cm [11]. The ideality factor \( n \) was 1.68 obtained from a semi log plot of the forward biased region (see Figure 5.4). The ideality factor is a figure of merit that describes the recombination behavior of the device. A diode governed purely by diffusion current will have \( n=1 \) (ideal diode), while a device dominated by recombination will have \( n=2 \). Recombination occurs at interfaces where opposing charge carriers can meet. Thus, the ideality factor is a manifestation of the
density of interfaces [12]. The ideality factor of 1.68 indicated the presence of considerable interfacial defects in the as-grown sample, which were in agreement with the lattice mismatch detected by the XRD shown in section 5.5.2.

**Figure 5.4:** Semi log plot of the dark current of the as-grown p-i-n photodiode.

**Figure 5.5:** 3-D view of AFM data on as-grown photodiode on InP substrate.
AFM data shown in Fig. 5.5 indicates that the MOCVD as-grown sample had a surface roughness of 0.38 nm, sufficiently flat for subsequent wafer bonding purpose.

5.3 Process flow for the transfer of a p-i-n photodiode

The schematic diagram in Fig. 5.6 shows our process flow for p-i-n photodiodes transfer on Si substrate. The MOCVD as-grown sample was coated with a 65nm-thick SiN\textsubscript{x} film using plasma enhanced chemical vapor deposition (PECVD) to protect the surface during ion implantation.

![Schematic diagram of the process flow for transferring a p-i-n photodiode onto Si](image)

Figure 5.6: Schematic drawing of the process flow for transferring a p-i-n photodiode onto Si, based on ion-cut and selective chemical etching.
H\(^+\) ions were implanted at 160 keV with a dose of \(8.5 \times 10^{16}\) cm\(^{-2}\) at -15 °C. After implantation the protective SiN\(_x\) layer was chemically removed using 1% hydrofluoric acid (HF), and the sample was cleaved into 1 x 1 cm\(^2\) pieces. A piece of implanted heterostructure sample and a piece of Si substrate, which had been coated with a 68 nm-thick thermal SiO\(_2\) layer, were cleaned with organic solutions (TCE, Acetone, and IPA in sequence). The heterostructure sample was then cleaned with 1% HF for 30 seconds. Then both pieces were cleaned with RCA1 solution (\(\text{NH}_4\text{OH}:\text{H}_2\text{O}_2: \text{H}_2\text{O}=1:2:10\)). After an oxygen plasma activation on both pieces for 30 seconds at a power of 150 W, the two pieces were placed in contact at room temperature in air, followed by a thermal anneal at 90 °C for 10 hours under an external applied pressure of 1 MPa to increase the bonding strength. Upon a subsequent annealing at 140 °C, the bonded structure exfoliated around the depth of the projected range of hydrogen in the original InP substrate and resulted in a structure of InP (350 nm)/InGaAs(300 nm) / InP(150 nm)/ InGaAs(260 nm)/ InP(140 nm)/ SiO\(_2\)(68 nm)/ Si substrate. The transferred structure was further annealed up to 650 °C in \(~10\%\) H\(_2\)/N\(_2\) forming gas for 15 minutes, and the top InP and InGaAs layers were selectively etched in sequence, resulting in an InP/InGaAs/InP \(n-i-p\) structure on the SiO\(_2\)/Si substrate.

5.4 Characterizations on \(p-i-n\) photodiode after implantation and transfer

To ascertain the effect of hydrogen ion implantation damage on device performance, \(p-i-n\) photodiodes were fabricated directly on the \(H^+\) as-implanted sample (see Figure 5.6(b)) using identical fabrication process as on the as-grown sample.
The I-V characteristic is shown in Figure 5.7. It is obvious that after hydrogen implantation, the p-i-n photodiodes exhibited a short-circuit element-like I-V behavior. Since at this as-implanted stage before any annealing steps, all hydrogen ions were inside the sample and all the implantation induced radiation damage was also in the sample. The presence of the high-density defects in the implanted sample enabled carrier hopping [13] through the whole p-i-n structure, resulting in a resistor-like behavior. This hopping effect will be further discussed in next section of this chapter.

**Figure 5.7:** I-V characteristics of the p-i-n photodiode made on as-implanted sample.

Figure 5.8 shows the top view of final device structure based on the transferred and etched device structure that went through annealing up to 650 °C. n-type metal contact of Ti/Au was first deposited on the transferred and etched n-InP.

After further patterned mesa etching, the p-type metal contact was deposited at the corner of the p-InP surface, as shown in Figure 5.8(b). It was difficult to make metal
contacts on the $p$-InP layer in the transferred structure due to the high resistance, thus Zn(50nm)/Au(150nm) was used to reduce the contact resistance on the p-InP surface. No surface degradations like surface bubbles were observed after all the processing steps. The “SiNx protecting layer” and the “external pressure” as described in Section 4.2 also played a crucial role in the device transfer process that effectively suppressed the temperature-dependent bubble formation.

The I-V characteristics of the final p-i-n photodiodes on Si are shown in Figure 5.9. Compared with the as-grown photodiode (Figure 5.3 (a)), the forward biased current
was higher in the low bias region (<1v) and lower in the high bias region (>1v). The breakdown behavior was not as sharp as in the as-grown sample.

![Graph showing current-voltage characteristics of a photodiode.](image)

**Figure 5.9:** I-V characteristics of the p-i-n photodiode fabricated on the final transferred and etched sample: (a) dark current in both forward and reverse bias regions; (b) dark current (blue line) and photo current (pink line) in the reverse biased region.

The dark current was ~ 1.5 orders higher than the as-grown sample and the photo current was comparable to the as-grown sample (Figure 5.3 (b)). The photo current is now a function of the applied field. The ideality factor n was extracted from a semi log
plot (not shown here) of Figure 5.9 (a) to be 1.84, larger than the n value (1.68) before implantation. This is reasonable since the implantation created more recombination sites for the carriers.

5.5 Effect of ion implantation damage on device performance

5.5.1 Effect of ion implantation on electrical properties

The change in the measured I-V characteristics after implantation and transfer was examined using differential Hall effect measurements based on the van der Pauw method [14]. For comparison, carrier concentration and mobility for the corresponding layers in the as-grown sample were estimated based on calibration growth runs and are listed in Table 5.1.

**Table 5.1:** Hall measurements on p-i-n structures after transfer

<table>
<thead>
<tr>
<th>Layer</th>
<th>Thickness (nm)</th>
<th>Carrier Concentration (cm⁻³)</th>
<th>Mobility μ (cm²/V·s)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>Transferred and annealed at 650 °C</td>
<td>As-grown</td>
</tr>
<tr>
<td>n-InP</td>
<td>150</td>
<td>2.2e18 ~ 3e18*</td>
<td>1100 ~ 1800*</td>
</tr>
<tr>
<td>i-InGaAs</td>
<td>260</td>
<td>5.8e16 ~ 2e16*</td>
<td>4130 ~ 9000*</td>
</tr>
<tr>
<td>p-InP</td>
<td>140</td>
<td>2.8e16 ~ 2e18*</td>
<td>105 ~ 80*</td>
</tr>
</tbody>
</table>

(* Estimated values based on calibration growth runs.)

After the layer transfer and annealing at 650 °C, the carrier concentration for the n-InP layer and the undoped InGaAs layer recovered to similar levels as for the as-grown layers, while the mobilities for these two layers were still lower than for the as-grown samples. The hole concentration of the Zn-doped p-InP layer dropped significantly from ~ 2 ×10¹⁸ cm⁻³ to 2.8 ×10¹⁶ cm⁻³. The out-diffusion of the dopant zinc at elevated
temperatures may cause difficulties on the recovery of hole concentration in the \( p \)-InP layer. For the annealing at 650 °C for 15 min used in this study, the zinc diffusion length was estimated to be a few µms, based on the equation \( L = \sqrt{4Dt} \), where \( t \) is the diffusion time and the diffusion coefficient \( D \) was taken as \( D = 4.9 \times 10^{-2} \exp (-1.52 \text{ eV}/k_B T) \text{ cm}^2/\text{sec} \) for zinc in InP [15]. By assuming a Gaussian diffusion profile, the remaining zinc dopant concentration in the \( p \)-InP layer is expected to be \( \sim 1 \times 10^{17} \text{ cm}^{-3} \), much higher than the measured value \( (2.8 \times 10^{16} \text{ cm}^{-3}) \). Therefore, ion damage, in addition to the zinc diffusion, is considered to have a significant effect on the electrical properties of the transferred layers.

The passivation of acceptors and donors in InP by atomic hydrogen has been widely reported [16-18]. In particular, the passivation effect of hydrogen on acceptors such as zinc is much more significant than on donors [17-18]. For example, the hole concentration dropped by 4 orders after a hydrogen plasma diffusion over a depth of 1.3 µm at 250 °C, while the electron concentration in another sample was only very weakly affected after the same diffusion process [16]. It has been suggested that hydrogen acts as a deep-level donor in InP substrate as it is in Si [17]. The hydrogen passivated \( p \)-InP layer started to recover the carrier concentration upon annealing at a typical temperature of \( \sim 350 \) °C [16], and it has been reported that hydrogen atoms completely leave the substrate at a temperature \( \sim 600 \) °C thus the passivation effect is almost completely removed [18].

However, in our case, after annealing at 650 °C, the \( p \)-InP layer still had a low hole concentration as \( 2.8 \times 10^{16} \text{ cm}^{-3} \), \( \sim 2 \) orders lower than in the as-grown sample.
Therefore it is likely that the hydrogen passivation of acceptors was not the main reason that caused the degradation of electrical property of p-InP layer. The major difference of our ion-cut process from those hydrogen plasma diffusion experiments is the method by which hydrogen atoms are introduced into the InP substrate. Instead of the hydrogen diffusion process used in those passivation studies [16-17], hydrogen ion implantation at relatively high energy and with relatively high dose was used in this study to induce the layer exfoliation. Thus the damage profile created by the implantation was much more significant than by the diffusion process.

The degradation of the electrical properties due to the damage induced by hydrogen implantation in InP has been demonstrated in the literature [13, 19,20] and also by this group [21, 22]. The antisite defects (In\textsubscript{P} and P\textsubscript{In}) and related defect complexes created in the replacement collisions are believed to act as the deep level carrier trapping centers, where In\textsubscript{P} is responsible for electron trapping and P\textsubscript{In} for the hole trapping [19, 20, 23].

For the hydrogen as-implanted sample without any annealing, the defect density is so high that these defect sites are spaced closely enough to allow electrons to hop from site to site, known as hopping. The hopping conduction mechanism has been reported to explain the resistivity evolution with annealing temperatures [13]. As a result of the defect-assisted hopping, a short circuit behavior was observed on the photodiode fabricated on the as-implanted sample, as shown in Figure.5.7.

The finished photodiodes on Si substrate, upon completion of all the processing steps had the heavily-damaged regions etched away from the top of the transferred structure. After thermal annealing, the defect density dropped significantly, leading to a
reduction in electrical conductivity. The carrier concentration in the \( n \)-InP and \( i \)-InGaAs layers recovered to a level similar to that of the as-grown sample. There was still considerable implantation damage, however, in the \( p \)-InP layer, that could not be removed by annealing at 650 °C. This agrees with the reported results that the \( P_{\text{In}} \) defects in \( p \)-InP are more difficult to be removed compared to \( In_p \) in \( n \)-InP [17]. These defect residues, mostly \( P_{\text{In}} \), act as deep-level donors in \( p \)-InP that compensate the original carrier concentration.\(^{16}\) The increase of resistivity in the \( p \)-InP layer also agrees with the observation that the forward current of the transferred sample was low in the high forward bias region where the layer series resistance dominates. The transferred sample showed a higher current than the as-grown sample at low forward bias voltage due to trap-assisted recombination. These observations suggest that the recovery of the implantation-induced damage determines to a large extent the performance of minority carrier devices.

Based on the discussions above, the hydrogen implantation in the ion-cut process significantly affects the electrical properties of the device layers, due to the implantation induced damage. The damage can not be easily removed even with annealing at 650 °C thus the electrical properties of implanted layers could not be fully recovered, especially for the \( p \)-InP layer.

### 5.5.2 Effect of ion implantation on strain

Similar to the use of double crystal X-ray diffraction (XRD) in chapters 3 and 4, XRD in (004) double axis \( \omega/2\theta \) scan mode was used to characterize the strain involved in the device transfer process, as shown in Figure 5.10 at log scale. The (004) diffraction
peak from (100) InP substrate in the as-grown sample was used as a reference point.

The InGaAs layer in the as-grown sample had a lattice mismatch of \(~200\) arcseconds (Fig.5.10(a)). After hydrogen implantation, a series of peaks was observed to the left of InP substrate diffraction peak with the maximum strain of \(~2100\) arcseconds. The point defects with a Gaussian-like distribution generated significant out-of-plane tensile strain (in-plane compressive stress) and contributed to a series of interference diffraction peaks as shown in Figure 5.10(b) [13, 24]. The presence of abundant point defects indicated by XRD data was in agreement with the hopping effect caused by high density point defects as discussed in last section. After the layer transfer process and annealing up to \(400\) °C, the transferred layers had much less out-of-plane strain compared to the as-implanted sample. Upon subsequent annealing at \(650\) °C and selective etching, the strain further reduced. The full width half maximum (FWHM) of the diffraction peak dropped from \(~475\) arcseconds (Figure 5.10(c)) to \(~260\) arcseconds (Figure 5.10(d)). There may be still substantial defects left in the transferred layers that affect the electrical properties of the layers.
Figure 5.10: X-ray diffraction data from: (a) as-grown p-i-n on InP sub; (b) H\(^+\) as-implanted sample; (c) transferred sample with annealing to 400 °C before etching; (d) further annealed to 650 °C then etched down to the final structure of n-InP/i-InGaAs/p-InP/SiO\(_2\)/Si sub.

5.6 Conclusion

In summary, InP/InGaAs/InP p-i-n photodiodes, initially grown on an InP substrate, was transferred onto a SiO\(_2\)/Si substrate using the combination of ion-cut and
selective etching. This study demonstrates the feasibility of this process and its initial application to the formation of functioning minority carrier devices on Si using the ion-cut process. Much of the implantation damage in both the $n$-type and undoped layers was removed by annealing at 650 °C combined with selective etch after transfer. The $p$-InP did not recover to as large an extent as the $n$-InP as reflected in the measured current-voltage characteristics. Further improvement of the device performance may be achieved by annealing at higher temperatures under pressure. It is expected that this transfer process would be applied to majority carrier devices as well, such as $n$-channel InP devices, since they are less sensitive to implantation damage.
Reference


6.1 Summary of this dissertation

In this dissertation research, the integration of III-V materials with Si based on the process of ion-cut has been demonstrated. Relatively high crystalline quality InP based III-V materials have been transferred onto Si substrates coated with a thin SiO$_2$ layer. Both fundamental physics behind ion-cutting of III-V materials and novel approaches for III-V device integration with Si for optoelectronic integrated circuits (OEIC) applications have been presented. The most important points are listed as below:

(1) The effects of hydrogen implantation conditions (temperature, dose rate, and energy) on the III-V ion-cut process were investigated. It was found that both the point defects induced by the hydrogen implantation and the in-plane compressive stress are necessary for hydrogen trapping and H-platelet nucleation and growth. Thus it is necessary to keep the implantation temperature at a relatively low level, for example, no more than room temperature in our case. An empirical formula based on the Morehead-Crowder model was used to rationalize the implantation condition dependence and predict a critical implantation temperature ($T_c$) above which hydrogen implantation would not cause surface blistering or layer exfoliation. Based on the understandings on the effects of hydrogen implantation conditions on the ion-cut process, appropriate hydrogen implantation conditions have been established to induce InP surface blistering or layer transfer.
(2) A new layer transfer approach that combines conventional ion-cutting and selective chemical etching for InP-based III-V layer transfer has been demonstrated. This layer transfer scheme takes advantage of the ion-cut process by conserving III-V substrates for reuse, and simultaneously improving the transferred layer quality and surface condition without using chemical and mechanical polishing. InP/SiO$_2$/Si structure was obtained with a relatively high crystalline quality InP layer that had less radiation damage and smoother surface, compared with the transferred layers obtained by conventional ion-cut.

(3) The feasibility of using our transferred InP/SiO$_2$/Si as a template for subsequent epitaxial regrowth of III-V layers has been demonstrated. As a common problem, surface bubbles often appear on the surface of the transferred structure when the sample is heated up to the typical growth temperature of ~ 600 °C. These temperature-dependent bubbles significantly degrade the transferred film quality. In this study, hydrocarbon contaminations and vapor pressure from the mixture of In and P hydrides and hydroxides at the bonding interface were found to cause the bubble issue. The “SiNx protecting layer” and the “external pressure” method developed in our process can effectively suppress the surface bubble formation and enable the transferred structures survive at 650 °C for regrowth without any surface degradation. An InP epitaxial layer was then grown on the InP/SiO$_2$/Si structure with only a slight increase on the FWHM of the XRD diffraction peak. Various chemical cleaning processes on the transferred and etched sample immediately before regrowth of InP were conducted and cleaning with 1% HF resulted in a clean and smooth surface for InP regrowth.

(4) For the first time to the best of our knowledge, the transfer of a pre-fabricated
optoelectronic device using ion-cutting and selective etching has been demonstrated. An InP/InGaAs/InP $p$-$i$-$n$ photodiode initially grown on InP substrate was transferred onto a SiO$_2$/Si substrate using the combination of ion-cutting and selective etching that was developed in our study. Using this method, the III-V photodiodes were integrated with Si substrate without any regrowth. This study demonstrates the feasibility of this process and its initial application to the formation of functioning minority carrier devices on Si using the ion-cut process. Much of the implantation damage in both the $n$-type and undoped layers was removed by annealing at 650 °C combined with selective etch after transfer. The $p$-InP did not recover to as large an extent as the $n$-InP as reflected in the measured current-voltage characteristics.

6.2 Future work

Based on the results obtained in this dissertation, there are a few interesting points that may be further explored, including:

(1) The effects of hydrogen implantation conditions on the ion-cut process of III-V materials are very important that significantly affect the success of the layer transfer of III-V materials. InP was the only III-V materials that was studied in this study. It would be interesting and also meaningful to study the effects of hydrogen implantation conditions on the surface blistering and exfoliation of other III-V or group IV materials, such as GaAs, InAs, and Ge. This will enable more controllable ion-cut processes for more materials.

(2) Due to the limitation of the wafer bonding capacity, only relatively small pieces (typically 1cm by 1cm) were used in this study for layer transfer. Due to the
imperfection of the wafer bonding and subsequent etching process after transfer, even
smaller area was obtained for the regrowth study or device fabrication, making the
studies after transfer rather difficult. It would be more efficient if full-scale wafer
bonding can be achieved. This will benefit all the following processing, especially for
the applications of using transferred structure as growth templates.

(3) A $p$-$i$-$n$ photodiode was chose as the first demonstration of a device transfer
using ion-cut based approach. It was observed that this minority carrier device suffered
from the hydrogen implantation damage after transfer and the annealing up to 650 °C
could not completely remove the effect of implant damage. It would be interesting to
explore the possibilities of transferring other types of devices, for example, majority
carrier devices such as a MESFET. Majority carrier devices are probably not as sensitive
to the implantation damage as minority carrier devices. The ion-cut process has a wide
range of potential applications on materials and devices transfer and integration.