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Direct growth of single-crystalline III–V semiconductors on amorphous substrates

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The III–V compound semiconductors exhibit superb electronic and optoelectronic properties. Traditionally, closely lattice-matched epitaxial substrates have been required for the growth of high-quality single-crystal III–V thin films and patterned microstructures. To remove this materials constraint, here we introduce a growth mode that enables direct writing of single-crystalline III–V’s on amorphous substrates, thus further expanding their utility for various applications. The process utilizes templated liquid-phase crystal growth that results in user-tunable, patterned micro and nanostructures of single-crystalline III–V’s of up to tens of micrometres in lateral dimensions. InP is chosen as a model material system owing to its technological importance. The patterned InP single crystals are configured as high-performance transistors and photodetectors directly on amorphous SiO2 growth substrates, with performance matching state-of-the-art epitaxially grown devices. The work presents an important advance towards universal integration of III–V’s on application-specific substrates by direct growth.
Owing to their high-electron mobilities and direct band gaps, III–V compound semiconductors are ideal for many electronic and optoelectronic applications such as high-performance transistors, photovoltaics, and photodetectors. The development of epitaxial growth techniques such as molecular beam epitaxy, metal-organic chemical vapour deposition (MOCVD) and pulsed laser deposition have enabled the growth of single-crystalline III–V thin films with excellent performance for device applications. In order to obtain such high-quality single-crystalline thin films, the growth must be done on a closely lattice-matched substrate. The growth of single crystals onto amorphous substrates would further enable new applications, such as providing a simplified pathway for heterogeneous integration of III–V devices onto application-specific substrates. However, deterministic synthesis of single-crystalline semiconductors on amorphous substrates presents a fundamental challenge in the field of materials science—one that arises from the thermodynamics and kinetics of nucleation and crystal growth. Specifically, the slow kinetics governing coalescence of two grains into a single grain dictates that any single-crystalline structure on an amorphous substrate must be grown from a single nucleus. Thus, for single-crystalline growth, the first nucleus that forms must grow to fill the desired volume before another nucleus is formed. Within most growth approaches, the relative nucleation and growth rates are difficult to control, and the maximum grain size attainable is often on the order of the material thickness, resulting in nanocrystalline structures for nanoscale thickness materials.

Because of the tremendous technology-driven need for single-crystalline semiconductors on amorphous substrates, a number of synthesis techniques have been explored in recent years. These approaches include (i) epitaxial growth of thin films on single-crystalline substrates followed by selective layer transfer to a desired substrate, (ii) vapour–liquid–solid, (iii) vapour–solid or aerosol-based nanowire growth. For GaN, in particular, the usage of ‘pre-orienting’ layers to conduct local hetero-epitaxy has also been demonstrated. While such approaches have resulted in broadening the scope and functionality of various electronic materials with unique properties, direct growth of single-crystalline semiconductors with ‘user-defined’ geometries and dimensions on amorphous substrates has yet to be demonstrated. Such an approach would offer major advantages in terms of compatibility with traditional device processing technology, scalability and processing cost. In addition, it would provide a direct pathway to three-dimensional integration of electronic materials and devices with appreciable levels of complexity.

Here, we introduce templated liquid-phase (TLP) crystal growth (Fig. 1a) as a synthetic approach for growth of high-performance, nano- and micro-scale single-crystalline compound semiconductors with user-defined geometries on arbitrary substrates. Indium phosphide is chosen as a model III–V material system owing to its importance in a wide variety of fields, from high-speed electronics to lasers and photovoltaics. Thermally grown SiO$_2$ and glass are selected as examples of amorphous materials on which TLP crystal growth can be performed.

**Results**

**TLP growth and crystal quality.** For TLP growth of InP, indium metal is first lithographically patterned onto a Si/SiO$_2$ or glass substrate with a thin (1–10 nm) MoO$_x$ nucleation layer, and subsequently encapsulated by evaporated SiO$_x$ (Supplementary Fig. 1). Growth is carried out in a low-pressure furnace at 500–535 °C in the presence of phosphine (PH$_3$) and H$_2$. At the growth temperature, In is transformed into the liquid phase, but remains mechanically confined by the SiO$_x$ template.

**Figure 1 | Growth mechanism of single-crystalline InP.** (a) Schematic of the process flow for TLP crystal growth. (b) SEM images of an array of 7 μm InP circles and (c) their corresponding EBSD maps. Scale bar, 10 μm. (d) The average number of grains per circle, measured via EBSD versus the circle diameter, showing a quadratic dependence. (e) TEM cross-sectional image of a portion of a patterned InP thin film showing the well-defined InP lattice on top of a MoO$_x$/MoP$_x$ layer on amorphous SiO$_2$. Scale bar, 5 nm.
Phosphorous diffuses through the SiOₓ cap, and supersaturates the liquid In, precipitating out in the form of an InP nucleus. The key feature of this growth mode is that a phosphorous depletion zone forms around each growing nucleus, preventing further nucleation. Previously, we have shown that for continuous In thin films, this depletion zone can be on the order of hundreds of µm, leading to ultra-large grain sizes²⁻⁴. Here, we show that through pre-patternning the indium in mechanically confined templates such that the phosphorous depletion zone from the first nucleus occupies the entire template, ‘single crystalline’ InP growth in user-defined geometries can be achieved.

Scanning electron microscope (SEM) images of the InP crystal arrays shaped into circles, rings and squares grown via TLP crystal growth are shown in Fig. 1b and Supplementary Fig. 2. Critically, the original In layout geometry is maintained after growth, allowing for deterministic shape control of InP crystals. The stoichiometry of the films is confirmed by electron dispersive spectroscopy (EDS) to be 1:1 In:P. X-ray diffraction spectroscopy on an array of InP circles (Supplementary Fig. 3) displays only peaks corresponding to zincblende InP, indicating that all of the In has converted to InP. The crystallinity of the InP patterns with lateral dimensions of ~5–7 µm is confirmed via electron backscatter diffraction (EBSD) mapping, showing that excluding twinning, each individual pattern is a single crystal but with different crystal orientations (Fig. 1c, Supplementary Fig. 2, Methods section, Supplementary Note 1). In addition, from the orientation distribution obtained from EBSD, it can be seen that there is a preferential texturing of the growth in the (1 0 1) direction, where n ranges between 1 and 2 (Supplementary Fig. 4).

To study the effect of growth conditions and InP feature size on the number of grains, InP circles with diameters varying from 3 to 20 µm were patterned using TLP crystal growth at two different PH₃ partial pressures. From Fig. 1d and Supplementary Fig. 5, it can be seen that the number of grains per circle increases according to a quadratic relation with the circle diameter, d, which can be fit by the equation:

\[ N_{\text{grains}} = 1 + \beta d^2 \]  \hfill (1)

\( N_{\text{grains}} \) is the average number of grains per circle and \( \beta \) is a proportionality factor that takes into account growth parameters such as P flux, the geometry associated with nucleation and the resulting average nucleation rate (Supplementary Fig. 6, Supplementary Note 2). As expected from our model, there is also a strong dependence of the number of grains on the PH₃ partial pressure. As the PH₃ partial pressure is lowered, the P flux into the liquid decreases, resulting in a reduced nucleation rate and larger P depletion zones (Supplementary Note 2). This is reflected in a drop in \( \beta \) from \( 3 \times 10^{-3} \) to \( 4 \times 10^{-4} \) as the PH₃ partial pressure is reduced from 1 to 0.1 Torr, allowing the average number of grains per feature to be maintained at near unity even for diameters as large as 20 µm.

Transmission electron microscopy (TEM) was used to examine the crystallinity of the InP patterns. From the cross-sectional TEM image of an InP sample shown in Fig. 1e, it can be seen that a crystalline InP lattice sits on top of the amorphous SiO₂ substrate with a thin MoOₓ/MoPx nucleation layer in between, clearly showing the non-epitaxial nature of TLP crystal growth. To demonstrate the versatility of the TLP crystal growth technique, the world’s smallest version of the ‘Lorem Ipsum’ placeholder text is written in crystalline InP lettering with a stroke width of 150 nm (Fig. 2a). In addition, a single-crystalline Berkeley ‘Cal’ logo with dimensions of 80 × 60 µm is shown in Fig. 2b with its structural, compositional and optoelectronic properties characterized via EBSD, EDS mapping and photoluminescence imaging (Fig. 2c, Supplementary Fig. 7), respectively. While letters are used for demonstration purposes,
the geometric degrees of freedom available to grow single-crystalline materials with TLP crystal growth are of great significance for the fabrication of practical electronic and photonic devices.

One major advantage of TLP crystal growth is ease of scalability. Unlike traditional III–V growth where both group III and V elements are introduced in the vapour phase, only the group V element is in the vapour phase, and the geometry is fixed by the template. This allows for simple reactor designs which can be easily scaled up to large scales. Furthermore, as growth only occurs when both group III and group V elements are present, the templates essentially provide a self-limiting growth mechanism, preventing unwanted thickness or compositional variation across a wafer. As a demonstration, Fig. 2d–f shows optical images as well as a corresponding photoluminescence image of arrays of InP circles outlined by InP bars, grown across a full 4-inch Si/SiO₂ wafer using a simple cold-wall furnace.

The relatively low temperature required for TLP crystal growth also allows for a broad range of substrates upon which single-crystalline III–V's can be grown. As an example, InP circles were directly written onto a borosilicate glass slide (Fig. 2g) and their optical quality was verified via photoluminescence imaging (Supplementary Fig. 8). In addition, the grown InP can be fully transferred onto plastic substrates for applications where a flexible substrate is desired. As an example, Fig. 2h and Supplementary Fig. 9, show an optical image and the corresponding photoluminescence image, respectively, of the InP circle arrays transferred onto a polyethylene terephthalate (PET) substrate using polymeric acid²⁶.

A unique feature of the TLP crystal growth process is that complex 3D architectures can be achieved, beyond the limits of traditional processes. For instance, multilayers of InP single crystals separated by amorphous SiO₂ layers can be grown in one cycle by starting with substrates consisting of multilayer In/SiO₂ layers, as demonstrated in the cross-sectional SEM image in Fig. 2i. This can have broad implications for future design of monolithic 3D electronics.

**In situ doping.** A critical component of semiconductor growth is the ability to tune the optical and electrical properties; in particular, the doping concentration. To explore this capability, GeH₄ gas was introduced into the growth chamber during growth to achieve controlled in situ n-type Ge doping of InP. Figure 3a shows the normalized photoluminescence spectra of InP single crystals grown under different partial pressures of GeH₄. Significant blue-shifting of the photoluminescence spectra versus a lightly doped reference wafer (Supplementary Fig. 10) is observed as the GeH₄ partial pressure is increased (see Methods section). The electron concentrations, approximated from the photoluminescence peak energies, are plotted versus the GeH₄ partial pressure in Fig. 3b indicating that TLP grown InP can be doped up to a degenerate level near the upper limit of electron doping in InP³⁰. From the photoluminescence spectra, the Urbach tail parameter is also extracted and plotted versus the carrier concentration level in Fig. 3c (ref. 31). The Urbach tail parameter is an important figure of merit regarding the band edge sharpness arising from crystal defects, thermal vibrations and charged impurities³²,³³. As can be seen, the Urbach tails of our non-epitaxial TLP grown samples are similar to the values reported in literature for InP single crystal wafers at various respective levels of doping³⁴,³⁵.

**Electronic characterization.** The electronic quality and practical utility of TLP-growth InP in the shape of microwires (µWires) were explored by fabricating long-channel Schottky n-type metal-oxide-semiconductor field effect transistors (MOSFETs) with top gates (Fig. 4a–c). The transfer and output characteristics of an InP transistor on a Si/SiO₂ substrate with a gate length of 3 µm and body thickness of ~125 nm are shown in Fig. 4d,e, respectively. The device exhibits an ON-current of 120 µA µm⁻¹ at VGS = VTS = 2 V with an ON/OFF current ratio of ~10⁵ and peak extrinsic transconductance of 100 S µm⁻¹, which is excellent for a long-channel device. An effective electron mobility of μ = 675 cm² V⁻¹ s⁻¹ is extracted from device simulations (see Methods section), which compares favourably with unpassivated InP nanowire/microwire MOSFETs in literature⁹, illustrating the excellent electronic quality of the InP grown here. In addition, top-gated InP photo-MOSFETs were also fabricated on Si/SiO₂ substrates using the device structure above except that a transparent indium tin oxide (ITO) gate electrode is used with a channel length of L₀ = 20 µm. The device electrical characteristics were measured under dark and under steady-state illumination from a bandpass filtered white light source with an optical intensity of 15.6 mW cm⁻². The device exhibits a strong photoresponse (Fig. 4f) with a peak responsivity of ~700 A W⁻¹ at VGS = 3.4 V (Fig. 4g). Furthermore, the specific

![Figure 3](image-url)
detectivity (D*) of this device displays a maximum of \(8.4 \times 10^{11}\) Jones at room temperature, comparable to state-of-the-art single-crystalline epitaxial InGaAs detectors.¹⁴

**Discussion**

In conclusion, we have demonstrated a technique that enables direct ‘writing’ of optoelectronic-quality single-crystalline III–V semiconductors on amorphous substrates. The elimination of the requirement for lattice-matched substrates as well as the improved scalability of this growth mode enables ubiquitous integration of III–V semiconductors for a wide range of applications on user-defined substrates. While InP was used as a model growth system in this work, the TLP crystal growth method is one that, from a thermodynamic and kinetic point of view, is expected to be applicable to other technologically important III–V’s. As an example, proof of concept demonstrations using the TLP process to grow GaP and InSb are shown in Supplementary Fig. 11. In addition, single crystals grown via the TLP growth process may potentially be utilized as a virtual substrate in epitaxial growth processes, allowing for the realization of high-quality semiconductor heterostructures grown directly onto amorphous substrates. Future work on control of crystal orientation of individual patterns may further extend the tunability of the TLP growth mode, for instance, by making nucleation of a specific orientation thermodynamically favourable through surface engineering of the nucleation layer or via the introduction of geometric constraints using principles from graphoepitaxy.¹²

**Methods**

**Patterning and growth of InP.** First, a clean Si wafer with a 50-nm thick thermal oxide was lithographically patterned with the desired InP shape (Supplementary Fig. 1a). For the glass sample in Fig. 2g, a borosilicate glass slide was patterned instead. A thin 1–10 nm thick MoO₃ layer was evaporated (Supplementary Fig. 1b) followed by evaporation of In of the desired thickness and a 10–100 nm thick SiOₓ layer (Supplementary Fig. 1c). As SiOₓ has a high surface energy for nucleation, the MoO₃ layer helps to promote nucleation of the InP. To obtain a smooth In film, the evaporation of the In and SiOₓ bilayer was done with the substrate chuck cooled to \(<150\) K using liquid N₂. The whole MoO₃/In/SiOₓ stack was then lifted off (Supplementary Fig. 1d). After liftoff, angled evaporation was utilized to coat the exposed side regions of the In with SiOₓ, with thicknesses ranging from 4 to 50 nm (Supplementary Fig. 1e,f). During the growth, the SiOₓ template confines the liquid In so that the resulting InP crystal has the same shape as that of the original In pattern. Growth of the InP patterns for EBSD crystal analysis and transistors were carried out in a hot-wall CVD tube furnace. In all, 10% PH₃ in H₂ was used as the phosphorous source and was further diluted to the desired dilution. Growth of the 4-inch wafer, sample on glass and doping-dependent studies were done in a cold-wall CVD system. In all, 10% GeH₄ in H₂ was used as the Ge dopant source. The samples were grown for 10–20 min at pressures of 100–300 Torr (partial PH₃ pressure of 0.1–10 Torr) and growth temperatures ranging between 500 and 535 °C.

**EBSD characterization.** EBSD characterization was carried out in an FEI Quanta SEM with an Oxford Instruments EBSD detector. Analysis of the maps were done by the Oxford Aztec and Tango software programs. Orientation maps were generated and plotted using the inverse pole figure colour scheme. Twin boundary removal was done by ignoring the \(<111>\) 60° rotational boundaries within the crystals and plotting the surface orientation of each grain.

**Photoluminescence spectra and imaging.** Photoluminescence spectra were taken by a HORIBA LabRAM HR800 tool with a 532 nm excitation wavelength. For photoluminescence imaging, a red LED was used as the excitation light source and images were taken by an Andor silicon CCD camera through an optical microscope with a GaAs wafer used to filter out the irradiation wavelengths.

**Electron concentration extraction.** The electron concentration, \(n\), can be approximated using the equation:²⁶

\[
n = 10^{19} \left( \frac{\Delta E \ m}{16.9 m_0} \right)^{1/2}
\]

where \(\Delta E\) is the shift of the photoluminescence peak energy from an undoped reference (1.34 eV taken from a \(5 \times 10^{13}\) cm⁻³ doped reference wafer, Supplementary Fig. 10) and \(m/m_0\) is the ratio of the effective electron mass of InP to the free electron mass.
Urbach tail fitting. The absorption at the band edge, is related to the photoluminescence spectra by the van Roosbroek-Schockley equation by

\[ P(\nu) \propto (e^{\nu/kT} - 1)^{-3/2} \]

where \( P(\nu) \) is the photoluminescence intensity as a function of frequency \( \nu \), \( k \) is Planck’s constant, and \( T \) is the thermal energy (25.6 mV at room temperature). \( E_0 \), the slope at the absorption band edge, is the Urbach tail parameter, which describes the sharpness at the band edge and is a good indicator of crystal and optoelectronic quality.

Device fabrication. InP microwires with dimensions of 1 × 50 µm and thickness of 125 nm were grown using TLP crystal growth as described above. Photolithography was used to lithographically define the source/drain contacts followed by evaporation of 310/40 nm of Ge/Al/In and liftoff. The source/drain contacts were subsequently annealed at 375 °C for 5 min to allow the Ge with InP in the contact regions to improve contact resistance. In all, 10 nm of ZrO2 was then deposited via atomic layer deposition at a temperature of 200 °C. Finally, photolithography was used once again to define the gate electrode. For the insight on material film for the final photo-MOSFETs, 30 nm of ITO was deposited via sputtering instead to allow optical access to the channel.

Sentaurus simulations. Detailed semi-classical drift-diffusion simulations were carried out utilizing the Sentaurus Device simulator to accurately model the device performance. The parameter extraction was carried out by first matching the subthreshold region (−0.2 V < VGS < 0.15 V) utilizing 30 nm of Ge/Al/In and liftoff. The source/drain interface traps and gate work function as the fitting parameters and performing a least squares error fit, enabling accurate simulation of the mobile charge versus gate voltage. The mobility and series resistance of the device were extracted by squares error fit, enabling accurate simulation of the mobile charge versus gate voltage. The mobility and series resistance of the device were extracted by minimizing the least squares error for all the Ids-Vgs curves (0 V < Vgs < 2 V) for Vds = 0.4, 0.8, 1.2, 1.6 and 2 V simultaneously.

References

Additional information
Supplementary Information accompanies this paper at http://www.nature.com/naturecommunications
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Author contributions

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