High efficiency linear envelope tracking and envelope elimination and restoration power amplifier for WLAN OFDM applications

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Publication Date
2006-01-01

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High Efficiency Linear Envelope Tracking and Envelope Elimination and Restoration Power Amplifier for WLAN OFDM Applications

A dissertation submitted in partial satisfaction of the requirements for the degree Doctor of Philosophy in Electrical Engineering (Electronic Circuits & Systems)

by

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2006
The Dissertation of Feipeng Wang is approved, and it is acceptable in quality and form for publication on microfilm:

Chair

University of California, San Diego

2006
To my parents, brother, and wife.
# Table of Contents

**Signature Page** .......................................................................................................................... III

**Dedication** ................................................................................................................................. IV

**Table of Contents** ....................................................................................................................... VI

**List of Figures** ............................................................................................................................. VIII

**List of Tables** ............................................................................................................................... XVI

**Acknowledgements** .................................................................................................................. XVII

**Vita, Publications and Fields of Study** ..................................................................................... XXII

**Abstract** ....................................................................................................................................... XXIV

**Chapter 1 Introduction** ............................................................................................................... 1
  1.1 Motivations ................................................................................................................................. 3
    1.1.1 PA Trade-off on Efficiency and Linearity ........................................................................ 3
    1.1.2 WLAN OFDM Signal ...................................................................................................... 6
  1.2 PA Efficiency Enhancements for High PAR Signals ........................................................ 9
    1.2.1 Linearization Techniques ............................................................................................... 9
    1.2.2 Efficiency Enhancement Techniques .......................................................................... 10
  1.3 Dissertation Objectives and Organization ............................................................................ 11

**Chapter 2 Envelope Tracking and Envelope Elimination and Restoration Power Amplifier Architectures for Wideband WLAN OFDM Applications** ................................................................................................. 13
  2.1 Traditional ET and EER Power Amplifier Architectures .............................................. 13
  2.2 Hybrid EER Power Amplifier ............................................................................................ 16
  2.3 A Wideband ET Power Amplifier for WLAN 802.11g Applications ....................... 19
    2.3.1 Class B RF PA Design ................................................................................................. 20
    2.3.2 Envelope Amplifier Design ......................................................................................... 22
    2.3.3 ET Power Amplifier Design ....................................................................................... 22
2.3.4 Baseband Digital Pre-distortion for WLAN ET System ................. 26
2.3.5 Measurements ................................................................................. 29
2.4 A Hybrid EER Power Amplifier for WLAN 802.11g Applications ....... 33
2.5 Summary ............................................................................................. 38

CHAPTER 3 ENVELOPE TRACKING AND ENVELOPE ELIMINATION AND
RESORATION PAS TIME ALIGNMENT ALGORTIHMA ........................................ 40
3.1 Time Mismatch Analysis .................................................................... 40
  3.1.1 Cann Model .................................................................................. 40
  3.1.2 Time Mismatch Analysis ................................................................. 43
3.2 Adaptive Time Alignment Algorithm ................................................. 55
3.3 Measurements ..................................................................................... 63
3.4 Summary ............................................................................................. 66

CHAPTER 4 WIDEBAND HIGH EFFICIENCY ENVELOPE DESIGN .................. 67
4.1 Envelope Signal Power Spectrum Characteristics .............................. 69
4.2 Principle of High Efficiency Wideband Envelope Amplifier Operation .... 70
  4.2.1 Case I: Linear Operation for Small-Signal Envelops ....................... 75
  4.2.2 Case II: Nonlinear Operation for Large-Signal Envelopes ............... 82
  4.2.3 Case III: The Transition from Small-Signal Linear Operation to Large-
           Signal Nonlinear Operation ............................................................. 85
4.3 Design of the Envelope Amplifier for an OFDM 802.11g Signal ............. 88
4.4 Envelope Amplifier Efficiency Analysis .............................................. 93
  4.4.1 Linear Stage Efficiency Analysis .................................................... 93
  4.4.2 Switch Stage Efficiency Analysis .................................................... 95
4.5 Measurements ..................................................................................... 99
4.6 Summary ............................................................................................. 105

CHAPTER 5 ET IC DESIGN AND MEASUREMENTS ........................................ 107
5.1 Wideband High Efficiency Envelope Amplifier Design ....................... 107
5.2 Two-stage SiGe PA Design ................................................................. 110
5.3 ET IC Measurements ......................................................................... 113

vi
5.4 Summary

CHAPTER 6 CONCLUSIONS

REFERENCES
List of Figures

Figure 1.1 Simplified RF PA.................................................................3
Figure 1.2 Simplified transistor loadline of (a) linear PA and (b) switching PA........4
Figure 1.3 Ideal Class A and B linear PA efficiency vs. output power...............6
Figure 1.4 WLAN 802.11a/g spectrum mask [21-22]........................................8
Figure 1.5 WLAN 802.11a/g EVM requirements [21-22]...............................8
Figure 1.6 CCDF of 802.11g OFDM signal................................................10
Figure 1.7 Power amplifier gain plot showing gain compression and the effect of linearization.................................................................10
Figure 1.8 Traditional Envelope Elimination and Restoration (EER) PA block diagram. .................................................................11
Figure 1.9 Traditional Envelope Tracking (ET) PA block diagram....................11
Figure 2.1 Traditional Envelope Tracking (ET) PA block diagram.................14
Figure 2.2 The dynamic load-line of the PA in ET system; the biasing points of the PA dynamically track the input power..............................15
Figure 2.3 Traditional Envelope Elimination and Restoration (EER) PA block diagram. .................................................................15
Figure 2.4 The RF transistor achieves high efficiency when its output power is in the compression or saturation region. (PD: pre-distortion.) .................15
Figure 2.5 Modern EER system structures. The transmitter is also referred as a polar transmitter [29, 30].................................................................17
Figure 2.6 Simulations of (a) the spectra of the complex baseband and the phase signals; (b) EVM as a function of baseband system bandwidth for the EER system. The required EVM is 5% for a WLAN 802.11g PA...............18
Figure 2.7 Hybrid EER structure: RF input signal is both envelope and phase modulated signal and RF PA is designed as a switch mode PA........19
Figure 2.8 GaAs MESFET Class AB 2.4GHz RF PA schematic diagram.........20
Figure 2.9 Class B PA measurement over 1.4GHz to 2.8GHz............................21
Figure 2.10 Measurement and simulation results of MWT-871 GaAs MESFET Class B RFPA. Single tone results at 2.4 GHz.................................................................21
Figure 2.11 Simplified envelope amplifier schematic diagram..................................................22
Figure 2.12 Agilent ADS Simulation of the optimum (for maximum PAE) of VDD, VGG and Pin for the 2.4 GHz GaAs MESFET Class-AB PA. The theoretical envelope amplitude of the output signal is (RLPout) ½ when the load is RL....................................................................................................24
Figure 2.13 Comparison of amplifiers when the drain bias is varied for maximum PAE as shown in Figure 2.12 (envelope tracking) and the drain bias is fixed at 4.4V. The 802.11g 64QAM output amplitude power probability distribution is also shown when the average output power is 15dBm.......25
Figure 2.14 Block diagram of wide-band ET architecture with baseband pre-distortion and time alignment algorithms..........................................................27
Figure 2.15 AM-AM and inverted AM-AM functions of the Case 3 ET system in Table 2.2. .............................................................................................................27
Figure 2.16 Simulated amplifier output with 802.11g signal, before and after pre-distortion. .............................................................................................................28
Figure 2.17 AM-AM (a) without and (b) with pre-distortion at Pout = 20dBm. .......30
Figure 2.18 AM-PM (a) without and (b) with pre-distortion at Pout = 20dBm. .......31
Figure 2.19 Output spectrum before and after pre-distortion at Pout = 20dBm.............32
Figure 2.20 Simplified schematic of Class E PA .................................................................34
Figure 2.21 Simplified Class E PA schematic.................................................................35
Figure 2.22 Simulation and measurement of Class E PA at 2.36GHz when Vcc=2V).35
Figure 2.23 Measurement of optimal EER PA efficiency obtained by sweeping input power at different collector voltages (under CW condition at 2.4GHz). A constant Vdd (6V) HFET Class AB PA measurement at 2.4GHz is shown for comparison. ..........................................................................................36
Figure 2.24 Spectrum before and after pre-distortion at Pout=19dBm (80mW). ACPR is improved by 10 dB after the pre-distortion and memory effect mitigation. The ACPR improvement is limited by the system bandwidth of 40MHz. .36
Figure 2.25 Constellation of 64QAM OFDM signal at output power 19.56dBm: (a) before pre-distortion, EVM 6.6%; (b) after memory effect pre-distortion, EVM 3%. The required EVM is 5% by 802.11g specifications.........37

Figure 3.1 Comparison of ADS simulation and Cann model of the GaAs MESFET PA. A least-squares fit to the simulation data provides $g = 1.24 + 0.38VDD$, $L = 0.09 + 1.15VDD$, and $s = 5$..........................42

Figure 3.2 ET system AM/AM simulation by ADS and Cann model simulation......42

Figure 3.3 Simulated two-tone EER system with time mismatch between baseband amplitude and RF phase. The modulation frequency is 20MHz, and the baseband amplitude path time delay is 2.5 ns.................................45

Figure 3.4 Simplified ET system block diagram. The time mismatch between the baseband amplitude and RF amplitude/phase is ........................................47

Figure 3.5 Two-tone ET system with time mismatch between baseband amplitude and RF amplitude/phase. The modulation frequency is 20MHz, and the baseband amplitude path time delay is 2.5 ns.................................47

Figure 3.6 Simulation of two-tone ET amplifier with time delay mismatch. Note the distortion in the output amplitude due to the time mismatch between the baseband amplifier and RF amplitude signals and the limiting action of the amplifier. The baseband amplitude path time delay is 2.5 ns...............52

Figure 3.7 Two-tone error signal standard deviation vs. time mismatch for EER system and ET system. Note the EER is more sensitive to path mismatch effects than the ET system. The simulation results deviate from the theory at high mismatch values due to the high time-mismatch for the higher order harmonic components and nonideal predistortion.............................54

Figure 3.8 The simulation and theory analysis of the ET system for the time mismatch sensitivity for WLAN 802.11g signal. The Cann model simulation agrees very well with the theory analysis if $F=2$. In this case, the envelope time delay is 10ns, and from the above graphic, the effective time delay is about 5ns.................................................................55
Figure 3.9 Simulated covariance of RF input amplitude $A_{in}$ and RF output amplitude $A_{out}$ (refer to Eq. (3.33)) for different values of $T_{env}$, $TRF$, and $TFB$ for OFDM 802.11g signal. Note that the peak of the covariance occurs at the sum of $TFB$ and a weighted average of $T_{env}$ and $TRF$.

Figure 3.10 Simulated EVM (a) and $L_{max}$ (b) ($TFB$ is zero). (for $TRF$=0); (for $TRF$=0.5 samples); (for $TRF$=1 samples).

Figure 3.11 Simulated EVM and $L_{max}$ for variations in $TFB$. Note that the minimum EVM occurs when $T_{env}$=$TRF$, and $L_{max}$=-$TFB$-($TRF$+$T_{env}$)/2.

Figure 3.12 Simulated rms phase error for different values of $T_{env}$, $TRF$, and $TFB$. Note that the curve of $T_{env}$=0, $TRF$=9.3 ns and $TFB$=0 overlay with the curve of $T_{env}$=0, $TRF$=9.3 ns and $TFB$=9.3 ns. Therefore, the phase error is relatively insensitive to $TFB$.

Figure 3.13 Simulated value of $PL_{min}$ as a function of $T_{env}$. The value of $T_{env}$ where $PL_{min}$ crosses zero is equal to $TRF$, and its value is independent of $TFB$.

Figure 3.14 Simulated value of $PL_{min}$ vs. the time mismatch between $TRF$ and $T_{env}$. Note that this is independent of $TFB$.

Figure 3.15 Simulation and measurement of EVM vs. baseband amplitude path time-delay for ET and EER system for 802.11g signal. The measurement is made with the GaAs MESFET RF PA with $P_{out}$ = 15dBm. Note that the measured slope of the EVM vs. time mismatch agrees well with the theory. The measured minimum error floor of 3% is due to other impairments in the RF path unrelated to the time-mismatch.

Figure 3.16 Measured EVM vs. baseband amplitude path time-delay $T_{env}$ for WLAN 802.11g application (data rate 54Mpbs). The minimum EVM indicates the time difference between the RF path and baseband amplitude path is approximately 1110 ns.

Figure 3.17 Measured $PL_{min}$ vs. baseband amplitude path time-delay $T_{env}$ for WLAN 802.11g application (data rate 54Mpbs). The zero-crossing of $PL_{min}$ indicates the time difference between the baseband amplitude path
and RF amplitude/phase path is approximately 1110 ns, which agrees well with the result from Figure 3.14. Note that the average slope of PLmin vs. the time mismatch is approximately 0.5, which agrees well with the theory of F/ =2 for 802.11g signal.

Figure 3.18 “Hybrid” EER system time-alignment feature

Figure 4.1 Simulated envelope amplifier bandwidth requirement for an 802.11g signal in ET and EER systems

Figure 4.2 (a) Spectrum of OFDM envelope signal; (b) OFDM envelope signal energy cumulative distribution

Figure 4.3 Envelope amplifier design; ideal circuit model of the voltage-controlled current-parallel envelope amplifier

Figure 4.4 Envelope amplifier design; the circuit implementation

Figure 4.5 Block diagram of hysteresis current feedback control

Figure 4.6 Mathematical behavioral model of the envelope amplifier, where h is the hysteresis voltage of the comparator (assuming the op-amp is an ideal voltage source with infinite bandwidth, and the PA is modeled as a simple resistor R2)

Figure 4.7 (a) Linearized output voltage and; (b) AC switch current waveforms for DC input envelope signal

Figure 4.8 Simulation of (a) voltage and current waveforms and (b) spectrums. The DC signal is 1.94V. In simulation, VDD is 5.5V, h is 7mV, Rsense is 1 Ohm, Rload is 47 Ohm, L is 12 uH. The simulated switching frequency is 7 MHz. The calculated switching frequency from (4.12) is 7.5 MHz

Figure 4.9 Comparison of simulation and theory for switching frequency vs. duty ratio of the DC envelope signal. All the circuit parameters are identical to Figure 4.8

Figure 4.10 Simulation of (a) switching waveform and error signal voltage; (b) spectra of waveforms. The input envelope signal is . The simulated average switching frequency is 6.4 MHz. The calculated average switching
frequency from (4.15) is 6.7 MHz. VDD = 5.5V, h = 7mV, Rsense = 1 Ohm, Rload = 47 Ohm, L = 12 uH.

Figure 4.11 Comparison of simulation and theory for the switching frequency vs. signal amplitude in the small-signal linear operation region. The input sinewave signal frequency is 20kHz. The amplitude is determinate by G (signal amplitude coefficient), where , . All the circuit parameters are identical to Figure 4.8.

Figure 4.12 Simulation of (a) switching waveform and error signal; (b) spectrums. The input envelope signal is . From simulation the switching frequency is 4.95 MHz. The calculated switching frequency from (4.18) is 5MHz. All the circuit parameters are identical to Figure 4.8. The asymmetry of is determined by the duty ratio D.

Figure 4.13 Simulation of circuit behavior by sweeping AC frequency of the envelope signal: (a) average slew rate; (b) average switching frequency; (c) efficiency; (d) AC current from linear stage and switch stage; (e) EVM. Input envelope signal . All the circuit parameters are identical to Figure 4.8.

Figure 4.14 (a) Simulated average switching signal frequency vs AC frequency for different normalized AC amplitudes (the AC amplitudes are normalized to the signal DC component); (b) Simulated combinations of the signal AC amplitude and AC frequency under the minimum switching condition and the matched slew rate condition.

Figure 4.14 (c) Simulated efficiency vs. AC frequency under the minimum switching condition and the matched slew rate condition. The circuit parameters are identical to Figure 4.8.

Figure 4.15 Simulation of the circuit behavior by sweeping the hysteresis value for an 802.11g signal: average switching frequency vs. h; and EVM vs. h.

Figure 4.16 (a) Simulated average switching frequency vs. L.
Figure 4.16 (b) Simulated average slew rate vs. L; (c) Simulated efficiency vs. L. The simulation parameters are identical to Figure 4.8. The sinewave signal: 802.11g signal DC =1.7V, RMS =1.9V.

Figure 4.17 (b) comparison of simulation and theory for the linear stage efficiency. The efficiency of the linear stage is zero at the DC level of the input signal, where the DC power is supplied by the switch stage.

Figure 4.18 Switch stage circuit implementation.

Figure 4.19 Simulation of envelope amplifier efficiency with the OFDM signals probability density function.

Figure 4.20 Comparison of simulated and measured envelope amplifier for small signal: The average switching frequency from both the simulation and measurement is 5.75 MHz.

Figure 4.21 Comparison of the simulated and measured envelope amplifier for large signal. The average switching frequency for both simulation and measurement is 2MHz.

Figure 4.22 Comparison of the simulated and measured envelope amplifier by sweeping the signal AC frequency: The switch stage current gain is defined as the ratio of fundamental component of the switch stage current to the linear stage current. In the simulated efficiency, the quiescent current and the power loss in the comparator is not included.

Figure 4.23 Comparison of the simulated and measured envelope amplifier for an 802.11g signal. The average switching frequency from simulation is 5.7MHz and from measurement is 5.3 MHz.

Figure 4.24 Measurement of the envelope amplifier for an 802.11g signal in “hybrid” EER system with Class E RFPA as the load. The circuit parameters are identical to Figure 12 except the resistor load is replaced by Class E RF PA [see Section 2.4 for the details of Class E RF PA design]. The measured
802.11g signal DC level is 1.93V, RMS level is 2.05V; the equivalent voltage supply VDD in (4.15) is 5V considering 0.5V drop across PMOS. The output collector voltage is shifted up of 0.5V for higher linearity and PAE.

Figure 5.1 Simplified schematic of the comparator [58]. Hysteresis value is +/-10mV, delay is 5ns.

Figure 5.2 Simplified schematic of Class AB rail-to-rail Op-Amp (the load and the switch stage are respectively simplified as a resistor and a DC current source). Op-Amp quiescent current is 3mA. The closed loop gain is 3dB. Maximum output voltage 3V. Closed loop bandwidth at 3dB gain is 20MHz.

Figure 5.3 Simplified schematic of switch stage and switch driver. Since M1 is much larger than M2, M2 turns on much faster than M1 turns off. To prevent the shoot-through current, a delay is introduced by inverter M10-M11 and an NAND M5-M7 [60].

Figure 5.4 Schematic of SiGe HBT 2.4 GHz power amplifier. Vcc=3.3V.

Figure 5.5 Die and package photo of SiGe BiCMOS ET PA. Chip size 1mm x 4 mm.

Figure 5.6 Measured gain, output power and power-added efficiency of the SiGe power amplifier when operated in CW mode at 2.4 GHz, Vcc=3.3V.

Figure 5.7 (a) ET PA AM-AM before predistortion; (b) ET PA AM-AM after predistortion; (c) ET PA AM-PM before predistortion; (d) ET PA AM-PM after predistortion. Maximum PA output is 19dBm.

Figure 5.8 Spectrum of ET PA at 19dBm output power before predistortion (BP) and after predistortion (BP). Negligible switching noise is present at the PA output.

Figure 5.9 Measured input RF signal and envelope signal under time-alignment condition when RF output power is 19dBm.

Figure 5.10 Measured envelope amplifier, switch stage, and input waveforms. The envelope signal is the amplitude of OFDM signal. Average switching frequency is 5MHz. Maximum Vout is 3V.
List of Tables

Table 1.1 WLAN 802.11g Transmitter Specifications [21-22]................................. 7

Table 2.1 Comparison between EER, ET and hybrid EER............................................. 19

Table 2.2 Simulated performance of fixed VDD class AB PA and different ET configurations @ Pout = 12dBm ........................................................................................................ 26

Table 2.3 Comparison between before and after pre-distortion and back-off. The PA is the “Case 3” configuration of Table 2.2 ...................................................... 28

Table 2.4 Comparison between constant Vdd (4.4V) GaAs MESFET Class AB RF PA and ET P, with and without predistortion......................................................... 32

Table 2.5 Summary of “Hybrid” EER, WBET and constant class AB PA with OFDM signal .................................................................................................................. 38

Table 4.1 Simulated power losses and efficiency of the envelope amplifier for an 802.11g signal ........................................................................................................ 98

Table 4.2 Envelope amplifier performance in “Hybrid” EER system ......................... 104

Table 4.3 Comparison of published envelope amplifiers and the work presented in this paper ........................................................................................................... 105

Table 5.1 Envelope amplifier performance in WLAN ET system.............................. 118

Table 5.2 Comparison of ET PA and constant bias PA with OFDM signal .............. 120
Acknowledgements

For me the past four years is a special journey mixed with anxiousness, excitement, depression, and enjoyment. It brought me a lot of precious memories. Without many people’s great assistance, it is hard for me to achieve this work.

First of all, I would like to express my appreciation to my advisor Prof. Larson. Prof. Larson supported me for this unique opportunity to learn and discover my research potentials. He guided me through my PhD pursuit with his great academic wisdom and enthusiasm on the research. Every time when I feel depressed, he tried his best to encourage me and push me moving forward with his trust and support. And it was one of my most enjoyable experiences learning from his profound knowledge and expertise in these areas.

Don Kimball is a fantastic co-advisor. His sharpest understanding on this research topic is critical to its success. His sense of talent on the engineering prevented me from many meanders along the road. His kindness and willingness to help others at any moment makes him the most popular advisor and friend in the group. The idea he brought in and the test equipments he set up in the UCSD makes our lab the most unique attractive place in this field. His contributions are crucial to this project.

I am indebted to Prof. Asbeck for his invaluable guidance on my research project. I benefited intensely from Prof. Asbeck’s group meetings and many interesting brainstorming discussions. Thanks to Prof. Asbeck and his group for facilitating me on the convenient research circumstance and equipments in the lab.
With Prof. Asbeck’s insightful advice and encouragement, my research was enhanced to a higher level.

I am grateful to Dr. Donald Lie in SPAWAR for his intensive help and many inspiring discussions, for his generous support on the IC fabrication and circuit measurements. It is enjoyable to learn from his profound knowledge both on the technical elaborations and non-techniques.

I would like to thank Prof. Laurence Milstein, Prof. Chung-Kuan Cheng, and Prof. Robert Bitmead for their generous efforts to serve on my thesis examination committee.

I would like to appreciate Ms. Ni Wan, Dr. Xudong Wang, and Dr. Jack Pekarik in IBM for their support on the chip fabrication. Thanks for their helpful suggestions.

I would like to specially thank to Ms. Annie Yang (SPAWAR), Mr. Horace Ng (Nokia), Mr. Jeremy Popp, Dr. David Choi (Nokia), and Mr. Ojo Dayo (Broadcom) for their heartfelt support during the hardest periods.

The long journey at UCSD would not be so remarkable and pleasant without making these friends and learning from them on their respective wisdom and expertise. I would like to specially acknowledge Dr. Dongjiang Qiao, Dr. Jinho Jeong, Adam, Jeremy Rode, Mr. Paul Draxler, David Keogh, Tsai-pi, Chin Hsia, Mingyuan Lie, Tomas O’Sullivan, Yu Zhao, Sataporn Pornpromlikit, and Paul Theilmann in Prof. Asbeck’s group, for many stimulating discussions and their considerate supports in the
lab. I would like to thank Dr. Chengzhou Wang, Dr. Junxiong Deng, Dr. Liwei Sheng, Dr. John Fairbanks, Dr. Vincent Leung, Himanshu, Yiping, Joe, Marcus, Mohammad, Rahul, Danel, Sean, Sanghong, in Prof. Larson’s group for their great help. I would like to thank Kevin in Prof. Galton’s group for his assistance on the Cadence tool. I am especially grateful to Cuong Vu in CalIT2 for his a lot of professional work on the PCB implementation.

I am especially grateful to Arya Behzad, Ali Afsahi, Hao Jiang, HH Liao, Paymen, Vikram and Paul of Broadcom for their generous support and help during my internship.

I would like to acknowledge Dr. Allan Barrow of Analog Device Inc. for the generous support of the ISSCC 2006 ADI outstanding student designer award.

I also want to gratefully acknowledge the financial support from the UCSD Center for Wireless Communications and its Member Companies, Powerwave Inc., Ericsson Inc., Intersil (now Conexant Inc.), Nokia Inc., IBM Inc., Broadcom Inc., and the UC Discovery Grant.

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wideband envelope amplifier for WLAN 802.11g applications,” IEEE MTT-S Int.

amplifier with pre-distortion for WLAN 802.11g,” IEEE MTT-S Int. Microwave
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IMS 2004 student paper competition.)


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Studies in Circuit and System Design for Wireless Communications. Advisors: Professor Lawrence E. Larson and Donald Kimball
ABSTRACT OF THE DISSERTATION

High Efficiency Linear Envelope Tracking and Envelope Elimination and Restoration Power Amplifier for WLAN OFDM Applications

by

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Doctor of Philosophy in Electrical Engineering (Electronic Circuits and Systems)

University of California, San Diego, 2006

Professor Lawrence E. Larson, Chair

High efficiency radio frequency (RF) power amplifiers (PAs) are critical in portable battery-operated wireless communication systems because they can dominate the power consumption. Linear power amplifier is required for envelope modulated signal. Traditionally, linear power amplifiers are implemented by “backing-off” the
Class-A or Class-AB PA. However for a high peak-to-average (PAR) signal, the average efficiency is much lower than the peak efficiency, which is well down as the inherent trade-off between linearity and efficiency.

This dissertation focuses on Envelope Elimination and Restoration (EER) and Envelope Tracking (ET) efficiency enhancement techniques to improve the PA average efficiency for high PAR signal. The EER and ET PA structures are investigated. Wideband ET and “hybrid” EER structures are proposed for WLAN 802.11g signal at 20MHz signal.

Two major challenges of the wideband EER and ET PAs are investigated:

(1) An adaptive time-alignment algorithm was proposed to calibrate the time-mismatch in wideband EER and ET systems;

(2) A high efficiency wideband envelope amplifier is designed for wideband EER and wideband ET applications.

A monolithic wideband high efficiency ET power amplifier is designed and implemented for WLAN 802.11g applications in IBM SiGe BiCMOS technology. Digital pre-distortion was implemented to reduce the EVM of the amplifier. The measured overall power-added efficiency of the amplifier is 28% at 20 dBm (100mW) output power.
Chapter 1
Introduction

High efficiency radio frequency (RF) power amplifiers (PAs) are critical in portable battery-operated wireless communication systems (such as cellular phones, PDAs, and laptops) because they can dominate the power consumption [1-2]. Power amplifiers demonstrate the highest efficiency when operated in the compression region (such as in Class A, Class AB and Class B modes) or in the switching mode (such as Class D, E, F) [3-5]. However, these highly efficient nonlinear power amplifiers can only amplify constant envelope modulation signals (such as GSM or AMPS) without nonlinear distortion. With modern wireless communication systems evolving to more spectrally efficient and higher data rate modulation formats, highly linear power amplifiers are required to avoid the out-of-channel interference (e.g., adjacent channel power ratio (ACPR) ) and distortion (e.g., error vector magnitude (EVM) ).

The traditional approach to linearly amplify the non-constant envelope modulated signal is to “back-off” the linear Class A or Class AB PA’s output power until the distortion level is within acceptable limits. Unfortunately, this lowers efficiency significantly, especially for high Peak-to-Average-Ratio (PAR) signals. Thus, there is an inherent tradeoff between linearity and efficiency in PA design.
This problem has been thoroughly investigated over many years and Envelope Elimination and Restoration (EER) [6-10], Pre-distortion [3] [4], feedback [3] [4], feed-forward [4], Doherty [3], Envelope Tracking (ET) [11-17], linear amplification with nonlinear control (LINC) [18], and gate dynamic biasing [19-20] are just some of the techniques explored.

This research focuses on the EER and ET technologies, especially for wideband applications, such as wireless LAN systems. Two major challenges of the EER and ET techniques, especially when they are used for wideband applications, are the time-alignment between the baseband amplitude and the RF signal, and the wide-band high-efficiency envelope amplifier design. This dissertation will addresses those two challenges for wideband EER and ET PAs and demonstrate an IC design of a wideband ET PA for WLAN 802.11g application.

This introductory chapter will provide the background for this research. To begin with, we will explore the motivations of high efficiency linear power amplification for wireless LAN applications. It will be followed by a review of the PA efficiency enhancement technologies. We will conclude this chapter by presenting the objectives and the organization of the dissertation.
1.1 Motivations

1.1.1 PA Trade-off on Efficiency and Linearity

The trade-off between PA efficiency and linearity has been studied in many books and papers in recent years [1-20]. The traditional PA is either very linear or very efficient, but both are rarely achieved simultaneously. Figure 1.1 shows a simplified schematic of a RF power amplifier with an inductor load. The input and output matching networks are applied to match the RF transistor input and output impedance to the desired source and load impedance. The RF transistors itself operates either as a linear transconductor or a switcher. Figure 1.2 (simplified transistor IV curves and loadline) shows the current and voltage behavior of the linear-mode PA and switching-mode PA.

![Figure 1.1: Simplified RF PA.](image-url)
When the PA operates in the switching-mode, the transistor is either “off” \((I_{ds} = 0, V_{ds} = \text{max})\), or “on” (saturation) \((I_{ds} = \text{max}, V_{ds} = 0)\). Ideally, no power is consumed in the transistor in either condition and the PA efficiency can be as high as 100% theoretically. However, since the PA works only in the “on” or “off” states, the output amplitude is fixed. If the input signal is envelope modulated, the output signal will be clipped and distorted, which creates nonlinearity. Therefore, the switching-
mode PA can only be utilized for a constant envelope signal, such as FM or GMSK signals. [1-2]

When the PA operates in the linear-mode the transistor itself operates as a linear transconductor. The input voltage signal is transferred linearly to the output current through the modulation effect of the RF transistor. For the linear PA, the efficiency is proportional to output power, e.g:

\[ \eta_{\text{linPA}} \propto f(P_{\text{out}}) \]  

(1.1a)

where the efficiency is:

\[ \eta_{\text{linPA}} = \frac{P_{\text{out}}}{P_{\text{dc}}} \]  

(1.1b)

For example, the efficiency of the Class A PA is linearly proportional to output power and the Class B PA efficiency is linearly proportional to the square root of the output power, as shown in Figure 1.3 [1-2]. The linear mode PA achieves peak efficiency only at the maximum output power. To prevent clipping the signal, the PA average output power will be backed-off from the maximum output power; therefore the PA average efficiency decreases and is much lower than the peak efficiency, especially for high Peak-to-Average (PAR) signals (e.g. WLAN 802.11g signal), as discussed in the following section.
1.1.2 WLAN OFDM Signal

Wireless local area networks (LANs) have been widely used in daily wireless communications, such as Bluetooth, Wi-Fi and so on. The WLAN 802.11g is a wide bandwidth IEEE standard, and the key parameters for the RF circuit designer are summarized in Table 1.1 [21-22]. To meet the standard spectrum mask and the error vector magnitude (EVM) requirements, the transmitted WLAN 802.11g signal requires very high linearity. Figure 1.4 shows spectrum mask requirement of WLAN 802.11g signal and Figure 1.5 summarizes the EVM requirements.
At the same time, according to the orthogonal frequency division multiplexing (OFDM) modulation requirements, the signal PAR could be as high as 10dB. Figure 1.6 shows the simulated complementary cumulative distribution function (CCDF). Therefore, the PA operates in the back-off region from the peak output power, and the average efficiency is low [23-24].

Table 1.1 WLAN 802.11g Transmitter Specifications [21-22]

<table>
<thead>
<tr>
<th>Specification</th>
<th>Specification Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Frequency band</td>
<td>2.4-2.4835GHz</td>
</tr>
<tr>
<td>Numbers of Carriers</td>
<td>52 (48 data and 4 pilots)</td>
</tr>
<tr>
<td>Channel bandwidth</td>
<td>16.25MHz</td>
</tr>
<tr>
<td>Data rate</td>
<td>6 to 54Mbps</td>
</tr>
<tr>
<td>Carrier type</td>
<td>OFDM</td>
</tr>
<tr>
<td>Modulation</td>
<td>BPSK, QPSK, 16QAM or 64QAM</td>
</tr>
<tr>
<td>Max. instantaneous output power</td>
<td>1W (in USA)</td>
</tr>
<tr>
<td>EVM</td>
<td>5.6% or -25dB for 54Mbps</td>
</tr>
</tbody>
</table>
| Spectrum mask                      | -20dBc @ 11MHz offset  
|                                    | -28dBc @ 20MHz offset  
|                                    | -40dBc @ 30MHz offset  |
Figure 1.4: WLAN 802.11a/g spectrum mask [21-22].

<table>
<thead>
<tr>
<th>Data rate (Mbits/s)</th>
<th>Relative constellation error (dB)</th>
</tr>
</thead>
<tbody>
<tr>
<td>6</td>
<td>$-5$</td>
</tr>
<tr>
<td>9</td>
<td>$-8$</td>
</tr>
<tr>
<td>12</td>
<td>$-10$</td>
</tr>
<tr>
<td>18</td>
<td>$-13$</td>
</tr>
<tr>
<td>24</td>
<td>$-16$</td>
</tr>
<tr>
<td>36</td>
<td>$-19$</td>
</tr>
<tr>
<td>48</td>
<td>$-22$</td>
</tr>
<tr>
<td>54</td>
<td>$-25$</td>
</tr>
</tbody>
</table>

Figure 1.5: WLAN 802.11a/g EVM requirements [21-22].
Figure 1.6: CCDF of 802.11g OFDM signal.

1.2 PA Efficiency Enhancements for High PAR Signals

1.2.1 Linearization Techniques

The major goal of PA linearization is to push the “linear” PA closer to ideal linearity. Since the PA transistor deals with the large signal, the transconductance of the transistor will be nonlinear when the PA approaches the 1dB compression point. Figure 1.7 shows an AM-AM plot of a Class-AB PA. Also AM-PM of the transistor is caused by the nonlinear capacitance and nonlinear input/output impedance. When the linearization techniques (e.g. digital/RF/analog pre-distortion, feedback and feedforward) are implemented in the PA, the 1dB compression point is pushed closer
to the saturation point. By this way, the PA efficiency is increased to some extant by increasing 1dB compression output power.

![Power amplifier gain plot showing gain compression and the effect of linearization.](image)

**Figure 1.7**: Power amplifier gain plot showing gain compression and the effect of linearization.

### 1.2.2 Efficiency Enhancement Techniques

Both EER and ET utilize power supply control schemes. EER uses a combination of a switching-mode PA and an envelope re-modulation circuit. Envelope tracking (ET) utilizes a linear PA and a supply modulation circuit where the supply voltage tracks the input envelope. Figure 1.8 and Figure 1.9 shows the simplified EER and ET block diagrams. When the supply voltage tracks the instantaneous envelope modulation signal, it is called Wide Bandwidth ET (WBET) [11-13, 17]; when the supply voltage tracks the long-term average of the input envelope power, it is called Average ET (AET) [14-15]; when the supply voltage switches to different step levels
according to the input envelope power, it is called Step ET (SET) [16, 23]. The AET and SET are especially useful for dynamic power control schemes such as the reverse link in CDMA systems where the variation in average power is much greater than 20dB [26].

**Figure 1.8: Traditional Envelope Elimination and Restoration (EER) PA block diagram.**

**Figure 1.9: Traditional Envelope Tracking (ET) PA block diagram.**

### 1.3 Dissertation Objectives and Organization

This dissertation will focus on the wideband ET and EER techniques. Two major challenges are investigated for wideband ET and EER techniques: (1) time-alignment
of the RF signal path and envelope signal path; (2) wideband high efficiency envelope amplifier design.

Chapter 2 reviews the EER and ET techniques. The two techniques are compared from the system level. A hybrid EER structure is propose to utilize both high efficiency of EER and wideband implementation of ET. Two examples are demonstrated respectively for EER and ET PA for WLAN applications.

In Chapter 3, a mathematical model for the ET and EER systems is discussed. Based on the model, the effect of the time mismatch between the envelope path and RF path is analyzed. A simple time alignment algorithm is developed based on the transmitted signal itself. The analysis and algorithm are verified by the experimental results.

In Chapter 4 a high efficiency wideband envelope amplifier is proposed. A model of the wideband envelope amplifier is developed and the key design parameters are given based on the signal statistical characteristics. The measurements of the envelope amplifier in the EER and ET system demonstrate its capability in WLAN OFDM applications.

Based on the time-alignment algorithm and the high efficiency envelope amplifier analysis developed in Chapter 3 and 4, Chapter 5 demonstrates a BiCMOS wideband ET IC circuit for the WLAN 802.11g applications.

Chapter 6 concludes the dissertation.
Chapter 2
Envelope Tracking and Envelope Elimination and Restoration Power Amplifier Architectures for Wideband WLAN OFDM Applications

This chapter focuses on the system level design of the ET and EER PAs for wideband applications. Two examples of the wideband ET and wideband hybrid EER are demonstrated for WLAN 802.11g applications.

2.1 Traditional ET and EER Power Amplifier Architectures

Figure 2.1 shows the principles of traditional ET systems. ET utilizes a linear PA and a controlled supply voltage, which tracks the input envelope. When the supply voltage tracks the instantaneous envelope modulation signal, it is called Wide Bandwidth ET (WBET) [11-13, 17]; when the supply voltage tracks the long-term average of the input envelope power, it is called Average ET (AET) [14-15]; when the supply voltage switches to different step levels according to the input envelope power, it is called Step ET (SET) [16, 25].
Figure 2.2 shows the principle of the ET to improve the PA average efficiency by dynamic biasing the RF transistor so that the RF transistor working in the high efficiency compression region over a wide dynamic range of output power.

![Block Diagram of Traditional Envelope Tracking (ET) PA](image)

**Figure 2.1: Traditional Envelope Tracking (ET) PA block diagram.**

In contrast, EER uses a combination of a high efficiency switch-mode PA with an envelope re-modulation circuit [6-10]. Figure 2.3 shows the principles of traditional EER systems. The RF signal is clipped by the limiter; only the phase modulated signal is inputted to the switch mode PA. The envelope signal is detected before the limiter and is re-modulated to the signal through the drain or the collector of the RF transistor. Theoretically, EER is more efficient than ET, since the RF transistor is always operating in a switching mode. Figure 2.4 demonstrates the comparison of the different efficiency points for traditional Class AB, EER and ET PAs.
Figure 2.2: The dynamic load-line of the PA in ET system; the biasing points of the PA dynamically track the input power.

Figure 2.3: Traditional Envelope Elimination and Restoration (EER) PA block diagram.

Figure 2.4: The RF transistor achieves high efficiency when its output power is in the compression or saturation region. (PD: pre-distortion.)
2.2 Hybrid EER Power Amplifier Architecture

In the traditional EER system, the input RF signal is clipped by a limiter; usually the limiter is challenging to realize for a wide dynamic range OFDM signal where the peak-to-minimum ratio is infinite [27].

In modern EER systems, the amplitude and phase signals are generated directly in the baseband domain and up-converted to RF as shown in Figure 2.5. For the complex modulated signal, the baseband signal can be expressed with $I(t)$ and $Q(t)$ or $A(t)$ and $\Phi(t)$ as:

$$s_{BB}(t) = I(t) + jQ(t) = A(t)\Phi(t)$$  \hspace{1cm} (2.1)

where the envelope signal is:

$$A(t) = \sqrt{I(t)^2 + Q(t)^2}$$  \hspace{1cm} (2.2)

and the phase signal is

$$\Phi(t) = e^{j\arctan(Q/I)}$$  \hspace{1cm} (2.3)

According to the nonlinear transfer function as shown in (2.3), the Fourier Transfer of (2.3) will be a Bessel function [28]; therefore the bandwidth of phase signal $\Phi(t)$ is much wider than that of baseband signal $s_{BB}(t)$ as shown in Figure 2.6. Hence the bandwidth requirement of the phase signal imposes practical challenges and limits the traditional EER transmitter to narrow-bandwidth applications [29, 30]. In contrast, the
RF signal bandwidth in ET systems is identical to the baseband signal bandwidth, which is much narrower than the phase signal bandwidth in EER systems. In addition, as we will discuss in more detail in the following two chapters, since ET maintains the amplitude information in the RF signal, it requires a lower envelope amplifier bandwidth and less precise time-alignment between the envelope and RF paths [13].

![Figure 2.5: Modern EER system structures. The transmitter is also referred as a polar transmitter [29, 30].](image)

To utilize the high efficiency operation of EER and at the same time reduce the stringent requirements of bandwidth and time-alignment, the “hybrid” EER structure was proposed recently [31-33]. Figure 2.7 shows the principle of the hybrid EER system, where the PA input signal is still a complex-modulated signal, but the PA is designed to operate in the switching-mode at higher input powers. Compared with traditional EER systems, the hybrid EER provides the following potential advantages:

1. lower RF bandwidth requirement;

2. lower envelope bandwidth requirement;
(3) higher gain and therefore higher average PAE;

(4) lower sensitivity to the time-mismatch between envelope and RF paths.

Figure 2.6: Simulations of (a) the spectra of the complex baseband and the phase signals; (b) EVM as a function of baseband system bandwidth for the EER system. The required EVM is 5% for a WLAN 802.11g PA.
Table 2.1 shows a comparison between EER, WBET and “Hybrid” EER.

Table 2.1 Comparison between EER, ET and hybrid EER

<table>
<thead>
<tr>
<th></th>
<th>EER</th>
<th>WBET</th>
<th>“Hybrid” EER</th>
</tr>
</thead>
<tbody>
<tr>
<td>Average Efficiency</td>
<td>Highest</td>
<td>High</td>
<td>Highest PAE</td>
</tr>
<tr>
<td>Envelope Path Bandwidth</td>
<td>Very Wide</td>
<td>Wide</td>
<td>Wide</td>
</tr>
<tr>
<td>RF Bandwidth</td>
<td>Wider than complex IQ bandwidth</td>
<td>IQ bandwidth</td>
<td>IQ bandwidth</td>
</tr>
<tr>
<td>Time-alignment</td>
<td>Very precise time-alignment</td>
<td>Modest time-alignment</td>
<td>Modest time-alignment</td>
</tr>
</tbody>
</table>

2.3 A Wideband ET Power Amplifier for WLAN 802.11g Application

A high efficiency wideband ET PA circuit design and measurement results are demonstrated in this section. The ET PA is composed of a high efficiency Class B RF
PA and a high efficiency wideband envelope amplifier. Digital pre-distortion and time-alignment are implemented into the system. The ET PA is measurement for WLAN 802.11g signal.

2.3.1 Class B RF PA Design

A MWT-871 GaAs MESFET transistor is used to implement a 2.4GHz RF PA. The large-signal model of the device is included in Agilent Advanced Design System for the PA simulation. The Class-AB RF PA schematic is shown in Figure 2.8. The drain and gate biasing is provided through a quarter-wave transmission line. The input and output is matched to 50 Ohms respectively by a high pass and a low pass matching network. Figure 2.9 shows the measurement of the PA from 1.4GHz to 2.8GHz. Figure 2.10 shows the simulation and measurement results at 2.4 GHz. For the 2.4 GHz single tone test, the measured gain is 13 dB and the peak PAE is 52%.

Figure 2.8: GaAs MESFET Class AB 2.4GHz RF PA schematic diagram.
Figure 2.9: Class B PA measurement over 1.4GHz to 2.8GHz.

Figure 2.10: Measurement and simulation results of MWT-871 GaAs MESFET Class B RFPA. Single tone results at 2.4 GHz.
2.3.2 Envelope Amplifier Design

Wideband high efficiency envelope amplifier design is one of the key challenges for the practical wideband EER and ET transmitter. Figure 2.11 shows the envelope amplifier schematic, which is composed of a linear stage, a comparator, and a buck switcher stage [34]. This configuration provides high efficiency and high fidelity for the wideband signal. The details of the design of the envelope amplifier will be discussed in Chapter 4.

![Envelope Amplifier Schematic Diagram](image)

Figure 2.11: Simplified envelope amplifier schematic diagram.

2.3.3 ET Power Amplifier Design

Mathematically, the power amplifier can be modeled as having three independent inputs ($P_{RFin}$, $V_{DD}$ and $V_{GG}$) and two outputs ($P_{RFout}$ and $I_{DD}$) i.e.
\[ P_{RF_{out}} = f_1(P_{RF_{in}}, V_{DD}, V_{GG}) \]  
\[ I_{DD} = f_2(P_{RF_{in}}, V_{DD}, V_{GG}). \]

where \( P_{RF_{in}} \) and \( P_{RF_{out}} \) refer to the input and output RF signal powers, \( V_{DD} \) is the dynamic drain supply voltage, \( V_{GG} \) is the dynamic gate biasing voltage, and \( I_{DD} \) is the dynamic drain supply current.

Since the output power probability density function is fixed [21-22], we can control the independent variables \( P_{RF_{in}}, V_{DD}, \) and \( V_{GG} \) to obtain the highest PAE at each output power. For example, Figure 2.12 shows a single-tone ADS simulation of the optimal (in the sense of highest PAE) \( P_{RF_{in}}, V_{DD}, \) and \( V_{GG} \) for the 2.4 GHz GaAs MESFET Class-AB power amplifier described in Section 2.3.1.

Based on the probability density function of the RF signal, the average drain efficiency can be calculated as [17], [26]:

\[ \eta_{ave} = \frac{\int_0^{P_{RF_{out, max}}} p(P_{RF_{out}}) P_{RF_{out}} dP_{RF_{out}}}{\int_0^{V_{DD}(P_{RF_{out}})} p(P_{RF_{out}}) V_{DD}(P_{RF_{out}}) I_{DD}(P_{RF_{out}}) dP_{RF_{out}}} \]  
(2.6)

where \( V_{DD}(P_{RF_{out}}) \) and \( I_{DD}(P_{RF_{out}}) \) are the drain voltage and drain current, which are the functions of the output RF signal power \( P_{RF_{out}} \), and \( p(P_{RF_{out}}) \) is the probability function of the output power.
Figure 2.12: Agilent ADS Simulation of the optimum (for maximum PAE) of $V_{DD}$, $V_{GG}$ and $P_{in}$ for the 2.4 GHz GaAs MESFET Class-AB PA. The theoretical envelope amplitude of the output signal is $(R_L P_{out})^{1/2}$ when the load is $R_L$.

Note from Figure 2.12 that the optimal $V_{DD}$ curves coincide with the theoretical envelope given by $V_{DD, opt} = (R_L P_{out})^{1/2}$ where $R_L$ is the load resistor of the transistor, so a linear transformation of the baseband amplitude signal is optimum for the envelope amplifier. Also note that a constant $V_{GG}$ provides nearly optimal performance, where the device is biased deeply into Class-AB mode.

The wide gain variation illustrated in Figure 2.12 will result in significant nonlinear distortion and poor EVM. We describe an improved baseband AM-AM and AM-PM pre-distortion technique in Section 2.3.4 to improve the linearity so that the ACPR and EVM requirements are met. Figure 2.13 shows a comparison of simulated PAE between the constant $V_{DD}$ Class AB performance and “ideal” ET performance.
using the biasing approach of Figure 2.12. Note that the PAE is improved significantly over a wide range of output powers.

Another important issue is determination of the optimum minimum drain voltage when $P_{RFin}$ approaches zero. Table 2.2 compares the simulated EVM and efficiency results between the fixed-bias Class-AB PA ($V_{DD} = 4.4V$), and two ET amplifiers with $V_{DD,\text{min}} = 0V$ and 0.5V respectively. The ET $V_{DD,\text{min}} = 0.5V$ case provides both improved linearity and PAE, due to the higher gain at $V_{DD} = 0.5V$.

![Graph showing OFDM Probability Distribution](image.png)

**Figure 2.13:** Comparison of amplifiers when the drain bias is varied for maximum PAE as shown in Figure 2.12 (envelope tracking) and the drain bias is fixed at 4.4V. The 802.11g 64QAM output amplitude power probability distribution is also shown when the average output power is 15dBm.
Table 2.2 Simulated performance of fixed $V_{DD}$ class AB PA and different ET configurations @ $P_{out} = 12$dBm.

<table>
<thead>
<tr>
<th>$V_{DD}$ configuration</th>
<th>Case 1</th>
<th>Case 2</th>
<th>Case 3</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{DD}$ constant</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Gain (dB)</td>
<td>13.9</td>
<td>5.0</td>
<td>7.5</td>
</tr>
<tr>
<td>Drain $\eta$ (%)</td>
<td>9.9</td>
<td>51</td>
<td>43.9</td>
</tr>
<tr>
<td>PAE (%)</td>
<td>9.5</td>
<td>34.9</td>
<td>36.1</td>
</tr>
<tr>
<td>EVM (rms%)</td>
<td>3.2</td>
<td>14.9</td>
<td>10.0</td>
</tr>
</tbody>
</table>

2.3.4 Baseband Digital Pre-distortion for WLAN ET System

Since the ET system has inherent nonlinearity associated with the gain variation as the drain voltage changes as illustrated in Figure 2.12, baseband predistortion is implemented to improve the system linearity. Figure 2.14 shows the wideband ET transmitter architecture with digital pre-distortion. The distorted signal amplified by the ET system is downconverted and feedback to the baseband DSP block. Then the distorted received signal is compared with the original signal and the AM-AM and AM-PM characteristics of the ET system are generated. Figure 2.15 shows the simulation results of AM-AM curves of the Case 3 (signal envelope + 0.5V) in Table 2.2 by using 802.11g signal. By using MATLAB, the inverted AM-AM curves are generated. Figure 2.16 shows the simulation of the output spectrum before predistortion and after predistortion. Table 2.3 demonstrate the simulation of the performance with pre-distortion and without pre-distortion in terms of output power,
efficiency, and EVM, also included is the performance of the back-off technology without pre-distortion.

Figure 2.14: Block diagram of wide-band ET architecture with baseband pre-distortion and time alignment algorithms.

Figure 2.15: AM-AM and inverted AM-AM functions of the Case 3 ET system in Table 2.2.
Figure 2.16: Simulated amplifier output with 802.11g signal, before and after pre-distortion.

Table 2.3 Comparison between before and after pre-distortion and back-off. The PA is the “Case 3” configuration of Table 2.2.

<table>
<thead>
<tr>
<th></th>
<th>Before pre-distortion</th>
<th>After pre-distortion</th>
<th>Back-off</th>
</tr>
</thead>
<tbody>
<tr>
<td>$P_{out}$ (dBm)</td>
<td>18.01</td>
<td>15.699</td>
<td>4.5dB</td>
</tr>
<tr>
<td>Gain (dB)</td>
<td>8.509</td>
<td>8.105</td>
<td>7.842</td>
</tr>
<tr>
<td>Drain $\eta$</td>
<td>57 %</td>
<td>54.2 %</td>
<td>51.2 %</td>
</tr>
<tr>
<td>PAE</td>
<td>49 %</td>
<td>45.8 %</td>
<td>42.8 %</td>
</tr>
<tr>
<td>EVM (dB)</td>
<td>-21.2</td>
<td>-26.2&lt;-25</td>
<td>-26.3&lt;-25</td>
</tr>
<tr>
<td>EVM (rms%)</td>
<td>8.6</td>
<td>4.8&lt;5</td>
<td>4.8&lt;5</td>
</tr>
</tbody>
</table>
2.3.5 Measurements

The ET system for the 802.11g power amplifier was measured, along with an optimally biased Class-AB power amplifier with fixed $V_{dd}$, for comparison. We implemented the GaAs MESFET class AB PA designed in Section 2.3.1 and wideband high efficiency envelope amplifier in Section 2.3.2 into the ET system. The measured AM-AM and AM-PM characteristics of the ET system for the 802.11g OFDM signal are shown in Figs. 2.17 and 2.18. Table 2.4 compares the measured results of the constant $V_{dd}$ Class AB RFPA with the ET amplifier, both with and without pre-distortion. Figure 2.19 shows a comparison of the output signal spectrum before and after pre-distortion. There is approximately 5 dB improvement of ACPR by utilizing the baseband pre-distortion technique, without a significant degradation in overall efficiency.

It is important to note that the overhead associated with the finite dc power dissipation of the envelope amplifier is included in these measured results of efficiency and EVM, but the overhead associated with the extra dc power dissipation of the digital logic for the predistortion and envelope calculations are not included. It is expected that these terms will play an increasingly less significant role in future digital communications systems as VLSI technology continues to advance.
Figure 2.17: AM-AM (a) without and (b) with pre-distortion at $P_{\text{out}} = 20\text{dBm}$.
Figure 2.18 AM-PM (a) without and (b) with pre-distortion at $P_{\text{out}} = 20\text{dBm}$.
Figure 2.19 Output spectrum before and after pre-distortion at $P_{out} = 20$dBm.

Table 2.4 Comparison between constant Vdd (4.4V) GaAs MESFET Class AB RF PA and ET P, with and without predistortion.

<table>
<thead>
<tr>
<th></th>
<th>ET Amplifier</th>
<th>Class AB amplifier</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>w/o PD</td>
<td>w/ PD</td>
</tr>
<tr>
<td>Pout</td>
<td>16.1dBm</td>
<td>15.1dBm</td>
</tr>
<tr>
<td>Gain</td>
<td>8.8 dB</td>
<td>8.6 dB</td>
</tr>
<tr>
<td>Overall drain</td>
<td>32%</td>
<td>29%</td>
</tr>
<tr>
<td>efficiency</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Overall PAE</td>
<td>28%</td>
<td>25%</td>
</tr>
<tr>
<td>EVM</td>
<td>7.9%</td>
<td>3.2%</td>
</tr>
</tbody>
</table>
2.4  A Hybrid EER Power Amplifier for WLAN 802.11g Applications

Switched-mode PA topologies, particularly the Class-E PA [35], can afford dramatically increased power added efficiency (PAE) over current-mode PA topologies. The distinct feature of switched-mode power amplifiers, including the Class E PA, is that the active power devices are used as switches as opposed to transconductors. Figure 2.20 shows the Class E PA principles. Four requirements characterize ideal Class E PA operation: (a) the switch voltage is zero when the switch is ‘ON’; (b) the voltage slope is zero when the switch if first turned ‘ON’;(c) all the current during the ‘OFF’ state is integrated onto the shunt capacitor; and (d) the output tank delivers in phase current and voltage at the fundamental frequency to the load. This guarantees that the voltage and current across the switch are never simultaneously non-zero, and charge is not shunted by the switch during each RF cycle. Therefore, power is dissipated across the switch is minimized and the power at the fundamental is transferred to the load. These requirements can be optimized with proper sizing of the switch device, shunt capacitance, choke inductor, and the high Q-factor output resonant tank [35-37].
A STMicro START499 silicon BJT transistor, ATC RF capacitors, and high Q Coilcraft microCoil inductors were used to implement the Class E RF PA as shown in Figure 2.21. Class E analytical design equations and Cadence Spectrum simulation with component optimization were done to achieve collector efficiency as high as 75% and a PAE of 57%. It was found that using an “L” impedance matching network on the output designed for 20 ohms and input designed for 35 ohms gave optimum PAE results. Figure 2.22 shows Class E PA CW simulation and measurement. Figure 2.23 shows the CW performance of Class E PA at different collector voltages at 2.4 GHz. The optimal EER PA efficiency is formed by peak efficiency point of each of the fixed Vcc efficiency curves. The comparison between EER PA and Class AB PA is also shown in Figure 2.23.

The Hybrid EER system was measured for the WLAN 802.11g power amplifier. Since the EER system has inherent nonlinearity associated with the gain variation, baseband predistortion was implemented to improve the system linearity using a digital pre-distortion described in Section 2.3.4. The envelope amplifier is described in
Section 2.3.2 (more details on the wideband envelope amplifier is discussed in Chapter 4). Figure 2.24 shows a comparison of the measured PA spectrum with and without pre-distortion. Figure 2.25 shows the 64 QAM OFDM signal constellation before and after memory effect pre-distortion. Table 2.5 summaries the comparison of the measured results of the EER amplifier and the constant $V_{dd}$ Class AB RFPA implemented in a GaAs HFET technology for WLAN OFDM signal.

![Figure 2.21: Simplified Class E PA schematic.](image)

![Figure 2.22: Simulation and measurement of Class E PA at 2.36GHz when $V_{cc}=2V$.](image)
Figure 2.23: Measurement of optimal EER PA efficiency obtained by sweeping input power at different collector voltages (under CW condition at 2.4GHz). A constant $V_{dd}$ (6V) HFET Class AB PA measurement at 2.4GHz is shown for comparison.

Figure 2.24: Spectrum before and after pre-distortion at $P_{out}=19\text{dBm}$ (80mW). ACPR is improved by 10 dB after the pre-distortion and memory effect mitigation. The ACPR improvement is limited by the system bandwidth of 40MHz.
Figure 2.25: Constellation of 64QAM OFDM signal at output power 19.56dBm: (a) before pre-distortion, EVM 6.6%; (b) after memory effect pre-distortion, EVM 3%. The required EVM is 5% by 802.11g specifications.
Table 2.5 Summary of “Hybrid” EER, WBET and constant class AB PA with OFDM signal

<table>
<thead>
<tr>
<th></th>
<th>This work “Hybrid” EER</th>
<th>WBET [17]</th>
<th>Traditional Class AB RFPA [16]</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pout</td>
<td>19dBm (80mW)</td>
<td>19.5dBm (90mW)</td>
<td>20dBm (100mW)</td>
</tr>
<tr>
<td>Gain</td>
<td>6.5dB</td>
<td>8dB</td>
<td>9.8dB</td>
</tr>
<tr>
<td>Overall drain/collector efficiency</td>
<td>36%</td>
<td>30%</td>
<td>14%</td>
</tr>
<tr>
<td>Overall PAE</td>
<td>28%</td>
<td>25%</td>
<td>12%</td>
</tr>
<tr>
<td>EVM</td>
<td>2.8%</td>
<td>2.3%</td>
<td>2%</td>
</tr>
</tbody>
</table>

Note: the required EVM is 5% by 802.11 specifications.

Overall drain/collector efficiency = RF modulated output power/envelope amplifier input dc power.

Overall power added efficiency (PAE) = RF modulated output power/envelope amplifier input dc power plus RF input power.

2.5 Summary

A wideband high efficiency ET and hybrid EER power amplifier employing a high efficiency envelope amplifier has been designed and implemented for application to WLAN 802.11g. The efficiency of the envelope amplifier is 50%–60% for WLAN OFDM envelope signals. The hybrid EER overall efficiency is 36% at 19 dBm output power; the PAE is greater than 28%. The wideband ET overall efficiency is 29% at 15 dBm output power; the PAE is greater than 25%. The linearity requirements are met by implementing the baseband pre-distortion technology and adaptive time-alignment. Compared with a Class AB RFPA, both wideband ET and hybrid EER efficiency and PAE is roughly doubled.
Chapter 3
Envelope Tracking and Envelope Elimination and Restoration PAs Time Alignment

A major concern with any supply control amplifier (either ET or EER) is the sensitivity of EVM and distortion to the time mismatch between the two signal paths. In this chapter, we will propose a general model for the time-mismatch analysis for ET and EER systems. The time mismatch sensitivity between the amplitude path and RF path was compared between the ET and EER systems. An adaptive time alignment algorithm was developed for ET system and the simulation and measurement shows the finite time alignment resolution could be smaller than 0.5ns, satisfying the 802.11g OFDM applications.

3.1 Time-Mismatch Analysis

3.1.1 Cann Model

To study the effect of the nonlinearity and time mismatch of the power amplifier, we used the Cann model for the behavior of the nonlinear amplifier [38]:

40
\[ v_o = \frac{g v_{in}}{[1 + \left( \frac{g}{L} v_{in} \right)^s]^s} \]  

(3.1)

where \( g \) and \( L \) are functions of \( V_{DD} \): \( g \) models the small signal gain (in the PA linear region), \( s \) models the transition from the linear to the saturation region and is roughly independent of \( V_{DD} \), and \( L \) models the saturated output value. (the amplifier nonlinear behavior is modeled as AM-AM as (3.1). Compared to AM-AM, AM-PM can be neglected for small devices [14].)

In this case, \( V_o \) and \( V_{in} \) are the RF output and input voltages respectively. Figure 3.1 compares the \( V_{out} \) vs. \( V_{in} \) for differing \( V_{DD} \) by ADS simulation of the circuit described in and the Cann model. Figure 3.2 compares the ET system’s simulated AM-AM performance with ADS simulation and ET model simulation. The excellent agreement demonstrates that the higher level model is useful for system level design of the Cann system. With this model the time-mismatch sensitivity can be analyzed.
Figure 3.1: Comparison of ADS simulation and Cann model of the GaAs MESFET PA. A least-squares fit to the simulation data provides $g \approx 1.24 + 0.38V_{DD}$, $L \approx 0.09 + 1.15V_{DD}$, and $s \approx 5$.

Figure 3.2: ET system AM/AM simulation by ADS and Cann model simulation.
3.1.2. Time Mismatch Analysis

The relative simplicity of the two-tone test signal eases the mathematical analysis of sensitivity of the EER and ET systems to the time mismatch (between the amplitude path and RF path). The two-tone modulated RF signal is defined by:

\[ s_{RF}(t) = \cos \omega_m t \cos \omega_c t \quad (3.2) \]

where \( \omega_m \) is baseband modulation frequency, and \( \omega_c \) is the RF carrier frequency.

Thus, the baseband signal of the two-tone RF signal is:

\[ s_{BB}(t) = \cos \omega_m t = A(t) \cdot e^{j\phi(t)} \quad (3.3) \]

where the amplitude and phase signals are:

\[ A_m(t) = |\cos(\omega_m t)| \quad (3.4) \]

\[ \phi_m(t) = \frac{\pi}{2} [1 - c(\omega_m t)] \quad (3.5) \]

\( c(\omega_m t) \) is a square wave with a value of +1 or -1 with the same period as the modulation frequency. Expansion of the amplitude signal as a Fourier series produces:

\[ A(t) = a_0 + \sum_{n=2,4,6,...} a_n \cos(n\omega_m t) \quad (3.6) \]
where

\[ a_n = 2 / \pi; \quad a_n = \frac{4 \ (-1)^{(n-2)/2}}{\pi (n^2 - 1)} \quad n = 2, 4, 6, \ldots \tag{3.7} \]

If the time mismatch between the baseband amplitude and the RF phase path is \( \tau \) for an EER system, then \( A_{\text{out}}(t) = A_{\text{in}}(t - \tau) \), \( \varphi_{\text{out}}(t) = \varphi_{\text{in}}(t) \). And, therefore,

\[ s_{BB,\text{out}}(t) = A_{\text{in}}(t - \tau) \cdot e^{j\varphi_{\text{in}}(t)} \tag{3.8} \]

Figure 3.3 shows the simulated EER amplitude signal, phase signal, distorted output baseband signal, and error signal for a two-tone input with a time mismatch of 2.5ns. The distorted output baseband signal indicates that, even for the ideal EER system, a time mismatch between the amplitude and phase produces error and intermodulation distortion. According to Raab [39] and Su [9], for small delay, the magnitude of the intermodulation distortion introduced by the time mismatch for a two-tone signal is

\[ \text{IMD} \approx (2 / \pi) B_{RF} \tau^2 \tag{3.9} \]

where \( B_{RF} \) is the bandwidth of the two-tone signal: \( B_{RF} = 2\omega_m / 2\pi \); and \( \tau \) is the time mismatch between the baseband amplitude and RF phase.

By contrast, the output envelope of the WBET system is (from (3.1))
\[ A_{sat}(t) = \frac{g(V_{DD}(t)) \cdot A_{in}(t)}{[1 + \frac{g(V_{DD}(t))}{L(V_{DD}(t))}A_{in}(t)]^{s}} \]  

(3.10)

where \( V_{DD}(t) \) is the dynamic drain voltage and it is a linear time delayed function of the input envelope signal, i.e.

![Figure 3.3: Simulated two-tone EER system with time mismatch between baseband amplitude and RF phase. The modulation frequency is 20MHz, and the baseband amplitude path time delay is 2.5 ns.](image)

\[ V_{DD}(t) = V_{\text{min}} + kA_{in}(t - \tau) \]  

(3.11)

The quantities \( g(V_{DD}) \) and \( L(V_{DD}) \) are functions of dynamic drain voltage \( V_{DD} \) (extracted in Figure 3.1.) as:
\[ g(V_{DD}) = g_0 + g_1 \cdot V_{DD} \]  
(3.12)

\[ L(V_{DD}) = L_0 + L_1 \cdot V_{DD} \]  
(3.13)

Since the WBET amplifier is nonlinear, pre-distortion is implemented in our proposed system. To focus on the distortion caused by the time mismatch and the resulting nonlinear limiting behavior, we assume the pre-distortion is ideal, and any intermodulation and harmonic products generated by the nonlinearity of (3.10) will therefore be eliminated. However, nonlinear distortion is then re-introduced due to the time-mismatch of the amplitude and RF signals. As a result of the pre-distortion, the Cann model parameter \( s \) approaches infinity, and the denominator of (3.10) becomes a “hard limiter,” i.e.

\[
A_{out}(t) = \begin{cases} 
  g(V_{DD}(t)) \cdot A_{in}(t) & g(V_{DD}(t))A_{in}(t) \leq L(V_{DD}(t)) \\
  L(V_{DD}(t)) & g(V_{DD}(t))A_{in}(t) > L(V_{DD}(t))
\end{cases}
\]  
(3.14)

By calculating the linear delayed amplitude signal before hard limiting and then limiting the resulting signal as shown in Figure 3.4, the output amplitude signal is shown in Figure 3.5.
Figure 3.4: Simplified ET system block diagram. The time mismatch between the baseband amplitude and RF amplitude/phase is $\tau$.

Figure 3.5: Two-tone ET system with time mismatch between baseband amplitude and RF amplitude/phase. The modulation frequency is 20MHz, and the baseband amplitude path time delay is 2.5 ns.
Prior to hard limiting, the amplitude of the RF output signal is:

$$A_{delay}(t) = g(V_{DD}(t)) \cdot A_{in}(t)$$ (3.15)

Substituting (3.11) and (3.12) into (3.15), the amplitude of the RF output signal is:

$$A_{delay}(t) = g_0 A_{in}(t) + g_1 A_{in}(t) \cdot [V_{min} + kA_{in}(t - \tau)]$$

$$= (g_0 + g_1 V_{min}) A_{in}(t) + g_1 kA_{in}(t) A_{in}(t - \tau)$$ (3.16)

Note that in (3.16) the delayed magnitude signal $A_{delay}(t)$ is a nonlinear function of $A_{in}(t)$: the multiplication of $A_{in}(t)A_{in}(t - \tau)$ will generate intermodulation products. However, the pre-distortion will eliminate those nonlinear terms, leaving a remaining linear but delayed result.

The multiplication of $A_{in}(t)A_{in}(t - \tau)$ is described as (from (3.6)):

$$A_{in}(t)A_{in}(t - \tau) = \left(a_0 + \sum_{n=2,4,6,\ldots} a_n \cos(n\omega_m t)\right) \cdot \left(a_0 + \sum_{n=2,4,6,\ldots} a_k \cos(n\omega_m (t - \tau))\right)$$ (3.17)

From the above, the linear product of the multiplication is

$$DC + a_0 \sum_{n=2,4,6,\ldots} a_n \left[\cos(n\omega_m t) + \cos(n\omega_m (t - \tau))\right]$$ (3.18)

where DC represents the sum of all the dc components resulting from the mismatch, and the nonlinear part is
\[
\sum_{n=2,4,6,\ldots} a_n \cos(n\omega_m t) \cdot \sum_{k=2,4,6,\ldots} a_k \cos(k\omega_m (t - \tau))
\] (3.19)

Adding (3.18) to (3.16) yields

\[
A_{\text{delay}}(t) = DC + (g_0 + g_1 V_{\text{min}}) \sum_{n=2,4,6,\ldots} a_n \cos(n\omega_m t) \\
+ g_1 k a_0 \sum_{n=2,4,6,\ldots} a_n [\cos(n\omega_m t) + \cos(n\omega_m (t - \tau))] \\
= DC + (g_0 + g_1 V_{\text{min}} + g_1 k a_0 + g_1 k a_0 \cos n\omega_m \tau) \sum_{n=2,4,6,\ldots} a_n \cos(n\omega_m t) \\
+ g_1 k a_0 \sin n\omega_m \tau \sum_{n=2,4,6,\ldots} a_n \sin(n\omega_m t) \\
= DC + \sum_{n=2,4,6,\ldots} c_n' a_n \cos(n\omega_m (t - \tau_{\text{eff}}))
\] (3.20)

where

\[
c_n' = \sqrt{c_n^2 + d_n^2}
\] (3.21)

\[
c_n = g_0 + g_1 V_{\text{min}} + g_1 k a_0 + g_1 k a_0 \cdot \cos n\omega_m \tau
\] (3.22)

\[
d_n = a_0 g_1 k \cdot \sin n\omega_m \tau
\] (3.23)

\[
\tau_{\text{eff}} = \frac{1}{n\omega_m} \tan^{-1} \left( \frac{d_n}{c_n} \right)
\] (3.24)

Assuming the time mismatch \( \tau \) is very small
\[ \tau_{\text{eff}} \approx \frac{a_0 g_1 k}{g_0 + g_1 V_{\text{min}} + g_1 k a_0 + g_1 k a_0} \cdot \frac{\tau}{F} = \tau \]  \tag{3.25}

where the factor \( F \) represents the desensitization factor of the time mismatch in an ET system, i.e.

\[ F = \frac{g_0 + g_1 V_{\text{min}} + 2 g_1 k a_0}{a_0 g_1 k} \approx 2 + \frac{g_0}{a_0 g_1 k} \]  \tag{3.26}

where \( g_1 V_{\text{min}} \) is small (for this example, \( g_0 = 1.24, g_1 = 0.38, V_{\text{min}} = 0.37 \)). By comparison, the value of \( F \) for an EER system is unity and the value of desensitization factor \( F \) for an ET system is always greater than two.

From (3.21)-(3.24) \( c'_n \) represents a linear amplification of the original signal, and therefore

\[ A_{\text{delay}}(t) = G \cdot A_n(t - \frac{\tau}{F}) \]  \tag{3.27}

where \( G \) represents the linear gain between the input and output magnitude signals:

\[ G = c'_n = \sqrt{c^2_n + d^2_n} \approx g_0 + 2 g_1 k a_0 \]  \tag{3.28}

Limiting may then occur if there is a significant time mismatch between the baseband amplitude signal and the RF signal. This effect is shown in Figure 3.5 and Figure 3.6, where the mismatch between the RF amplitude/phase input and the baseband amplitude amplifier leads to severe distortion. This can be modeled by
substituting (3.11), (3.13), (3.15) and (3.27) into (3.10). Then, the normalized ET output amplitude signal is:

\[
A_{\text{out\_norm}}(t) = \begin{cases} 
A_{\text{in}}(t - \frac{\tau}{F}) & \text{if } A_{\text{in}}(t - \frac{\tau}{F}) \leq \frac{L_1 k A_{\text{in}}(t - \tau)}{G} \\
\frac{L_1 k A_{\text{in}}(t - \tau)}{G} & \text{if } A_{\text{in}}(t - \frac{\tau}{F}) > \frac{L_1 k A_{\text{in}}(t - \tau)}{G}
\end{cases}
\]  

(3.29)

As an example, we extracted the Cann parameters from the ADS simulations of the circuit described in the Section 2.3.1 and extracted \( g_0 = 1.24, g_1 = 0.38, V_{\text{min}} = 0.37, \) \( k = 2, L_0 = 0.1, L_1 = 1.15. \) Substituting the above parameters into (3.26) and (3.28) we obtained \( \bar{F} = 4.5, \bar{G} = 2.2 \) and \( \frac{L_1 k}{G} = 1.05 \), the normalized ET output amplitude is:

\[
A_{\text{out\_norm}}(t) = \begin{cases} 
A_{\text{in}}(t - \frac{\tau}{F}) & \text{if } A_{\text{in}}(t - \frac{\tau}{F}) \leq 1.05 A_{\text{in}}(t - \tau) \\
1.05 A_{\text{in}}(t - \tau) & \text{if } A_{\text{in}}(t - \frac{\tau}{F}) > 1.05 A_{\text{in}}(t - \tau)
\end{cases}
\]  

(3.30)

Figure 3.5 also shows the comparison between the theoretical calculation and Cann model simulation, and the two agree well. Figure 3.6 shows the RF input amplitude signal, the normalized linear delayed amplitude signal after amplification but before limiting (refer to Figure 3.4), the normalized limiting signal (the delayed amplitude amplifier output) \( L(V_{\text{DD}}(t))/G \), and the normalized output RF amplitude signal after limiting. From Figure 3.6, during approximately half of the cycle, the output amplitude signal is the same as the linear delayed amplitude signal, which has a delay of \( \tau/F \) as shown earlier. During the other half of the period, the output is
limited by the drain amplitude signal, which has a delay of $\tau$. Thus, the normalized output amplitude signal can be approximated by a simple expression, i.e.

$$A_{\text{out\_norm}}(t) \approx A_{\text{in}}(t - \frac{\tau}{F/\alpha})$$

(3.31)

where $\alpha$ is the “limiting effect factor” and $F/\alpha$ is approximately two for the two-tone signal, since the amplitude signal is limited by the envelope delay during half the period only.

![Figure 3.6: Simulation of two-tone ET amplifier with time delay mismatch. Note the distortion in the output amplitude due to the time mismatch between the baseband amplifier and RF amplitude signals and the limiting action of the amplifier. The baseband amplitude path time delay is 2.5 ns](image-url)
Finally, from (3.31), the complex normalized baseband output signal is:

\[ s_{BB,\text{out norm}}(t) \approx A_{in}(t - \frac{\tau}{F/\alpha}) \cdot e^{j\phi_{in}(t)} \]  

(3.32)

Comparing (3.32) (the ET output signal) with (3.8) (the EER output signal), the time mismatch between the baseband amplitude path and RF path for ET system is decreased (desensitized) by a factor of \( F/\alpha \), thus the IMD magnitude is decreased by a factor of \((F/\alpha)^2\) compared to (3.9) for EER. Figure 3.7 compares the error signal standard deviation between EER simulation, ET Cann simulation, the theoretical calculation with limiting effect by using (3.29), and the equivalent theoretical calculation by using (3.31) for a two-tone test signal. The ET simulation agrees with the theoretical analysis very well when the time mismatch is less than three nanoseconds. Beyond three nanoseconds, due to the nonideal predistortion, the simulation shows a larger error signal standard deviation than the theoretical calculations. Figure 3.8 compares the Cann simulation and the equivalent theoretical calculation by using (3.31) for 802.11g signal.

For example, suppose \( F \) is infinite, then the linear delayed amplitude signal will overlay with the original RF input amplitude signal. From Figure 3.6, during half of the cycle, the output amplitude signal is the same as the RF input amplitude signal, which has a delay of zero, during the other half of the time, the output is limited by the drain amplitude signal, which has a delay of \( \tau \). Thus, the normalized output envelope signal is delayed by \( \tau/2 \).
Figure 3.7: Two-tone error signal standard deviation vs. time mismatch for EER system and ET system. Note the EER is more sensitive to path mismatch effects than the ET system. The simulation results deviate from the theory at high mismatch values due to the high time-mismatch for the higher order harmonic components and nonideal predistortion.

To summarize the results of this Section, we have derived an expression for the “effective” time alignment mismatch between the amplitude (drain) and RF (gate) signals of an envelope tracking amplifier, based on the Cann nonlinear model, assuming ideal pre-distortion. It was demonstrated that the ET amplifier is significantly less sensitive than the traditional EER amplifier to this misalignment – a crucial benefit for wide bandwidth operation. These results agree well with detailed simulation results, as well as measured results (refer to Section 3.3), and can be used to estimate the resulting errors in a complete system. The next Section will suggest an algorithm to precisely time-align the amplitude and RF signals.
Figure 3.8: The simulation and theory analysis of the ET system for the time mismatch sensitivity for WLAN 802.11g signal. The Cann model simulation agrees very well with the theory analysis if $F=2$. In this case, the envelope time delay is 10ns, and from the above graphic, the effective time delay is about 5ns.

3.2 Adaptive Time Alignment Algorithm

As shown in the previous Section, time alignment is required for the ET system to align the baseband amplitude path and RF path, especially for wideband OFDM signals. An adaptive real-time time-alignment technique is needed because of inevitable environmental variations. A time alignment of better than two nano-seconds is required to make the EVM lower than 3% for an OFDM 802.11a/g signal. In this case, the signal bandwidth is approximately 20 MHz, and with a data converter sample rate of approximately 100MHz, linear interpolation will be required to achieve the necessary sub-sample delay accuracy.
Referring to Figure 2.14, we first calculate the covariance between the original amplitude signal and the down converted feedback signal. The covariance is calculated for amplitudes of $s_{in}$ and $s_{out}$ as:

$$C_{A_{in}, A_{out}}(L) = E[(A_{in}(t + L) - \mu_{A_{in}}) \cdot (A_{out}(t) - \mu_{A_{out}})]$$

(3.33)

where $E$ is the expectation operator, $\mu_{A_{in}}$ and $\mu_{A_{out}}$ represent the mean value of the input amplitude signal $A_{in}$ and output amplitude signal $A_{out}$. The parameter $L$ is the time offset of the covariance (note this $L$ is different from the Cann model parameter “$L$” in the previous Section) and $L_{\text{max}}$ is the time offset corresponding to the maximum covariance. For example, Figure 3.9 shows the simulated covariance of $A_{in}$ and $A_{out}$ for different values of $T_{\text{env}}$, $T_{RF}$ and $T_{FB}$ for an 802.11a/g OFDM signal applied to the envelope tracking amplifier described in the previous Section. This information can be used to time-align the amplitude and RF signals.

Figure 3.10 shows the simulated EVM (Figure 3.10(a)) and $L_{\text{max}}$ (Figure 3.10(b)) vs. $T_{\text{env}}$ for different values of $T_{RF}$ when $T_{FB}$ is zero. As expected, the minimum in the EVM occurs when $T_{\text{env}}$ is equal to $T_{RF}$. From Figure 3.10, in the case where $T_{FB}$ equals zero,

$$L_{\text{max}} \approx -\frac{T_{RF} + T_{\text{env}}}{2}.$$  

(3.34)
Figure 3.9: Simulated covariance of RF input amplitude $A_{in}$ and RF output amplitude $A_{out}$ (refer to Eq. (3.33)) for different values of $T_{env}$, $T_{RF}$, and $T_{FB}$ for OFDM 802.11g signal. Note that the peak of the covariance occurs at the sum of $T_{FB}$ and a weighed average of $T_{env}$ and $T_{RF}$.

However, in practice, the practical feedback path time-delay $T_{FB}$ is not zero, due to the various filters in the RF path and other components. Figure 3.11 shows the simulated $L_{max}$ and EVM vs. $T_{env}$ for different values of $T_{RF}$ and $T_{FB}$. From Figure 3.11, the function of $L_{max}$ vs. $T_{env}$, $T_{RF}$ and $T_{FB}$ is

$$L_{max} \approx - (T_{FB} + \frac{T_{RF} + T_{env}}{2}).$$

(3.35)

and the general expression for $L_{max}$ is

$$L_{max} \approx -(T_{FB} + T_{RF} + \frac{T_{env} - T_{RF}}{F/\alpha}).$$

(3.36)
Figure 3.10: Simulated EVM (a) and \( L_{\text{max}} \) (b) (\( T_{\text{FB}} \) is zero). \( L_{\text{max}} \approx -T_{\text{env}}/2 \) (for \( T_{\text{RF}} = 0 \)); \( L_{\text{max}} \approx -1/4 - T_{\text{env}}/2 \) (for \( T_{\text{RF}} = 0.5 \) samples); \( L_{\text{max}} \approx -1/2 - T_{\text{env}}/2 \) (for \( T_{\text{RF}} = 1 \) samples).
Figure 3.11: Simulated EVM and $L_{\text{max}}$ for variations in $T_{FB}$. Note that the minimum EVM occurs when $T_{\text{env}} = T_{RF}$, and $L_{\text{max}} = -T_{FB}(T_{RF} + T_{\text{env}})/2$.

which represents the weighting of the time-delay of the baseband amplitude and RF signal when applied to the ET amplifier. This agrees with the previous section analysis that the effective amplitude delay of the ET system is approximately the average of the time mismatch between the baseband amplitude path delay and RF path delay (i.e, $F/\alpha$ is approximately two).

Given that we can determine $L_{\text{max}}$ by experimentally measuring the maximum of the covariance, we then compensate for the delay mismatch between baseband amplitude and RF amplitude by delaying the complex baseband signal $s_{\text{in}}(t) = s_{\text{in}}(t-L_{\text{max}})$. Before this compensation the output phase signal is $\varphi_{\text{out}}(t) = \varphi_{\text{in}}(t - T_{RF} - T_{FB})$. 
After this delay mismatch compensation is completed, the output phase signal becomes:

\[
\varphi_{\text{out}}(t) = \varphi_{\text{in}}(t - T_{\text{RF}} - T_{\text{FB}} - L_{\text{max}}) = \varphi_{\text{in}}(t - \frac{T_{\text{RF}} - T_{\text{env}}}{F/\alpha})
\]  

(3.37)

The \textit{rms} value of the difference between the input and output phase signal (phase error signal) after delay compensation is:

\[
e(t, PL) = \varphi_{\text{in}}(t) - \varphi_{\text{out}}(t - PL)
\]  

(3.38a)

\[
C_{\varphi_{\text{in}} - \varphi_{\text{out}}}(PL) = \sqrt{\frac{1}{T} \int (e(t, PL) - \overline{e(t, PL)})^2 \, dt}
\]  

(3.38b)

where \( PL \) is defined the time offset and \( \overline{e(t, PL)} \) represents the mean value of the error signal.

Figure 3.12 shows the simulated error signal standard deviation vs. \( PL \) for different \( T_{\text{env}}, T_{\text{RF}}, \) and \( T_{\text{FB}}. \) \( PL_{\text{min}} \) is the value of \( PL \) corresponding to the minimum rms error signal. Figure 3.13 shows the simulated value of \( PL_{\text{min}} \) as a function of \( T_{\text{env}} \) for different values of \( T_{\text{RF}} \) and \( T_{\text{FB}}. \) Note that – as expected - \( PL_{\text{min}} \) is equal to zero when \( T_{\text{env}} \) is equal to \( T_{\text{RF}} \) and this result is independent of \( T_{\text{FB}}. \)

Another way of looking at this result is shown in Figure 3.14, where the simulated value of \( PL_{\text{min}} \) vs. \( (T_{\text{RF}} - T_{\text{env}}) \) is plotted for different values of \( T_{\text{FB}} \) and \( T_{\text{RF}}. \)
Note that the average slope of $PL_{min}$ vs. $(T_{RF} - T_{env})$ is approximately 0.5, which agrees well with (3.37) when $F/\alpha=2$. From Figure 3.12 to Figure 3.14, we can see that $PL_{min}$ is only dependent on the time difference between $T_{RF}$ and $T_{env}$ and it is independent of the values of $T_{env}$, $T_{RF}$ and $T_{FB}$. Thus the time alignment scheme that we have outlined here is very robust to the inevitable variations in these parameters.

![Figure 3.12: Simulated rms phase error for different values of $T_{env}$, $T_{RF}$, and $T_{FB}$. Note that the curve of $T_{env}=0$, $T_{RF}=9.3$ ns and $T_{FB}=0$ overlay with the curve of $T_{env}=0$, $T_{RF}=9.3$ ns and $T_{FB}=9.3$ ns. Therefore, the phase error is relatively insensitive to $T_{FB}$.


Figure 3.13: Simulated value of $PL_{\text{min}}$ as a function of $T_{\text{env}}$. The value of $T_{\text{env}}$ where $PL_{\text{min}}$ crosses zero is equal to $T_{RF}$, and its value is independent of $T_{FB}$.

Figure 3.14: Simulated value of $PL_{\text{min}}$ vs. the time mismatch between $T_{RF}$ and $T_{\text{env}}$. Note that this is independent of $T_{FB}$.
3.3 Measurements

The time-alignment model and algorithm is tested with wideband ET and hybrid EER systems discussed in Chapter 2. The WLAN baseband OFDM signal is upconverted digitally to an IF of 26.88 MHz at a sample rate of 107.52 MHz. Then, by a Xilinx FPGA running at 200MHz and a dual port RAM, the digital IF signal, as well as the amplitude signal, are output to two 107.52 MHz 14 bit D/A converters. The IF signal is then up-converted to 2.4GHz, and amplified by the ET amplifier. The output RF signal is down-converted to an IF of 26.88 MHz and digitized by a 107.52MHz 12 bit ADC and a buffer (a logic analyzer). Figure 3.15 shows the comparison between the theoretical calculation using (3.31), simulation and measurement of the EVM of a WBET amplifier for an OFDM 802.11g signal. The agreement between the experimental data, the simulations, and calculations, is excellent. From Figure 3.15, the EVM is a linear function of the time-mismatch \( \tau \) i.e.

\[
EVM = \beta \cdot \tau
\]

(3.39)

where the proportionality factor \( \beta \) for EER is roughly six, and for ET, since the effective delay is half of the time mismatch between the envelope path and RF path, the proportionality factor is only three. Compared with the ET system, the EER system’s EVM is approximately twice as sensitive to the time-mismatch. The measurement results agree well with the results predicted in (3.31).
Figure 3.15: Simulation and measurement of EVM vs. baseband amplitude path time-delay for ET and EER system for 802.11g signal. The measurement is made with the GaAs MESFET RF PA with $P_{out} = 15\text{dBm}$. Note that the measured slope of the EVM vs. time mismatch agrees well with the theory. The measured minimum error floor of 3% is due to other impairments in the RF path unrelated to the time-mismatch.

Figs. 3.16 and 3.17 show the measured EVM and $PL_{min}$ vs. the time-mismatch between the RF path and baseband amplitude path before and after pre-distortion. Note that the average slope of $PL_{min}$ vs. the time mismatch is approximately 0.5 for the time mismatch +/- 20 ns around 1110 ns, which agrees well with the theory of $F/\alpha = 2$ for 802.11g signal (refer to (3.37)). Comparing Figure 3.17 with Figure 3.14, the measurement results agree with the simulation and theory very well, and the zero-crossing of $PL_{min}$ is independent of the output power. Figure 3.18 shows the measured EVM with the time-mismatch between the RF path and envelope path for hybrid EER described in section 2.4. Note the similar time-alignment feature between hybrid EER and ET.
Figure 3.16: Measured EVM vs. baseband amplitude path time-delay $T_{env}$ for WLAN 802.11g application (data rate 54Mpbs). The minimum EVM indicates the time difference between the RF path and baseband amplitude path is approximately 1110 ns.

Figure 3.17: Measured $PL_{min}$ vs. baseband amplitude path time-delay $T_{env}$ for WLAN 802.11g application (data rate 54Mpbs). The zero-crossing of $PL_{min}$ indicates the time difference between the baseband amplitude path and RF amplitude/phase path is approximately 1110 ns, which agrees well with the result from Figure 3.14. Note that the average slope of $PL_{min}$ vs. the time mismatch is approximately 0.5, which agrees well with the theory of $\frac{\Delta f}{\Delta \alpha} = 2$ for 802.11g signal.
Figure 3.18: “Hybrid” EER system time-alignment feature.

3.4 Summary

A general mathematical model was proposed to study the time alignment requirement for the ET system. The time mismatch sensitivity between the amplitude path and RF path was compared between the ET and EER systems. The simulation and measurement for the two-tone signal and WLAN OFDM signal generally verify the simple ET system model and the analysis. An adaptive time alignment algorithm was developed for ET and hybrid EER systems and the simulation and measurement shows the fine time alignment resolution could be smaller than 0.5ns, satisfying the 802.11g OFDM requirements.

This chapter, in part or in full, is a reprint of the material as it appears in “Design of wide-bandwidth envelope-tracking power amplifiers for OFDM applications,” IEEE Trans. Microwave Theory Tech, April 2005. The dissertation author was the primary researcher and the first author listed in these publications.
Chapter 4
High Efficiency Wideband Envelope Amplifier Design

The use of dynamic supply control in EER and ET can boost the RF PA drain/collector average efficiency, but the total system efficiency is determined by the product of the envelope amplifier efficiency and the RF transistor drain/collector efficiency. Thus a high-efficiency envelope amplifier design is critical to the EER/ET system. The high efficiency envelope amplifier is usually realized by a DC/DC converter, and the switching frequency is required to be several times the signal bandwidth [2, 39]. For narrow bandwidth applications, most high efficiency switching mode DC/DC converters are realized by traditional delta-modulation [9, 32, 40, 41] or pulse width modulation (PWM) [13, 42, 43] modulators. However, the high switching frequency will introduce a significant switching loss for a wideband signal. For example, a 20 MHz envelope bandwidth is required in ET PA for a WLAN OFDM signal for low EVM as simulated in Figure 4.1, so the switching frequency of the traditional DC/DC converter will be at least 100 MHz, which introduces a significant switching loss [2].
To overcome the trade-off between the efficiency and bandwidth of the traditional DC/DC converter, a switching-mode envelope amplifier assisted by linearization is proposed in [44-45]. The structure is based on feed-forward topology, which requires a time-alignment between the switch and linear parts and a power combiner at the output of the envelope amplifier.

![Figure 4.1: Simulated envelope amplifier bandwidth requirement for an 802.11g signal in ET and EER systems.](image)

In this chapter, the proposed wideband high efficiency envelope amplifier uses hysteretic current feedback control. This topology is a derivative of Rectangular Wave Delta Modulation (RWDM) [46-48] and has been used in audio amplifier applications, where it was originally proposed to improve the fidelity of the class-D audio amplifier [49-54]. We revisit this topology in this paper for wideband EER/ET applications. Section 4.1 characterizes the spectrum of the envelope signal to illustrate the mechanics of the high efficiency wideband envelope amplifier. Section 4.2
investigates the principle of the proposed wideband envelope amplifier and an expression for the average switching frequency is developed. In Section 4.3 the design of an envelope amplifier for 802.11g applications is discussed. In Section 4.4 the efficiency is analyzed and simulated for the envelope amplifier. The analysis and simulation results are validated in Section 4.5 by experimental measurements.

4.1 Envelope Signal Power Spectrum Characteristics

Figure 4.2 shows the spectra of the WLAN OFDM envelope signal $A(t)$ and the signal energy distribution. The nonlinear transformation from $I(t)$ and $Q(t)$ to the envelope signal $A(t)$ will expand the envelope signal bandwidth to infinity. However, most of the energy is concentrated from DC to several kHz (e.g., more than 85% for an OFDM waveform), and 99% of the energy is concentrated below the signal RF bandwidth of 20MHz. This characteristic of the signal energy implies that a “split-band” envelope amplifier can achieve a high efficiency over a wide bandwidth. The split-band envelope amplifier is composed of a wideband (but rather low efficiency) linear stage and a high-efficiency narrowband switch stage, where the overall efficiency is a combination of the two efficiencies, i.e. [44, 55],

$$\eta_{EA, ave} = 1/[\alpha/\eta_{sw, ave} + (1-\alpha)/\eta_{lin, ave}]$$ (4.1)

where the overall average efficiency $\eta_{EA, ave}$ (the envelope amplifier output power/envelope amplifier input dc power) dependent on the switch stage efficiency $\eta_{sw, ave}$ (the switch stage output power/switch stage input dc power) and linear stage
efficiency $\eta_{lin, ave}$ (the linear stage output power/linear stage input dc power), as well as on the power ratio $\alpha$, which is defined as the ratio of the signal power from the switch stage to the total signal power [44].

Figure 4.2: (a) Spectrum of OFDM envelope signal; (b) OFDM envelope signal energy cumulative distribution.

4.2 Principle of High Efficiency Wideband Envelope Amplifier Operation

A hysteretic current feedback control is used to realize the smooth power split between switch stage and linear stage amplification. The topology of the wideband envelope amplifier is composed of a linear stage voltage source $V_s$ in parallel with a switch stage current source $i_{sw}$ as shown in Figure 4.3. The load voltage $V_o$ is
controlled by the linear voltage source \( V'_L \); the load current \( i_{\text{load}} \) is a combination of the linear stage current \( i_{\text{lin}} \) and the switch stage current \( i_{\text{sw}} \), i.e.,

\[
\begin{align*}
  i_{\text{lin}} &= i_{\text{load}} - i_{\text{sw}} \\
  i_{\text{load}} &= \frac{V_s}{R_{\text{load}}} \quad \Rightarrow i_{\text{lin}} \to 0 \text{ when } i_{\text{sw}} \to \frac{V_s}{R_{\text{load}}} 
\end{align*}
\]  

(4.2)

Figure 4.3: Envelope amplifier design; ideal circuit model of the voltage-controlled current-parallel envelope amplifier.

Figure 4.4: Envelope amplifier design; the circuit implementation.
Figure 4.4 shows the circuit implementation of the envelope amplifier using an op-amp as the linear voltage source and buck converter as the current source (switch stage). The hysteresis current feedback control is composed of a current sense resistor $R_{\text{sense}}$, which senses the current direction and a hysteresis comparator to control the single-pole-double-throw switch, consisting of a PMOS device and a diode. When the P-MOSFET switch is turned on, the voltage at the cathode of the diode is $V_{DD}$ and thus the diode is off. When the P-MOSFET switch is turned-off, the inductor tends to turn on the diode. The current flowing through the linear stage is minimized as an error signal in the current feedback.

This description of the operation is accurate when the switch noise generated in the switch stage is filtered out by the linear stage and the input envelope signal is within the “slew rate” limitation of the switch stage. The instantaneous and average slew rates of the switch and load currents are defined as:

$$SR_{i_{\text{sw}}}(t) = \frac{\Delta i_{\text{sw}}(t)}{\Delta t} = \frac{1}{L} \left( V_{\text{sw}}(t) - V_o(t) \right)$$  \hspace{1cm} (4.3a)

$$SR_{i_{\text{load}}}(t) = \frac{\Delta i_{\text{load}}(t)}{\Delta t} = \frac{1}{R_{\text{load}}} \left( \frac{\Delta V_{\text{c}}(t)}{\Delta t} \right)$$  \hspace{1cm} (4.3b)

$$SR_{i_{\text{sw, ave}}} = \overline{SR_{i_{\text{sw}}}} \approx \frac{2}{L} (1-D)V_{s_{\text{ave}}}$$.  \hspace{1cm} (4.3c)

$$SR_{i_{\text{load, ave}}} = \overline{SR_{i_{\text{load}}}} = \frac{1}{R_{\text{load}}} \overline{\frac{\Delta V_{\text{c}}}{\Delta t}}$$  \hspace{1cm} (4.3d)
where $V_{sw}$ and $V_o$ are the voltages at the switch node and output node (refer to Figure 4.4), $R_{load}$ is the load resistor, $i_{sw}$ and $i_{load}$ are the switch and load currents, $SR_i_{sw}$ and $SR_i_{load}$ are the instantaneous slew rates of the switch and load currents, $SRi_{sw\_ave}$ and $SRi_{load\_ave}$ are the average slew rates of the switch and load currents, the envelope signal average duty ratio $D = V_{s\_dc}/V_{DD}$, $V_{s\_dc}$ is the average of the envelope signal $V_s$, and $V_{DD}$ is the supply voltage.

When the load current average slew rate (4.3d) is much smaller than the switch current average slew rate (4.3c), we define the envelope signal as “small-signal” and the circuit operates in the linear region; when (4.3d) is much larger than (4.3c), the switch stage enters the “voltage saturation” region and the linear stage provides significant signal current to the load, thus the circuit operates in the large-signal nonlinear region; when (4.3c) equals to (4.3d), the circuit operates in the so-called “matched slew-rate” point.

The block diagram of the model of the circuit is shown in Figure 4.5. The transient response of the wideband envelope amplifier is a highly nonlinear phenomenon. Figure 4.6 shows the mathematical behavioral model of the circuits for simulations. Since the general behavioral model is based on time differential equation, switch control conditions, KCL and KVL, the simulation based on Figure 4.6 will reflect the real circuit behavior no matter whether it works in the linear region for small-signal or nonlinear region for large-signal.
Figure 4.5: Block diagram of hysteresis current feedback control.

Figure 4.6: Mathematical behavioral model of the envelope amplifier, where $h$ is the hysteresis voltage of the comparator (assuming the op-amp is an ideal voltage source with infinite bandwidth, and the PA is modeled as a simple resistor $R_2$).

To fully understand the circuit behavior, we separate the analysis into the following three cases:
4.2.1 Case I: Linear Operation for Small-Signal Envelopes

In this case, the envelope signal slew rate is within the slew rate limitation of the switch current. The simplicity of the single-tone envelope signal eases the analysis, i.e.,

$$V_s(t) = V_{s,dc} + V_{s,ac} \sin(2\pi f_s t)$$

(4.4)

where $V_{s,dc}$ is the dc component of the envelope signal, $V_{s,ac}$ is the amplitude of the sinewave (note that for an envelope signal $V_{s,dc}$ is always greater than $V_{s,ac}$), $f_s$ is the envelope sinewave frequency. At output node $V_o$ (refer to Figure 4.4):

$$\frac{V_s(t) - V_o(t)}{R_{sense}} + i_{sw}(t) = \frac{V_s(t)}{R_{load}}$$

(4.5)

The switch current (inductor current) $i_{sw}(t)$ is composed of the switch noise current $i_{sw\_noise}(t)$ and signal current $i_{sw\_signal}(t)$, where the signal current is defined as $V_s(t) / R_{load}$, hence:

$$i_{sw}(t) = i_{sw\_signal} + i_{sw\_noise} = \frac{V_s}{R_{load}} + i_{sw\_noise}$$

(4.6)

Substituting (4.6) into (4.5):

$$V_o(t) - V_s(t) = \frac{R_{sense} R_{load}}{R_{sense} + R_{load}} i_{sw\_noise} \approx R_{sense} i_{sw\_noise} \text{ if } R_{sense} \ll R_{load}$$

(4.7)
For small-signal operation:

\[ \left| R_{\text{sense}} i_{\text{sw_noise}} \right| \leq h \quad (4.8) \]

where \( h \) is the hysteresis value of the comparator in Figure 4.4. Hence, for small values of \( h \)

\[ V_o(t) \approx V_s(t) \quad (4.9) \]

For the circuit designer, the switching frequency is a primary figure of merit since it determines the switch stage efficiency. To develop an expression for the switching frequency, we set the ac component of the envelope signal to zero. Then the input envelope signal is:

\[ V_s(t) = V_{s_{dc}} = D \cdot V_{DD} \quad (4.10) \]

where \( V_{DD} \) is the switch stage voltage supply and \( D \) is the duty ratio, between zero and one for a buck converter. The inductor voltage and current waveforms are shown in Figure 4.7: from 0 to \( T_1 \), the switch is on (connected to \( V_{DD} \)) the switch current starts to rise; from \( T_1 \) to \( T_2 \), the switch is connected to ground and the switch current decreases, i.e.,

\[ \begin{align*}
\frac{\Delta(i_{\text{sw_ac}})}{T_1} &= \frac{V_{DD} - D \cdot V_{DD}}{L} & \text{from } 0 \text{ to } T_1 \\
\frac{\Delta(i_{\text{sw_ac}})}{T_2 - T_1} &= -\frac{D \cdot V_{DD}}{L} & \text{from } T_1 \text{ to } T_2
\end{align*} \quad (4.11) \]
where \( \Delta(i_{\text{sw, ac}}) = \frac{2h}{R_{\text{sense}}} \). From (4.11), the switching frequency for a DC signal becomes:

\[
f_{\text{sw}} = \frac{1}{T_2} = \frac{R_{\text{sense}}}{L} \cdot \frac{V_{\text{DD}}}{D(1 - D)2h}
\]  \(\text{(4.12)}\)

Note that the switching frequency is not dependent on \( R_{\text{load}} \).

![Diagram of linearized output voltage and AC switch current waveforms for DC input envelope signal.](image)

Figure 4.7: (a) Linearized output voltage and; (b) AC switch current waveforms for DC input envelope signal.

Figure 4.8 (a) shows the simulation of the current and voltage waveforms, note that the error signal \( V_o - V_i \) is within the hysteresis value of the comparator as assumed in (4.9). Figure 4.8 (b) plots the spectrum of the currents. Note that all dc components are generated from the switch stage and the switch noise is filtered out by the linear
stage so that the load current harmonics are much smaller compared to the inductor currents. Figure 4.9 plots the comparison of the switch frequency between (4.12) and the simulation. The excellent agreement between the simulation and (4.12) confirms the analysis.

Given (4.12), the switching frequency for a DC plus sinewave envelope signal is straightforward to develop. In this case, the duty ratio is a function of time:

\[
D(t) = \frac{V_{s_{dc}} + V_{s_{ac}} \sin(\omega t)}{V_{DD}}
\]  

(4.13)

Since small-signal linear operation is still assumed here, (4.13) can be substituted directly into (4.12) and the instantaneous switching frequency is:

\[
f_{sw\_inst}(t) = \frac{R_{sense}}{L} \cdot \frac{V_{DD}}{2h} D(t)(1 - D(t))
\]  

(4.14)

The average switching frequency for the DC plus sinewave signal is defined as:

\[
f_{sw\_ave} = \bar{f}_{sw\_inst} = \frac{R_{sense}}{L} \cdot \frac{V_{DD}}{2h} D(1 - D) \frac{V^2}{V^2_{s_{rms}}}
\]  

(4.15)

where \(V^2_{s_{rms}} = V^2_{s_{dc}} + \frac{1}{2} V^2_{s_{ac}}\). Note that the average switching frequency is a function of both the DC and AC components of the envelope signal.
Figure 4.8: Simulation of (a) voltage and current waveforms and (b) spectrums. The DC signal is 1.94V. In simulation, \( V_{DD} \) is 5.5V, \( h \) is 7mV, \( R_{sense} \) is 1 Ohm, \( R_{load} \) is 47 Ohm, \( L \) is 12 uH. The simulated switching frequency is 7 MHz. The calculated switching frequency from (4.12) is 7.5 MHz.
Figure 4.9: Comparison of simulation and theory for switching frequency vs. duty ratio of the DC envelope signal. All the circuit parameters are identical to Figure 4.8.

Figure 4.10 shows the circuit behavior for a sinewave envelope signal. Figure 4.10 (a) shows the simulation of the switching and output waveforms. The switching frequency $f_{sw_{inst}}(t)$ is a function of time as predicted. Note that the error signal $V_o - V_s$ is within the hysteresis value of the comparator as predicted from (11). Figure 4.10 (b) plots the spectra of the current: all the signal DC and AC components are provided by the switch stage and the switch noise is filtered out by the linear stage, so the load current harmonics are suppressed compared to the switch current. Figure 4.11 shows the comparison of the simulated switching frequency and calculated from (4.15) for different AC amplitude and the agreement is excellent.
Figure 4.10: Simulation of (a) switching waveform and error signal voltage; (b) spectra of waveforms. The input envelope signal is $V_s = 1.94 + 1.2 \sin(2\pi 500kHz \cdot t)$. The simulated average switching frequency is 6.4 MHz. The calculated average switching frequency from (4.15) is 6.7 MHz. $V_{dd} = 5.5\,V$, $h = 7\,mV$, $R_{sense} = 1\,\text{Ohm}$, $R_{load} = 47\,\text{Ohm}$, $L = 12\,\mu\text{H}$. 
Figure 4.11: Comparison of simulation and theory for the switching frequency vs. signal amplitude in the small-signal linear operation region. The input sinewave signal frequency is 20kHz. The amplitude is determinate by G (signal amplitude coefficient), where \( V_{s_{dc}} = G \cdot \left( \frac{V_{DD}}{2} \right) \), \( V_{s_{ac}} = 0.9 \cdot G^2 \cdot \left( \frac{V_{DD}}{2} \right) \). All the circuit parameters are identical to Figure 4.8.

### 4.2.2 Case II: Nonlinear Operation for Large-Signal Envelopes

When the load current average slew rate (4.3d) is much larger than the switch current average slew rate (4.3c), the input ac signal is beyond the slew rate limitation of the switch stage (either from a large amplitude signal at low frequency or a small amplitude signal at high frequency), the switch stage can only provide the DC signal power. Hence,

\[
i_{sw\_noise}(t) = \frac{-V_{s_{ac}} \sin(2\pi f t)}{R_{load}}
\]  (4.16)
and

\[ V_o(t) - V_s(t) \approx R_{\text{sense}} \cdot \frac{-V_{s,\text{ac}} \sin(2\pi f_s t)}{R_{\text{load}}} \] (4.17)

which shows that the linear stage starts to provide the ac signal current to the load.

Since \( R_{\text{sense}} \ll R_{\text{load}} \), the error signal is still small, but greater than \( h \). In this case, the switching frequency is equal to the AC signal sinewave frequency, i.e.

\[ f_{\text{sw,ave}} = f_s \] (4.18)

Figure 4.12 shows the simulated circuit behavior for a large sinewave envelope signal. Note that the simulated switching frequency is equal to the sinusoidal frequency as predicted by (4.18). DC current is provided by the switch stage. The linear stage not only filters out the switch noise, but also provides the ac component of the signal current.
Figure 4.12: Simulation of (a) switching waveform and error signal; (b) spectrums. The input envelope signal is \( V_s = 1.94 + 1.2 \sin(2\pi 5 \text{MHz} \cdot t) \). From simulation the switching frequency is 4.95 MHz. The calculated switching frequency from (4.18) is 5 MHz. All the circuit parameters are identical to Figure 4.8. The asymmetry of \( V_o - V_s \) is determined by the duty ratio \( D \).
4.2.3 Case III: The Transition from Small-Signal Linear Operation to Large-Signal Nonlinear Operation

Figure 4.13 shows the simulated circuit transition behavior between the two regions, by sweeping the AC frequency with fixed DC and AC amplitudes. When the circuit transitions from the small-signal linear operation to large-signal nonlinear operation, the average switching frequency decreases. There is a point where the circuit operates at the minimum average switching frequency, called the “minimum switching” point. At this point the circuit switching frequency equals the signal frequency, and the circuit efficiency reaches a peak value (refer to Section 4.4 for more detail analysis on the circuit efficiency analysis).

Note that at this point, the average slew rate of the switch current is equal to the slew rate of the load current, defined before as the “matched slew rate” point. Therefore the “minimum switching” point is the same as the “matched slew rate” point. Figure 4.13 (d) shows the partition of the AC signal between the linear stage and the switch stage, which illustrates the capability of the split-band envelope amplifier for smooth transition between the switch stage and the linear stage. Figure 4.13 (e) shows the error signal increasing during the transition to large-signal nonlinear operation region, which is predicted from (4.8) and (4.17).

Figure 4.14 further demonstrates the circuit behavior by sweeping both the AC frequency and amplitude. Figure 4.14 (a) shows the simulated average switching frequency as a function of AC frequency and AC amplitude. Figure 4.14 (b) shows that the matched slew rate condition overlays with the minimum switching frequency
condition when the AC amplitude is large. When the AC amplitude is small, the AC current following through the current sensor resistor $R_{\text{sense}}$ is not large enough to switch the hysteresis comparator; therefore the switching frequency becomes close to the average switching frequency of the DC envelope signal. Figure 4.14 (c) shows that the circuit efficiency under the minimum switching condition is at most 5% higher than that under the matched slew rate condition, which implies matched slew rate condition can be used to optimize the circuit parameters.

Figure 4.13: Simulation of circuit behavior by sweeping AC frequency $f_s$ of the envelope signal: (a) average slew rate; (b) average switching frequency; (c) efficiency; (d) AC current from linear stage and switch stage; (e) EVM. Input envelope signal $V_s = 1.94 + 1.2 \sin(2\pi f_s \cdot t)$. All the circuit parameters are identical to Figure 4.8.
Figure 4.14: (a) Simulated average switching signal frequency vs AC frequency for different normalized AC amplitudes (the AC amplitudes are normalized to the signal DC component); (b) Simulated combinations of the signal AC amplitude and AC frequency under the minimum switching condition and the matched slew rate condition.
4.3 Design of The Envelope Amplifier for an OFDM 802.11g Signal:

For the envelope amplifier designer, the goal is to maximize the circuit efficiency and at the same time to maintain the high fidelity of the signal. Among the five circuit parameters \( (L, h, R_{\text{sense}}, R_{\text{load}}, V_{DD}) \), only \( L \) and the hysteresis \( h \) are determined by the circuit designer. The current sense resistor \( R_{\text{sense}} \) is chosen to be much smaller than \( R_{\text{load}} \) for low loss. The equivalent load resistor \( R_{\text{load}} \) is determined by the required PA output power and the drain/collector efficiency \( \eta_{\text{RF transistor}} \), i.e.,
\[ \frac{V_{s\_rms}^2}{R_{\text{load}}} = \frac{P_{\text{RF\_output}}}{\eta_{\text{RF\_transistor}}} \]  

(4.19)

where \( V_{s\_rms} \) is the root mean square of the envelope signal. For example, for a 5.5V supply voltage and 9 dB PAR signal, the equivalent \( R_{\text{load}} \) is in the range of 30 ~ 60 Ohm for a 60% efficiency PA when the output power is 16~19 dBm.

The determination of \( h \) is a trade-off issue between the signal fidelity and the average switching frequency; a smaller \( h \) will lead to a smaller error from (11) but a larger switching frequency from (4.15). From the simulation, the 7mV hysteresis value gives the optimized switching frequency and a low EVM (lower than 1%) for the 802.11g signal. Figure 4.15 demonstrates the simulated average switching frequency and EVM by sweeping the hysteresis value. From the simulation, a 7mV hysteresis value gives the low EVM (lower than 1%) for the 802.11g signal and the optimized switching frequency.

Figure 4.15: Simulation of the circuit behavior by sweeping the hysteresis value for an 802.11g signal: average switching frequency vs. \( h \); and EVM vs. \( h \).
Figure 4.16 shows the simulated values of the optimum inductor value for a
sinewave signal and for an 802.11g signal. Figure 4.16 (a) shows that in the small-
signal region, for both signals, the average switching frequencies converge to the
calculated average switching frequency (4.15). Figure 4.16 (b) shows that with
increasing inductor value, the average slew rate of the switch current decreases but the
average slew rate of the load current stays constant, thus the circuit transitions from
linear operation to nonlinear operation. In the transition region, the average switching
frequency decreases and becomes smaller than the calculated average switching
frequency (4.15). In the large-signal region, the average switching frequency trends
close to a constant as predicted from (4.18). Therefore there is a cross-over point
between the circuit average switching frequency and the calculated switching
frequency from (4.15). Note since the 802.11g signal can be considered to be a
combination of multiple consecutive sinewave signals, its transition behavior between
small-signal and large-signal is more gradual than the single-tone sinewave.

At the matched slew-rate point, the efficiency reaches a peak for the single-tone
envelope signal and flattens out for the 802.11g signal (see Section 4.4 for more
details on the efficiency analysis). The inductor value at the matched slew-rate point
is:

\[
L_{\text{matched, } \Delta \text{SR}} = \frac{2(1 - D)V_{s_{dc}} \cdot R_{\text{load}}}{\left| \Delta V_s(t) / \Delta t \right|}
\]  

(4.20)

Given the 802.11g signal DC amplitude and its average slew rate \( \left| \Delta V_s(t) / \Delta t \right| \), the
calculated inductor value from (4.20) is 3.6uH, agreeing well with the simulated value of 3uH. From the simulation, a larger inductor will produce a slightly higher efficiency for the 802.11g signal. But a larger inductor value will also introduce a higher parasitic resistor, which will eventually lead to decreasing efficiency in practice. Also, a larger inductor will require more space on the circuit board. Finally, a larger inductor will have greater inter-winding capacitance that could decrease circuit stability. We found experimentally that a 12uH inductor is the optimum value in this case. From the simulation, the average switching frequency is 5.7MHz, which agrees well with the calculated average switching frequency of 6.2MHz from (4.15). The optimized inductor value is chosen to be approximately four times the calculated value from (4.20) and the average switching frequency can be estimated accurately by (4.15).

![Figure 4.16: (a) Simulated average switching frequency vs. $L$;](image)
Figure 4.16: (b) Simulated average slew rate vs. $L$; (c) Simulated efficiency vs. $L$. The simulation parameters are identical to Figure 4.8. The sinewave signal:

$$V_s = 1.94 + 1.2 \sin(2\pi 500 \times 10^3 t)$$

802.11g signal DC =1.7V, RMS =1.9V.
4.4 Envelope Amplifier Efficiency Analysis

4.4.1 Linear Stage Efficiency Analysis

A high efficiency linear output stage can be realized by a rail-to-rail push-pull Class B configuration as shown in Figure 4.17 (a). The loss comes from the PMOS and NMOS devices, i.e.,

\[ P_{\text{loss}_\text{lin}} = P_{\text{loss}_\text{NMOS}} + P_{\text{loss}_\text{PMOS}} \]  \hspace{1cm} (4.21)

\[ P_{\text{Loss}_\text{NMOS}} = \left( I_{\text{sw}} - \frac{V_{\text{out}}}{R_{\text{load}}} \right) \cdot V_{\text{out}} \]  \hspace{1cm} (4.22a)

\[ P_{\text{Loss}_\text{PMOS}} = \left( \frac{V_{\text{out}}}{R_{\text{load}}} - I_{\text{sw}} \right) \cdot (V_{\text{DD}} - V_{\text{out}}) \]  \hspace{1cm} (4.22b)

where \( V_{\text{DD}} \) is the voltage supply, \( V_{\text{out}} \) is the output voltage at the load, \( I_{\text{sw}} \) is the switch stage current and \( R_{\text{load}} \) is the simplified equivalent resistance model of the RF PA. For simplicity of analysis, we assume the switch stage provides only DC current to the \( R_{\text{load}} \), i.e. \( I_{\text{SW}} = V_{\text{out\_dc}} / R_{\text{load}} \). Thus the linear stage output power is

\[ P_{\text{out\_lin}} = V_{\text{out\_dc}}^2 / R_{\text{load}} \]  \hspace{1cm} (4.23)

and the linear stage efficiency is:

\[ \eta_{\text{linear\_stage}} = \frac{P_{\text{out\_lin}}}{P_{\text{out\_lin}} + P_{\text{loss\_lin}}} \]  \hspace{1cm} (4.24)
Figure 4.17 (b) shows a comparison of the simulated linear stage efficiency and calculated from (4.21)-(4.24). In this example, we chose a National Semiconductor LMH6639 Op-Amp for the linear stage. Note that the real op-amp has non-zero quiescent current and non-zero saturation voltage which reduces the efficiency further.

Figure 4.17: Linear stage efficiency analysis: (a) circuit topology of the high efficiency push-pull class B linear stage (the load and the switch stage are respectively simplified as a resistor and a DC current source);
Figure 4.17: (b) comparison of simulation and theory for the linear stage efficiency. The efficiency of the linear stage is zero at the DC level of the input signal, where the DC power is supplied by the switch stage.

4.4.2 Switch Stage Efficiency Analysis

The switch stage is realized by a buck converter as shown in Figure 4.18, which is composed of a PMOS switch and a diode. When the P-MOSFET is turned on, the voltage at the cathode node of the diode is higher than the voltage at the anode node and the diode is off. When the P-MOSFET is turned-off, the inductor tends to turn on the diode. The resulting switch stage loss is composed of three sources:
1) Conduction loss ($Ron$ loss) when the switcher (PMOS or diode) is on:

$$P_{on\_diode\_loss} = (1 - D) \cdot I_{on} \cdot V_{on\_diode}$$  \hspace{1cm} (4.25a)$$

$$P_{on\_pmos\_loss} = D \cdot I_{on}^2 \cdot R_{on}$$  \hspace{1cm} (4.25b)$$

where $\bar{I}_{on} = I_{sw\_dc}$, and duty ratio $D = V_{out\_dc} / V_{DD}$.

2) Commutation loss due to the PMOS non-zero turn-on and turn-off time:

$$P_{comm\_loss} = I_{on} \cdot V_{off} \cdot (t_{on} + t_{off}) \cdot f_{sw\_ave} \cdot \alpha$$  \hspace{1cm} (4.25c)$$

where $f_{sw\_ave}$ is the average switching frequency, $t_{on}$ and $t_{off}$ are the switcher turn-on and turn-off time, and $\alpha$ is the commutation parameter (assuming $\alpha = 2$ for the worst case [56]). Note that the power loss in the PMOS output capacitor $C_{ds}$ is included in the commutation loss.

3) Driver loss consumed by charging and discharging the input capacitor $C_{gs}$ and the Miller capacitor $C_{gd}$ of the MOSFET:
\[ P_{\text{driver\_loss}} = Q_g \cdot V_{gs} \cdot f_{\text{sw\_ave}} \]  

(4.25d)

where \( Q_g \) is the MOSFET input charge.

A low conduction loss requires a low resistor \( R_{on} \); the low driving loss and low switching loss require low input and output capacitance. In our design, we chose a Fairchild Semiconductor FDV302P digital FET for the P-MOSFET switch. The diode is a Zetex ZLLS400 Schottky diode. The comparator is National Semiconductor LMV7219 with a measured hysteresis value of 3~7mV. There is a measured delay (10~20 ns) along the control loop from the comparator to the switcher. Its effect on the average switching frequency can be included in (4.15) by adjusting the hysteresis value (the effective hysteresis value is the weighted combination of the comparator hysteresis value and the delay). Table 4.1 illustrates an example of the simulated power loss and efficiency of the envelope amplifier for a 47 Ohm load. Figure 4.19 shows the simulated efficiency of the envelope amplifier vs. the normalized output voltage. Note that the efficiency curve matches the probability distribution function of the 802.11g envelope signal. The calculated average efficiency of the envelope amplifier is 65% and agrees with the experimental result in Section 4.5.
Table 4.1: Simulated power losses and efficiency of the envelope amplifier for an 802.11g signal

<table>
<thead>
<tr>
<th>Circuit parameters</th>
<th>VDD=5.5V; L = 12uH; h= 7mV; Rsense= 1Ohm; Rload = 42 Ohm.</th>
</tr>
</thead>
<tbody>
<tr>
<td>Average switching frequency</td>
<td>5.7 MHz</td>
</tr>
<tr>
<td>Linear stage output power</td>
<td>15 mW</td>
</tr>
<tr>
<td>Linear stage PMOS loss</td>
<td>16.6 mW</td>
</tr>
<tr>
<td>Linear stage NMOS loss</td>
<td>11.4 mW</td>
</tr>
<tr>
<td>Linear stage efficiency</td>
<td>35%</td>
</tr>
<tr>
<td>Switch stage output power</td>
<td>75 mW</td>
</tr>
<tr>
<td>Switch stage PMOS conduction loss</td>
<td>3.11mW</td>
</tr>
<tr>
<td>Switch stage diode conduction loss</td>
<td>(Vdiode = 0.4V) 12 mW</td>
</tr>
<tr>
<td>Switch stage driver loss</td>
<td>(Qg = 0.22nC) 6.8 mW</td>
</tr>
<tr>
<td>Switch stage commutation loss</td>
<td>(Ion = 43mA, Voff = 5.5V) 19 mW</td>
</tr>
<tr>
<td>Switch stage efficiency</td>
<td>64%</td>
</tr>
<tr>
<td>Envelope amplifier output power</td>
<td>90mW</td>
</tr>
<tr>
<td>Envelope amplifier efficiency</td>
<td>55%</td>
</tr>
</tbody>
</table>

Figure 4.19 shows the simulated efficiency of the envelope amplifier vs. the normalized output voltage. Note that the efficiency curve matches the probability distribution function of the 802.11g envelope signal. The calculated average efficiency of the envelope amplifier is 65% and agrees with the experimental result in Section 4.5.
Figure 4.19: Simulation of envelope amplifier efficiency with the OFDM signals probability density function.

4.5 Measurements

Figs. 4.20 – 4.22 show the comparisons of the simulation and measurement of the envelope amplifier respectively for the small-signal linear operation, the large-signal nonlinear operation and the transition from small-signal to large-signal by sweeping the AC frequency. Figure 23 shows the comparison of the simulation and measurement for an 802.11g signal with 47 Ohm resistor load. Figure 24 shows the measurement of the envelope amplifier in a hybrid EER system with a Class E PA as the load for an 802.11g signal. The measured average switching frequency is 6.3MHz and the calculated average switching frequency from (4.15) is 6.5MHz. Table 4-2 summaries the performance of the envelope amplifier and Table 4-3 summarizes a comparison of this work and other published envelope amplifiers.
Figure 4.20: Comparison of simulated and measured envelope amplifier for small signal: $V_s = 1.94 + 1.2 \sin(2\pi \cdot 10^4 \cdot t)$. The average switching frequency from both the simulation and measurement is 5.75 MHz.
Figure 4.21: Comparison of the simulated and measured envelope amplifier for large signal $V_s = 1.94 + 1.2\sin(2\pi \cdot 2 \cdot 10^6 \cdot t)$. The average switching frequency for both simulation and measurement is 2MHz.
Figure 4.22: Comparison of the simulated and measured envelope amplifier by sweeping the signal AC frequency: $V_s = 1.94 + 1.2 \sin(2 \pi f_s \cdot t)$. The switch stage current gain is defined as the ratio of fundamental component of the switch stage current to the linear stage current. In the simulated efficiency, the quiescent current and the power loss in the comparator is not included.
Figure 4.23: Comparison of the simulated and measured envelope amplifier for an 802.11g signal. The average switching frequency from simulation is 5.7 MHz and from measurement is 5.3 MHz.
Figure 4.24: Measurement of the envelope amplifier for an 802.11g signal in “hybrid” EER system with Class E RFPA as the load. The circuit parameters are identical to Figure 12 except the resistor load is replaced by Class E RF PA [see Section 2.4 for the details of Class E RF PA design]. The measured 802.11g signal DC level is 1.93V, RMS level is 2.05V; the equivalent voltage supply $V_{dd}$ in (4.15) is 5V considering 0.5V drop across PMOS. The output collector voltage is shifted up of 0.5V for higher linearity and PAE.

<table>
<thead>
<tr>
<th>Table 4.2 Envelope amplifier performance in “hybrid” EER system</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Supply Voltage</strong></td>
</tr>
<tr>
<td><strong>Output voltage</strong></td>
</tr>
<tr>
<td><strong>Output Current</strong></td>
</tr>
<tr>
<td><strong>Output power</strong></td>
</tr>
<tr>
<td><strong>Bandwidth</strong></td>
</tr>
<tr>
<td><strong>Op-Amp Efficiency</strong></td>
</tr>
<tr>
<td><strong>Switch DC-DC efficiency</strong></td>
</tr>
<tr>
<td><strong>Total $V_{dd}$ Amp efficiency</strong></td>
</tr>
<tr>
<td><strong>Average switching frequency</strong></td>
</tr>
</tbody>
</table>
Table 4.3: Comparison of published envelope amplifiers and this work.

<table>
<thead>
<tr>
<th>Envelope amplifier</th>
<th>Application</th>
<th>Signal</th>
<th>Bandwidth</th>
<th>Efficiency (not including RF PA)</th>
</tr>
</thead>
<tbody>
<tr>
<td>[17]</td>
<td>WBET</td>
<td>CDMA</td>
<td>1MHz</td>
<td>65~74% (peak efficiency)</td>
</tr>
<tr>
<td>[9]</td>
<td>EER</td>
<td>NADC</td>
<td>100kHz</td>
<td>80% (peak efficiency)</td>
</tr>
<tr>
<td>[14]</td>
<td>Average ET</td>
<td>CDMA</td>
<td>20kHz</td>
<td>90% (peak efficiency)</td>
</tr>
<tr>
<td>[15]</td>
<td>Average ET</td>
<td>CDMA</td>
<td>20kHz</td>
<td>65% (peak efficiency)</td>
</tr>
<tr>
<td>[11]</td>
<td>WBET</td>
<td>CDMA</td>
<td>1.23MHz</td>
<td>85% (peak efficiency)</td>
</tr>
<tr>
<td>[32]</td>
<td>Hybrid EER</td>
<td>CDMA</td>
<td>2MHz</td>
<td>80% (peak efficiency)</td>
</tr>
<tr>
<td>[44]</td>
<td>EER</td>
<td>-</td>
<td>5MHz</td>
<td>-</td>
</tr>
<tr>
<td>This work</td>
<td>Hybrid EER</td>
<td>WLAN</td>
<td>20MHz</td>
<td>60% (average efficiency)</td>
</tr>
<tr>
<td></td>
<td>EER</td>
<td>OFDM</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

4.6 Summary

A highly efficient wideband envelope amplifier is designed for wideband EER and wideband ET (WBET) applications. The envelope amplifier is analyzed in the small-signal linear operation and large-signal nonlinear operation. A design method is developed to optimize the efficiency of the envelope amplifier for given Peak-to-Average-Ratio (PAR) and average slew rate of the envelope signal. The efficiency of the wideband envelope amplifier is optimized to approximately 60% for a WLAN OFDM envelope signal. Compared with traditional switching DC/DC converter, the proposed envelope amplifier achieves both high efficiency and wideband applications.
This chapter, in part or in full, is a reprint of the material as it appears in the paper to be published in F. Wang, D. Kimball, J. Popp, A. Yang, D. Lie, P. Asbeck, and L. Larson “An improved power added efficiency 19dBm hybrid envelope elimination and restoration power amplifier for 802.11g WLAN applications,” IEEE Trans. Microwave Theory Tech, vol. 54, no. 12, pp. 4086-4099, Dec. 2006. The dissertation author was the primary researcher and the first author listed in these publications.
Chapter 5
ET IC Design and Measurements

A monolithic IBM SiGe BiCMOS [57] Envelope Tracking power amplifier is demonstrated for 802.11g OFDM applications at 2.4 GHZ. The 4 mm$^2$ die includes a high-efficiency high-precision envelope amplifier, and a two-stage SiGe HBT power amplifier for RF amplification. Off-chip digital pre-distortion is employed to improve EVM performance. The IC design and measurements are discussed in this chapter.

5.1 Wideband High Efficiency Envelope Amplifier Design

For the envelope amplifier designer, the goal is to maximize the circuit efficiency and at the same time to maintain the high fidelity of the signal. The envelope amplifier is composed of a high-speed comparator, wideband high efficiency envelope amplifier, and high efficiency switching DC/DC converter. The design method is discussed in Chapter 4.

The comparator was based on a standard CMOS design, as described in [58]. Figure 5.1 shows the simplified comparator schematic. The simulated hysteresis value is approximately 11mV, quiescent current is smaller than 2mA and the delay is smaller than 7ns.
The operational amplifier is designed for a wide gain-bandwidth product and low dc power consumption, so a traditional folded-cascode topology with a rail-to-rail Class-AB output stage is employed as shown in Figure 5.2 [59]. In order to minimize the dc power consumption, a low-quiescent current rail-to-rail Class-AB output buffer is employed to provide the linear bias current to the power amplifier. Since this linear current can be as high as 200 mA, the PMOS and NMOS devices must be sized to supply the necessary current; in this case, the NMOS device (M2) is 2mm x 0.4μm and the PMOS device (M1) is 8mm x 0.4μm. The operational amplifier/class-AB output buffer has a quiescent dc current consumption of 3 mA, and when operated in the closed-loop mode has a simulated gain of 3 dB, and a bandwidth of 20 MHz when driving a load of 6.3 Ω in parallel with 5 pF.

Maximizing the efficiency of the class-AB stage is the key to maximizing the overall linear amplifier efficiency. The fundamental power losses from the class-AB
output stage are due to the finite voltage across the output stage when it is sourcing or sinking current. These losses limit the overall efficiency of the linear amplifier to a maximum of approximately 30% for a typical OFDM waveform, as was discussed in Chapter 4.

Figure 5.2: Simplified schematic of Class AB rail-to-rail Op-Amp (the load and the switch stage are respectively simplified as a resistor and a DC current source). Op-Amp quiescent current is 3mA. The closed loop gain is 3dB. Maximum output voltage 3V. Closed loop bandwidth at 3dB gain is 20MHz.

The switch stage is realized by a buck converter and requires an off-chip inductor (10 uH). Along with the linear stage, the efficiency of the buck converter stage is the key to achieve a high overall efficiency. The power lost by the switch
stage is dominated by three factors: conduction loss (*Ron* loss) when the switcher PMOS or NMOS transistor is on, commutation loss due to the PMOS non-zero turn-on and turn-off time, and finally the power consumption of the switch drivers. To trade off the conduction loss and switching loss, the PMOS device is sized to be 2cm x 0.4 μm and the NMOS device is 0.7cm x 0.4 μm in order to keep the loss minimal with an average switching current of up to 0.2A.

The “shoot-through” loss due to the NMOS and PMOS devices being “on” simultaneously is minimized with the circuit shown in Figure 5.3 [60].

![Figure 5.3: Simplified schematic of switch stage and switch driver. Since M1 is much larger than M2, M2 turns on much faster than M1 turns off. To prevent the shoot-through current, a delay is introduced by inverter M10-M11 and an NAND M5-M7. [60]](image)

### 5.2 Two-stage SiGe RF PA Design

A high efficiency common-emitter SiGe HBT two-stage PA was designed for
operation on the same die as the envelope amplifier, and its schematic is shown in Figure 5.4. The total emitter area of the driver stage was 400 $\mu m^2$ and the emitter area of the final stage is 1500 $\mu m^2$. Special care was taken to achieve isolation between the envelope amplifier and the power amplifier, and so the two circuits were placed on separate ends of the die, with separate substrate contacts and dedicated substrate rings surrounding each circuit. The input match and interstage matching circuits were implemented on-chip, but the output match was implemented off-chip using high-Q surface mount components. The PA was implemented in a 0.18 $\mu$m SiGe BiCMOS technology [57], and the HBT devices demonstrate a peak $f_T$ of 25 GHz and a $BV_{CEO}$ of 6V. The 1x4 mm die was packaged in an MLF44 package as shown in Figure 5.5. Ten and five ground bondwires are assigned respectively to the output and driver transistors. The bondwire inductor (the output emitter bondwire inductor is around 115pH and driver emitter bondwire inductor is around 232pH) and resistor were considered in the simulation. The measured and simulated results for the PA operated at a constant $V_{cc}$ of 3.3V in CW mode are shown in Figure 5.6. The peak power-added efficiency was approximately 40% at an output power of 29 dBm at 2.4 GHz. The small-signal gain was 13.8 dB.
Figure 5.4: Schematic of SiGe HBT 2.4 GHz power amplifier. Vcc=3.3V

Figure 5.5: Die and package photo of SiGe BiCMOS ET PA. Chip size 1mm x 4 mm.
Figure 5.6: Measured gain, output power and power-added efficiency of the SiGe power amplifier when operated in CW mode at 2.4 GHz, Vcc=3.3V.

5.3 ET IC Measurements

The complete WBET system was measured for an OFDM signal with Peak Average Ratio (PAR) of 7dB. Since the WBET system has a significant nonlinearity associated with the collector modulation, as well as the intrinsic nonlinearity of the amplifier, off-chip baseband digital pre-distortion was implemented to improve the system linearity, using a previously published approach [61-62]. Figure 5.7 shows a comparison of the measured AM-to-AM and AM-to-PM distortion before and after digital predistortion, clearly demonstrating the improvement in linearity that can be achieved with this technique. The “haze” around the AM-PM curve at the low input power is a consequence of the uncertainty in the measurement of phase at low power levels, and is not indicative of excessive memory effects. Note that this pre-distortion
is implemented digitally in baseband prior to complex upconversion. The measured spectrum with and without pre-distortion is shown in Figure 5.8, and the signal easily meets the spectral regrowth mask associated with the 802.11g standard.
Figure 5.7: (a) ET PA AM-AM before predistortion; (b) ET PA AM-AM after predistortion.
Figure 5.7: (c) ET PA AM-PM before predistortion; (d) ET PA AM-PM after predistortion. Maximum PA output is 19dBm.

Figure 5.8: Spectrum of ET PA at 19dBm output power before predistortion (BP) and after predistortion (BP). Negligible switching noise is present at the PA output.

The output of the envelope amplifier has to be “time-aligned” to the output of the RF amplifier, so that extra distortion is not created by the resulting time mismatch between the two paths. The effect of this misalignment was investigated in [13] and an alignment algorithm was proposed, which is used here. Fortunately, the WBET system is less sensitive to this misalignment effect than the traditional EER amplifier, and so the effect of small misalignment on EVM is negligible. Figure 5.9 shows the measured time domain output of the envelope amplifier superimposed on the measured output of the RF amplifier, and the two signals are very well aligned.
Figure 5.9: Measured input RF signal and envelope signal under time-alignment condition when RF output power is 19dBm.

The envelope amplifier, which consists of both the switching stage and the linear stage, had an output voltage that varied from 0.3V to 3V, operating from a 3.3V supply. Its peak output current was 330 mA, and its quiescent current was only 5 mA. Its measured bandwidth was 20MHz, and it had an overall efficiency (envelope power out / dc power in) of 65%, at an average switching frequency of 5MHz for a 20 dBm OFDM signal. Figure 5.10 shows the detailed operation of the switcher stage in conjunction with the input and output of the envelope amplifier. The measured efficiency of the switch stage was 75%, and the linear stage had an efficiency of 24%. The normalized rms error of the envelope amplifier (determined by measuring the difference between input and output with an OFDM waveform) was 3% and it consumed 3mm^2 of die area. These results are summarized in Table 5.1.
Figure 5.10: Measured envelope amplifier, switch stage, and input waveforms. The envelope signal is the amplitude of OFDM signal. Average switching frequency is 5MHz. Maximum Vout is 3V.

Table 5.1: Envelope amplifier performance in WLAN ET system.

<p>| | |</p>
<table>
<thead>
<tr>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply Voltage</td>
<td>3.3V</td>
</tr>
<tr>
<td>Output voltage</td>
<td>0.3V to 3V</td>
</tr>
<tr>
<td>Output Current</td>
<td>180 mA (rms)</td>
</tr>
<tr>
<td></td>
<td>330 mA (peak)</td>
</tr>
<tr>
<td>Quiescent Current</td>
<td>5mA</td>
</tr>
<tr>
<td>Output power</td>
<td>230 mW (rms)</td>
</tr>
<tr>
<td></td>
<td>990 mW (peak)</td>
</tr>
<tr>
<td>Bandwidth</td>
<td>20MHz</td>
</tr>
<tr>
<td>$V_{dd}$ Amp efficiency</td>
<td>65%</td>
</tr>
<tr>
<td>Average switching frequency</td>
<td>5MHz</td>
</tr>
<tr>
<td>Normalized RMS of error voltage</td>
<td>3%</td>
</tr>
<tr>
<td>Die Area</td>
<td>3 sq mm</td>
</tr>
</tbody>
</table>
The total PA overall efficiency (RF modulated output power / envelope amplifier dc power plus RF input power) is 28% with an EVM 5% at an output power of 20 dBm. Table 5.2 summarizes the performance of the amplifier along with a comparison to the power amplifier operated with a fixed 3.3V power supply. Note that the efficiency of the amplifier operated in this more traditional mode is also quite high (roughly 19%) thanks to the digital pre-distortion. It can be inferred from the overall system efficiency (28%) and the efficiency of the envelope amplifier (65%), that the RF stage operated with an average efficiency of 43% for the OFDM signal. An efficiency higher than observed in the test of Figure 5.6 is reasonable, since the thermal load on the RF stage was much smaller for the OFDM signal than in the single-tone CW test, and as a result, self-heating effects would be greatly diminished. Moreover, the high efficiency is maintained over a wide range of output power because of the variation of Vcc along with the signal level. This particular implementation of the WBET system, with the Linear Control of Delta Modulation (LCDM) envelope amplifier, generates negligible switching noise at the output of the RF amplifier, as shown in Figure 5.8, since the switching noise is within the bandwidth of the linear amplifier and the RF amplifier does not enter saturation during normal operation.
Table 5.2: Comparison of ET PA and constant bias PA with OFDM signal.

<table>
<thead>
<tr>
<th></th>
<th>ET PA</th>
<th>3.3V PA</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pout</td>
<td>20dBm (100mW)</td>
<td>20dBm (100mW)</td>
</tr>
<tr>
<td>Gain</td>
<td>11dB</td>
<td>13.7dB</td>
</tr>
<tr>
<td>Overall efficiency</td>
<td>28%</td>
<td>19%</td>
</tr>
<tr>
<td>EVM</td>
<td>5%</td>
<td>5%</td>
</tr>
</tbody>
</table>

Note: the required EVM is 5% by 802.11 specifications.
Overall efficiency = RF modulated output power/ final stage dc power plus RF input power.
Digital pre-distortion is implemented to both ET PA and 3.3V PA to achieve 5% EVM.

5.4 Summary

A monolithic wideband high efficiency envelope tracking power amplifier, employing a high efficiency envelope amplifier has been designed and implemented for WLAN 802.11g applications in a SiGe BiCMOS technology. A highly efficient wideband envelope amplifier was designed for wideband ET (WBET) applications. The measured efficiency of the wideband envelope amplifier is approximately 65% for a WLAN OFDM envelope signal. The overall power-added efficiency of the amplifier (including the envelope amplifier and the RF power amplifier, but not including digital circuit power consumption relating to the baseband pre-distortion and time-alignment or the envelope amplifier DAC) is 28% at 20 dBm (100mW) output power. Digital pre-distortion was implemented to reduce the EVM of the amplifier. The
measured results demonstrate that high efficiencies can be obtained in a wideband OFDM amplifier implemented in monolithic silicon technology.

This chapter, in part or in full, is a reprint of the material as it appears in the paper F. Wang, D. Kimball, D. Lie, P. Asbeck, and L. Larson “A monolithic high-efficiency 2.4GHz SiGe BiCMOS envelope tracking OFDM power amplifier,” submitted to IEEE Journal of Solid-State Circuits. The dissertation author was the primary researcher and the first author listed in these publications.
Chapter 6
Conclusions

High linearity PAs are required for WLAN 802.11g application according to high PAR statistic characteristics. Traditionally, linear power amplifiers are implemented by “backing-off” Class-A or Class-AB PAs. However for a high PAR signal, the average efficiency is much lower than the peak efficiency, which demonstrates the inherent trade-off between linearity and efficiency for PA designers.

This dissertation focuses on EER and ET efficiency enhancement techniques to improve the PA average efficiency for high PAR signal. The EER and ET PA structures are investigated. Wideband ET and a “hybrid” wideband EER PAs are proposed for WLAN 802.11g signal at 20MHz signal bandwidth.

Two major challenges of wideband EER/ET PAs are investigated in this dissertation:
(1) A general mathematical model was proposed to study the time alignment requirement for the ET system. The time mismatch sensitivity between the amplitude path and RF path was compared between the ET and EER systems. The simulation and measurement for the two-tone signal and WLAN OFDM signal generally verify the simple ET system model and the analysis. An adaptive time alignment algorithm was developed for the ET system, and the simulation and measurement shows the fine time alignment resolution could be smaller than 0.5ns, satisfying the 802.11g OFDM requirements.

(2) A high efficiency wideband envelope amplifier is designed for wideband EER and wideband ET (WBET) applications. The envelope amplifier is analyzed in the small-signal linear operation and large-signal nonlinear operation. A design method is developed to optimize the efficiency of the envelope amplifier for given Peak-to-Average-Ratio (PAR) and average slew rate of the envelope signal. The efficiency of the wideband envelope amplifier is optimized to approximately 60% for a WLAN OFDM envelope signal.

Two examples are demonstrated for hybrid EER and wideband ET PAs for WLAN 802.11g applications:

(1) The hybrid EER PA demonstrates the overall efficiency of 36% and the PAE of 28% at 19 dBm output power for 802.11g signal;

(2) The wideband ET PA demonstrates the overall efficiency of 29% and PAE of 25% at 15dBm output power for 802.11g signal.
Both hybrid EER and ET PAs implement digital predistortion for PA linearization.

A monolithic wideband high efficiency envelope tracking power amplifier, employing a high efficiency envelope amplifier has been designed and implemented for WLAN 802.11g applications in IBM SiGe BiCMOS technology. A high efficiency wideband envelope amplifier was designed for Wideband ET (WBET) applications. The measured efficiency of the wideband envelope amplifier is approximately 65% for a WLAN OFDM envelope signal. The overall power-added efficiency of the amplifier is 28% at 20 dBm (100mW) output power. Digital pre-distortion was implemented to reduce the EVM of the amplifier. The measured results demonstrate that high efficiencies can be obtained in a wideband OFDM amplifier implemented in monolithic silicon technology.

Future work on the wideband EER/ET transmitter would be interesting on the following topics:

1) ET/EER model including AM/PM and memory effect;

2) theoretical analysis of the optimal envelope bandwidth by including both the envelope amplifier model and PA model;

3) the interaction analysis between envelope amplifiers and RF power amplifier;
(4) a complete EER/ET model including envelope amplifier and RF power amplifier with temperature considerations.
References


[22] “Making 802.11g transmitter measurement,” Agilent Application Note, AN 1380-4.


