UCLA
UCLA Previously Published Works

Title

Tunneling spectroscopy of metal-oxide-semiconductor field-effect transistor at low temperature

Permalink

https://escholarship.org/uc/item/3tk4f4bc

Journal

Applied Physics Letters, 86(24)

ISSN

0003-6951

Authors

Bao, Mingqiang
Liu, F
Baron, F
et al.

Publication Date

2005-06-01

Peer reviewed

eScholarship.org Powered by the California Digital Library
University of California

HTML ABSTRACT + LINKS

Tunneling spectroscopy of metal-oxide-semiconductor field-effect transistor at low temperature

Mingqiang Bao,[a] Fei Liu, Filipp Baron, and Kang L. Wang
Department of Electrical Engineering, University of California at Los Angeles, Los Angeles, California 90095

Ruigang Li
Jazz Semiconductor, 4321 Jamboree Road, Newport Beach, California 92660

(Received 20 December 2004; accepted 19 May 2005; published online 8 June 2005)

Electron tunneling spectroscopy is used to study drain-source current spectra of metal-oxide-semiconductor field-effect transistors (MOSFETs). Measured at liquid helium temperature (4.2 K), experimental results reveal that as drain-source voltage (V_{ds}) increases, the first derivative of drain-source current (or conductance) first decreases, then increases to a maximum and finally decreases again at higher V_{ds}, which is different from the monotonous decreasing feature described by the conventional MOSFET theory. In addition, the measured MOSFET spectra show that there are fine features on the second derivative spectra, and these features may be used to extract trap information. © *2005 American Institute of Physics*. [DOI: 10.1063/1.1951055]

Tunneling spectroscopy was used by Hall[1] for studying current-voltage (*I-V*) characteristics of Esaki tunnel diodes at low temperature. Hall's study revealed that the tunneling process in *p-n* junctions was assisted by phonons. Since the tunneling spectroscopy method has high sensitivity and resolution, it was used to explore the density of states and band gap of superconductors, molecular vibrations, band structure of semiconductors, and defects in semiconductors and insulators.[2–4] Recently, there has been a great deal of interest in applying this method to study traps and molecular vibrations in ultrathin oxides[5] and high-*k* gate dielectrics.[6] All previously mentioned research was focused on studying tunneling processes through two-terminal devices, such as tunnel diodes, metal-insulator-metal junctions, or metal-insulator-semiconductor junctions. In this letter, we report the results of applying tunneling spectroscopy to study metal-oxide-semiconductor field-effect transistors (MOSFETs) in both the subthreshold and the linear regions at 4.2 K.

Figure 1 shows our experimental setup. In our spectroscopy measurement system, a computer is used to control two voltage sources to provide the programmed dc biases, namely, drain bias and gate bias, and to read data from three multimeters. A 1 kHz ac small signal from the oscillator output of a lock-in amplifier is superimposed upon the dc drain bias. Thus, there are harmonic contents in the drain-source current. The current is amplified by an operational amplifier: Drain-source dc current is converted into dc voltage through an accurate adjustable resistor, and the dc voltage is then read by a multimeter. The first-derivative (dI_{ds}/dV_{ds}) and the second-derivative (d^2I_{ds}/dV_{ds}^2) terms are converted into ac voltages. Those ac voltages are read by two lock-in amplifiers which are tuned to detect the frequencies of 1 kHz and 2 kHz, respectively.

Figure 2(a) shows the typical first derivative of drain current I_{ds} versus drain voltage V_{ds} of an *n*-channel MOSFET with a gate length of 0.14 μm and a width of 0.22 μm at 4.2 K. The corresponding second derivative is shown in Fig. 2(b). In addition, similar results were observed from other sizes of both *n*- and *p*-cannel MOSFETs at 4.2 K.

But according to the conventional MOSFET theory in both the subthreshold and the linear regions, dI_{ds}/dV_{ds} versus V_{ds} should monotonously decrease and d^2I_{ds}/dV_{ds}^2 should monotonously increase,[7] shown as the solid lines in the insets to Figs. 2(a) and 2(b), respectively. In addition, due to a lightly doped drain (LDD) structure introduced for minimizing hot-carrier effect in MOSFET, dI_{ds}/dV_{ds} spectra will have a **peak** at low drain voltage at low temperature, illustrated as the dashed line in the inset to Fig. 2(a).[8–10]

However, our experimental results show that the dI_{ds}/dV_{ds} curve has a different shape, which has a **valley** followed by a **peak**, as clearly shown in Fig. 2(a). Further experimental data show that at higher temperatures, both the valley and the peak of dI_{ds}/dV_{ds} will gradually disappear, and at temperatures above 63 K, the MOSFET obeys the conventional MOSFET theory as stated above. Thus, it is clear that the valley and the peak in dI_{ds}/dV_{ds} versus V_{ds} curve and the peak in d^2I_{ds}/dV_{ds}^2 versus V_{ds} curve in Fig. 2 are due to some other effects at low temperature.

One possible explanation for the above experimental results is as follows. Due to the lack of the gate-source and

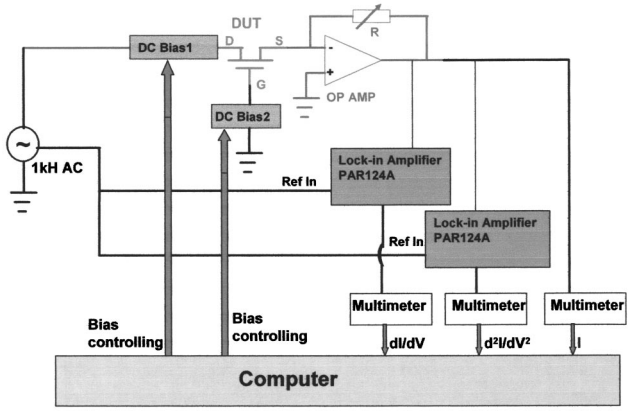

FIG. 1. Schematic diagram of tunneling spectroscopy system for MOSFET.

[a]Electronic mail: baoming@ee.ucla.edu

 © 2005 American Institute of Physics
Downloaded 08 Jun 2005 to 128.97.88.74. Redistribution subject to AIP license or copyright, see http://apl.aip.org/apl/copyright.jsp

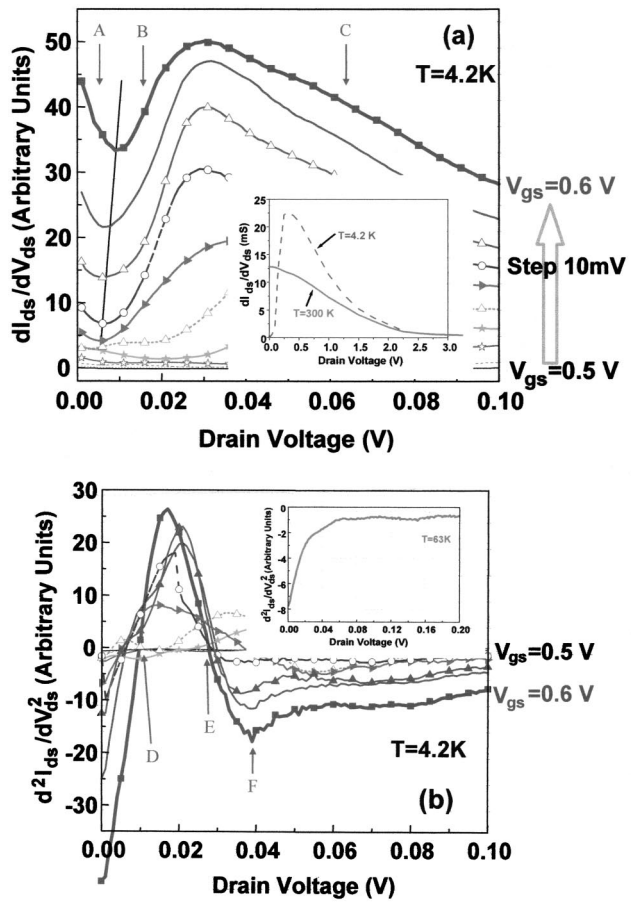

FIG. 2. First derivative and second derivative spectra of *I-V* characteristics of a MOSFET of 0.14 μm (gate length)* 0.22 μm (gate width) at different gate biases at 4.2 K. (a) First derivative spectra show that as V_{ds} increases, dI_{ds}/dV_{ds} decreases (Region A) at first, then increases to a peak (Region B), and finally decreases again (Region C). Futhermore, the higher gate bias, the larger Region A. (Inset: Typical literature dI_{ds}/dV_{ds} characteristics on LDD MOSFET at room temperature and 4.2 K) (see Ref. 9). (b) Second derivative spectra give additional information on the changes of current and the first derivative, for example, for the gate bias 0.60 V curve, Point D corresponds to the valley of dI_{ds}/dV_{ds}, Point E corresponds to the peak of dI_{ds}/dV_{ds}, and Point F indicates the boundary beyond that conventional MOSFET theory applies. (Inset: Second derivative spectra at 63 K, which has the same curve shape as at room temperature, and it can be exactly predicted by conventional MOSFET theory).

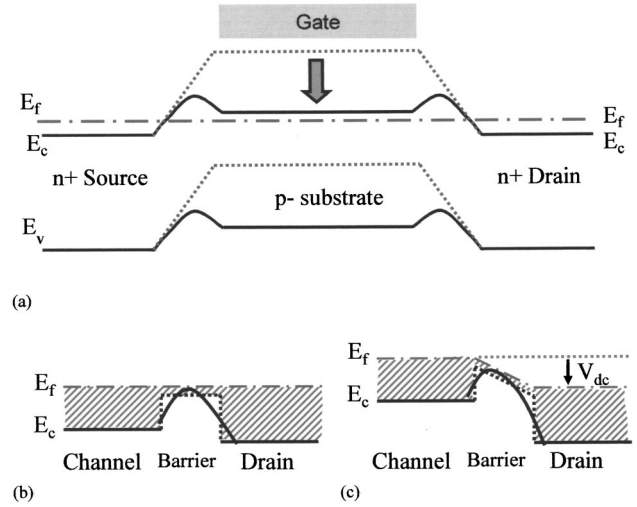

FIG. 3. Energy band diagram for a MOSFET showing two potential hills along the channel due to two LDD regions. (a) When $V_{gs} < V_{th}$ (threshold voltage) and $V_{ds}=0$. Dotted line shows $V_{gs}=0$. (b) Simplified model (dashed lines) and enlarged figure of LDD barrier for $V_g > V_{th}$ and $V_{ds}=0$. (c) Enlarged figure for $V_{ds} > 0$.

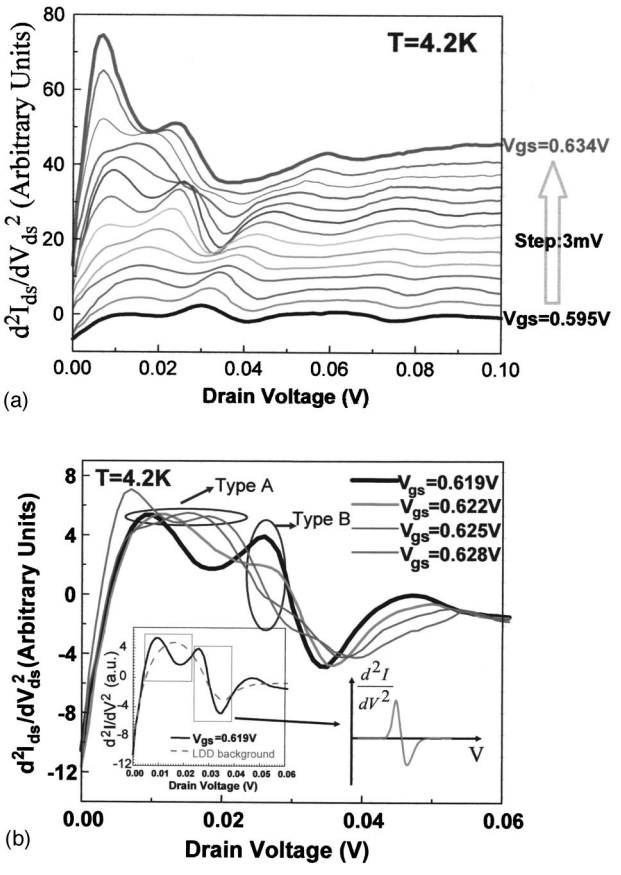

FIG. 4. Second derivative spectra of an *n*-channel MOSFET of 0.32 μm (gate length)* 0.36 μm (gate width). (a) Second derivative curves are intentionally offset to different values at different gate biases for clarity. (b) Four curves selected from (a) but without intentional offset. From (b), Type A feature—where the peak moves as gate bias V_{gs} increases while the peak height remains constant, and Type B feature—where the peak appears only at specific V_{gs} and V_{ds} are observed. Right insert shows typical $d^2I/dV^2 \sim V$ characteristic of trap-assisted tunneling. Left insert shows the second derivative spectra with LDD background spectra when the gate is biased at 0.619 V.

gate-drain overlaps, potential barriers along the channel of the MOSFET are formed at the LDD regions, as illustrated in Fig. 3(a).[8] For model simplification and easy visualization, 0 K temperature and rectangular potential barriers are assumed. When the gate bias is higher than the threshold voltage V_{th}, and the drain voltage is very small, the barrier height and its shape do not change too much with the drain bias, as illustrated in Fig. 3(b). So, the MOSFET operates as predicted by the conventional room-temperature MOSFET theory, which corresponds to Region A in Fig. 2(a). When the drain bias is increased, the potential barrier shape and height are modified by the drain bias, as illustrated in Fig. 3(c). Under this condition, the conduction current I_{ds} is related exponentially to drain voltage V_{ds}.[10,11] As the results indicate, G_{ds} (dI_{ds}/dV_{ds}) will increase with V_{ds}, which corresponds to Region B in Fig. 2(a). At higher drain voltage, a more typical *I-V* characteristic is expected since the potential barrier height is much smaller than the drain bias and has less effect on conduction electrons,[8] and thus G_{ds} (dI_{ds}/dV_{ds})

Downloaded 08 Jun 2005 to 128.97.88.74. Redistribution subject to AIP license or copyright, see http://apl.aip.org/apl/copyright.jsp

decreases again, which is shown in Region C of Fig. 2(a). In addition, for higher V_{gs}, the potential barriers are depressed and more conduction electrons do not experience the barriers, so Region A becomes larger, as shown in Fig. 2(a).

Furthermore, our experimental results show that the d^2I_{ds}/dV_{ds}^2 of some MOSFETs has fine features. The d^2I_{ds}/dV_{ds}^2 spectra has other valleys and peaks besides one main peak, which are shown in Fig. 4(a). Figure 4(b) shows four curves selected from Fig. 4(a) but without an intentional offset. From Fig. 4(b), at least two types of fine features are observed: Type A feature—where the peak moves to the right as gate bias V_{gs} increases but the peak height remains constant, and Type B feature—where the peak appears only at specific V_{gs} and V_{ds}.

These fine features may be attributed to traps, namely, being the result of electron elastically resonant tunneling via a single trap or two traps. The two cases are briefly discussed in the following:

If a trap is present in a potential barrier region, and this trap can assist electrons elastic resonant-tunneling through the potential barrier, then d^2I_{ds}/dV_{ds}^2 spectra will have the feature of peak, as shown in the right insert of Fig. 4(b). As the discussed above, the features of Fig. 4(b) also include the large background of LDD spectra, which are shown as the dashed line in the left insert of Fig. 4(b). After deducting the LDD background spectra, it is clear that the remainder has the feature of trap-assisted tunneling. Since at higher gate bias, the trap energy level will be lower with respect to the source's Fermi level, a higher drain bias will be needed to open the tunneling channel. Thus, the peak of the second derivative will move with the gate bias, and the type A feature is observed. Similarly, the Type B feature may be attributed to two traps aligned together for elastic resonant tunneling. This kind of tunneling only appears within a very small range of gate and drain biases, because two-trap alignment only happens at specific gate and drain biases. Thus, under this condition, the peak of second derivative appears only at specific V_{gs} and V_{ds}. The traps are mostly related to ion implanted defects. But the exact nature of these defects cannot be identified at this time.

In conclusion, the tunneling spectroscopy technique was applied to study the first and second derivative spectra of MOSFET drain-source current. Experimental results showed that at 4.2 K, due to the potential barriers at LDD regions, dI_{ds}/dV_{ds} spectra show a valley followed by a peak. Furthermore, fine features were found on the second derivative spectra, and these fine features may be useful for extracting information about traps and potential barriers induced by LDD.

This work is supported by Microelectronics Advanced Research Corporation (MARCO) Focus Center on Functional Engineered Nano Architectonics (FENA).

[1] R. N. Hall, J. H. Racette, and H. Ehrenreich, Phys. Rev. Lett. **4**, 456 (1960).
[2] I. Giaever and K. Megerle, Phys. Rev. **122**, 1101 (1961).
[3] A. G. Chynoweth, R. A. Logan, and D. E. Thomas, Phys. Rev. **125**, 877 (1962).
[4] R. C. Jaklevic and J. Lambe, Phys. Rev. Lett. **17**, 1139 (1966).
[5] C. Petit and G. Salace, Rev. Sci. Instrum. **74**, 4462 (2003).
[6] W. He and T. P. Ma, Appl. Phys. Lett. **83**, 5461 (2003).
[7] Y. Taur and T. H. Ning, *Fundamentals of Modern VLSI Devices*, (Cambridge University Press, Cambridge, UK, 1998), Chap. 3.
[8] S. H. Wu and R. L. Anderson, Solid-State Electron. **17**, 1125 (1974).
[9] I. M. Hafez, G. Ghibaudo, F. Balestra, and M. Haond, Solid-State Electron. **38**, 419 (1995).
[10] A. Edmundo and D. Gutierrez, IEEE Electron Device Lett. **16**, 85 (1995).
[11] C. G. Rogers, Solid-State Electron. **11**, 1079 (1968).

Downloaded 08 Jun 2005 to 128.97.88.74. Redistribution subject to AIP license or copyright, see http://apl.aip.org/apl/copyright.jsp