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Publication Date
2013

Peer reviewed|Thesis/dissertation
Built-In Self-Test Circuits for Silicon Phased Array Applications

A dissertation submitted in partial satisfaction of the requirements for the degree Doctor of Philosophy

in

Electrical Engineering (Electronic Circuits and Systems)

by

Ozgur Inac

Committee in charge:

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Professor Brian Keating

2013
The dissertation of Ozgur Inac is approved, and it is acceptable in quality and form for publication on microfilm and electronically:


Chair

University of California, San Diego

2013
DEDICATION

To my parents, Esat and Vicdan, and my brother Mesut.
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ACKNOWLEDGEMENTS

This dissertation would not have been possible without the help and support of many people. First, I would like to thank my advisor, Prof. Gabriel Rebeiz. He has invested enormous amount of time in my technical training and I’ve learned a lot from him which are not limited to technical topics. He is a very demanding advisor, always asking the best we can do. However, this attitude taught me that I shouldn’t settle for mediocre or average. His extreme attention to details but at the same time keeping the big picture always in mind, will be a fundamental principle in my future life. I know that he will help me whenever I need in future and I’ll always look for his advice and opinions for the rest of my life. It has been a great pleasure and honor working with him for the last five years, and I’ll definitely miss him.

Next, I would like to thank my dissertation committee members, Prof. Peter M. Asbeck, Prof. James F. Buckwalter, Prof. Gert Cauwenberghs and Prof. Brian Keating for their time, interest, and valuable comments about my research.

I would also like to thank Prof. Yasar Gurbuz at Sabanci University, Istanbul, Turkey, for his support and attention during my undergraduate studies and his encouragement to do a Ph.D. in the U.S.

I want to thank my co-authors: Donghyup Shin, Sang Young Kim, Choul-Young Kim, Fatih Golcuk, Tumay Kanar and Mehmet Uzunkol. I used phased-array channel designs from Donghyup, Sang Young and Fatih to demonstrate the built-in self-test ideas, which is the main topic in my thesis. Tumay and Mehmet helped me to design and implement several parts in my designs and I am grateful to them for their support. I also want to thank Dr. Andy Fung from NASA Jet Propulsion Laboratory for his help in my measurements. I learned a lot from him about measurement techniques above 100 GHz.

I’d like to thank my parents, Esat and Vicdan, for their support, encouragement and unending love. They have stood by the name they gave me (Ozgur means independent in Turkish), and provided me an environment, where I can freely express my opinions. I’d also like to thank my little brother, Mesut, for his friendship and interesting questions almost about everything. Trying to explain ideas to him helped me to understand concepts in a deeper and more fundamental way.

I’d like to specially thank to Yusuf A. Atesal, Berke Cetinoneri and Mehmet Uzunkol. We graduated from the same university in Turkey (Sabanci University), and they have helped me a lot since my graduate school application to UCSD. We shared the same house for the first two and a half years of my Ph.D and their friendship and support made the transition to live in U.S.
much easier for me.

I’d like to thank my Turkish friends Fatih Golcuk, Tufan Gokirmak, Tumay Kanar, Ozan Dogan Gurbuz, Samet Zihir, and Bilgehan Avser. Their friendship have been invaluable to me.

There are many people in the TICS group, who are either currently in the group or graduated, that I would like to acknowledge here for their support and friendship: Woorim Shin, Chirag Patel, Kevin Ming-Jiang Ho, Sang Young Kim, Donghyup Shin, Hsin Chang ”Ken” Lin, Yang Yang, Chih-Hsiang ”Elmer” Ko, Bon-Hyun Ku, Hosein Zareie, Chenhui Niu, Michael Chang, Jennifer Edwards, Mohammed El-Tanani, Tiku Yu, Jason May, Kwang-Jin Koh, Romain Stefanini, Isak Reines, Alex Grichener, Seyhmus Cacina, Dong-Woo Kang, Yi-Chyun Chiou, Chih-Chieh Cheng, Yu-Chin Ou, Ramadan Alhalabi, Choul-Young Kim, Rashed Mahameed, Hojr Sedaghat Pisheh, Hong-Ming Lee, Tao Yang, Abdullah Al-Azemi, Achref Yahiaoui, Hyun-Ho Yang, Young Ho Cho, Chulwoo Byeon.

The material in this dissertation is based on the following papers which are either published, or has been submitted for publication.

Chapter 2 is based on and mostly a reprint of the following paper:

Chapter 3 is based on and mostly a reprint of the following paper:

Chapter 4 is based on and mostly a reprint of the following paper:

Chapter 5 is based on and mostly a reprint of the following paper:

The dissertation author was the primary author of the work in these chapters, and coauthors (Prof. Gabriel M. Rebeiz, Dr. Donghyup Shin, Dr. Sang Young Kim, Dr. Choul-Young
Kim, Mr. Fatih Golcuk, Mr. Tumay Kanar, and Dr. Mehmet Uzunkol) have approved the use of the material for this dissertation.

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ABSTRACT OF THE DISSERTATION

Built-In Self-Test Circuits for Silicon Phased Array Applications

by

Ozgur Inac

Doctor of Philosophy in Electrical Engineering (Electronic Circuits and Systems)

University of California, San Diego, 2013

Professor Gabriel M. Rebeiz, Chair

The thesis presents built-in self-test circuits for phased array applications, and the characterization of a 45 nm CMOS SOI technology for millimeter-wave systems. First, an X-Band phased-array RF integrated circuit with built-in self-test (BIST) capabilities is presented. The BIST is accomplished using a miniature capacitive coupler at the input of each channel and an on-chip I/Q vector receiver. Systematic effects introduced with BIST system are covered in detail and are calibrated out of the measurements. The BIST can be done at a rate of 1 MHz with 55 dB signal-to-noise-ratio (SNR) and allows for the measurement of an on-chip array factor. Measurements done with BIST system agree well with S-parameter data over all test conditions.

Next, a 16-element phased array receiver for 76-84 GHz applications with BIST capabilities is presented. The chip contains an I/Q mixer suitable for automotive FMCW radar applications and which is also used as part of the BIST system. The chip achieves 4-bit RF
amplitude and phase control, an RF to IF gain of 30-35 dB at 77-84 GHz, an I/Q balance of $< 1 \text{ dB}$ and $< 10^\circ$ at 76–84 GHz, and a system noise figure of 18 dB. The on-chip BIST covers the 76–84 GHz range and determines, without any calibration, the amplitude and phase of each channel, a normalized frequency response, and can measure the gain control using RF gain control. System level considerations are discussed together with extensive results showing the effectiveness of the on-chip BIST as compared to standard S-parameter measurements.

For W-band transmit/receive phased-array modules, the first BIST system is presented. Low-loss high-isolation switches are attached to the RF input and output ports using quarter-wavelength transmission-line sections which result in a high shunt impedance when the BIST is disabled and minimal penalty in additional loss. A well-balanced W-band I/Q down-conversion mixer/receiver is also implemented on-chip and is used as an on-chip vector network analyzer. The BIST allows the measurement of the S-parameters in both transmit and receive modes with high accuracy (4-bit phase response, $< 0.5 \text{ dB}$ amplitude variation) at 90–100 GHz without any external calibration. The BIST also results in a normalized frequency response which agrees well with the measured S-parameters at 90–100 GHz.

An in-depth study of a 45 nm CMOS silicon-on-insulator (SOI) technology is presented. Several transistor test cells are characterized and the effect of finger width, gate contact and gate poly pitch on transistor performance is analyzed. The measured peak $f_t$ is 264 GHz for a $30 \times 1007$ nm single-gate contact relaxed-pitch transistor and the best $f_{max}$ of 283 GHz is achieved by a $58 \times 513$ nm single-gate contact regular pitch transistor. The measured transistor performance agrees well with the simulations including R/C extraction up to the top metal layer. Passive components are also characterized and their performance is predicted accurately with design kit models and electromagnetic simulations. Low noise amplifiers from Q- to W-band are developed in this technology and they achieve state-of-the-art noise figure values.
Chapter 1

Introduction

1.1 Phased Array Systems

Phased array systems have been widely used since the 1970s for radar and communications systems, with their unique ability to scan the antenna beam electronically [1]. Until recently, this field was mostly dominated by III-V monolithic microwave integrated circuits (MMICs) due to their higher performance compared to Silicon CMOS or Silicon-Germanium (SiGe) BiCMOS technologies. However, implementation cost of III-V (GaAs or InP) technologies is relatively high because of the discreet implementation and relatively low yield in these technologies. On the other hand, silicon based technologies offer a huge cost reduction in phased array systems both by reducing the unit chip cost by implementing many channels in a single chip with their high yield, uniformity and integration capabilities, and simplifying the layout on printed circuit boards (PCB) by reducing the number of chips to be assembled on PCB.

In recent years, substantial performance improvement of silicon CMOS and SiGe BiCMOS allowed the implementation of transmit (Tx), receive (Rx) or transmit/receive (T/R) phased array systems in these technologies. Many microwave and millimeter-wave phased array systems have been demonstrated with 4-32 channels on a single silicon chip for a variety of applications such as: X-Band radars [2], 24 GHz and 77 GHz automotive radars [3–5], 35 and 45 GHz satellite communication systems [6, 7], 60 GHz high data rate, short range communication systems [8–10], E-Band point-to-point communication links [11], and W-Band power generation [12,13]. Some of these chips further benefitted from the integration capability of silicon and contain local oscillator and phase locked loop (PLL), I/Q receiver or up-convertor, and on-chip antennas [5, 8, 9, 11–13].
However, one of the key bottlenecks of silicon-based phased arrays is the S-parameter testing of many different channels in a single chip. The typical characterization method uses expensive ground-signal-ground (GSG) probes and millimeter-wave vector network analyzers (VNAs). This method is time consuming and also the measurement costs can exceed the chip cost [14]. The use of an on-chip built-in self-test (BIST) system would not only reduce the measurement time and cost, but also will allow the chip to be tested in-situ and recalibrated versus aging, temperature and packaging effects. In this thesis, a BIST technique is proposed, an in-depth systematic analysis is done, and implementations of the BIST technique are presented for different cases from X- to W-Band.

1.2 Thesis Overview

The thesis presents built-in self-test circuits for phased array applications, and the characterization of a 45 nm CMOS SOI technology for millimeter-wave systems.

Chapter 2 presents an X-Band phased-array RF integrated circuit with built-in self-test (BIST) capabilities. The BIST is accomplished using a miniature capacitive coupler at the input of each channel and an on-chip I/Q vector receiver. Systematic effects introduced with BIST system are covered in detail and are calibrated out of the measurements. The BIST can be done at a rate of 1 MHz with 55 dB signal-to-noise-ratio (SNR) and allows for the measurement of an on-chip array factor. Measurements done with BIST system agree well with S-parameter data over all test conditions.

Chapter 3 presents a 16-element phased array receiver for 76-84 GHz applications with BIST capabilities. The chip contains an I/Q mixer suitable for automotive FMCW radar applications and which is also used as part of the BIST system. The chip achieves 4-bit RF amplitude and phase control, an RF to IF gain of 30-35 dB at 77-84 GHz, and I/Q balance of < 1 dB and < 10° at 76–84 GHz, and a system noise figure of 18 dB. The on-chip BIST covers the 76–84 GHz range and determines, without any calibration, the amplitude and phase of each channel, a normalized frequency response, and can measure the gain control using RF gain control. System level considerations are discussed together with extensive results showing the effectiveness of the on-chip BIST as compared to standard S-parameter measurements.

Chapter 4 presents the first BIST system for W-band transmit/receive phased-array modules. Low-loss high-isolation switches are attached to the RF input and output ports using λ/4 transmission-line sections which result in a high shunt impedance when the BIST is disabled and minimal penalty in additional loss. A well-balanced W-band I/Q down-conversion
mixer/receiver is also implemented on-chip and is used as an on-chip vector network analyzer. The BIST allows the measurement of the S-parameters in both transmit and receive modes with high accuracy (4-bit phase response, < 0.5 dB amplitude variation) at 90–100 GHz without any external calibration. The BIST also results in a normalized frequency response which agrees well with the measured S-parameters at 90–100 GHz.

Chapter 5 presents An in-depth study of a 45 nm CMOS silicon-on-insulator (SOI) technology. Several transistor test cells are characterized and the effect of finger width, gate contact and gate poly pitch on transistor performance is analyzed. The measured peak \( f_t \) is 264 GHz for a 30\( \times \)1007 nm single-gate contact relaxed-pitch transistor and the best \( f_{max} \) of 283 GHz is achieved by a 58\( \times \)513 nm single-gate contact regular pitch transistor. The measured transistor performance agrees well with the simulations including R/C extraction up to the top metal layer. Passive components are also characterized and their performance is predicted accurately with design kit models and electromagnetic simulations. Low noise amplifiers from Q- to W-band are developed in this technology and they achieve state-of-the-art noise figure values.

The thesis concludes with a summary of the work and suggestions for future work.
Chapter 2

An X-Band Phased-Array RFIC with Built-In Self-Test Capabilities

2.1 Introduction

Silicon-based arrays have been demonstrated in transmit and receive modes for microwave and millimeter-wave applications. The All-RF architecture is predominant in phased-array designs due to its simplicity and its scalability to a large number of elements [4, 9, 15–24]. The silicon designs allow the integration of many channels on the same chip, together with the power combining network, and all the necessary digital control electronics. Recently, wafer-scale power combining arrays have been demonstrated at 90 – 100 GHz [12], and phased-arrays systems with a local oscillator, PLL and I/Q receiver (Rx) or up-converter (Tx) have been demonstrated up to 16 elements, and these form the basis of several Gbps communication systems [8, 9].

One of the key bottlenecks of RFIC-based phased arrays is the S-parameter testing of so many different channels on a single chip. This is typically done using expensive ground-signal-ground (GSG) probes and is time consuming. In fact, the cost of testing a phased array far exceeds the cost of the chip itself, especially at millimeter-wave frequencies [14]. The use of on-chip built-in self-test (BIST) capabilities would not only lower the testing cost, but will also allow the phased array to be tested in-situ and recalibrated vs. temperature and aging. The BIST should be able to measure each channel individually and with high accuracy (better than the number of phase and amplitude bits required for proper operation) and should not reduce the RF performance of the chip (additional loss, NF, or coupling). Also it should be done in a short time (preferably < 1 \mu s per measurement point) and should not occupy a large area on the
RFIC. This chapter presents the first on-chip BIST for an X-band phased array and with all the performance parameters listed above.

2.2 Built-In Self-Test System Design

2.2.1 System-Level Description

The BIST can be designed in a variety of ways depending on the phased array chip functionality. Fig. 2.1(a) presents a phased array chip used in systems where the system-level transceiver is located at the sum port of the entire antenna (8 – 2000+ elements). In this case, a low power oscillator is integrated on-chip to provide the BIST test signal and is coupled to all the antenna ports using a $\sim 20$ dB coupler. Each channel is then turned on individually and a compact I/Q receiver is integrated on-chip to measure the amplitude and phase of the injected signal, thus determining the channel vector response. Alternatively, the BIST signal can be provided from an external source and distributed to all the chips in the phased-array.

Fig. 2.1(b) presents a self-contained 8 – 16 elements phased-array communication (or radar) system with an integral oscillator and I/Q down-converter. In this case and during BIST operation, the local oscillator is routed to the antenna ports using switches, and the I/Q receiver is used to measure the channel response. The BIST systems in Fig. 2.1 are based on the homodyne approach, and therefore, the mixer I/Q outputs are mostly at DC. This is acceptable since the signal levels are high enough and the DC drifts can be normalized out of the measurements. For self-contained systems, the operational amplifier after the mixer can be part of the standard IF amplifier chain, or as a stand-alone unit that is engaged when the BIST mode is selected.

The BIST systems are shown in the receive mode, but similar BIST systems can be implemented for transmit or transmit/receive phased arrays or for systems using IF or LO beam-forming [25–27]. It is also possible to build a heterodyne BIST system with a low intermediate frequency, but perhaps at the expense of higher power consumption.

The BIST should also be operational under two different conditions: 1) input ports left open-circuited and BIST is done on a low cost station with DC and low-frequency probes (testing a chip before use in an actual phased array) and 2) input ports connected to antennas and BIST is done “in the field”. The difference between these conditions is the impedance seen at the RF input ports, which can affect the coupling value between the BIST line and the input ports. This will be discussed below.
Figure 2.1: BIST systems for (a) large phased arrays and (b) self-contained phased arrays.
2.2.2 BIST Couplers and their Effect on Channel-to-Channel Coupling

A key component in the BIST system is the compact coupler between the BIST transmission line and the antenna port. The BIST line feeds all the antenna ports and is terminated with a matched resistor so as to eliminate any end reflections and result in an accurate coupling value. In fact, most of the power in the BIST line is coupled into this terminating resistor since the coupling value is low (-23 to -30 dB). There are two types of couplers that can be used: An electrically-small coupler that is capacitive or resistive in nature with no coupler directivity, or a transmission-line coupler with high directivity [28].

Fig. 2.2 presents a 2-channel system with a capacitive coupling mechanism (C = 34 fF). The same coupling value can be achieved if a \( \sim 450 \Omega \) resistor is used between the BIST and RF lines. In this case, the insertion loss is \(< 0.1 \text{ dB}\) and the coupling value is \( S_{45} = c = -26 \text{ dB}\) for a matched load at Port 2, but increases to -20 dB for an open-circuit load. A high-directivity coupler is not affected by the RF input port impedance and is a preferable choice, but it has 0.5 – 1 dB insertion loss, and requires a large area, which may not be compatible with a multi-element phased array.

The BIST-to-RF line coupling must be necessarily low since it also determines the coupling between the phased array channels on the same chip. For the case of standard operation (no BIST signal is engaged), the BIST couplers are still present and provide a leakage path between the phased array channels (Fig. 2.2). In this case, \( S_{41} = S_{32} = -52 \text{ dB}\) for matched loads at all ports. While this may appear as sufficiently low coupling, care must be taken in phased-array operation. Consider a 4-channel array as in Fig. 2.3 with a BIST transmission-line delay \( \phi_b \) between the ports and a coupling value of \( c = -26 \text{ dB}\) (matched ports). For a plane-wave incidence angle of \( \theta \) such that \( \gamma = kd\cos\theta \), \( k = 2\pi/\lambda \), \( d \) is the antenna-to-antenna spacing), the inputs at ports 1 – 4 are:

\[
\begin{align*}
a_1 &= e^{-j0} \\
a_3 &= e^{-j2\gamma} \\
a_4 &= e^{-j3\gamma}
\end{align*}
\]

Assuming \( c \ll 1 \) and after S-matrix manipulations:

\[
\begin{align*}
b_5 &= 1 + c^2(e^{-j(\gamma+\phi_b)} + e^{-j(2\gamma+2\phi_b)} + e^{-j(3\gamma+3\phi_b)}) \\
b_6 &= e^{-j\gamma} + c^2(e^{-j(\phi_b)} + e^{-j(2\gamma+\phi_b)} + e^{-j(3\gamma+2\phi_b)}) \\
b_7 &= e^{-j2\gamma} + c^2(e^{-j(2\phi_b)} + e^{-j(\gamma+\phi_b)} + e^{-j(3\gamma+\phi_b)}) \\
b_8 &= e^{-j3\gamma} + c^2(e^{-j(3\phi_b)} + e^{-j(\gamma+2\phi_b)} + e^{-j(2\gamma+\phi_b)})
\end{align*}
\]
Figure 2.2: Simulated S-parameters of a BIST-to-RF line capacitive coupler.

Figure 2.3: Effect of BIST-to-RF couplers on phased-array channel-to-channel coupling ($\phi_b = 21^\circ$, $d = 0.5\lambda_c$, $f = 10$ GHz).
where the first term denotes the through signal coming from the antenna and the second term represents the power coupled to each channel through the BIST couplers. If $\gamma = \phi_b$ for a specific angle $\theta$, all coupling vectors are in phase for Port 8 and a maximum coupling of $|3c^2e^{-j3\gamma}|$ (-42.5 dB) is obtained for $c = 0.05$ (-26 dB). In general, for an N-element phased array connected using a non-directional coupler line, the maximum coupling is $(N - 1)c^2$. Conversely, it is also possible to obtain a coupling value of $<-70$ dB, when all the coupling vectors cancel coherently for a specific angle (Fig. 2.3). It is therefore essential that the coupling, $c$, is low enough so that the total coupling is $<-35$ dB under all conditions and does not limit the phased-array performance.

2.2.3 Other Applications of BIST

On-Chip Phased Array Patterns: The BIST transmission line feeds all channels at the same time, and therefore, an on-chip phased array pattern can be obtained if all the channels are turned on together and phase/amplitude controlled. This is also an ideal way to test the entire RFIC and find any asymmetry in the chip layout or power combiner.

Frequency Response and Absolute Gain: The BIST can also be used to determine the normalized frequency response, and the absolute gain can also be obtained with on-chip power detectors. However, as will be seen in Section V, the absolute gain is hard to measure accurately if a non-directional coupler is used and the RF ports are connected to antennas with a reflection coefficient of -10 dB.

2.3 X-band Phased Array with BIST: Building Blocks

2.3.1 Phased Array Channel

The phased array channel design and Wilkinson power combiner were presented in detail in [2] and a short summary is included here. The chip is designed in the IBM8RF 0.13 $\mu$m CMOS process with $f_t = 100$ GHz and 8 metal layers. An amplifier/phase-shifter/amplifier approach is used with a center frequency of 9.5 GHz. The channel has a 5-bit phase shifter based on switched-LC unit cells, 3-bit gain control with a gain variation of 5 – 6 dB, an average gain of 10.3 dB, a NF of 3.5 dB and an input $P_{1dB}$ of -13 dBm, all at 9.5 GHz, and consumes 20 mA from a 1.8 V supply. The channel also provides input and output match of $<-10$ dB at 9 – 11 GHz. The measured on-chip S-parameters over the 32 phase states are shown in Fig. 2.4.
Figure 2.4: Block diagram of the phased array channel and measured S-parameters.
2.3.2 BIST Transmission-Line and Coupler

The RF transmission-line is built using a CPW configuration using the top metal layers (MA to LY) and the BIST transmission line is defined in the MQ layer below the RF line and ground plane (LY) (Fig. 2.5).

The BIST transmission line needs to feed multiple channels, and therefore it is important to simulate its insertion loss and propagation constant (Fig. 2.5). The BIST line has a simulated loss of 0.9 dB/mm at 10 GHz, and for a channel-to-channel spacing of 550 µm, the BIST signal at channel 1 is -0.8 dB and -21° as compared to channel 2. For 16-element chips arranged with 8-channels on each side, a difference of 3 – 4 dB exists between channel 1 and channel 8, and this can be calibrated out in the measurements.

The capacitive coupler is implemented by moving up the BIST transmission line to E1 layer and enlarging it underneath the RF line, and the overlap area determines the coupling value (Fig. 2.6). An overlap of 44×76 µm² results in a coupling value of -26 dB (all ports matched) and -20 dB (port 1 open circuited) at 9-10 GHz. The simulations are done using Sonnet, a full-wave electromagnetic simulator [29]. The BIST coupler has very little effect on the S-parameters of the RF CPW line, and the simulated $S_{31}$ is $<-0.1$ dB and is given by the CPW line loss (0.2 dB/mm at 9.5 GHz).

2.3.3 BIST Circuits (I/Q Mixer, Op-Amp, Switch)

The BIST phased array chip block diagram is shown in Fig. 2.7 for a single channel test. Note that the Wilkinson power combiner has an additional 3 dB loss since the other channel is not active.

The BIST circuits need to occupy a small amount of area on the chip and therefore are implemented without any inductors (Fig. 2.8). For this demonstration, the BIST signal is generated off-chip and is fed using a GSG (CPW) probe. The signal is first divided between the BIST coupler line and the BIST LO line for the on-chip I/Q receiver using a wideband 3-port resistive splitter with 6 dB loss. The I/Q receiver is based on differential passive mixers built using 0.13 µm CMOS with a simulated conversion loss of 6 dB. The BIST LO signal is amplified using an active balun, and a single-stage polyphase filter and limiting amplifiers are used to drive the I/Q mixers. The RF signal, coupled from the output of the chip, also passes by an RF active balun, and the signal is current divided into two paths (in phase) and fed to the I/Q mixers. Operational amplifiers, with a simulated closed-loop voltage gain of 25 dB and a 3 dB bandwidth of 3.15 MHz and built using wide CMOS transistors for low 1/f noise and are DC
**Figure 2.5:** The IBM8RF metal stack-up (all dimensions in μm) and simulated transmission-line characteristics of the embedded BIST and RF transmission lines.

**Figure 2.6:** Sonnet 3D view and simulated S-parameters of the BIST coupler using back-end metal in IBM8RF process.
coupled to the mixer outputs. The Op-Amps have a closed-loop output impedance of 620 Ω, and an output noise of 251 µV integrated over the entire 3 MHz bandwidth (needed for fast BIST operation). The noise is much lower if averaged over a narrower bandwidth using an off-chip DSP.

The I/Q down-converter consumes 30 mA from a 1.5 V supply with a simulated voltage gain of 15 – 12 dB at 8.5 – 10.5 GHz (Fig. 2.9(a)). Due to the all-resistive design, the frequency response of the I/Q receiver is not constant vs. frequency, and it can be calibrated out of the measurements. The simulated BIST system results in < 0.6° and < 0.3 dB imbalance between the I and Q channel responses at 8-12 GHz, which is mostly due to device and layout mismatch. The input $P_{1dB}$ at 9.5 GHz is -9 dBm at plane B (see Fig. 2.7), which is more than enough for BIST operation. The BIST LO balun has a $P_{1dB}$ of -7 dBm, and a power level of 0 dBm at the BIST input port is enough to drive the I/Q receiver.

The output BIST sampler (Fig. 2.8) can be designed using a 10 to 20 dB coupler or using a switched resistive load. A switch was chosen for improved signal to noise ratio (SNR) and to also provide a near 50 Ω impedance at the output port of the Wilkinson power combiner under standard operation and BIST conditions. This is achieved as follows: If the phased-array chip is tested without any termination on its output port (i.e., not connected to a phased array), then the CMOS switch is engaged and the switch on-resistance together with the 65 Ω and the
**Figure 2.8**: Block diagram of I/Q receiver and schematics of blocks. All active transistors are biased through current mirrors and not shown here. All unlabeled capacitors are 1 pF.
input impedance of the RF balun provide a 50 $\Omega$ load to the Wilkinson power combiner and a coupling value of -3 dB. If a 50 $\Omega$ termination is present at the output port, then the CMOS switch is not engaged, and a $Z_{sh}$ of 150-$j$95 $\Omega$ load at 10 GHz is connected in shunt across the RF line (Fig. 2.8). This results in an effective impedance of 40-$j$5 $\Omega$ at the Wilkinson output port (still matched to $<-17$ dB from 8 to 12 GHz), a coupling value of -18 dB and an RF insertion loss of 1.1 dB at 10 GHz. The added insertion loss may not be acceptable in certain systems, and a directional coupler could be a better choice at this location.

### 2.3.4 BIST Signal-to-Noise Ratio

The signal power at plane A ($S_A$) is -26 dBm for an input BIST signal of 0 dBm and an open circuit at the RF input port. The simulated single-sideband noise figure ($NF_{SSB}$) at plane B is 38.5 dB (Fig. 2.9(b)) which translates to an $NF_{SSB}$ of 28.3 dB at plane A due to the channel gain. This results in an equivalent noise power at plane A ($N_A$) in a 3 MHz IF bandwidth of

$$N_A = kT \text{ (dBm/Hz)} + NF_{SSB} \text{ (dB)} + BW \text{ (Hz)}$$

$$= -174 + 28.3 + 64.8 = -80.9 \text{ dBm.}$$

and the resulting SNR at plane A is

$$SNR_A = S_A / N_A = 54.9 \text{ dB.}$$
The output signal and noise voltages can also be calculated using a similar approach. For an input at plane A of -26 dBm at 9.5 GHz, the signal level at plane B is -18.7 dBm (25.9 mV\textsubscript{rms}) and the output voltage (calculated as $\sqrt{(I^2+Q^2)}$) is 153.1 mV. The simulated output rms noise in a 3 MHz bandwidth is 194.7 $\mu$V, which results in an SNR of 54.9 dB.

The SNR is large enough to allow for a lower BIST input power (-10 dBm instead of 0 dBm) and very fast BIST operation in < 1 $\mu$s testing speeds. The measured rms gain and phase errors using BIST with an LO power of -10 dBm to +10 dBm are shown in section IV.

### 2.4 Measurements

The 2-element phased-array chip with BIST is shown in Fig. 2.10. Note the BIST coupler, resistive splitter and BIST I/Q receiver.

#### 2.4.1 Individual Channels

The phased array response was measured using the BIST technique at 8.5 – 11 GHz with 250 MHz steps, but only few frequencies are shown for brevity. Fig. 2.11 presents the measured I/Q outputs at 9.5 GHz for all 32 phase states and a BIST input signal level of 0 dBm (channel 1 active and channel 2 turned off). The small steps in the I and Q voltages are not noise but actual change in the channel amplitude response at different phase states (the phase shifter has PM-AM conversion). The I and Q data are then processed externally to obtain the normalized amplitude and phase response using the standard formulas:

$$A = \sqrt{I^2 + Q^2}$$

$$Phase = \tan^{-1}(Q/I)$$

Fig. 2.12 presents a comparison of the measured BIST and S-parameter channel response vs. phase states at 8.75, 9.5 and 10.25 GHz. The measurements are normalized to the -90° state (i.e., phase set to -90°, average amplitude set to 0 dB) and the BIST measurements clearly predict the phase response and amplitude modulation due to the switched-LC phase shifters. Also, one can accurately measure the large jump in phase at 8.75 GHz due to the use of a high-pass/low-pass network for the 180° phase shifter cell and the use of a low-pass only network for the 11°, 22°, 45° and 90° cells (more detail in [2]). The difference between the BIST and S-parameter phase measurements at 10.25 GHz is mainly due to the I/Q mismatch in the BIST receiver, since the center frequency of the I/Q polyphase network is designed to be at 9.5 GHz.
**Figure 2.10**: Chip microphotograph of fabricated 2-channel phased array with BIST. Chip size is 2.95×1.52 mm².

**Figure 2.11**: Measured I and Q voltages at 9.5 GHz vs. 32 phase states.
Figure 2.12: Measured channel 5-bit response using BIST and S-parameters at (a) 8.75 GHz, (b) 9.5 GHz.
Figure 2.12: (Continued.) Measured channel 5-bit response using BIST and S-parameters at (c) 10.25 GHz.

Figure 2.13: Measured rms gain and phase error using BIST and S-parameters.
Figure 2.14: Measured normalized frequency response using BIST and S-parameters for state 00111 and state 10101.

Figure 2.15: Measured gain control using BIST and S-parameters: amplitude and phase.

Figure 2.16: Measured rms phase and gain error at 9.5 GHz vs. BIST power level.
The rms amplitude and phase errors can be calculated from the BIST measured data and agree well with S-parameter measurements (Fig. 2.13).

The frequency response can also be measured and is shown in Fig. 2.14 for two representative states (00111 and 10101). The response is normalized at 9.5 GHz due to the absence of on-chip power meters. Note that the BIST signal is higher at 8.5 GHz and lower at 10.5 GHz due to the frequency response of the BIST I/Q receiver with a maximum error of 1.9 dB. The gain control and any associated AM-PM conversion can also be measured using BIST and good agreement is obtained with S-parameter measurements (Fig. 2.15).

Channel 1 response was also tested vs. the BIST signal level and no change in the channel response was observed other than an absolute level change in the output I and Q voltages. Fig. 2.16 presents the measured BIST rms gain and phase error vs. BIST power level. The rms gain error reduces vs. LO power due to compression in RF and LO BIST paths. Still the change is < 0.1 dB and the BIST can be operated over a 20 dB power range.

The time domain response of the BIST system is shown in Fig. 2.17. In this case, the phase shifter is changed between two phase states with a 180° difference and the Op-Amp output was captured on an oscilloscope with 14 pF input capacitance. The measured 10% – 90% fall time is 165 ns which results in an Op-Amp bandwidth of 2.1 MHz. The 90% system settling time is 235 ns, but this is not accurate enough for 5-bit phase shifter measurements since an 11° phase shift has < 2% amplitude modulation in the I and Q vectors. Therefore, it is important to quote the 98% settling time of 340 ns, and the BIST can be operated at 1 MHz rate with no problems. This means that an 8-element array can be tested in < 1 ms over a wide range of amplitude and phase settings.

Measurements on channel 2 were identical to channel 1 and are not repeated. However, as expected, channel 2 shows 0.8 dB higher gain and a +21° phase shift as compared to channel 1 (Fig. 2.18(a) - only I channel shown). This is due to the loss and the propagation constant of the BIST line, and agrees well with Sonnet simulations as shown in Fig. 2.18(b). In Fig. 2.18(b), the measured amplitude and phase difference is determined by comparing the amplitude and phase for the 0° phase states of the two channels. The 0.5 dB error at 8.5 GHz is due to an impedance mismatch at the phased array input port (S_{11} = -7 dB) which changes the coupling between the BIST line and RF ports.
Figure 2.17: Measured time domain response of BIST measurement.

Figure 2.18: (a) Measured channel 1 and channel 2 I-vector responses vs. phase states at 9.5 GHz using BIST, and (b) measured amplitude and phase difference between channel 1 and channel 2 due to the BIST line.
2.4.2 On-Chip Array Factor

As mentioned above, one of the most useful features of BIST is the possibility to synthesize an on-chip array factor. In this case, both channels 1 and 2 are turned on and summed using the Wilkinson power combiner. The RF signal is then sampled using the BIST resistive coupler. Fig. 2.19(a) presents the measured I and Q voltages and Fig. 2.19(b) shows the corresponding amplitude response \( \sqrt{I^2+Q^2} \) when the phase of channel 2 is set at 0\(^\circ\) (state 00000) and 180\(^\circ\) (state 10000) and the phase of channel 1 is changed from 0\(^\circ\) to 360\(^\circ\). One can clearly see the 2-element array factor. Note the peak voltage is 235 mV which is twice that of a single channel as expected from a 6 dB power increase. This is due to the signals in the two channels adding coherently (+3 dB) and to the fact that the Wilkinson power combiner has an additional 3 dB of loss when a single channel is tested. The BIST phase difference between the channels, which is due to the finite length of the BIST line (21\(^\circ\)) can be obtained from this measurement assuming that the channels’ electrical lengths are identical. In the 0\(^\circ\) case, perfect cancellation occurs when channel 1 is at 180\(^\circ\), but due to the 21\(^\circ\) delay between the channels, cancellation occurs at state 13 (180\(^\circ\)-22\(^\circ\)). The BIST gain difference due to BIST line between the channels (-0.8 dB) can also be obtained by setting the channel phases 180\(^\circ\) apart and adjusting the channel gains to obtain a deep null. However, the phase shifter PM-AM conversion must be first calibrated out from each channel since it is of the same order.

Fig. 2.19(c) presents the synthesized 2-channel array factor where the BIST transmission line phase and amplitude difference is calibrated out of the measurements. In this case, perfect cancelation occurs at state 15 (180\(^\circ\)) for 0\(^\circ\) setting of channel 2. Also, the nulls in the calibrated on-chip array factor are much deeper than the un-calibrated case due to the correction of the 0.8 dB amplitude difference in the BIST line.

2.5 Discussion

The BIST system can be used with calibrated power detectors to result in absolute gain and input \( P_{1dB} \) measurements which is very useful. This can be done using a calibrated power detector at the output port and is straightforward when the phased array chip is not connected to the antennas (stand-alone test mode). In this case, the coupling value can be simulated using Sonnet, is constant vs. frequency and is not dependent on the RF port impedance (it is an open-circuit). However, when the chip is being used in a phased array system, the RF port impedance (or antenna impedance) depends on frequency and on the scan angle, and the coupling value
is dependent on the RF port impedance since the lumped-element coupler does not have any
directivity. Fig. 2.20(a) presents the simulated coupling value for a capacitive cross-over with
C = 34 fF (c^2 = -26 dB at 10 GHz when all ports are matched) and for an RF port VSWR of
1.0, 1.4, 2.0 and 2.6. The large variation in the coupling value, even at VSWR of 2.0, indicates
that the simple capacitive (or resistive) coupler cannot be used to determine an accurate gain or
a frequency response unless the RF port is well matched (-16 dB reflection coefficient).

The effect of the antenna impedance can be reduced with the use of CMOS switches.
A series switch at the RF port isolates the lumped-element coupler when the BIST is engaged at
the expense of additional loss (Fig. 2.20(b)). A shunt switch can also be used at the RF port, and
can be resonated out using a shunt inductor when the BIST is not engaged which results in very
low loss (< 0.2 dB). However, when the BIST is engaged and the shunt switch is ON with a low
impedance to ground (10 Ω), the coupling value becomes |c(1 + Γ_o)|^2 = -35.5 dB (for c^2 = -26
dB and Γ_o = -0.66) which may affect the system dynamic range. Of course, directional couplers
at the RF port solve this problem and should be employed if space allows.

The proposed BIST technique can be extended to large arrays, but care must be taken
to calibrate out the amplitude and phase difference between the channels. In this case and for an
8-element array, the amplitude and phase difference between channel-1 and channel-8 would be
5.6 dB and 147°, respectively. This difference can be predicted accurately using EM simulations
and can be calibrated out of measurements. Another challenge in large arrays is the additional
loss due to power combining network (for passive power combiners). Since only one channel is
turned on during BIST operation, each Wilkinson power combiner presents an additional 3 dB
loss, and this results in a 9 dB more loss for an 8-element array. Still, as long as the output SNR
is sufficient for accurate measurements, the additional loss will not be a limitation.

2.6 Conclusion

This chapter presented the first on-chip BIST for phased-array RFICs. The effect of
BIST coupler on the phased-array performance is presented in detail and it is shown that, for
non-directional couplers, it is important to have a low coupling value at the input of the chip.
The BIST measurements agree very well with S-parameter measurements. It is expected that the
BIST technique will be used in millimeter-wave phased arrays and will greatly reduce the RFIC
testing costs.
Figure 2.19: (a) Measured I and Q voltages during array-factor measurements with BIST. (b) Measured 2-channel array factor using BIST at 9.5 GHz. (c) Synthesized 2-channel array factor at 9.5 GHz with the BIST line amplitude and phase difference calibrated out of measurement (see text).
Figure 2.20: (a) Effect of antenna port impedance on coupler performance and (b) proposed switch network for accurate gain measurements.

2.7 Acknowledgement

This work was supported in-part by an Intel/UC-Discovery Program, Ian Young and Jad RIzk program monitors, and in part by the US-Army Research Office, Alfred Hung and Edward Viveiros, program monitors.

Chapter 2 is mostly a reprint of the material as it appears in IEEE Transactions on Microwave Theory and Techniques, 2012. Ozgur Inac; Donghyup Shin; Gabriel M. Rebeiz. The dissertation author was the primary author of this material.
Chapter 3

A 76-84 GHz 16-Element Phased Array Receiver with a Chip-Level Built-In Self-Test System

3.1 Introduction

Millimeter-Wave automotive radars at 77 GHz (FMCW systems) and 79–81 GHz (UWB systems) have been traditionally based on a switched-beam design or a digital beam-forming approach [30–34]. The switch-beam design is based on 4–5 elements placed on the focal plane of a plastic lens and results in angle coverage of $\pm 10^\circ$, and is therefore used for long-range applications, such as cruise control (Fig. 3.1(a)). The digital beam-forming approach employs an array of planar antennas together with a mixer on each antenna element, and the array patterns with scanning capabilities up to $\pm 50^\circ$ are synthesized in the digital domain (Fig. 3.1(b)). However, since each antenna element has a wide beam in the azimuth plane, the mixers are subjected to large interferers especially from near scattering targets such as guard rails. Therefore, the mixers are designed to have high linearity, which requires large LO power levels. In fact, in many systems, the mixer is used without an LNA due to the required linearity, resulting in a system noise figure (NF) of 16–18 dB [30, 32, 34]. These systems have been implemented using SiGe and GaAs chips, and SiGe solutions have been particularly successful due to their low phase noise at DC–5 MHz, and their operation at 125°C, which is required in automotive applications. Also, as is well known, SiGe results in complex chips with high yields due to its density of integration as compared to GaAs.
Figure 3.1: Millimeter-wave automotive radar systems: (a) switched-beam (b) digital beam-forming receiver (c) RF beam-forming receiver.
Phased arrays with 16–32 elements can enhance the performance of automotive radars by providing a narrow scanned beam before the receiver (Fig.3.1(c)). These arrays can be configured to provide a narrow beam with $\pm 10^\circ$ scanning for long-range radars, or a wider beam with $\pm 50^\circ$ scanning for collision avoidance radars. Also, due to their ability to position several nulls (zeroes) in the far-field pattern, they are less susceptible to short-range wide-angle interferers. However, they are expensive to implement due to the large number of elements especially for low-cost automotive systems.

The next-generation automotive phased-array radars require a large number of elements, and it is currently possible to integrate 8–32 phased-array channels on a single SiGe or CMOS chip as demonstrated by UCSD, IBM, Intel and several other groups at millimeter-wave frequencies [7–10, 21, 35]. Also, it is now possible to integrate high-efficiency antennas on the same chip, therefore resulting in wafer-scale phased arrays having no transitions in and out of the wafer [12, 13]. These phased array chips require expensive test procedures since each channel is individually measured using a mm-wave vector network analyzer and CPW probes. Therefore, an on-chip built-in self-test (BIST) system that can quickly measure individual channels will greatly reduce the chip testing cost and help in system-level diagnostics. A practical BIST implementation has been demonstrated earlier at X-band frequencies using a dedicated homodyne I/Q BIST circuit [36]. Other BIST implementations at mm-wave frequencies have been shown in [37].

Another application of mm-wave phased arrays is for point-to-point communication systems, such as E-band communications at 71–76 GHz and 81–86 GHz [38–42]. These systems are currently based on reflector antennas, but phased arrays are proposed to solve the costly alignment issue between two reflector antennas located on towers. In this case, the SiGe phased array must be proceeded by a low noise InP amplifier (one per channel) since the system noise figure (NF) must be very low (4–5 dB) for long distance communications.

This work expands on [43] and presents a 16-element phased array receiver for 76–84 GHz applications with BIST capabilities. The chip contains a wideband I/Q mixer suitable for automotive FMCW applications and which is also used as part of the BIST system. The on-chip BIST covers the 76–84 GHz range and determines, without any calibration, the amplitude and phase of each channel, a normalized frequency response, and can measure the gain control range using RF or IF gain control. System level considerations are discussed together with extensive results showing the effectiveness of the on-chip BIST as compared with standard S-parameter measurements.
Figure 3.2: (a) Block diagram of the 76-84 GHz 16-element phased array receiver with a chip-level built-in self-test (BIST) system and (b) block diagram of a single channel.
3.2 Phased Array Receiver Design

3.2.1 Architecture

Fig. 3.2(a) presents a 76–84 GHz 16-element phased-array chip with a 16:1 passive Wilkinson combiner, an I/Q receiver and a 38-42 GHz local-oscillator (LO) input. The LO signal is first doubled to 76–84 GHz and split into two paths: The BIST and LO paths. When the BIST mode is selected, the cascode active switch connects the BIST signal to a differential transmission-line on the left (Ch. 1-8), right (Ch. 9-16) or both sides of the array (Ch. 1-16). This BIST signal is then fed to the phased-array channels using miniature differential couplers located at the input of each channel. The signal passes by the channels (each with amplitude and phase control), the 16:1 combiner, and is translated to DC I and Q voltages using a homodyne mixing technique. This allows for measuring the phase and amplitude response of individual channels if one channel is turned on at a time. It also allows for measuring an on-chip array factor if several channels are turned on and the phase between them is varied.

Fig. 3.2(b) presents the phased-array channel based on an alternating amplifier/phase-shifter topology. This topology presents a compromise between gain, NF, power consumption and has been presented in [44] for a single-ended design. A passive balun is used at the input of each channel for single-ended RF input port, which is compatible with microstrip circuits and antennas. The differential signal is then fed into a SiGe cascode LNA+VGA. Switched-LC phase shifters are used at the input of each channel for the 11°, 22.5°, 45° and 90° phase-shifter cells, and a SiGe Gilbert-cell is used for the 180° phase shift.

The outputs of all 16 channels are then fed to a 16:1 differential Wilkinson combiner with a net gain of 5 dB (12 dB summing gain, 7 dB ohmic loss), followed by an I/Q down-converter based on Gilbert-cell mixers with an input $P_{1dB}$ of -5 dBm, and DC coupled operational amplifiers with a 3-dB bandwidth of 5 MHz. An RF monitor section is also implemented to measure the chip performance without the need of a local oscillator signal. This is done using a 10 dB resistive coupler attached to the main RF line. The chip is controlled using an SPI interface and contains a PTAT biasing circuit. The overall chip size is 5.5 × 5.8 mm² with a channel spacing of 700 µm and consumes 500-600 mA from a 2 V supply (1–1.2 W).

The chip is built using the IBM 8HP SiGe BiCMOS process with an $f_T$ of 200 GHz. It has 7 metal layers with a 4 µm thick top layer (AM) (Fig. 3.3). The 100 Ω differential coplanar-waveguide (CPW) transmission lines (gap-signal-gap-signal-gap = 9-6-10-6-9 µm) are built using the AM and MQ layers with a 9.2 µm thick interlayer dielectric ($\varepsilon_{eff} = 3.9$), and
have a simulated loss of 1.05 dB/mm at 80 GHz.

### 3.2.2 Balun

A passive balun is preferred at the input port since it does not consume any DC power and can act as an ESD protector (Fig. 3.4). The passive balun is a two-layer design with a primary turn implemented using the AM layer and the secondary turn implemented using the LY layer. Capacitors are used to provide wideband matching ($S_{11} < -10$ dB for 70–100 GHz) and the simulated loss is 1.2 dB at 80 GHz.

### 3.2.3 Amplifiers

Fig. 3.5 presents a two-stage cascode amplifier with a center frequency of 80 GHz. The first stage is biased at 0.4 mA/µm to result in the lowest noise figure, which is less than the optimal bias current for the highest gain as given by the IBM design manual. The inductors are designed using microstrip lines between AM and M1, with a width of 4 µm and Q of 12 at 80 GHz. Capacitors are built using custom Metal-Oxide-Metal (MOM) capacitors between M3 and M4 with a simulated Q of 50 at 80 GHz. Shunt resistors at the loads help to widen the 3-dB bandwidth to 19.6 GHz at the expense of 0.6 dB increase in noise figure. The simulated gain and noise figure are 10–11.1 dB and 8.9–9.2 dB, respectively, at 75–86 GHz for a total bias current of 9 mA. The amplifier results in a wide impedance matching ($S_{11}, S_{22} < -10$ dB at 66–100 GHz, 73–91 GHz, respectively), an input $P_{1dB}$ of -20 dBm, and 2-bit gain control is realized by adjusting the bias current of the second stage. All the inductors and MOM capacitors are designed and optimized using Sonnet, and global EM simulation is performed (see Fig. 3.5 for the Sonnet EM model).

### 3.2.4 Phase Shifter

The design of the $11^\circ$, $22.5^\circ$, $45^\circ$ and $90^\circ$ phase shifters are based on switched-LC networks and are differential versions of earlier designs [6, 44] (Fig. 3.6(a)). In the bypass state (T1 is ON and T2 is OFF), $L_p$ resonates with the off-state parasitic capacitance of T2, and $L_s$ and $C_p$ are in parallel with the on-state resistance ($R_{on1}$) of T1. As long as $R_{on1}$ is small enough, then $L_s$ and $C_p$ have minimal impact on the insertion phase. In the phase-delay state (T1 is OFF and T2 is ON), the input is connected to the output using the low-pass $\pi$-network composed of $C_p$-$L_s$-$C_p$. The $L_s$ and $C_p$ values are chosen to provide the desired phase difference between the bypass and phase-delay states. Also, transistors T1 and T2 can be chosen to result in relatively
Figure 3.3: IBM 8HP metal stack-up with a representative 100 Ω differential CPW line.

Figure 3.4: Schematic and layout of the passive balun, which is used at every element.

Figure 3.5: Schematic and layout of the two-stage W-band cascode amplifier
Figure 3.6: Schematic and layout of (a) 90°, 45°, 22.5° and 11° phase shifters and (b) 180° phase shifter.

Figure 3.7: Simulated phase difference and gain of the cascaded 5-bit phase shifter.
Table 3.1: Phase shifter component values

<table>
<thead>
<tr>
<th></th>
<th>90°</th>
<th>45°</th>
<th>22°</th>
<th>11°</th>
</tr>
</thead>
<tbody>
<tr>
<td>T1 (µm)</td>
<td>14/0.12</td>
<td>10/0.12</td>
<td>6/0.12</td>
<td>2/0.12</td>
</tr>
<tr>
<td>T2 (µm)</td>
<td>10/0.12</td>
<td>6/0.12</td>
<td>6/0.12</td>
<td>6/0.12</td>
</tr>
<tr>
<td>Ls (pH)</td>
<td>54</td>
<td>44</td>
<td>52</td>
<td>52</td>
</tr>
<tr>
<td>Cp (fF)</td>
<td>43</td>
<td>24</td>
<td>17</td>
<td>17</td>
</tr>
<tr>
<td>Lp (pH)</td>
<td>55</td>
<td>85</td>
<td>∞</td>
<td>∞</td>
</tr>
</tbody>
</table>

low insertion loss when the transistors are ON. However, the 0.13 µm CMOS technology, which is available in the IBM8HP process, results in a large substrate capacitance and contributes to a high insertion loss at millimeter-wave frequency even when the transistors are off. T1, T2, Ls and Cp are therefore optimized to result in similar insertion loss in the bypass and phase-delay states for low rms amplitude error versus 32 phase states (see Table 3.1).

In the previous single-ended design [44], the 180° phase shifter was built by cascading two 90° switched-delay phase shifters, and its insertion loss was too high (8–9 dB). However, in the differential design, the 180° phase shifter can be easily implemented by controlling the quad switches of a Gilbert cell such that gain is achieved rather than loss (Fig. 3.6(b)).

The 90° phase shifter has an insertion loss of 3–4.3 dB and a $S_{11}$ (or $S_{22}$) < -12.7 dB from 70–83 GHz for the bypass and phase-delay states. The 180° phase shifter has 2.9 dB gain at 80 GHz, with $S_{11}$ and $S_{22}$ < -15 dB at 71-90 GHz and 76-83 GHz, respectively for both states. By placing the active 180° phase shifter in the center of other phase shifter cells as shown in Fig. 3.2(b), the effect of the impedance mismatch between two different states of the passive cells is minimized due to the high isolation of the active phase shifter ($S_{12}$ < -35 dB).

The performance of the 5-bit cascaded phase shifter is shown in Fig. 3.7. Due to the non-identical loss of the phase shifter cells in the bypass and phase shift states, and the cascading of non-ideal 100 Ω differential blocks, the simulated gain is -8.0 ± 1.5 dB versus 32 phase states. The variable gain amplifiers are therefore used to compensate for this effect and to result in a low rms gain error. The simulated phase error is ±4.4° at 80 GHz (rms phase error of ~ 2.2°). Note that the 11°, 22.5°, 45° and 90° LC phase shifters are of the true-time delay type, while the 180° phase shifter is a constant-phase design. Therefore, there is an inherent mismatch in the slope of the phase delay between the 180° phase shifter and the other cells, and this results in added phase error versus frequency. Still, for relatively narrowband circuits, this design results in acceptable performance and the rms phase error remains < 12° at 76-84 GHz.
3.2.5 Phased Array Channel

The phased-array channel is shown in Fig. 3.2(b), with a balun at the input and an LNA/VGA placed on both sides of the 5-bit phase shifter. The simulated peak gain is 15.5 dB at 77–79 GHz with a 3-dB BW of 72.5–83.6 GHz (Fig. 3.8). Two 2-bit VGAs are used, one on each side of the phase shifter, with a total gain control of 8.7 dB and a ∼0.6 dB gain step.

The simulated NF is 11.8 dB and increases to 13.7 dB at the lowest gain setting. The simulated input $P_{1dB}$ is -25.9 dBm at 80 GHz, and results in an output $P_{1dB}$ of -11.8 dBm which is fed to the 16:1 Wilkinson combiner. The input $P_{1dB}$ increases to -25 dBm at minimum gain setting and is limited by the last LNA/VGA. Each channel consumes 25 mA of current from 2 V at maximum gain setting.

3.2.6 Differential Wilkinson Combiner/Divider

Fig. 3.9 presents the 100 Ω differential Wilkinson combiner/divider, designed using two $\lambda/4$ sections of 141 Ω CPW lines (Q=13 at 80 GHz). Simulations indicate an insertion loss of ∼0.9 dB and $S_{11}/S_{22}/S_{33} < -20$ dB at 72–88 GHz. The isolation between the two ports, $S_{23}$, is < -25 dB at 72–88 GHz. The cross-overs at the 90° turn and at ports 2 and 3 (with the resistor connections) were optimized using Sonnet to result in equal phase delay in each line of the GSSG differential line. The Wilkinson combiner is wideband and has no effect on the channel S-parameters except for an additional 0.9 dB loss per stage. It also allows for combining at high power levels with no DC power consumption. The 16:1 combiner network results in 7 dB loss at 80 GHz: The Wilkinson combiners have a combined loss of 3.6 dB ($4 \times 0.9$), and the additional transmission lines used to connect all 16 inputs to the mixers (3.3 mm in total) result in an additional loss of 3.4 dB.

3.2.7 Doubler

The 38–42 GHz FMCW LO input signal is provided externally and is up-converted using an on-chip doubler. The 38 GHz LO results in a lower distribution loss between the Tx and Rx chip on the Teflon board and an easier flip-chip (or bond-wire) transitions. Also, any coupling between the LO ports and the RF ports results in a high IF which is filtered by the DC – 5 MHz IF amplifiers. The doubler is an active balanced design biased near the class-B region in order to generate the second harmonic components efficiently (Fig. 3.10) [45]. A cascode stage is added to increase the conversion gain and isolation between the input and output ports. The simulated conversion gain is 4 dB for an input power of -5 dBm at 38.5 GHz with $S_{11}$ and $S_{22}$
**Figure 3.8:** Simulated gain and NF of the phased array channel at maximum, medium and minimum gain settings ($0^\circ$ phase setting).

**Figure 3.9:** Schematic and layout of the differential Wilkinson combiner/divider.
Figure 3.10: Schematic of the doubler.

Figure 3.11: (a) Block diagram of LO path, schematic of (b) IQ generator, (c) Amp2. (d) Simulated delivered power from the LO port ($P_{in}$) to the I/Q mixers ($P_{LO}$).
Figure 3.12: (a) Schematic of the mixer. Simulated (b) voltage conversion gain and (c) single sideband noise figure of the mixer.
< -10 dB at 36–44 GHz and 72–87 GHz, respectively. The simulated output power at 1\textsuperscript{st}, 2\textsuperscript{nd} and 4\textsuperscript{th} harmonics with -5 dBm input power are -60 dBm, -54 dBm and -18 dBm respectively.

3.2.8 LO Path

As shown in Fig. 3.2(a), the doubled LO signal is first converted to a differential signal using a passive balun and then split into two paths using a differential Wilkinson divider: The BIST path and the LO path. In the LO path (Fig. 3.11(a)), a set of I and Q signals are generated using a single-stage RC-CR polyphase filter (Fig. 3.11(b)). In order to compensate the balun, Wilkinson divider and I/Q network losses, two amplifiers are added and act as limiting amplifiers for the I/Q mixers (Fig. 3.11(c)). Amp1 and Amp2 have a simulated gain of 8.5 dB and 12.6 dB at 80 GHz, with an output $P_{1dB}$ of -4.7 dBm and -0.7 dBm, respectively. Each amplifier consumes 15 mA and the total current of the LO chain (doubler, Amp1 and Amp2) is 56 mA from a 2 V supply. The simulated LO power delivered to the I (or Q) mixer is > -2 dBm at 75–84 GHz for $P_{in}$ > -5 dBm (Fig. 3.11(d)).

3.2.9 I/Q Mixer

The active I/Q mixers are based on a double-balanced mixer topology (Gilbert cell) (Fig. 3.12(a)) with inductive degeneration for high linearity. At the IF output, 130 Ω resistive loads are added for wideband IF operation and a 1 pF capacitor is used as a filter to eliminate any RF and LO leakage. The simulated voltage conversion gain is 8 dB for an LO input power of 0 dBm (Fig. 3.12(b)), and a return loss at the RF and LO ports of > +10 dB at 70–86 GHz. The simulated NF with a 2 kΩ load is 16.6 dB at 10 kHz IF (Fig. 3.12(c)). The mixer input $P_{1dB}$ is -5.8 dBm with a current consumption of 13.3 mA from a 2 V supply.

3.2.10 IF Amplifier

The IF amplifier is shown in Fig. 3.13(a) and is built using an RC-compensated 2-stage op-amp with 2-bit gain control (Fig. 3.13(b)), followed by an inverter-type buffer (Fig. 3.13(c)). BJT transistors are used at the input of the op-amp due to their lower 1/f noise. An inverter-type buffer with resistive feedback is used for driving the low impedance output loads. The simulated closed-loop differential output impedance of the IF amplifier is 260 Ω. The voltage gain of the IF amplifier is 26/19/12/3 dB with a high impedance load, and the gain drops by 11 dB if the output is terminated with a 100 Ω differential load. The differential output voltage swing at 1-dB compression point is 2.86 V_{ppk} with a high impedance load.
Figure 3.13: (a) Block diagram of the IF amplifier, (b) schematic of the 2-stage op-amp, and (c) schematic of the buffer.
The closed-loop 3-bandwidth is 5.8 MHz at the highest gain setting. This is larger than required for FMCW radars and additional filtering is used on the PCB. The total current consumption of the op-amp and buffer is 7.7 mA from a 2 V supply.

### 3.2.11 RF Monitor

In order to measure the chip in the absence of an LO signal, an RF monitor section is implemented as shown in (Fig. 3.2(a)), and provides both an RF output port and a power detector port. The 16:1 combiner output is sampled using a differential resistive -10 dB coupler (Fig. 3.14(a)) and fed into a differential amplifier with a gain of ~9 dB. This amplifier output is converted to a single-ended signal and connected to a GSG pad for measurement purposes. Another resistive -10 dB coupler is used after the balun and the sampled signal is fed to a power detector (Fig. 3.14(b)). The detector output is then amplified using an Op-Amp with a gain of 20 dB and a 3-dB BW of 11.5 MHz. The simulated responsivity is 83 kV/W including the Op-Amp with an NEP of 3.4 pW/√Hz, resulting in an output noise of 282 nV/√Hz. This translates into an input power of -41 dBm at any RF port (one at a time) with an SNR of 10 dB in a 1 kHz bandwidth. For antenna pattern measurements with power at all RF ports, the input power per channel is -45 dBm for a 30 dB SNR so as to accurately measure all the sidelobes.
Figure 3.15: (a) Setup for gain and NF simulations. (b) Simulated conversion gain and NF versus RF frequency for the entire chip (0° phase setting).
3.2.12 RF Path System Simulation

The RF path gain, defined as the output IF voltage in 2 kΩ load divided by the RF voltage at the input of a channel \(V_{RF} = \sqrt{P \times Z_o}\), is then simulated using the blocks defined above (Fig. 3.15(a)). The peak gain is 39 dB with a 3-dB bandwidth of 73–83 GHz (Fig. 3.15(b)). The system NF is 18–22 dB at an IF of 100–10 kHz, respectively, due to the 1/f noise in the mixer and IF amplifiers. For this simulation, the Wilkinson 7 dB ohmic loss was taken into account, but the 12 dB combiner gain was not included. If all 16 channels are activated, the electronic gain does not change since the additional 12 dB will be taken into account as a larger antenna aperture with a higher received power. The system linearity is -26 dBm when all channels are activated since the power available at the mixer input is still < -6 dBm at maximum gain.

3.3 Built-In Self-Test System Design

Fig. 3.16 presents the on-chip BIST system. A Wilkinson power divider and an absorptive active SPDT switch are used after the doubler to distribute the LO signal to the left side, right side, or even both sides of the chip (this LO signal is the BIST signal). These units are located at the center of the chip (next to the doubler), and therefore, a 3.75 mm long transmission line is required to connect the SPDT switch to channels 8 and 16. The BIST transmission lines continue through the length of the chip (left and right sides) up to channels 1 and 9 with a total length of 4.9 mm each, and are terminated with 100 Ω resistors for minimal reflections. Differential couplers with a coupling value of -26 dB are used to connect the BIST signal to every phased array channel. After passing by the phased-array channels (generally turned on one at a time), the BIST signal mixes in the on-chip I/Q receiver in a homodyne fashion, thereby resulting in DC voltages at the I and Q outputs which are proportional to the gain and phase settings of each channel. The BIST system employs the standard DC-5 MHz I/Q receiver and does not require any additional circuitry other than the Wilkinson divider and active SPDT switch.

The differential BIST transmission-line and coupler are shown in Fig. 3.17. The BIST line is built using the M3 layer \((Z_o = 85 \, \Omega, \text{loss} = 4 \, \text{dB/mm at 80 GHz})\) and is shielded from the RF line and silicon substrate using the MQ and M1 ground layers. A lumped-element coupler is built at each channel by locally opening the MQ ground layer, moving up the BIST line to M4, dropping the RF line to MQ, and widening both to \(11 \times 12 \, \mu m^2\), thereby creating a capacitive coupler. The BIST and RF line are coupled at two different positions to ensure an
Figure 3.16: BIST diagram showing signal gain of each block.
equiphase response at port 2. Full-wave electromagnetic analysis using Sonnet shows $S_{23} = -26$ dB coupling when port 1 is terminated differentially with 100 Ω (i.e. attached to antennas) and -20 dB when port 1 is left open-circuited (i.e. chip test with no external connections). The 6 dB increase is due to the BIST voltage wave coupling to port 1, reflecting at the open circuit and then adding in phase with the BIST voltage wave coupling to port 2. The coupler effect on the RF line is minimal ($S_{21} < -0.2$ dB, $S_{11} < -20$ dB at 80 GHz).

Lumped-element couplers are very compact but non-directional and therefore create a permanent coupling path between any two channels. A coupling value of -26 dB was chosen for minimal effect on the phased array performance (details of this derivation are found in [36]).

Note that the BIST transmission-line loss is 4 dB/mm and therefore there is an additional loss of $\sim 2.7$ dB between the channels (spaced 700 µm apart) and a loss of 18.9 dB between channels 8 and 1. As will be seen later, the signal levels are high enough that the BIST system has acceptable dynamic range even for the far-away Channels 1 and 9.

The absorptive SPDT cascode switch is implemented using SiGe transistors. The design (Fig. 3.18) follows the current steering approach in [46] and has a simulated insertion gain of 1.1 dB at 80 GHz and an isolation $> 45$ dB at 70-100 GHz. The 3-dB gain bandwidth is 64–99 GHz. The design maintains an input return loss $> 10$ dB under all switch conditions (off, on port 2, on port 3, on port 2 and port 3). The simulated switching time is 15 ns.

There are several system-level issues to consider in the BIST system and are listed below:

- **SPDT Switch Isolation Effect:** Even when the BIST is non-activated, there is still a low-level signal present at each phased-array channel due to the finite SPDT switch isolation. This leakage BIST signal is downconverted and generates a dynamic DC offset voltage (with its associated phase noise spectrum) depending on the gain and phase state setting of the channels. An input power of -5 dBm after the Wilkinson coupler and a switch isolation of 40 dB results in a signal of -86 dBm at channels 8 and 16 (-86 dBm = -5 dBm - 40 dB - 15 dB - 26 dB). This is 55 dB lower than the expected coupling from the transmit antenna to the receive antenna ($\sim -35$ dB) knowing that the transmit power is 0–3 dBm. The BIST leakage remains 40 dB lower than the Tx-to-Rx antenna coupled signal even if 2-4 channels add coherently due to their phase shift settings (note that only 2-4 channels are considered due to $\sim 3$ dB loss in the BIST signal between every two adjacent channels).

- **SPDT Switch Reflection Coefficient Effect:** The BIST signal can reflect from the SPDT switch and add coherently (constructively or destructively) with the direct LO path for
Figure 3.17: (a) BIST coupler layout and Sonnet 3-D view (ground planes are removed for clarity) and (b) simulated S-parameters.
Figure 3.18: Absorptive active SPDT switch for on-chip BIST.

the I/Q mixer. Therefore, a Wilkinson power divider is used which provides $> 20$ dB isolation between its output ports. The SPDT switch is also designed to be absorptive under all switch states with a minimum reflection coefficient of -10 dB. Therefore, the BIST signal reflecting back into the LO path is $< -35$ dBm (-5 dBm -10 dB -20 dB) and has little effect on the main LO path.

c) BIST Dynamic Range: Referring to Fig. 4.9, a signal power of -5 dBm at Plane A and an SPDT switch gain of 2 dB results in an injected test signal level of $\sim -45$ dBm at Plane B of Channel 8. The simulated single-sideband noise figure of a single channel (with all other channels off) is 27 dB due to the 19 dB Wilkinson power combiner loss. The equivalent noise power at Plane B in a 5.8 MHz IF bandwidth can be calculated as:

$$N_B = kT \text{ (dBm/Hz)} + NF_{SSB} \text{ (dB)} + BW \text{ (Hz)}$$

$$= -174 + 27 + 67.5$$

$$= -79.5 \text{ dBm.}$$

The resulting SNR at plane B is

$$SNR_B = \frac{S_B}{N_B}$$

$$= 34.5 \text{ dB (5.8 MHz Bandwidth)}$$

$$= 50 \text{ dB (} \sim 200 \text{ kHz Bandwidth).}$$

These values correspond to an output signal of 49 mV and an rms output noise voltage of 653 $\mu$V in 5.8 MHz bandwidth. The noise drops to 121 $\mu$V if the bandwidth is reduced to
200 kHz using an off-chip low-pass filter. A bandwidth of 5.8 MHz (or 200 kHz) results in a measurement time of 107 ns (or 3.1 µs) for 98% settling value. Note that due to the 20 dB signal loss between Channels 8 and 1 (and Channels 16 and 9), it is preferable to use a 200-500 kHz measurement bandwidth so as to maintain a large SNR even at the edge of the chip.

3.4 Measurements

3.4.1 Single-Element

The single-element test cell employs an additional balun at the output port to convert the differential signal into a single-ended signal for measurement purposes (Fig. 3.19(a)). S-parameter measurements of the channel are performed using an Agilent E8361A Vector Network Analyzer and W-Band frequency extenders. A Short-Open-Load-Thru (SOLT) calibration is performed to set the reference plane at the probe tips, hence all measurements include the input and output GSG pad transition loss. The output balun loss is not deembedded out of the measurements.

The single channel consumes 30 mA from a 2 V supply. A wideband input and output matching is achieved with $S_{11}$ and $S_{22} < -9$ dB at 72–88 GHz and 73–86 GHz, respectively (not shown). Fig. 3.20 presents the measured amplitude and phase response of $S_{21}$ and its rms errors for 16 phase states. The measured average power gain ($S_{21}$) is $> 10$ dB for 76.4–90 GHz, and the rms gain error is $< 1$ dB for 74–84.2 GHz. The rms phase error is $< 11^\circ$ at 73.6–83.6 GHz. In order to optimize the rms phase error, the $11^\circ$ phase shifter value is used, thus making the 5-bit design effectively a 4-bit design. The measured reverse isolation ($S_{12}$) is $<-45$ dB (not shown).

Fig. 3.21 presents measured VGA operation with 4-bit digital control. The VGA can be controlled over an 8 dB range with $\leq \pm 5.3^\circ$ phase change. The noise figure (NF) is measured for several gain states: At the maximum gain state, the NF is 11.4–13 dB at 77–87 GHz and increases by 1.5 dB at the minimum gain state (Fig. 3.22). Fig. 3.23 presents the measured input $P_{1dB}$ of -20 dBm and -25.8 dBm at 77 GHz and 83 GHz, respectively, at the maximum gain state.

The channel gain performance versus temperature is shown in Fig. 3.24. The gain variation is $< 1.9$ dB up to 100°C. This is achieved by using Proportional-To-Absolute-Temperature (PTAT) bias circuits and results in an increased current consumption of the channel from 30 mA to 48.5 mA as the temperature increases from 25°C to 100°C.
Figure 3.19: Photograph of (a) single channel (2.0 x 0.65 mm$^2$) and (b) 16-element phased arrays (5.5 x 5.8 mm$^2$).
Figure 3.20: Measured (a) gain and rms gain error and (b) phase response and rms phase error for 16 phase states, for a single phased array channel.

Figure 3.21: Measured VGA operation at the 0° state in a phased array channel.
Figure 3.22: Measured noise figure for different gain settings for a single phased array channel.

Figure 3.23: Measured P$_{1dB}$ at 77 GHz and 83 GHz for VGA = 0000 (max. gain) for a single phased array channel.

Figure 3.24: Measured gain of a single channel at different temperatures.
In general, the single channel measurements agree well with simulations except for a
shift in frequency upwards from 78–79 GHz to 83–84 GHz. This is currently under investigation.

### 3.4.2 16-Element Phased Array

The 16-element phased array was also characterized using on-wafer probing (Fig. 3.19(b)). The differential LO signal (37.5–45 GHz) was generated using a WR-19 Hybrid Tee
with < 1 dB amplitude and < 5° phase imbalance over the measurement band. The RF signal
(75–90 GHz) was applied using a GSG probe to one channel at a time and the differential I/Q IF
outputs were measured in the voltage domain with a differential 1 kΩ load. All measurements
are referenced to signal I/O pads.

Fig. 3.25(a) presents the measured voltage conversion gain of the 16-element phased
array versus frequency, where conversion gain is defined as the ratio of the IF I/Q voltage to
the RF voltage at GSG input pad of the channel. Since one channel is fed at a time, there is an
additional 12 dB loss in the 16:1 differential Wilkinson combiner network and it is deembedded
from the results (12 dB is added for all conversion gain measurements). The measured peak
gain is 34–35 dB, which is ~5 dB lower than simulated. This can be due to ~2 dB more loss in
the Wilkinson combiners and transmission lines and ~2 dB lower gain in the I/Q mixers. The measured IF bandwidth is 5 MHz (Fig. 3.25(b)) and the required LO power is ~4 dBm at 77
GHz and ~0 dBm at 83 GHz (Fig. 3.25(c)). The measured I/Q imbalance is < 1 dB at 75–84
GHz and < 0.5 dB at 75–81 GHz as shown in Fig. 3.26. The I/Q phase error remains < 10° over
all frequencies.

Due to the additional 12 dB loss in the Wilkinson combiner network mentioned above,
the channel compresses before the down-conversion mixers and the 1-dB compression of the
entire receiver chip could not be measured.

Fig. 3.27 presents the measured RF and IF gain control of the receiver. The 4-bit VGA
of the phased array channel provides 11.2 dB range with ~0.75 dB steps, and the IF amplifier
results in a total 21 dB gain control using 2 bits.

The measured conversion gain for 12 different channels is presented in Fig. 3.28
(Channels 1, 2, 9 and 10 could not be measured since the north DC probe blocks the RF GSG
probe movement). The gain variation across channels is ±2.1 dB and this has been traced to a
layout mistake in the bias distribution.
Figure 3.25: Measured conversion gain of the entire receiver versus (a) RF frequency (b) IF frequency and (c) LO power. Input is at a single RF channel, and output is at the I and Q ports.
Figure 3.26: Measured I/Q amplitude and phase imbalance of the I/Q receiver.

Figure 3.27: Measured RF and IF gain control of the I/Q receiver.

Figure 3.28: Measured conversion gain of the receiver for different channels.
**Figure 3.29**: Leakage between two channels due to the BIST transmission-line and measured coupling between channel 3 and channel 4.
3.4.3 Channel to Channel Coupling

The -26 dB BIST couplers generate a permanent -52 dB coupling path between adjacent channels [36]. The coupling between the channels was characterized by measuring the down-converted I/Q voltage with an input at channel 3 and toggling the phase state of channel 4, and fitting a coupling vector, c. A coupling of -50 dB was measured at 77 GHz (Fig. 3.29). Measurements at several other frequencies and on several channels resulted in coupling values between -48 dB and -54 dB, which is very low and within expected values. Such coupling values have no effect on the phased-array operation.

3.4.4 Built-In Self-Test

S-Parameter measurements of the active absorptive SPDT switch are shown in Fig. 3.30. The switch has $>2$ dB gain in the on state and $<35$ dB isolation in the off state at 70–81 GHz. In both on and off states, the input and output return loss are $<-10$ dB at 70–90 GHz.

The loss of the BIST transmission-lines was characterized by measuring a 200 $\mu$m and an 800 $\mu$m long test cells. The measured loss is 7.5 dB/mm and is higher than the simulated value of 4 dB/mm (Fig. 3.31). We believe that this is due to the TiN adhesion layers surrounding the thin metal layers in M3-M4. This additional loss resulted in lower power injection to the channels, and reduced SNR in the BIST measurements.

The channel response in the 16-element array was measured using the BIST technique at 75–85 GHz. During the measurements, only the LO signal is provided to chip, which is used both as a test signal to channels and an LO to the I/Q receiver. The LO BIST signal is routed to the channels using the SPDT switch and one channel is turned on at a time and measured versus 32 phase states. The BIST measurements were performed with the channel input port terminated with 50 $\Omega$ using a GSG probe and the channel input port left open circuited. This represents conditions of the chip connected to antennas, or a die being tested on-wafer without any RF probes.

The measured differential DC I/Q voltages versus 32 phase states for a 77 GHz test signal at channel 15 are shown in Fig. 3.32 for both input termination conditions. The I and Q data settled in $\sim2$ $\mu$s due to low-pass filtering in the readout electronics. The channel amplitude and phase response were then obtained using:

$$A = \sqrt{I^2 + Q^2}$$

$$Phase = \tan^{-1}(Q/I)$$
Figure 3.30: Measured (a) gain and isolation (b) input and output return loss of BIST SPDT switch.

Figure 3.31: Measured and simulated loss of differential buried (M3) BIST transmission line.
Figure 3.32: Measured I and Q voltages of channel 15 at 77 GHz with (a) channel input terminated and (b) channel input left open circuited.
Figure 3.33: Measured relative phase, phase error and gain error from the ideal phase state of channel 15 at 77 GHz with (a) channel input terminated and (b) channel input left open circuited.
Figure 3.34: Measured phase and gain error from the ideal phase state of channel 5 at 77 GHz with (a) channel input terminated and (b) channel input left open circuited.
Figure 3.35: Measured phase and gain error from the ideal phase state with and without I/Q error correction of (a) channel 7 and (b) channel 13 at 83 GHz with channel input terminated.
Figure 3.36: Measured RMS phase and gain error of channel 5 with (a) channel input terminated and (b) channel input left open circuited. Same with channel 15 in (c) and (d).
Figure 3.37: Measured gain control of channel 14 at 77 GHz with channel input terminated.

Figure 3.38: Effect of antenna port termination on coupler performance.
Fig. 3.33 presents the comparison of the BIST and S-parameter measurements, showing good agreement. As another case, Fig. 3.34 shows the BIST and S-parameter measurement comparison of channel 5 at 77 GHz. Due to higher loss in the BIST transmission line up to channel 5 (37.7 dB versus 20.4 dB simulated), the signal power at the input of channel 5 is lower than expected, resulting in a lower SNR. Still, good agreement is seen even with a low signal level of ∼70 dBm.

The BIST measurements rely on accurate I/Q balance in the receiver and any I/Q phase and amplitude error reflects on BIST measurements. Fig. 3.35(a) presents the BIST measured response of channel 7 at 83 GHz. Due to the I/Q mismatch, the measured BIST response deviates from the S-parameter measurements. The channel response can be recalculated using the previously measured I/Q imbalance data (Fig. 3.26) and the I/Q error correction significantly improves the agreement between BIST and S-parameter measurements. Fig. 3.35(b) presents the same error correction procedure on channel 13 with similar performance improvement.

The calculated RMS gain and phase error versus frequency for channel 5 and channel 15 are presented in Fig. 3.36 for both channel input termination conditions. Channel 14 VGA operation is characterized with BIST, and relative gain and phase measurements are shown in Fig. 3.37.

Finally, the BIST results in accurate gain measurement versus frequency for the entire receiver system. However, it is a relative gain measurement since absolute power meters are not used at the input and output ports. The BIST value is normalized to the measured gain at 77 GHz and as seen in Fig. 3.25(a), predicts the relative gain accurately at 75–80 GHz.

3.5 Discussion

The BIST system worked well at 75–80 GHz and then at 83–84 GHz, but there was a sharp dip in the measured I and Q levels at 81–82 GHz which affected the SNR and the measurement accuracy. The I and Q signals decrease was especially high when the RF port was in the open-circuit condition. This was traced to placing the -26 dB coupler between the balun and the LNA. Since the coupler is bidirectional, half of the power couples to the balun, passes by the balun, reflects at the open circuit, and then passes by the balun again. This path can result in a 180° phase shift at certain frequencies and cancel the main coupling path to the LNA, resulting in a very low injected signal and reduced SNR, as seen in Fig 3.38. Note that the simulations indicate a null at ∼90 GHz, but the actual null was found to be at 81–82 GHz. This is due to the EM modeling of the balun and the fact that the null is based on phase cancellation (and very
<p>| | |</p>
<table>
<thead>
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<tbody>
<tr>
<td><strong>Table 3.2: Performance Summary</strong></td>
<td></td>
</tr>
<tr>
<td><strong>Frequency</strong></td>
<td>76–84 GHz</td>
</tr>
<tr>
<td><strong>Number of elements</strong></td>
<td>16</td>
</tr>
<tr>
<td><strong>Channel gain</strong></td>
<td>11 dB @ 77 GHz</td>
</tr>
<tr>
<td></td>
<td>16 dB @ 83 GHz</td>
</tr>
<tr>
<td><strong>Array gain</strong></td>
<td>30 dB @ 77 GHz</td>
</tr>
<tr>
<td></td>
<td>33 dB @ 83 GHz</td>
</tr>
<tr>
<td><strong>Number of phase bits</strong></td>
<td>4-bits</td>
</tr>
<tr>
<td><strong>Number of gain bits</strong></td>
<td>4-bits (RF)</td>
</tr>
<tr>
<td></td>
<td>2-bits (IF)</td>
</tr>
<tr>
<td><strong>RMS phase error</strong></td>
<td>&lt; 11°</td>
</tr>
<tr>
<td><strong>RMS gain error</strong></td>
<td>&lt; 1 dB</td>
</tr>
<tr>
<td><strong>NF (channel)</strong></td>
<td>11.4–13 dB</td>
</tr>
<tr>
<td><strong>NF (system)</strong>*</td>
<td>18 dB</td>
</tr>
<tr>
<td><strong>Input P_{1dB}</strong></td>
<td>-26 dBm</td>
</tr>
<tr>
<td><strong>Gain control</strong></td>
<td>11.2 dB (RF)</td>
</tr>
<tr>
<td></td>
<td>21 dB (IF)</td>
</tr>
<tr>
<td><strong>Power consumption</strong></td>
<td>1–1.2 W</td>
</tr>
</tbody>
</table>

*simulated.
accurate models are needed). Fortunately, this problem can be easily remedied in future designs. The BIST line and coupler should be single-ended and placed between the GSG pad and the balun. This would not only eliminate the balun double-reflection problem, but also result in higher SNR since buried single-ended CPW lines have less loss than buried differential lines.

### 3.6 Conclusion

This chapter presented a 16-element phased array receiver with built-in self-test capabilities and the measured performance is summarized in Table 3.2. It is shown that the BIST can be used to accurately measure many key parameters of the phased-array chip (gain and phase variation versus phase state, gain, control, etc.), including the relative gain versus frequency of the entire receiver. This phased array chip has been packaged with 16 antennas and resulted in pattern scanning up to $\pm 50^\circ$ with -17 dB sidelobes. Also, it has been used in FMCW radar system to achieve a state-of-the-art W-band imaging system. These results can be found in [47].

### 3.7 Acknowledgement

This work was supported in part by Toyota Research Institute of North America, Ann Arbor, Michigan and by Intel Corp., Portland, Oregon.

Chapter 3 is mostly a reprint of the material as it is submitted for publishing to IEEE Microwave Theory and Techniques, 2013. Sang Young Kim; Ozgur Inac; Choul-Young Kim; Donghyup Shin; Gabriel M. Rebeiz. The dissertation author was the primary author of this material.
Chapter 4

A 90-100 GHz Phased-Array Transmit/Receive Silicon RFIC Module with Built-In Self-Test

4.1 Introduction

Millimeter-Wave phased arrays based on silicon RFIC chips have been recently demonstrated from 30–100 GHz and with a large number of elements on a single chip [7, 8, 10, 21, 35, 43, 48–51]. The All-RF architecture is the dominant architecture due to its simplicity and its scalability to large phased arrays with thousands of elements [52]. The silicon designs allow the integration of many channels on the same chip, but also all the necessary digital control electronics, and therefore, are now playing an essential role in lowering the cost of large mm-wave phased array systems. However, the testing of these multi-channel chips is still based on expensive CPW probes, especially at mm-waves, which greatly increases the cost of the RFIC chip. In fact, the cost of testing a phased array far exceeds the cost of the chip itself, especially at millimeter-wave frequencies.

In order to solve this problem, Inac et al. demonstrated in [36] a two-channel X-band phased array chip with built-in-self-test (BIST) capabilities. The on-chip BIST was based on non-directional couplers at the input of each phased-array channel, and was able to measure each channel individually and with high accuracy. In fact, the channel was measured to an accuracy better than 5-bit phase control, and 0.5 dB gain control at 8.5-11 GHz, and with a settling time of only 300 ns. The work was further extended to a 16-element 76-84 GHz phased array
for automotive radars in [43] again with excellent agreement between BIST data and standard probe-based S-parameter measurements. Other methods which offer BIST capabilities are based on loop-back techniques as demonstrated in [53]. The techniques presented in [36, 43, 53] are compatible with a receive only, or a transmit only, but not a transmit-receive (T/R) chip which is typically used in pulsed-based radar systems.

This chapter presents the first built-in-self-test system for T/R modules and which is based on low-loss high-isolation switches (Fig. 4.1). The BIST allows S-parameter measurements for all channels in both directions (transmit and receive) with high accuracy and with minimal penalty in additional loss. The system is implemented on a complex 90-100 GHz T/R chip with vertical and horizontal channels for polarimetric mm-wave radars [54].

### 4.2 On-Chip Built-In Self-Test System

#### 4.2.1 BIST Architecture

The single-element block diagram with BIST capabilities is shown in Fig. 4.1. In this design, the transmit mode is sequentially polarimetric, that is, a single polarization is transmitted at a time (V or H). On the other hand, the receive mode is fully polarimetric and two simultaneous phased-array receive channels, one for the vertical and one for the horizontal polarization, are used. The chip is fabricated in the IBM8HP SiGe BiCMOS process with an $f_t/f_{max}$ of 200 GHz, 0.12 $\mu$m CMOS transistors, and 7 metal layers with 2 thick top metals (Fig. 4.2). Grounded coplanar waveguide (G-CPW) transmission lines are used throughout the chip with a simulated loss of 1 dB/mm at 90-100 GHz (for 50 $\Omega$ lines), results in a Q of 16. All transmission-lines components are simulated with Sonnet [55], a full-wave EM program, for added accuracy. Details of the T/R module circuit design are presented in [56].

Fig. 4.1 also presents the BIST system surrounding the polarimetric T/R module, with key elements being the low "additional insertion-loss" SPDT switches and a well balanced W-band I/Q receiver. Note that in this case, "additional insertion loss" does not refer to the traditional switch insertion-loss (in fact, compact lossy switches are used), but to the additional loading and insertion loss on the main RF lines which is caused by the SPDT switch. The system operates as follows: An oscillator generates the BIST signal at 90-100 GHz and is divided using a -18 dB capacitive coupler into an injection (BIST) path and a local oscillator path. The coupler is built using a capacitive overlap design [36] and has an insertion loss of $< 0.2$ dB at 90-100 GHz (Fig. 4.3). The BIST path is connected to Switch 1 which selects the BIST signal injection
**Figure 4.1**: Block diagram of the T/R module with BIST.

**Figure 4.2**: IBM8HP metal stack-up with a representative 50 Ω G-CPW line.
point, either from the antenna side or from the transmit/receive electronics side. Switches 5 and 6 select the vertical or horizontal channel to be measured. Switches 2, 3, 4 are tied to switch 1 logic state, and connect the antenna side or the transmit/receive electronics side to the I/Q receiver. For example, the configuration shown in Fig. 4.1 is for measuring the receive vertical-polarization channel.

### 4.2.2 Switch Network Design

Switches 1, 2, 3, 4 are standard SPDT routing switches and are based on series-shunt switches for high isolation (Fig. 4.4). L1, C1 and L2, C2 are used as matching components and result in a total switch dimension of 150×310 µm². The simulated S-parameters show an insertion loss of ∼6 dB at 90-100 GHz with an isolation of ∼32 dB and a wideband impedance match.

Switches 5 and 6 are the key switches which are attached to the vertical and horizontal ports, and must result in low (< 0.5 dB) additional insertion loss on the RF lines since they have a direct effect on the gain and noise figure in the receive mode (and output power reduction in the transmit mode). These switches also create a permanent coupling path between the V and H channels and therefore, this coupling path must be very low (< -50 dB) when the BIST is not activated. This is achieved using a series-shunt switch and λ/4 lines on each side which connects the SPDT switch to the main RF lines (Fig. 4.5(a)). In this case, the low impedance presented by M3 or M4 when turned on (∼4 Ω) results in a high impedance at the RF line (∼385 Ω at 95 GHz) and thus minimal loading. When the BIST mode is activated (for example, V_C1 = 1, V_C2 = 0), the SPDT switch results in an insertion loss, S_{25}, of ∼10 dB and an isolation, S_{45}, of ∼35 dB (Fig. 4.5(b)). However, when the BIST mode is not activated and both arms of the SPDT are turned off (V_C1 = 0, V_C2 = 0), then the isolation between the V and H channel is > 62 dB at 90-100 GHz (Fig. 4.5(b)).

The "additional insertion loss" on the RF line is due to the large but finite impedance loading and is S_{21}=S_{43}=-0.5 dB at 90-100 GHz which is acceptable in most systems (Fig. 4.5(c)). Note that the loading does not degrade the S_{11} of the main RF line at 90-100 GHz (Fig. 4.5(c)).

### 4.2.3 LO Path and I/Q Receiver

The design of an accurate 90-100 GHz I/Q homodyne (direct-conversion) receiver is essential for a high-performance BIST system and care is taken to achieve very low gain and phase imbalance (Fig. 4.6(a)). The LO signal (i.e. BIST signal from source) first passes by a
Figure 4.3: Sonnet 3-D view and simulated S-parameters of the -18 dB coupler.

Figure 4.4: (a) Schematic of the SPDT switches 1-4 and (b) simulated S-parameters.
Figure 4.5: (a) Schematic of the SPDT switches 5-6, (b) simulated S-parameters and (c) its loading effect on RF line.
Figure 4.6: (a) Block diagram of the BIST I/Q receiver, (b) layout and the amplitude and phase imbalance of the I/Q generator, (c) schematic of the differential LO buffer, (d) schematic and the layout of the double balanced passive mixer, (e) layout and the simulated response of RF-path I/Q signal splitting, (f) schematic of the IF amplifier.
Figure 4.7: Simulated (a) conversion gain and noise figure of the BIST I/Q receiver versus frequency and (b) conversion gain versus LO power.

Figure 4.8: Simulated noise figure of the BIST I/Q receiver.
Figure 4.9: (a) BIST diagram showing signal gain of each block and (b) simulated frequency response of BIST system, with the channel replaced by a transmission line.
coupled-line I/Q network which generates a near zero phase imbalance and ±0.6 dB amplitude variation at 90-100 GHz (Fig. 4.6(b)). The I and Q LO signals are then fed to baluns which have a finite even- and odd-mode components at their output ports. Differential limiting amplifiers with a gain of 6.8 dB are then used to remove the common mode component and reduce the amplitude imbalance to 0 dB when operating in the saturation mode (Fig. 4.6(c)). The high-level (±1.5 V_{peak}) I and Q LO signals then drive two passive double-balanced mixers, and the IF signals are DC coupled to two op-amps with a 3-dB bandwidth of 7 MHz. Double-balanced passive mixers are used due to their low voltage offsets and low 1/f noise properties, both critical for direct conversion receivers with a low IF bandwidth (Fig. 4.6(d)(e)(f)). Also, passive mixers have a high input P1dB which allows testing in the transmit mode.

The W-band receiver is essentially the same I/Q receiver architecture as in [36, 43], but care is taken in the I/Q mixer layout to achieve near-ideal balance. Also, Sonnet is used to simulate all interconnects to ensure equiphase connections for the I and Q paths. The BIST circuitry, without the oscillator, consumes 42 mA from a 2 V supply. Most of the current is used in the LO drivers, since the switches and mixers are passive.

The simulated voltage conversion gain is 15-16 dB with a noise figure of 27-28 dB at 90-100 GHz at an LO power of 0 dBm (Fig. 4.7(a)). The I/Q mixer must be operated at a minimum LO power of -7 dBm so as to saturate the limiting amplifiers and ensure low I/Q imbalance (<0.3 dB) over the 90-100 GHz range (Fig. 4.7(b)). The simulated NF versus IF frequency at 94 GHz is shown in Fig. 4.8 and the average NF is 27.6 dB over the op-amp bandwidth. The settling time for each BIST measurement point is determined by the op-amp bandwidth and is 140 ns assuming a 98% settling value [36].

### 4.2.4 BIST Dynamic Range

Fig. 4.9 presents the BIST power levels when testing a phased-array channel in the transmit and receive modes. In a receive mode test and for an oscillator power of 0 dBm, the injected power at the input of the channel is -42 dBm and -36 dBm under terminated and open-circuit conditions, respectively. This is lower than the channel input P_{1dB} of -30 dBm. The noise figure referred to plane B (see Fig. 4.9(a)) is ~24 dB and includes the channel gain (~24 dB) and noise figure (NF_{channel}≈10 dB), the loss of switches 6, 4, 2 (19 dB) and the average noise figure of the I/Q receiver (~28 dB). The resulting S/N ratio is therefore ~46 dB for 7 MHz bandwidth, and can be improved to ~56 dB if the integration time is set to 700 kHz using an external capacitor (settling time is 1.4 µs).
Figure 4.10: (a) Chip microphotograph of the fabricated T/R module with BIST and (b) detail of BIST I/Q receiver. Chip size is $2 \times 2$ mm$^2$.

Figure 4.11: Measured IQ imbalance of the BIST receiver.
Figure 4.12: Measured I and Q voltages of RX-H channel at 94 GHz versus 16 phase states.

The BIST performance for a channel with $S_{21}=0$ dB at 90-100 GHz, defined as the output IF voltage divided by the BIST input power, is shown in Fig. 4.9(b). In this case, the Rx-H channel is replaced by a lossless transmission line and the normalization value is at 94 GHz. It is seen that the normalized BIST response drops by 4.5 dB at 100 GHz due to the increased switch loss and I/Q receiver response versus frequency. This is used in Section 4.3 in order to obtain an accurate frequency response of the channel under test.

In a transmit test, a main concern is that the coupled output transmit power saturates the BIST I/Q receiver. However, the switches have 19 dB loss and the input P1dB of the I/Q receiver is 1.3 dBm at 0 dBm of LO power (~2.5 dBm at -10 dBm LO power). This allows for an output power as high as +20 dBm with no saturation in the BIST circuit. For this T/R module, the output power is ~0 dBm and therefore, the BIST operates deep in the linear region.

4.3 Measurements

Fig. 4.10 presents the T/R module with the BIST circuitry. The BIST transmission lines were implemented using the top layers for clarity, but can also be in lower metal layers at an expense of higher loss [43]. Also note that the BIST oscillator was not implemented on-chip for this demonstration, and was injected using an external GSG probe. In future design, a $\times 8$ multiplier chain can be used to result in a 90-100 GHz BIST signal using an 11-12.5 GHz on-chip or external oscillator.

A stand-alone I/Q receiver test cell was not available, and the I/Q mixer was tested by injecting an RF signal at the transmit/receive electronics port using a GSG probe and selecting SW 6, 4 and 2 to be activated. Both the RF and LO were tuned together to keep the IF fixed at 1 kHz. The measured amplitude and phase imbalance in the I/Q receiver is $<0.5$ dB and 4-5°.
Figure 4.13: Measured relative phase, phase error and gain error from the ideal phase state of RX-H channel at 94 GHz.
Figure 4.14: Measured relative phase, phase error and gain error from the ideal phase state of RX-V channel at 94 GHz.
Figure 4.15: Measured relative phase, phase error and gain error from the ideal phase state of TX-H channel at 94 GHz.
Figure 4.16: Measured relative phase, phase error and gain error from the ideal phase state of TX-V channel at 94 GHz.
Figure 4.17: Measured RMS phase and gain error of (a) RX-H, (b) RX-V, (c) TX-H channels.
Figure 4.18: Measured phase error and gain error from the ideal phase state of TX-V channel at 94 GHz with and without IQ error correction.

Figure 4.19: Measured gain control function of (a) RX-H and (b) TX-H channels at 94 GHz.
Figure 4.20: Measured normalized frequency response of all four channels with respect to RX-H channel at 94 GHz where SPDT routing loss and BIST I/Q receiver frequency response is (a) not deembedded and (b) deembedded.
respectively at 90-100 GHz (Fig. 4.11).

Fig. 4.13-4.16 present the measured phased-array channel at 94 GHz in the receive and transmit modes using standard GSG-based S-parameter and BIST measurement modes. The BIST values are obtained after a 2 μs settling time. Note the excellent agreement between the measured values obtained using BIST and S-parameter techniques at 94 GHz. Similar measurements were done at 90-100 GHz in 1 GHz steps for the Rx-V, Rx-H and Tx-H channels, and with good agreement with S-parameter values (Fig. 4.17). Note that the Tx-V channel has an identical response in terms of phase and amplitude as the Tx-H channel since they both pass by the same phase shifter and VGA (see Fig. 4.1).

The measured I and Q imbalance can be used to obtain even more accurate BIST values, but the phase and amplitude errors are so small that they have minimal impact at 94 GHz (Fig. 4.18). The BIST can also be used to measure the normalized VGA performance vs. gain state, both amplitude and phase, in the transmit and receive modes (Fig. 4.19).

Finally, the normalized frequency response can be obtained in both the transmit and receive modes using the BIST circuit. A single normalization point is used at 94 GHz for the Rx-H channel (Fig. 4.20(a)), and this takes into account the switch network loss and the I/Q receiver conversion gain. It is seen that this normalization point can also be simultaneously used for the Rx-V and the Tx-V (and Tx-H) channels and results in an accurate frequency response at 90-96 GHz. The discrepancy above 96 GHz is due to the roll off of the injected power (and sampled power) using Switches 5 and 6 and due to the I/Q receiver frequency response (see Fig. 4.9(b)). If the simulated BIST frequency response is normalized out of the measurements, the BIST values agree well with the measured S-parameter frequency response over the entire 90-100 GHz band (Fig. 4.20(b)).

4.4 Conclusion

This chapter presented the first built-in-self-test system which is suitable for T/R modules. Different than previous designs, the BIST injection is based on high-isolation switches enhanced by λ/4 transmission-lines and not on passive couplers. The T/R module was successfully measured in the Rx and Tx modes and with excellent agreement with S-parameter values. The technique is demonstrated on a single element, but can be expanded to multi-elements silicon phased-array chips. The high-isolation injection switch can also be implemented using lumped-element components (for the λ/4 lines) to result in a more compact approach.
4.5 Acknowledgement

This work was supported by the DARPA 11-50 Program under a subcontract from Teledyne Scientific, Bruce Wallace and Alfred Hung, contract monitors. The authors would like to thank Dr. Mehmet Uzunkol, University of California, San Diego for helpful technical discussions.

Chapter 4 is mostly a reprint of the material as it is submitted for publishing to IEEE Microwave Theory and Techniques, 2013. Ozgur Inac; Fatih Golcuk; Tumay Kanar; Gabriel M. Rebeiz. The dissertation author was the primary author of this material.
Chapter 5

45 nm CMOS SOI Technology Characterization for Millimeter-Wave Applications

5.1 Introduction

The IBM 45nm CMOS SOI technology has been extensively used in the development of millimeter-wave low-noise amplifiers, multipliers, switches, RF and wireline transceivers, and power amplifiers [57–73]. It offers CMOS transistors with very high $f_t$ and $f_{max}$ (> 400 GHz) placed in an SOI technology, which isolates the transistor from the silicon substrate and allows for stacking so as to improve the circuit power handling and large signal swings. This has lead to the development of several complex chips using this technology with operation up to 170 GHz range [62, 68, 74–77].

This paper presents a systematic study of the IBM 45nm SOI technology, and presents the effect of finger width, total transistor width, single and double-gate contacts on regular and relaxed-pitch transistors. The transistors are measured up to 110 GHz, and $f_t$ and $f_{max}$ are obtained for 19 transistors with different characteristics. The paper does not study $NF_{min}$ for the different transistors and concentrates on S-parameter characterization, and clear trends are seen based on the transistor selection. It is seen that IBM model, together with RC extraction, accurately predicts the transistor performance up to the top metal layers, which greatly simplifies the circuit design (no EM simulations are used). Also, passive components such as transmission-lines, capacitors and inductors are characterized up to 110 GHz and compared with simulations.
obtained using the IBM models for the device coupled with electromagnetic models for the interconnect stack. Several low-noise amplifiers are presented, each with record performance, from 20 to 94 GHz, using this technology.

### 5.2 Technology

The IBM 45 nm CMOS SOI process [78] offers partially depleted floating-body NFET and PFET devices with 40 nm drawn gate length. The transistors are built in a 225 nm thick buried oxide layer which isolates the active device layers from the 13.5 Ω·cm resistivity substrate (Fig. 5.1). Various back-end metallization options are available and Fig. 5.1 presents the metal stack-up used in this work. The employed back-end option consists of 11 metal layers, which are all copper except for the top aluminum layer. The vias are tungsten and with a resistance of 3.5 Ω/via for M1-M2, M2-M3, M3-C1, 2.0 Ω/via for C1-C2, 1.5 Ω/via for C2-B1, B1-B2, B2-B3, 0.3 Ω/via for B3-UA, 0.1 Ω/via for UA-UB, and 0.02 Ω/via for UB-LB.

The technology also offers different gate poly pitches at 190 nm and 380 nm (referred as regular and relaxed pitch, respectively). The relaxed poly pitch transistors benefit from reduced parasitic capacitance due to wider separation between gate and source/drain contacts and enhanced stress response (higher $g_m$). IBM reported a measured peak $f_t$ of a regular and re-
laxed pitch 30×1 μm transistors as 406 and 485 GHz, respectively [57] including close-in metal routing (M1 level only). This demonstrates the intrinsic high performance capabilities of these transistors even at millimeter-wave frequencies.

5.3 Characterization

Several transistor and passive test cells have been fabricated and characterized from 1 GHz to 110 GHz. Measurements are performed in two different setups: A coaxial measurement setup is used up to 70 GHz, and a WR-10 waveguide setup is used for 70–110 GHz measurements.

5.3.1 Transistors

As mentioned in Section II, the intrinsic relaxed-pitch transistor has a peak $f_t$ of 485 GHz, including close-in metal routing parasitics at M1. However, interconnects up to the top metal layer have a significant effect on the transistor performance at millimeter-wave frequencies. Therefore, a Thru-Reflect-Line (TRL) calibration method is preferred which places the measurement reference planes in close proximity of the device under test (DUT), at the top metal layer as shown in Fig. 5.2. Microstrip transmission-lines are used to connect the device gate and drain to the GSG pads, and the source is grounded to M1, M2, M3, C1, C2 using a perforated two-dimensional ground plane so as to meet the metal-density rules. This ground plane is also used for the microstrip transmission-line.

In order to study the effects of the finger width, total transistor width, gate contacts and poly pitch at millimeter-wave frequencies, a total of 19 transistor test cells have been fabricated. The transistors are grouped into four categories, depending on their total transistor width and gate poly pitch: Regular pitch 30 μm (4 transistors), regular pitch 20 μm (5 transistors), regular pitch 14 μm (4 transistors) and relaxed pitch transistors (6 transistors). Technology library pcells are used in the test cells, but due to the discrete finger widths, the total transistor widths are not identical for the transistors in the same group. However, the transistor width variation in any group is less than ±2.6%, so they can still be grouped together.

All transistors are measured at a $V_{ds}$ = 1 V, and the $V_{gs}$ is swept from 0 V to 0.9 V. For a fair comparison, all measurements are presented versus current density.

Fig. 5.3 presents the measured $H_{21}$, Mason’s unilateral gain (U), maximum stable gain (MSG) and maximum available gain (MAG) of the 30×1007 nm single-gate contact regular pitch
Figure 5.2: Chip micrograph of the transistor test cell, 3D view of the transistor interconnect, detailed view of the transistor contacts, and the top view of the ground plane.
transistor at bias conditions of $V_{gs} = 0.55$ V, $V_{ds} = 1$ V and a current density ($J_{dc}$) of 0.31 mA/µm. The $H_{21}$ and $U$ extrapolations result in an $f_t$ and $f_{max}$ of 227 GHz and 213 GHz, respectively. Since the transistor is potentially unstable up to 110 GHz ($k$-factor < 1), the MSG and MAG are identical, and the transistor has an MSG (MAG) of 20.0, 10.3 and 8.9 dB at 6, 60 and 90 GHz, respectively.

A significant concern for millimeter-wave design is the model accuracy both at the device and interconnect levels. A BSIM4 model is used for the intrinsic transistor, and the interconnects are modeled with parasitic RC extraction up to the top metal layer using Calibre [79], and both are combined together to result in the model shown in Fig. 5.4. In order to validate the IBM models, the transistor parameters are calculated according to the equations given in [80], and the measured and simulated values are compared for the $30 \times 1007$ nm single-gate contact regular-pitch transistor (Fig. 5.5). The measurements, except for the $r_{ds}$, agree decently well with simulations up to 75 GHz. The discrepancy above 75 GHz is due to the interconnect inductance, which was not modeled in the RC extraction. A similar analysis is performed for the $30 \times 1007$ nm single-gate contact relaxed pitch transistor (Fig. 5.6), and the agreement between measurements and simulation follows the same trend as the regular pitch transistors. Note that the measured $g_m$ of the relaxed-pitch transistor is higher than the regular-pitch transistor due to the enhanced stress response in silicon [57]. Still, the relaxed-pitch transistors occupy 2× more area than the regular pitch transistors, and may not be suitable for highly dense mixed-signal circuits.

The same set of measurements are performed on all other transistors, but for brevity only $f_t$ and $f_{max}$ values will be presented as the figure of merits. Fig. 5.7(a) presents the measured $f_t$ values of all 30 µm regular pitch transistors versus current density. Single-gate contact $30 \times 1007$ nm and $38 \times 779$ nm transistors perform the best in terms of $f_t$ with peak values of 237 and 236 GHz, respectively, at a current density of 0.5 mA/µm. The peak $f_t$ slightly drops to 226 GHz for the single-gate contact $58 \times 513$ nm transistor. The double-gate contact $30 \times 1007$ nm transistor suffers from increased parasitic capacitance and results in an $f_t$ of 203 GHz, which is lower than the same device with a single-gate contact.

The measured $f_{max}$ of all 30 µm transistors are presented in Fig. 5.7(b). In this case, the single-gate contact $58 \times 513$ nm and double-gate contact $30 \times 1007$ nm transistors show the peak $f_{max}$ values of 283 and 278 GHz, respectively. Both of these transistors benefit from reduced gate resistance: the single-gate contact $58 \times 513$ nm due to a short finger width, and the double-gate contact $30 \times 1007$ nm due to the case of double contacts. Single gate contact
Figure 5.3: Measured $H_{21}$, $U$, and MSG and MAG of the $30 \times 1007$ nm single gate contact transistor.

Figure 5.4: Small signal model of the MOS transistor.
Figure 5.5: Measured and simulated transistor parameters of the 30×1007 nm single-gate contact regular pitch transistor.
Figure 5.6: Measured and simulated transistor parameters of the 30×1007 nm single-gate contact relaxed pitch transistor.
30×1007 nm and 38×779 nm transistors have lower peak $f_{\text{max}}$ values of 214 and 221 GHz, respectively, due to the increased gate resistance.

The measured transistor $f_t$ and $f_{\text{max}}$ values agree with expectations: Reducing finger width or using double-gate contacts increases the $f_{\text{max}}$ values by reducing the gate resistance, but at the expense of increased parasitic capacitance and a decrease in $f_t$. The measured $f_t$ and $f_{\text{max}}$ also agree decently well with simulations, with the measurements being about $\sim 5\%$ higher than the simulated values. This may be due to the peaking effect of interconnect inductance which is not included in the simulations.

The measured peak $f_t$ and $f_{\text{max}}$ of 20 $\mu$m and 14 $\mu$m regular pitch transistors also show a similar trend as the 30 $\mu$m transistors. A peak $f_t$ of 235 GHz is achieved for the 20 $\mu$m single-gate contact 20×1007 nm transistor (Fig. 5.8(a)). The double-gate contact 20×1007 nm transistor shows the highest $f_{\text{max}}$ of 255 GHz within the 20 $\mu$m transistors (Fig. 5.8(b)). The highest $f_t$ among 14 $\mu$m transistors is achieved using a single-gate contact 14×1007 nm transistor (Fig. 5.9(a)), whereas the double-gate contact 14×1007 nm transistor achieves the highest $f_{\text{max}}$ value of 218 GHz (Fig. 5.9(b)).

The measured $f_t$ and $f_{\text{max}}$ of relaxed-pitch transistors are presented in Fig. 5.10(a)- (b). Similar to regular-pitch transistors, single-gate contact transistors with longer finger widths show higher $f_t$ values as compared to double-gate contact transistors. The peak $f_t$ of a relaxed pitch transistor is 260 GHz for a 30×1007 nm single-gate contact transistor (Fig. 5.10(a)). The single-gate contact 30×1007 nm and double-gate contact 20×1007 nm transistors show the highest $f_{\text{max}}$ values of 260 and 259 GHz, respectively (Fig. 5.10(b)).

Fig. 5.11 summarizes the measured peak $f_t$ and $f_{\text{max}}$ of the regular pitch transistors (13 in total) versus total transistor width. The 30×1007 nm single-gate contact transistor shows the highest $f_t$ of 237 GHz among regular pitch transistors (Fig. 5.11(a)), whereas a maximum $f_{\text{max}}$ of 283 GHz is achieved for the 58×513 nm single-gate contact transistor (Fig. 5.11(b)). For the same total transistor width, using smaller finger widths or double-gate contacts reduces the $f_t$ due to increased parasitic capacitance but helps to increase the $f_{\text{max}}$ by reducing the input resistance. An important observation is the increased performance with larger total transistor widths, independent of the finger width or gate contact type. Since the transistors are not very large, interconnect parasitics are almost constant especially for the higher metal layers (B1, B2, B3, UA, UB, LB). This results in larger parasitics per unit length for smaller transistor sizes which reduces their high-frequency performance.

A summary of the relaxed-pitch transistors is presented in Fig. 5.12 versus total tran-
Figure 5.7: Measured $f_t$ and $f_{max}$ of 30 µm transistors with different gate finger widths.
Figure 5.8: Measured $f_t$ and $f_{max}$ of 20 $\mu$m transistors with different gate finger widths.
Figure 5.9: Measured $f_t$ and $f_{max}$ of 14 $\mu$m transistors with different gate finger widths.
Figure 5.10: Measured $f_t$ and $f_{\text{max}}$ of relaxed pitch transistors.
Figure 5.11: Measured peak $f_t$ and $f_{max}$ of regular pitch transistors versus total transistor width.
Figure 5.12: Measured peak $f_t$ and $f_{max}$ of relaxed pitch transistors versus total transistor width.
sistor width. Peak $f_t$ of 264 GHz (Fig. 5.12(a)) and $f_{max}$ of 260 GHz (Fig. 5.12(b)) are achieved for the $30 \times 1007$ nm single-gate contact transistor among relaxed pitch transistors. The effect of the total transistor width, finger width and gate contact type on relaxed pitch transistors are the same as regular pitch transistors.

A comparison of the single-gate contact relaxed and regular-pitch transistors for the same total transistor and finger width reveals a performance increase of 6–23% in $f_t$ and 11–30% in $f_{max}$ both in favor of relaxed-pitch transistors. However, for the double-gate contact transistors, the performance increase is virtually negligible (3.4% and 1.5% for $f_t$ and $f_{max}$, respectively). This is probably due to the increase in the parasitic routing capacitance which dominate the overall device capacitance and diminishes the benefits of using a relaxed-pitch transistor.

### 5.3.2 Passive Components

The performance and modeling of the passive components have significant importance at millimeter-wave frequencies. For this purpose, test cells composed of transmission-lines, capacitors and inductors have been fabricated and characterized up to 110 GHz.

A microstrip transmission line is preferred due to its lower loss compared to coplanar-waveguide (CPW) transmission lines at millimeter-waves. A 50 Ω line is built using a 12-μm top metal layer (LB) for the signal line and the bottom five metal layers (M1-C2) are stacked for the ground plane (Fig. 5.1(a)). The ground metal planes are meshed, in compliance with the metal density requirements. A blocking layer is used which completely prevents the dummy filling on the top metal layer and reduces the metal-fill percentage for the lower metal layers. Two transmission lines with 110 and 710 μm length, are measured with Short-Open-Load-Thru (SOLT) probe tip calibration, and the de-embedding method presented in [81] is used to remove the pad effects. The measured characteristic impedance, $Z_0$, and the relative permittivity, $\epsilon_r$, of the transmission line agree well with the simulated values (Fig. 5.13). The measured attenuation agrees very well with simulations up to 50 GHz. The discrepancy above 50 GHz is probably due to the calibration and measurement errors which can have a significant effect when comparing two short transmission lines.

IBM12SOI technology does not provide Metal-Insulator-Metal (MIM) capacitors but offers a vertical natural capacitor (vncap) with the already available back-end metal layers. The capacitors are realized using metal fingers in a dense and stacked fashion with user-defined first and last layer in the stack (only the bottom 8 metal layers can be used). Two capacitor test-
Figure 5.13: Measured characteristic impedance ($Z_o$), relative permittivity ($\varepsilon_r$) and loss of the microstrip transmission line.
Figure 5.14: Chip microphotographs of (a) 2-port 28 fF capacitor, (b) 1-port 260 fF capacitor and (c) 2-port 180 pH inductor. (d) 3-D layout and the cross-section of the 2-port 28 fF capacitor.
Figure 5.15: Measured and simulated capacitance of (a) 2-port 28 fF and (b) 1-port 260 fF capacitor.

Figure 5.16: Measured and simulated inductance of the 2-port 180 pH inductor.
cells have been fabricated, a 28 fF series and a 260 fF shunt capacitor (Fig. 5.14(a)-(b)). Both capacitors are realized between C1 to B3 metal layers, and the interconnects up to the top metal layer is modeled in Sonnet [55]. A 3-D view of the 28 fF capacitor including interconnects up to top metal layer is shown in Fig. 5.14(d). Physical dimensions of the 28-fF and 260-fF capacitors are $6 \times 6 \, \mu m^2$ and $15 \times 14.8 \, \mu m^2$, respectively. The capacitance density can be increased by adding lower metal layers (M1 to M3) to the stack at the expense of higher shunt parasitic capacitance to the substrate.

Measurements of the 28-fF series and 260-fF shunt capacitors agree well with simulations up to 110 GHz (Fig. 5.15). The intrinsic and interconnect inductance slightly increases the effective capacitance value at $> 60$ GHz, and this effect is captured in simulations and measurements.

A 180 fF spiral inductor test cell is also fabricated (Fig. 5.14(c)). The inductor is realized on the top metal layer with a 4 $\mu m$ trace width and is simulated in Sonnet. Measured and simulated inductance is calculated using both $Y_{21}$ and $Y_{11}$ (Fig. 5.16). In both cases, measurements agree well with the simulated values. Due to the two port test-cell, the inductor Q value could not be determined.

### 5.4 Low-Noise Amplifiers

In order to demonstrate the performance of the 45 nm CMOS SOI technology, several LNAs have been implemented at Q-, V- and W-Band (Fig. 5.17)

#### 5.4.1 Q-Band LNA

The Q-Band LNA is shown in Fig. 5.18(a). A 2-stage cascode amplifier topology is chosen due to its high gain and reverse isolation, and hence improved stability. Double gate contact 40$\times$1007 nm transistors are chosen to result in low power consumption as well as realizable inductor values, and all transistors are biased at the minimum noise figure current density (0.2 mA/$\mu m$).

Spiral inductors with a Q of 12 – 14 are used at the drain and gate nodes of the transistors whereas transmission-line stubs (Q of $\sim 12$) are used as emitter degeneration inductors due to required low inductance values. A 350 $\Omega$ resistor is placed at the second stage drain to increase the output impedance matching bandwidth at the expense of gain. Interdigitated vertical finger capacitors from IBM design kit are used in the matching networks and MOS capacitors
**Figure 5.17**: Chip microphotograph of the (a) Q-Band (b) V-Band and (c) W-Band LNA.
$V_{dd} = 1.3 \text{ V}$

(a) Q-Band

(b) V-Band

(c) W-Band

Figure 5.18: Schematic of the (a) Q-Band (b) V-Band and (c) W-Band LNA.
are used for supply decoupling. 10 Ω resistors are placed in series with the load inductors at the Vdd nodes in order to isolate the stages and provide wideband stability. Due to the decoupling capacitors, this has minimal effect on the in-band RF operation of the LNA except for an 80 mV DC voltage drop. The on-chip bypass network employs different resistor (5 – 20 Ω) and capacitor (0.3 – 2 pF) values to result in a wideband, low-Q and low impedance path from Vdd to ground.

Small signal measurements of the Q-Band LNA are performed after an SOLT calibration to the probe tips. The measured and simulated S-Parameters are presented in Fig. 5.19(a). The peak gain is 15 dB at 45 GHz with a 3-dB bandwidth of 39.7 – 53.4 GHz for three different samples. Input and output return loss is < -10 dB at 41.1 – 58.8 GHz and 41.3 – 54.5 GHz, respectively. The measured $S_{12}$ is < -40 dB (not shown) over the whole measurement band. The LNA consumes 20.8 mW from a 1.3 V supply.

The measured LNA noise figure is 3.3 dB at 45 GHz with nominal biasing of 0.2 mA/µm as shown in Fig. 5.19(b) and it is < 3.4 dB for a wide range of bias current. Large signal measurements of the LNA result in an output $P_{1dB}$ of 1.5 dBm at 45 GHz and an IIP3 value of -5.3 dBm at 45 GHz (not shown).

5.4.2 V-Band LNA

The V-Band LNA is designed using the same methodology (Fig. 5.18(b)). The transistor width is reduced to 30 µm for less parasitic capacitance, and the load inductors are realized using transmission-lines.

Fig. 5.20(a) presents the measured and simulated S-parameters of the V-Band LNA. Peak gain is 12.5 dB at 66 GHz with a 3-dB bandwidth of 60–73 GHz. $S_{11}$ and $S_{22}$ is < -10 dB at 57.8–80 GHz and 60.2–72.4 GHz, respectively. The LNA consumes 15 mW from a 1.3 V supply. LNA has a minimum NF of 4.0 dB at 65 GHz, and the NF remains < 4.4 dB for a wide range of bias current density (Fig. 5.20(b)). The measured output $P_{1dB}$ is -2 dBm at 65 GHz (not shown).

5.4.3 W-Band LNA

The W-Band LNA uses a 3-stage common source topology (Fig. 5.18(c)). All load inductors are realized as transmission line stubs except for the spiral inductor used at the input. Double-gate contact 20×1007 nm transistors are used at all three stages, and all transistors are biased at minimum noise figure current density.
Figure 5.19: Measured (a) S-parameters and (b) noise figure of the Q-Band LNA.
Figure 5.20: Measured (a) S-parameters and (b) noise figure of the V-Band LNA.
Figure 5.21: Measured (a) S-parameters and (b) noise figure of the W-Band LNA.
Table 5.1: LNA Performance Summary

<table>
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<th>K-Band [82]</th>
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<th>V-Band</th>
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<tr>
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<td>5.2</td>
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<td>15</td>
<td>13.5</td>
<td>52</td>
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Measured and simulated S-parameters of the W-Band LNA are presented in Fig. 5.21(a). The LNA achieves a peak gain of 13.5 dB at 83 GHz with 3-dB bandwidth of 76 GHz to 88 GHz, and it consumes 13.5 mW from a 1 V supply. $S_{11}$ and $S_{22}$ is $<-9$ dB at 82.4–92.7 GHz and 78–105 GHz, respectively (This was actually the first design and we feel that the layout and EM simulations were not accurately done, therefore resulting in a $\%10$ frequency shift). The noise figure of the W-Band LNA is characterized at 75–90 GHz and a minimum NF of 5.7 dB is achieved at 85 GHz. Similar to the Q- and V-Band LNAs, the W-Band design maintains a low NF for a wide range of bias current density (Fig. 5.21(b)). The W-Band LNA delivers an output $P_{1dB}$ of -1.5 dBm at 85 GHz (not shown).

The Q-, V- and W-Band LNAs have been characterized versus temperature from $25^\circ$C up to $95^\circ$C (Fig. 5.23). The measured peak gain of the LNAs drop by 1.1, 1.4 and 1.6 dB for Q-, V- and W-Band LNA, respectively. Measurements agree reasonably well with simulations which are normalized to the $25^\circ$C values so as to compare the gain drop, and the difference could be attributed to the resistance increase in the Ti/Cu back-end versus temperature since this is not taken into account in the Sonnet simulations.

The measured noise figure of the LNAs together with three published LNAs in the same technology [58,82,83] is presented in Fig. 5.22. All five LNAs achieve state-of-the-art NF values at their respective frequency bands. Performance summary of all five LNAs are presented in Table 5.1.
Figure 5.22: Measured noise figure of several LNAs in the 45nm CMOS SOI technology

Figure 5.23: Measured (solid) and simulated (dashed) gain of the Q-, V- and W-Band LNAs versus temperature
5.5 Conclusion

This paper presented an extensive study of the IBM 45nm SOI technology for millimeter-wave applications. It is seen that the best $f_t$ of 264 GHz is obtained for the $30 \times 1007$ nm single-gate contact relaxed-pitch transistor (lowest $C_{gs}$ and with a high $g_m$) and the best $f_{max}$ of 283 GHz is obtained for the $58 \times 513$ nm single-gate contact regular-pitch transistor (lowest $r_g$ with acceptable capacitance). Also, relaxed-pitch transistors result in better performance than standard pitch transistors, at the expense of space. The measured transistor performance agree well with simulations obtained using the IBM transistor model and RC extraction to the top metal layer, which greatly simplifies circuit design. Passive components are also well predicted using the IBM model and Sonnet models of the interconnects up to the top metal layer. This technology can be used for low noise amplifiers, among other circuits, and results in record noise figure from 20 GHz to 94 GHz.

5.6 Acknowledgement

Chapter 5 is mostly a reprint of the material as it is submitted for publishing to IEEE Microwave Theory and Techniques, 2013. Ozgur Inac; Mehmet Uzunkol; Gabriel M. Rebeiz. The dissertation author was the primary author of this material.
Chapter 6

Conclusion

The thesis presented built-in self-test (BIST) circuits for phased array applications from X- to W-Band, and the characterization of a 45 nm CMOS SOI technology for millimeter-wave applications. The first on-chip BIST for phased-array RFICs is presented in Chapter 2. The effect of BIST coupler on the phased-array performance is presented in detail and it is shown that, for non-directional couplers, it is important to have a low coupling value at the input of the chip. The BIST measurements agree very well with S-parameter measurements. It is expected that the BIST technique will be used in millimeter-wave phased arrays and will greatly reduce the RFIC testing costs.

Chapter 3 presented a 16-element phased array receiver with built-in self-test capabilities. It is shown that the BIST can be used to accurately measure many key parameters of the phased-array chip (gain and phase variation versus phase state, gain, control, etc.), including the relative gain versus frequency of the entire receiver. This phased array chip has been packaged with 16 antennas and resulted in pattern scanning up to ±50° with -17 dB sidelobes.

The first built-in-self-test system which is suitable for T/R modules was presented in chapter 4. Different than previous designs, the BIST injection is based on high-isolation switches enhanced by λ/4 transmission-lines and not on passive couplers. The T/R module was successfully measured in the Rx and Tx modes and with excellent agreement with S-parameter values. The technique is demonstrated on a single element, but can be expanded to multi-elements silicon phased-array chips. The high-isolation injection switch can also be implemented using lumped-element components (for the λ/4 lines) to result in a more compact approach.

Chapter 5 presented an extensive study of the IBM 45nm SOI technology for millimeter-wave applications. It is seen that the best $f_t$ of 264 GHz is obtained for the $30 \times 1007$ nm single-
gate contact relaxed-pitch transistor (lowest $C_{gs}$ and with a high $g_m$) and the best $f_{max}$ of 283 GHz is obtained for the 58×513 nm single-gate contact regular-pitch transistor (lowest $r_g$ with acceptable capacitance). Also, relaxed-pitch transistors result in better performance than standard pitch transistors, at the expense of space. The measured transistor performance agree well with simulations obtained using the IBM transistor model and RC extraction to the top metal layer, which greatly simplifies circuit design. Passive components are also well predicted using the IBM model and Sonnet models of the interconnects up to the top metal layer. This technology can be used for low noise amplifiers, among other circuits, and results in record noise figure from 20 GHz to 94 GHz.

6.1 Future Work

In Chapters 2, 3 and 4, BIST systems have been demonstrated for Rx, Tx and T/R systems. In these implementations, relative phase and amplitude response of channel versus phase and gain state and normalized frequency response have been characterized with BIST. As a future work BIST system can be improved for absolute gain measurements.

Fig. 6.1 presents a technique for on-chip gain measurements. In this method, identical directional couplers are used at the input and output of the channels. The directional coupler is followed by a power splitter, to route the sampled output signal to on-chip BIST I/Q receiver. If the coupling from the RF line to the detector input is $c$ and the detector responsivity is $R$, then the gain of channel-n, $G_n$, can be calculated by comparing output voltages of detectors:

$$G_n = \frac{P_{out}}{P_{in}}$$
$$V_n = P_{in} \times c \times R$$
$$V_{out} = P_{out} \times c \times R$$
$$\frac{V_{out}}{V_n} = \frac{P_{out} \times c \times R}{P_{in} \times c \times R} = \frac{P_{out}}{P_{in}} = G_n.$$

Furthermore, if the coupling coefficient, $c$, and the detector responsivity, $R$, are characterized with additional test cells, it is possible to measure the input and output $P_{1dB}$ compression point of the channel as well. However, this additional BIST functionality will increase the area of the additional BIST circuits and extreme attention should be paid in layout.
Figure 6.1: Proposed BIST idea for absolute gain measurements.
Bibliography


