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Solution-Processed Carbon Nanotube and Chemically Synthesized Graphene Nanoribbon Field Effect Transistors.

By

Patrick Bryce Bennett

A dissertation submitted in partial satisfaction of the requirements for the degree of Doctor of Philosophy in Applied Science & Technology and the Designated Emphasis in Nanoscale Science and Engineering in the Graduate Division of the University of California, Berkeley

Committee in charge:

Jeffrey Bokor, Chair
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Michael Crommie

Fall 2014
Solution-Processed Carbon Nanotube and Chemically Synthesized Graphene Nanoribbon Field Effect Transistors.

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by

Patrick Bryce Bennett
Abstract

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Doctor of Philosophy in Applied Science & Technology
Designated Emphasis in Nanoscale Science and Engineering

University of California, Berkeley

Professor Jeffrey Bokor, Chair

Carbon nanotubes (CNTs) possess great potential as high performance semiconducting channels due to their one-dimensional nature, extremely high mobility, and their demonstrated ability to transport electrons ballistically in transistors. However, the presence of metallic CNTs in CNT films and arrays represents a major impediment towards large-scale integration. Methods of solution purification have demonstrated partial success in metallic CNT removal, although their effects on device performance are unknown. While this problem may be solvable, new synthesis techniques have recently resulted in the creation of high-density films of graphene nanoribbons (GNRs) with atomically smooth edges, uniform widths, and uniform band structure. These may ultimately supplant CNTs in device applications due to their theoretically similar, but uniform electronic properties.

This work aims to study the effects of purification of semiconducting CNTs in thin film transistors (TFTs) and to develop methods to increase device performance when metallic CNTs are present. Devices consisting of large networks of CNTs as well as short channel, single CNT devices are characterized to determine the effects of solution processing on CNTs themselves. Short channel, bottom-up GNR devices are fabricated to compare their performance to CNT transistors.
The first half of this dissertation describes the methods of integrating CNTs from various sources into transistors. Growth and transfer are described, as well as methods of creating aqueous suspensions for solution processing. Development of novel surfactant materials based on biomimetic polymers used to suspend CNTs in solution are reported and characterized. Methods of deposition out of solution and onto insulating substrates are covered. Device fabrication from start to finish is detailed, with the subtleties of processing required to produce sub 10-nm channel length devices explained.

The second half reports devices produced via these techniques in order to study the performance of solution-processed CNT devices. TFT performance is limited by metallic CNTs that can short channels, but can be improved by structuring the CNT film, either through patterning or induced alignment. Increasing semiconducting CNT purity does not necessarily increase device performance because of the decreased lengths of the purified CNTs. Extremely high purity semiconducting CNT solutions, however, are not subject to these same limitations, with transistors exhibiting improved mobilities while also scaling to sub-\(\mu\)m channel lengths. Short channel devices down to 15 nm are then presented, demonstrating ballistic transport in solution-processed CNTs, despite their inferior electronic performance at \(\mu\)m-scale lengths. Finally, short channel devices utilizing chemically synthesized GNRs as channels are presented and characterized to directly probe the mechanisms of electron transport in these materials for the first time.
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Chapter 1

Introduction

As transistors continue to decrease in size, physical effects, previously of little concern to silicon devices, become proportionately greater and limit device performance. Within the last decade, multiple technologies beyond feature scaling alone have been employed to extend the use of silicon in ever-smaller devices, including the introduction of strained silicon to increase carrier mobility\(^1\), high-k dielectrics to keep leakage in check\(^2\), and, most recently, the introduction of tri-gate geometries to maintain electrostatic control of the channel\(^3,4\). These advances have allowed silicon-based transistors to continue to scale to increasingly small physical dimensions; however, further scaling may require the replacement of silicon with higher performance semiconducting materials. Nanoscale materials enable higher performance and better channel control in short channel transistors. The most promising of these materials has been the carbon nanotube (CNT).

Because production of CNTs is different than silicon, and because they operate in qualitatively different ways, new applications, such as high performance electronics integrated into flexible and transparent substrates\(^5-8\), are now possible. Furthermore, their unique structure enables new types of devices\(^9\) and lower-cost processing techniques\(^10,11\) to produce high-quality semiconducting films.

CNTs and graphene are allotropes of carbon that share the hexagonal crystal structure of graphite, but due to their confinement in one or more dimensions, possess physical properties unique in nature. Graphene exists as a two-dimensional sheet of carbon atoms, while carbon nanotubes are cylinders with translational periodicity of the lattice. Both exist only as a surface, with no bulk atoms, and as such behave completely differently from traditional materials.

Observations of cylindrical nanostructures composed of carbon can be traced as far back as 1952\(^12\). It was not until 1991, however, with the characterization of ‘helical microtubules of graphitic carbon’\(^13\) and subsequent theoretical studies predicting their unique nanoscale properties\(^14\), that CNTs became an active area of research. Since then, scientists have extensively studied their unique physical\(^15\), electronic\(^16-22\), optical\(^23-25\), and mechanical properties\(^26\). This explosion of interest has also resulted in the development of multiple growth processes\(^27,28\) and purification techniques\(^11,29-31\).
Electronic structure of graphene and CNTs

In graphene, a single layer of graphite (figure 1a), carbon atoms are arranged in a hexagonal honeycomb lattice. This results in hybridized $sp^2$ molecular orbitals of the carbon atoms. The two in-plane $p_x$ and $p_y$ atomic orbitals form $\sigma$ bonds, leaving the third $p_z$ orbital un-hybridized and perpendicular to the basal plane. These $p_z$ orbitals overlap with each other to form delocalized $\pi$ bonding and anti-bonding energy bands, presented in figure 1b, which are the origin of graphene’s exemplary electronic properties. At the corners of the Brillouin zone the energy bands converge. This results in a zero energy gap at the Fermi level, referred to as the Dirac point, around which the energy momentum dispersion relation is linear.

This linearity gives rise to electrons that behave as massless, relativistic particles\textsuperscript{33}. In high quality, defect free graphene crystals, carrier mobilities greater than $10^6 \text{ cm}^2/\text{Vs}$ are regularly observed experimentally in graphene transistors\textsuperscript{34}, 1000 times greater than standard silicon. This means electrons and holes travel over $\mu$m before scattering, compared to only 10s of nm in silicon. However, because graphene does not have a band-gap, conductivity cannot be turned on or off.

Carbon nanotubes (CNTs) are graphene cylinders that exert a quantization condition upon the two-dimensional lattice. A graphene sheet, presented in figure 2a, is overlaid with a chiral vector, labeled $C_H$, which represents the circumference of a CNT. In this case, it has a chirality of $(m,n)=(5,5)$, where $m$ and $n$ refer to the number of primitive lattice vectors between the two equivalent points, $A$ and $B$, on the circumference of the CNT. This cylindrical structure imposes a periodic boundary condition on the electron wave-function and sections the allowable states of the graphene band structure into one-dimensional energy sub-bands, as shown in figures 2b and 2c.
Figure 2: CNT band structures. (a) The graphite lattice overlaid with a chiral vector, $C_H$, defining a (5,5) ‘armchair’ (referring the edge structure perpendicular to $C_H$) CNT. (b) resultant 1D quantization and band structure for the (5,5) CNT. (c) The quantization and band structure for a (5,0) ‘zigzag’ CNT. Band structures are calculated following tight binding methods presented in reference 32.

In this work, all discussions of CNTs implicitly refer to single-walled CNTs, which are a single cylindrical graphene layer. However, the existence of CNTs with multiple stacked graphitic layers, known as multi-walled CNTs, should be mentioned briefly. The production methods of these CNTs are somewhat different from single-walled CNTs and their uses tend toward mechanical and macroscopic applications, where crystal defects in individual CNTs are less important. Multi-walled CNTs have also proven to possess impressive mechanical and electrical properties, and were the first to be integrated into commercial applications due to their relative ease of production and integration.

CNT band structure can vary greatly with chirality. As shown in figure 2b and 2c, a (5,5) CNT possesses a band-gap, whereas a (5,0) CNT does not. For chiralities where mod3(m-n)=0, the CNT energy bands intersect the Dirac points of the graphene reciprocal lattice and are metallic, i.e. does not possess a band-gap. Statistically, one third of all CNTs are metallic, but in practice synthesis techniques can be tuned to preferentially grow semiconducting chiralities 35-39. In applications where a semiconducting material is needed, elimination of metallic CNTs is critical to producing high yield of functioning devices.

Because of the symmetry in the graphene $\pi$ bands, semiconducting CNTs have a direct band-gaps with energy bands symmetric about the Fermi level, resulting in symmetric electron and hole transport properties. Roughly, the diameter of the CNT determines the strength of electron confinement, the band-gap, and effective carrier mass, with smaller band-gaps and effective masses for larger diameter CNTs. The chirality of the CNT is
also important in determining the specifics of the band structure, however, with CNT chiralities falling into families sharing similar diameter scaling trends for equal \((n-m)\). 

Graphene nanoribbons (GNRs) also may possess energy band-gaps due to lateral physical confinement\(^40,41\). For narrow GNRs, the confinement can be similar in strength to CNTs. The specific band structure is dependent on the edge properties of the GNR; GNRs with armchair edge construction are semiconducting\(^41\) while GNRs with zigzag edges are predicted to possess small band-gaps as well interesting spintronic behavior\(^42\). Spin-dependent transport behavior in zigzag GNRs has yet to be demonstrated because it is difficult to produce GNRs with perfect edge structure. Top down approaches, such as lithographic patterning, produce ribbons with rough edges that degrade transport quality and are too wide to induce significant quantum confinement\(^43,44\). Bottom-up methods, such as the unzipping of CNTs, produce smoother edged GNRs possessing both armchair and zig-zag edges\(^45,46\). These GNRs demonstrate much improved transport properties over top-down GNRs. The nature of their production is unreliable, however, and results in wide variation of GNR width, edge structure, and electronic behavior.

**CNTs as one-dimensional field effect transistors**

Because of their exemplary electronic properties\(^16\), CNTs are of great interest as semiconducting channels in high performance transistors\(^47\), potentially replacing silicon in future commercial applications\(^48\). Figure 3a presents a diagram of a CNT based transistor. A CNT is deposited upon an insulated substrate and contacted directly by two electrodes, the source and drain. A third electrode is placed on top of the CNT, but is insulated with a dielectric layer. This allows the gate to modulate the electric potential in the CNT channel region, while also remaining electrically isolated.

When a voltage bias is applied between the source and drain, current flows as electrons move under the influence of the electric field, as illustrated in figure 3b. Shifting the channel energy bands by applying a voltage to the gate, relative to the source and drain, can create a potential barrier and turn off conduction between contacts, as shown in figure 3b. Such devices are known as metal-oxide-semiconductor field effect transistors (MOSFET, or FET for short) and offer good electrostatic control of the channel region with minimal leakage currents. They form the basis of modern digital logic integrated circuits.

Due to their high mobilities, transistors utilizing CNT FETs exhibit excellent electronic transport behavior\(^18\). In isolated CNTs, ballistic transport free of impurity scattering has been demonstrated over micron long channels at low temperatures\(^49\). Furthermore, short channel devices, below 40nm, exhibit ballistic transport at room temperature\(^21\). Electrons transported ballistically experience essentially zero resistance as they travel from source to drain. This is in contrast to traditional diffusive transport, in which electrons are constantly scattering and the channel contributes additional resistance. Ballistic devices exhibit high drive currents, when turned on, at low operating voltages (similar to currently employed supply voltages in digital logic devices), suggesting densely packed arrays of CNTs will be able to output much higher current densities than current semiconducting channel materials\(^20,50\).
Figure 3. Transport in CNT transistors. Diagram of an n-type device and the relative spatial alignment of CNT energy bands for two different cases. (a) A schematic of the physical layout of the device, the insulated gate electrode applies an electric field that modulates the positions of the CNT energy bands in the channel, relative to the source and drain. (b) Electrons in the conduction band are free to enter the channel. (c) A negative gate voltage raises the potential of the channel relative to the source, creating a potential barrier that prevents electrons from entering the channel.

Additionally, their one-dimensional structure allows for the fabrication of gate electrodes that can fully control channel modulation by wrapping around the CNT entirely\textsuperscript{47}. As channel lengths continue to decrease, coupling of the source and drain electrodes to conventional channels begins to screen the gate, an effect referred to as drain induced barrier lowering\textsuperscript{51}, resulting in performance degradation and ultimately the inability of the device to effectively be turned off. One-dimensional channels, such as CNTs, offer better electrostatic control relative to two- and three-dimensional devices\textsuperscript{52}, with CNT channels shorter than 10 nm exhibiting good electrostatic gate control\textsuperscript{20}.

Simultaneously, CNTs have also demonstrated their worth as channel materials for low-cost and macroscale applications via thin films of CNTs deposited from solution\textsuperscript{53}. Films of overlapping CNTs form percolation networks through CNT-CNT connections, creating a continuous semiconducting film usable as a channel for a thin film transistor (TFT). Because of the high resistance added at each CNT-CNT junction, these films generally underperform relative to devices with direct source to drain CNT connections. However, their ease of formation and device uniformity, due to high CNT density, makes their integration into low performance applications more appropriate\textsuperscript{5,6,54}.

While both short-channel ballistic CNT FETs and large-area CNT TFTs exhibit exemplary electronic transport in their respective applications, there are still many hurdles to commercial integration that require intensive study\textsuperscript{55}. First and foremost is the presence of metallic CNTs that short devices. Purification processes isolate semiconducting CNTs\textsuperscript{31} but may also degrade their electronic properties. Alternatively, the presence of metallic CNTs may actually prove to be beneficial to TFT performance if properly engineered. Furthermore, it is unknown whether or not short-channel CNT TFTs will operate similarly to ballistic CNT FETs. Concurrent GNR synthesis improvements have yielded ideal GNR specimens that may prove to be comparable, if
not superior, to CNTs. While just a few of the many open areas of research into CNTs and GNRs, these are issues this work attempts to address.

**Dissertation Organization**

In this work, solution-processed CNT transistors are fabricated, using a variety of processing techniques, to study the role that fabrication technique and material selection have on thin film transistor device performance. Semiconducting enriched CNTs themselves are studied as both channels for diffusive and ballistic transport, and are compared to other types of CNTs previously studied. Methods to increase device performance and reduce variability are presented and characterized, while limiting factors in device performance are identified for future study. To observe whether or not ballistic transport is possible and whether or not short channel effects become prevalent in solution processed CNTs at short channel lengths, devices are made with channel lengths 4 µm long all the way down to 15 nm. Finally, electron transport is demonstrated for the first time in bottom-up, chemically synthesized, graphene nanoribbon transistors.

In chapter 2, work detailing the processes necessary for growth, transfer, and dispersion of CNTs in solution is presented. Chapter 3 reports the synthesis of a novel biomimetic surfactant polymer and demonstration of its ability to disperse CNTs in solution. Chapter 4 discusses a variety of CNT deposition techniques, the resultant films they produce, and their strengths and weaknesses in experimental applications. Fabrication techniques used in this research are presented in chapter 5. In chapters 6 and 7, TFT performance is correlated with semiconducting purity and deposition process of solution processed CNTs. Additionally, in chapter 8, conversion from high variability, low on-off ratio to low variability, high on-off ratio devices is demonstrated through post fabrication nanomesh patterning of TFT channels. In chapter 9, transistors fabricated with single CNTs deposited from solution are demonstrated with device performance studied at various channel lengths with ballistic transport in short channel solution processed CNT transistors observed. In Chapter 10, short channel devices with chemically synthesized GNR channels are demonstrated and discussed. Finally, in chapter 11, the work is summarized and future work is discussed.
Chapter 2

Growth, Transfer & Dispersion

While bulk semiconductors are their own substrates, CNTs due to their low dimensional nature, must be placed post-synthesis onto a macroscopic substrate to facilitate device fabrication. This presents both opportunities and challenges. On the one hand, this decouples the substrate and channel, and has allowed for the development of transparent and flexible circuitry utilizing plastic and polymer substrates\(^1,2\), among other novel applications\(^3\). However, this also necessitates the development of novel processing techniques for CNT manipulation and deposition, which depends upon the method of material growth.

Synthesis of CNTs can be carried out in multiple manners, the most common being chemical vapor deposition (CVD) using hydrocarbon precursors, high-pressure combustion of carbon monoxide (HiPCO), and laser ablation or arc discharge of graphite. Briefly, CVD is capable of growing long substrate bound SWNTs that are free of defects. HiPCO, laser ablation, and arc discharge produce large amounts of freestanding CNTs with a moderate amount of defects in addition to other reaction products. These three processes are different in execution, but produce similar material. A proper understanding of the CNTs produced through each process is critical to experimental design and application fitness.

CVD growth

CVD growth results in very different material from other synthesis processes. In CVD growth, a substrate with discrete catalyst regions, either patterned or nano-crystalline, is heated in a reaction chamber to temperatures between 800C and 1000C while a carbon source is flowed into the chamber. This produces CNTs, bound to a substrate by at least one point, through a vapor-liquid-solid (VLS) growth process. Catalyst particles, usually a metal such as iron, nickel, cobalt or molybdenum, absorb gaseous hydrocarbon molecules and precipitate the carbon into a CNT. Experimental demonstrations have shown this occurs both as the catalyst particle migrates along the surface, known as tip growth, and precipitation of the CNT by a stationary catalyst, known as base growth.

CNTs with specific alignment can be obtained by growth on specific crystalline substrates\(^4,5\). These substrates are cut along high crystallographic indices, creating steps as the crystal relaxes between lower index planes along which the catalyst travels, precipitating CNTs. Growths utilizing these substrates, typically sapphire or quartz, can produce linear arrays of CNTs of relatively high densities\(^6\), as shown in figure 1a. In specific cases, CNTs can switch chirality as the catalyst moves from one step to another during growth\(^7\).
Alternatively if the catalyst is not bound to the surface it can be held aloft through sufficient flow of precursor and carrier gases to produce growth in the air, this is referred to as flying catalyst or kite growth. CNTs mms long have been grown utilizing this method\textsuperscript{8}. When combined with a quartz substrate, serpentine ordering of the CNT along the crystal steps is common as it falls onto the surface\textsuperscript{9}, an example is presented in figure 1b.

![Figure 1](https://via.placeholder.com/150)

**Figure 1: CVD Growth mechanisms of CNTs.** (a) growth of aligned CNTs along a quartz substrate. Scale bar is 10 µm. (b) CNT serpentine alignment on quartz through floating catalyst growth on quartz. Notice the piled endpoint of the lower CNT as it deposited post growth. Scale bars represent 20 µm.

The size of the catalyst particle affects the diameter of the resultant CNT, and so some control of diameter has been demonstrated with nanoparticle catalysts with controlled diameters\textsuperscript{10,11}, however because of the high temperatures employed during growth, nanoparticle migration and amalgamation is common, so control is reduced. In one case, samples with near mono-disperse chiralities have been obtained through the use of specific catalyst particles. Other methods, such as plasma enhancement, low-pressure atmospheres, and introduction of oxidative materials during growth, have also been shown to produce some enhancement in semiconducting CNT chiralities due to slight differences in the chemical properties of these materials\textsuperscript{12,13}.

The choice of catalyst itself is fairly flexible. Nanoparticles can be deposited from solution or suspended in photoresist to allow for patterned placement. Thin films of evaporated metals are also common. These films, when oxidized, break into catalyst nanoparticles. Because of this, generally the thickness of evaporated metal layers is only a few angstroms thick. Growth processes using evaporated catalyst films generally produce CNTs with diameter distributions between 1.2-1.8nm, but can vary greatly, with CNTs as large as 3nm in diameter.
Transfer

While linear arrays of long CNTs are desirable, their growth occurs on an insulating substrate, which is generally not suitable for electronic applications, necessitating transfer of the CNTs to a secondary substrate as part of the device fabrication process. Illustrated in figure 2, first, an Au film is evaporated onto the CNTs and acts as an encapsulation layer, covering all but the bottom of the CNT that is in contact with the substrate. This layer provides the additional benefit of separating the CNTs from other organic materials involved in subsequent steps and allows for transfers of clean CNTs.

![Diagram showing the transfer process]

Figure 2: Transfer of CVD grown CNTs on quartz to arbitrary target substrates.

A piece of thermal release tape is then brought into contact with the Au layer and gently affixed to the surface. Thermal release tape is a common processing material used to protect substrate backsides during otherwise potentially damaging processing. A light touch is sufficient as the adhesion to the Au is stronger than the Au to the substrate surface. Too much force may push the adhesive layer of the tape through the thermal release layer and cause release and contamination in subsequent steps. Peeling the tape of the surface will now bring the Au and encapsulated CNTs.

Once liberated from its growth substrate, the CNT/Au film can be deposited on any substrate compatible with Au etchant, generally SiO2 due to it’s processing versatility and maturity. The film is placed and, again, lightly pressed onto the surface of the target substrate. The tape/Au/CNT/SiO2 stack is then heated to the release temperature. If too
much force has been used during the transfer process, the tape backing may be directly in contact with the adhesive layer and so release may fail.

\[ \text{Figure 3: Results of the CNT transfer.} \ (a) \text{ CNT transfer with too much applied force. (b) Transfer without sufficient cleaning. (c) CNTs and electrodes post transfer on optically patterned Pd contacts. As can be seen the coverage is continuous over hundreds of } \mu \text{m (d) with CNT alignment preserved. (e) Warping of the CNT array due to poor adhesion during transfer.} \]

Once the tape backing has been removed, the stack now consists of adhesive residue/Au/CNTs/SiO2. Failure to remove the residue before removal of the Au layer will result in heavy surface contamination and so post transfer cleaning is critical to clean transfers (figure 3a & b). This is accomplished through a two-step plasma process: organics are first removed with oxygen plasma that is then followed up with Ar sputtering to physically remove any remaining particulate. This will also sputter off part of the Au film and so care must be taken to avoid fully removing the encapsulation layer. Finally, the Au is removed with Au etchant. Potassium iodide etches Au but is nonreactive to other metals, allowing for direct transfer onto electrodes allowing for clean transfers directly onto electrical test structures, as presented in figure 3c & d.
This method of transfer can be performed on single chips with CNTs grown in small laboratory furnaces, to full wafers grown in large commercial furnaces. In the lab, however, it is temperamental. Small changes in pressure during transfer can cause part of the film to release, but not all, reducing coverage. Similarly, CNTs brought only partially into contact with the substrate, due to microbubbles under the transferred layer, are free to move after removal of the Au, causing bundling or ripping, presented in figure 3e. This is especially of concern if transferring onto pre-defined structures where the surface topology is not completely flat.

**Freestanding CNTs**

In contrast to CVD growths, in which CNTs are grown individually, bulk synthesis processes, such as HiPCO flow reactors, laser ablation, and arc discharge, produce large quantities of unbound materials. Because the material is not already in contact with a substrate, it must be further processed pre-deposition.

**Synthesis Techniques**

The use of combustion chambers continuously produces large quantities of freestanding material. In this process catalyst particles and carbon monoxide, CO, are injected into a high-pressure chamber between 700C and 950C. Sufficient gas flow supports the injected catalyst during growth upon which the CO decomposes into CNTs and CO2, which are then trapped separately. Remaining CO is re-injected into the reaction chamber to continue growth. Immediately after synthesis the metal catalyst is removed with an acid wash, leaving only carbon products.

Extensive mixing due of the suspension of the catalyst allows for uniform temperatures during growth. With specific catalysts, high chirality uniformity may be obtained, although the diameters of CNTs produced via this process are smaller than 1nm in diameter, and selective processes produce CNTs with diameters between .6-.7nm. This material is generally referred to as HiPCO CNTs.

Larger diameter CNTs can be produced via laser ablation. In this process, Graphite and catalyst particles are vaporizes using a pulsed high power laser in an inert high temperature environment. The resultant product consists of about 70% SWNT material, the rest consisting of amorphous carbon, MWNTs, and catalyst. CNTs produced in this manner tend to have diameters between 1-2nm. Larger diameter CNTs, grown via CVD, form ohmic contacts to Pd, making them more desirable for device applications. As such, laser ablation CNTs are also considered more appropriate for electronics so the majority of purification development effort has been pursued using this material.

Because these reactions can be implemented to continuously synthesize product and are scalable, CNT material produced via laser ablation and HiPCO processes has been available commercially for many years. In order to further manipulate CNTs, either to deposit or purify, they must be dispersed into single CNTs in solution.
Suspension in aqueous solution

The most straightforward method for working with these materials is to disperse the CNTs in a solution. This allows for more precise material characterization, purification of SWNT material from other carbon products, and sorting by chirality or electronic type\textsuperscript{15,17,18}. Their unique, highly hydrophobic and aromatic surfaces make CNTs insoluble in most solvents, however, without modification.

The simplest process is to suspend CNTs in organic solvents\textsuperscript{19,20}. Strong ultra-sonication will temporarily disperse CNTs as long as the concentration is low, in the range 10-30 µg/ml, however CNT bundling and aggregation will occur quickly and so samples must be prepared within a few days of use, preferably as quickly as possible. Amide solvents such as dimethylformamide (DMF) and N-methylpyrrolidone (NMP) have been shown to disperse CNTs better than other solvents.

In order to disperse SWNTs in aqueous solutions some functional modification is necessary. Covalent modification of the CNT sidewall, acid induced carboxylation or hydroxylation, is effective in increasing solubility\textsuperscript{19}, but the acid treatment induces defects and the covalent attachment of solubilizing functional group alters the electronic structure of the CNT and reduces electrical conductivity. Therefore it is necessary non-covalently solubilize CNTs for electronic applications. This is possible through the use of non-covalently bonded surfactant molecules.

The process of suspending CNTs in aqueous solutions using surfactant molecules is straightforward. Raw CNT material is added to a surfactant solution and ultra-sonicated. The trade-off between strength of dispersion is counterbalanced by potential damage and scission of CNTs in solution, reducing CNT length, which is undesirable for experimental design. Once dispersed, the solution is centrifuged to pellet out any amorphous carbon or large CNT bundles, which are higher density than dispersed CNTs. The supernatant is then extracted and is generally stable indefinitely. Suspension of isolated CNTs is verifiable through the presence of 1D resonances in optical absorption and photoluminescence excitations, examples of which are presented in figure 4.

A variety of amphiphilic molecules\textsuperscript{19}, polymers, and supramolecular structures\textsuperscript{21} have been shown to successfully functionalize and solubilize CNTs. These materials stack their hydrophobic groups on and around the CNT surface, allowing their hydrophilic groups remain in contact with water. This can be due to micelle formation, as is in the case sodium lauryl sulfate, in which alkyl chains assemble around the CNT, or through pi stacking of aromatic functional groups on the nanotube surface, as is in the case of sodium cholate. These materials produce stable dispersions of isolated CNTs indefinitely.
Polymers containing both hydrophilic and hydrophobic residues are also able to effectively solubilize CNTs. Most notable is DNA, with its highly charged phosphate backbone and hydrophobic nucleotide bases, wraps around CNTs, with bases π-stacking onto the CNT sidewall leaving the backbone exposed to the aqueous solution. Because of sequence specific secondary structure differences in DNA that result in varying affinity and wrapping helicity onto CNT surfaces, highly enriched solutions of single or few chirality CNTs are obtainable through ion exchange chromatography of CNT solutions solubilized with specific sequence DNA oligomers.

**Purification**

Because CNTs are generally considered desirable for electronics, either as metallic wires or semiconducting channels, purification is necessary in both applications. As previously mentioned, ion exchange column chromatography of DNA dispersed CNTs yields samples highly enriched in a few chiralities. However, this technique is delicate due to column chromatography and costly due to the use of DNA surfactant. Other column chromatography methods have also been shown to yield 99% semiconducting enriched samples, however further purification of the CNTs post-enrichment is necessary. Other methods such as salt precipitation of specific CNT types demonstrate promise, but are delicate and results are mixed.

One of the earliest and most successful methods of purification is density gradient centrifugation. In this process, CNTs are suspended in standard surfactant solutions, and then injected into a density gradient column. The column is then centrifuged and the CNT material stratifies according to their relative densities. The material can then be fractioned to isolate specific chiralities or electronic types. In samples utilizing narrow diameter CNTs, individual chiralities can be extracted. With larger diameter samples,
metallic and semiconducting CNTs can be extracted with enrichments over 90%. Reprocessing of the purified material produces samples of up to and over 99.9% semiconducting enriched material. Further precision using optical spectroscopy is not possible and so the purification may in fact be even greater. The yield of this process is limited by centrifuge size, and so commercial ventures have quickly scaled production, making highly enriched CNT samples, suspended in solution, easily obtainable.

CNTs in suspension are much shorter than typical CVD arrayed CNTs, with lengths between 100nm and a few µm. This is due to sonication induced cutting or breaking at defect sites, which bulk produced CNTs have more of. Despite these shortcomings, the ability to purify and solution process high performance electronic material enables new applications has made solution CNT device research of great interest to many research groups who continue to produce novel and exciting research daily.

Suspension and purification are the first steps in the fabrication of CNT-based electronic devices. Just as important as the choice of CNT material to device design is the deposition techniques employed. Device characteristics are as much a factor of CNT deposition technique, film geometry, and density as they are of the CNTs themselves.
Chapter 3

Peptoid surfactants for carbon nanotube suspension

One novel polymer in particular, the peptoid, presents unique opportunities for the intelligent design of functionalized surfactant polymers for CNTs. Peptoids and peptides share a similar CC(O)N backbone, but differ in placement of their residues, compared in figure 1a. In peptoids, residues are appended to the N atom instead of the α-C, eliminating the amide hydrogen responsible for fixed chirality in peptides. Additionally, the lack of this hydrogen enables the use of more general amine molecules, instead of only amino acids, during synthesis. This allows peptoids great flexibility in both conformation and functionality.

Amphiphilic peptoids are interesting candidates for dispersion and functionalization of CNTs. Synthesis is carried out through a two-step sub-monomer addition process, enabling full control over polymer sequence. Because peptoids are naturally achiral, functional groups are free to rotate relative to their neighbors, allowing for more flexibility in conformation when stacked on CNT surfaces. Additionally, precursor selection also allows for functionalization of the hydrophilic functional groups.

Peptoids have previously been used in the aqueous self-assembly applications. In one experiment, two peptoid polymers with AB residue motifs, where A is a phenyl residue and B is a carboxyl or amine residue, assembled laterally into sheets. Electrostatic attraction of the positively and negatively charged hydrophilic groups created lateral stacking of the polymers while vertically hydrophobic concerns directed assembly into a bilayer micelle. Based on this successful demonstration of amphiphilic self assembly, similar peptoids were studied as candidates for CNT dispersion.

Polymer Synthesis and CNT suspension

A peptoid consisting of 36 alternating monomers (figure 1b) 18 hydrophobic phenyl groups and 18 positively charged amine groups in an AB motif, was synthesized and purified using standard processes. The total length of this polymer was 13nm. The peptoid was then dissolved in water at a concentration of 100 µM, similar to standard molecular surfactant concentrations. Large diameter CNT material produced via laser ablation (Cheap Tubes Inc., 1-2nm diameter) is deposited into solution at a concentration of 1mg/ml. Pre-sonication, the black carbonaceous powder drifts to the bottom of the vial, unable to dissolve due to the strong attractive interaction between the hydrophobic CNTs packed together. The solution is then sonicated, causing it to turn black due to dispersion of the material, and finally centrifuged to pellet out amorphous material.
Figure 1: CNT suspension and dispersion with amphiphilic peptoid molecules. (a) Comparison between peptoid and peptide polymer structure. (b) Structure of the PC peptoid polymer. (c) Absorption spectra of large diameter CNTs suspended with the PC surfactant, normalized to 400 nm.

Results and discussion

Absorption spectra presented in figure 1b compare the relative absorption spectra of CNT solutions dispersed using 100µM DNA, 1 mg/ml sodium lauryl sulfate (SDS), and 100 µM PC surfactant solutions. Immediately observable are the similarities between all samples. Indeed, the peptoid polymer, as expected, produced dispersions similar SDS and DNA of larger diameter CNTs. Because of the large number of chiralities and larger diameters in this sample, identification of individual chirality absorption resonances is not possible, however the slight increases in absorption at the S22 and S33 transition energies (roughly 500 nm and 900 nm) suggests the peptoid polymer may disperse semiconducting CNTs more efficiently than other polymers. Atomic force micrographs of deposited CNTs confirm unbundled CNTs are present, however bundled CNTs are also present, as is also observable by the increased baseline absorption of the peptoid dispersion.

Figure 2: Reversible flocculation and dispersion utilizing peptoid surfactants. (a) image of flocculated material in low pH solution. (b) Optical absorption of peptoid/CNT solution pre-flocculation and post-re-dispersion through pH modification.
Because the hydrophilic functional group’s positive charge is dependent upon electron donation, adjusting the pH of the solution affects the solubility of the material. Starting with a neutral solution, the pH is reduced to 2.5 through the addition of hydrochloric acid. Immediately, the CNTs in solution flocculate within solution and quickly precipitate out, shown in figure 2a. This demonstrates that the solubility of the material is dependent upon the charged, polar amine group.

Interestingly, when pH is restored to a concentration of 11.4 by adding sodium hydroxide, the flocculated CNTs immediately re-disperse into solution without any secondary processing such as sonication. Optical absorption post-re-dispersion, presented in figure 2b, exhibits identical structure to that of the pre-flocculated spectra. Because of the attraction of the peptoid’s hydrophobic functional groups and the CNT, the polymer remains attached to the CNT after flocculation. While this may not be unique to peptoid surfactants, to date this has not been demonstrated with other surfactants and presents opportunities for unique processing steps.

Figure 3. Photoluminescence and Optical Absorption spectra of narrow diameter CNTs suspended utilizing PC peptoids. (a) Photoluminescence excitation spectra of PC suspended narrow diameter CNTs. (b) Absorption spectra of same sample indicates resonances quenched

The story changes for smaller diameter CNTs produced via HiPCO processing (Unidym Corp. 0.6-1.1nm in diameter). Samples prepared similarly to the previous sample, with two different surfactants, PC peptoid and SC, processed similarly exhibit radically different absorption spectra. Photoluminescence of the peptoid/CNT solution, figure 3a is maintained, there is strong broad energy transfer resonances indicating the presence of bundled CNTs. In this CNT sample, individual resonances associated with specific chiralities are discernable in the SC absorption spectra, but are quenched in the PC sample, figure 3b. This means that while the PC is capable of dispersing larger diameter CNTs, smaller CNTs remain bundled, where inter-tube interactions alter the energy structure of what would otherwise be 1D structures. This could be due to the inability of the peptoid to sufficiently adhere to the greater curvature of the narrow CNT surface.

With this in mind, a second peptoid, NC (figure 4(a)), with similar AB motif, 36 monomers in length, with an amine hydrophilic functional group, but a naphthalene
hydrophobic residue instead of a phenyl group, was synthesized. The strength of attraction due to π stacking increases rapidly with increasing polyaromaticity, and indeed many other reported CNT surfactants possess polyaromatic structures. Thus the adhesion of this peptoid should be stronger and result in proper CNT dispersion. It should be noted that the increased hydrophobicity of the napthyl-amine precursor necessitated synthesis be carried out in a pure NMP environment to maintain solubility of the precursor and product. This is in contrast to previous syntheses in which DMF or DMSO were sufficient.

Figure 4: Full CNT suspension with NC peptoid surfactants. (a) Chemical structure of NC peptoid. (b) Photoluminescence and (c) optical absorption spectra of NC/CNT suspension.

Peptoid NC was again dissolved in water at a concentration of 100 µM. Optical absorption of CNTs dispersed with NC surfactant is presented in figure 4(b). The Van-Hove singularities consistent with isolated CNTs demonstrate increased isolation of CNTs over the PC surfactant polymer. Additionally, Photoluminescence spectra presented in figure 4(c) demonstrates reduced broad energy transfer resonances suggesting physical separation of CNTs. Since PC and NC are identical polymers except for one extra aromatic ring, this result indicates that indeed increased π stacking in NC is responsible for enhanced CNT dispersion.

This also demonstrates the robustness of peptoid polymers as CNT surfactants. Slight changes in functional groups can have large effects on the dispersion. The addition of hydrophilic functional groups with specific chemical moieties could enable reaction chemistries to be performed at CNT interfaces without damaging crystal integrity. Alternatively, chiral functional groups could induce specific helicity to peptoids, creating preferential dispersion of specific CNT chiralities or allow for specific placement and alignment of CNTs onto molecular scaffolds. Their controllable synthesis and wide selection of functional monomers makes peptoid polymers ideal surfactant molecules for CNT dispersion.
Device fabrication begins with suspended CNTs in solution. While every experiment employs specific test structures and implements certain unique process techniques to improve performance, the general fabrication process consists of a few shared steps. First, channel material is first deposited onto an insulating substrate through a variety of methods. After this, pattern definition of electrodes is carried out through a lithographic process, after which an additive process, such as evaporation or CVD, deposits material in contact with the CNT.

Once in solution, isolated CNTs are ready to be placed on to substrates to form the channel material for semiconducting devices. The method of deposition will set critical design constraints such as device geometry, channel lengths and widths, and influence device performance in important ways. In research experiments, confirming physical behavior of a single CNT may be more important than of an arrayed CNT device. This does not mean however that a transistor consisting of an array of CNTs will exhibit scaled behavior of a transistor consisting of a single CNT, and so processing techniques capable of producing both isolated and arrayed CNTs are necessary for proper characterization.

![Image](image.png)

**Figure 1:** “coffee ring” nematic alignment of CNTs through evaporative deposition. Dense films are produced with some lamellar alignment of CNTs due to alignment along the surface/liquid interface during evaporation. Scale bar represents 2 µm.
Solvent evaporation

The most basic method of CNT deposition is solvent evaporation, in which CNTs are left on the substrate surface as solvent evaporates. This involves dropcasting small amounts of solution onto the substrate. As the solvent evaporates and the solution recedes, CNTs collect at the contact line and are pushed onto the surface. This results in some lamellar alignment with very high CNT density, an example of which is presented in figure 1.

Modifications to this process, such as vertical evaporation of solvent\(^1\), can produce linear arrays of high-density CNT films. The resultant films generally consist of many layers of CNTs, however, that lead to gate screening issues in devices and inefficient channel contacting. Improvements to this process allow for aligned bilayers of CNTs and holds promise as a new method for deposition of CNTs in the use of more complex circuits\(^2\).

Dielectrophoresis

On the opposite end of the spectrum, the precise placement of single CNTs is possible through the use of dielectrophoretic force\(^3,4\). By applying an AC electric field across two pre-patterned electrodes, which can also function as source and drain electrodes post deposition, an attractive or repulsive force can be exerted upon objects in solution due to the differences in their polarizability and electric permittivity. For cylindrical objects in solution, the dielectrophoretic force is defined as:

\[
F_{DEP} = \frac{\pi d^2 L}{8} \varepsilon_i R e \left( \frac{\varepsilon^*_{\ell} - \varepsilon_i^*}{\varepsilon_i^* + (\varepsilon^*_{\ell} - \varepsilon_i^*)L} \right) \nabla E^2
\]

(1)

\[
\varepsilon^*_{\ell, l} = \varepsilon_{\ell, l} - i \frac{\sigma_{\ell, l}}{\omega}
\]

(2)

where \(E\) is the applied electric field, \(\varepsilon_{\ell, l}\) and \(\varepsilon \sigma_{\ell, l}\) are the conductivity and permittivity of the CNT and liquid medium, \(d\) and \(l\) are the diameter and length of the CNT, \(L\) is the depolarization factor, and \(\omega\) is the applied signal frequency\(^5\). The magnitude and direction of this force depends on the frequency dependent permittivities of the solvent and the CNT, the magnitude of the applied field, and the electrode geometry through the electrical field gradient. Experimentally, this effect has been used to separate metallic and semiconducting CNTs\(^6\), deposit high density films over large areas, but also to deposit single CNTs at precise locations with alignment commensurate with the electric field\(^7,8\). This is achievable by fabricating narrow electrodes with separated by sub-micron gaps. Once one to two CNTs are deposited, the increased conduction within the gap reduces the effect of the dielectrophoretic field and minimizes further deposition.

Best results, a single CNT bridging two electrodes, are achievable through the use of very narrow electrode gaps, possible only through e-beam lithography. With optical lithography, with larger minimum widths and electrode gaps, variation in number of CNTs deposited becomes larger. As shown in figure 2a, careful tuning the applied voltage amplitude, CNT concentration, and applied field frequency allows for optimization of deposition to a degree. Similarly, deposition can be tuned to deposit high-density aligned devices with deposition localized to just channel gaps between...
electrodes, shown in figure 2b. However due to the small quantities of metallic CNTs in purified solutions, metallic shorting is highly likely due to the large amount of direct source to drain connections.

Figure 2: Dielectrophoresis of CNTs between predefined electrodes. (a) Deposition of a single CNT through parameter tuning. (b) high density CNT deposition between two contacts utilizing dielectrophoresis. In both images the scale bar represents 1 µm.

**Surface modified adhesion**

Without pre-patterned electrodes, adsorption of CNTs out of solution onto an unmodified silicon dioxide surface is minimal. Certain functional chemical substituents adsorb onto CNT surfaces. Similar, self-assembled monolayers with these head groups attract CNTs, drawing them out of solution. Amine functionalized monolayers preferentially bind to semiconducting CNTs, as opposed to phenyl terminated monolayers that attract metallic CNTs, making their use a standard fabrication step in solution CNT transistor processing. The two main molecules used in experiments are the (3-aminopropyl)triethoxysilane (APTES)\(^9\) and poly-L-lysine\(^10\), both of which are amine terminated and produce films of similar density and electrical properties in transistors.

While ordered monolayer formation is a delicate process, CNT deposition with disordered monolayers are not measurably different in density of alignment. To form the adhesive layer, a cleaned chip is incubated in a dilute solution of the monolayer molecule for a short period of time, after which it is rinsed. The presence of water affects the order of the monolayer and so the most rigorous deposition techniques involve the use of anhydrous solvents, with processing and annealing carried out in inert glove boxes. Monolayer formation is most easily identified through contact angle measurement, as bare oxide is hydrophilic and surfaces treated with APTES and lysine monolayers are hydrophobic.

Once the substrate is modified, CNT deposition can be carried out either via incubation or through spin coating. When incubated in a CNT solution, the substrate will come into contact with CNTs circulating due to thermal gradients, environmental disturbances, and Brownian motion etc. The CNTs that would normally bounce off an untreated surface are instead latched onto by the charged amine moiety and eventually are fully adsorbed onto the surface. The resultant film is normally randomly ordered with density dependent upon solution concentration, and deposition time, shown in figure 3a.
Since monolayer formation is strongly dependent on surface chemistry, patterning of the substrate allows for location specific monolayer formation. An already formed monolayer can be lithographically patterned and etched away, or an insulating material, such as a metal oxide that inhibits monolayer formation, can be deposited on the substrate pre-monolayer formation\textsuperscript{11}. Once patterned, alignment of randomly deposited CNTs can be induced by sufficient linear confinement of the monolayer. This requires the pitch of the confined stripe is narrower than the length of CNTs in solution. For purified samples this requires confinement less than a few hundred nm.

Alternatively, CNTs can be aligned through sheer force (figure 3b). This requires a flow of solution with sufficient sheer to align the CNT along the direction of flow and is achievable through the use of centrifugal forces created by spin coating. During spinning, solvent is spun off, the CNT solution is thinned, and radially aligned CNTs are forced onto the substrate. Density is dependent upon solution concentration and rotation speed with alignment and alignment variation also proportional to rotation speed. At moderate spin speeds and concentrations, films produced exhibit semi-alignment of overlapping CNTs. When concentration of the deposition solution is low and sheer alignment is high, films can be constituted of straight, isolated, CNTs, allowing for fabrication and characterization of single CNT devices.

**Figure 3:** Deposition of CNTs out of solution using an adhesive monolayer. (a) Random deposition of CNTs via incubation in solution and (b) spin-aligned CNTs. Scale bars in both cases represent 2 µm.
Chapter 5

Device Fabrication

The method of deposition and the CNT material employed dictate which specific contact fabrication process is best suited for an experiment. For example, e-beam lithography is capable of producing nm-scale features for sub-μm devices, but is only capable of patterning films a few tens of nm in thickness and too slow to reasonably pattern contact pads used for probing. Furthermore, it is unnecessary to use e-beam lithography to pattern μm-scale devices, where the resolution of optical lithography is sufficient. This chapter discusses the fabrication techniques employed to produce CNT and GNR transistors with channel lengths as short as 15 nm, to devices multiple μm long.

To probe CNTs and CNT networks, they must be contacted electrically through deposition of metallic electrodes. This process is carried out in three steps: lithographic patterning, metal evaporation, and lift off removal of unpatterned material. Each of these steps can be performed in multiple ways.

Optical Lithography

With CNTs, proper lithographic processing is critical to producing uncontaminated, clean contacts. Because of their carbon structure, standard cleaning processes like RCA, piranha cleans, and oxygen plasma descums are impossible, and so surface contamination is difficult to remove once in place. This is best controlled for through proper deposition, exposure, and development, resulting in clean exposed patterns.

To prepare for photolithography, photoresist dissolved in solvent is spuncast onto the substrate surface and baked to drive off solvent to produce a uniform layer that can then be patterned optically. Over-baking will crosslink the polymer and prevent full removal, so hard baking in general should be avoided, even though it is a standard step in silicon processing. This makes wet etch processing, to define a back gate contact pad through silicon dioxide for example, difficult without the use of an adhesion layer, HMDS or a bilayer resist process. Both sample preparation and exposure contribute to successful pattern transfer.

The simplest process is contact patterning, in which the substrate is brought into contact with a patterned mask and then exposed to transfer the mask pattern directly into the substrate. Because of this, feature size is limited to mask features, or about 2μm for standard masks. Underexposure of the photoresist usually leads to incomplete removal during development and so generally it is better to account for some overexposure of patterns. Overexposure will cause features to expand as the edges overexpose, leading to some partially controllable narrowing of small gaps. However, roughness of contact
defined features is high, a few hundred nm usually, and so narrowing through overexposure can easily cause closely separated patterns to merge. In general, it is best to plan for minimum feature sizes of 4\(\mu\)m. Contact aligners are relatively quick to operate, can perform \(\mu\)m-scale alignment, and are capable of patterning an entire wafer in one exposure.

Because of photoresist concerns due to working with CNTs, precautions regarding mask-substrate contact must be taken when using contact patterning. Without hard baking, some solvent may remain in the film, causing it to remain tacky. Excessive application of pressure to bring the mask and substrate into contact can cause stiction, so vacuum assisted and hard contact processing should be avoided.

Finer features can be optically patterned with a reduction stepper. Steppers project mask patterns through a microscope to decrease the physical mask pattern size at the substrate/image plane. This reduces the total field size and limits patterns to small chips arrayed across the full wafer. In the lab, optical reduction removes mask feature size limitations to patterning, allowing for finer features limited by resist sensitivity and optical wavelength. With standard I-line (365 nm wavelength) processing feature resolution down to .5\(\mu\)m is possible with proper dose and focus. Additionally, finer alignment marks enable sub-\(\mu\)m alignment.

### Lift off Bilayer Processing

Regardless of photolithography method, a bilayer resist process will produce smoother features with sharper definition, illustrated in figure 1a. In this process, a complimentary resist is first spun onto the substrate before the photoresist. This process can be a combination G-line/I-line or MMA/PMMA process, but the use of a specific ‘lift off resist’ is the most sensible due to ease of use and the secondary benefits associated with these polymers. Lift off resist is not photosensitive but is soluble in photo resist developer (TMAH). Once exposed, as the photoresist pattern is developed, the uncovered areas of the lift off layer also develops, but at a faster rate. This results in an undercut layer with larger features than the photoresist.

The use of lift off resist is advantageous for a few reasons. First and foremost, bilayer processing, illustrated in figure 1a, with an undercut layer eliminates sidewall deposition during metal evaporation, resulting in sharper features with less edge roughness as well as the elimination of ‘rabbit earing’, demonstrated in figure 1b. Without an undercut layer, material deposited on the edge of the photoresist remains post-lift off because it is connected to the patterned feature. These ‘rabbit ears’ create edges significantly taller than the bulk of the pattern and can either collapse onto the surface and short closely separated features or cause subsequent processing steps to fail through shadowing of subsequent evaporations. This can be mitigated by ensuring evaporation is carried out normal to the substrate surface, that the evaporation solid angle is minimized by increasing target-substrate distance, and the evaporated film is very thin relative to the resist thickness. However, the use of a bilayer process makes processing more reliable.
Figure 1: Efficacy of lift off resist. (a) Comparison of single and bilayer lift off processes. (b) SEM micrograph of two lift offs performed side by side, one utilizing an undercut layer of lift off resist, and one using only I-line resist. Scale bar is 20 µm.

Second, lift off resists tend dissolve cleanly, leaving minimal residues on the surface. Lift off resist degrades over time, however, and will begin to leave particulate as well as residues as it ages. While in a laboratory setting resist generally expires before it is used up and it is tempting to continue processing with the materials at hand, processes should be monitored carefully and photoresist quality should not be taken as given if contamination issues arise.

Finally, lift off resists convert surface hydrophobicity to allow for adhesion of photoresist without surface modification, such as a HMDS adhesion promoter process. This prevents delamination during wet processes such as development and wet etching.

**E-beam lithography**

E-beam lithography is a complimentary process to photolithography that is capable of producing near atomic-scale feature sizes. The basic preparation process is similar, e-beam resist is spuncast onto the substrate to produce a thin patternable film, which is then exposed and used to lift off an evaporated metal film, but because the resolution is so much finer and the pattern is produced through the rastering of an electron beam across the surface, process control is much more important. Because it is a raster process and is therefore much slower than optical field exposure, e-beam lithography is best used in concert with optical processing in experiments that require both large features, like contact pads, in addition to nanoscale patterns.

As with optical lithography, proper dosing is critical to fine feature resolution, however in e-beam lithography this is a much more complex process due to the physical nature of electrons. During the exposure process, electrons bombard the resist and instigate the scission of electron-sensitive polymers, for positive pattern transfer processes. These
high-energy electrons can also scatter within the polymer, at the polymer substrate interface, and within the substrate itself, and broaden the effect of the beam to produce nonlocal dosing of the resist. At high energies, electrons typically do not backscatter within the polymer, so acceleration voltages higher than 20kV are used, but higher 100kV energies are better because this also limits limit local scattering. This, however, results in deeper and broader scattering in the substrate as electrons collide with substrate nuclei, resulting in broader nonlocal dosing as backscattered electrons re-enter the resist. Broad background doses can overdose critical feature areas, and so proximity corrections, i.e. dose modulation at critical features to account for local and nonlocal broadening, can be employed for dense patterns. Spatial separation between large and fine features will also mitigate these effects. Because local dose broadening and nonlocal background exposure is non-negligible in e-beam lithography, pattern contrast, the difference in dose between developable and undevelopable, should be maximized for fine feature patterning. Process control to account for contrast enables single-nm feature resolution.

With poly(methyl methacrylate) (PMMA), features down to approximately 30nm can be resolved through standard development with 4:1 methyl-isobutyl ketone (MIBK) in IPA. This standard process requires a relatively low threshold dose and therefore can be high throughput, which is important to increasing sample turnover in shared user environments. This conversely limits its usefulness at high resolutions because it will readily dissolve fairly high molecular weight polymers, reducing contrast. For higher resolution patterning, multiple process parameters must be adjusted to fully optimize e-beam exposures with PMMA: acceleration voltage, use of low solubility developer\(^1\), Molecular weight of the resist\(^2\), reducing thermal motion during development\(^3\), and pattern design.

The acceleration voltage of electrons in the electron column will dictate the relative amounts of forward and back-scattering. Exposures performed with lower energy electrons are more susceptible to local exposure broadening and exhibit more pattern variation within a single exposure. The same exposure performed at both 50kV and 100kV, using with different tools, device variation for a 20nm channel length went from up to 15 nm down to 5 nm as acceleration voltage increased. In isolated devices, the tradeoff of increased background dose is offset by tighter pattern control.

![Figure 2: Patterning failure due to dose overlapping.](image)

Two patterns with equal dose but with different widths. (a) Successful patterning of a 100 nm wide channel. (b) Shorting of 200 nm wide channel. The short occurs at the center of the pattern where the dose overlapping is higher. Scale bars represent 100 nm.
Beam spot size and profile likewise affect pattern integrity as low dose tails overlap between neighboring exposed spots and can additively overdose regions within a pattern. The result of this can be seen in figure 2, in which a small gap is exposed with channel widths of 100 and 200 nm. While the exposure of the 100 nm gap is acceptable, the 200 nm pattern, due to extra local and overlap dosing, is overexposed and the channel is shorted. As seen here and will come up again later, to pattern very small gaps, the local patterns themselves must be spatially constrained or dose must be varied across the pattern. In practice, this overlap dose is significant; the difference in correct dose for a sub-100 nm circular dot is approximately double the correct dose for a 100 nm line.

Figure 3: Improper e-beam doses. (a) Two underdosed contacts. Note the organic nature of the pattern. (b) An overdosed exposure with regularly arrayed dots of cross-linked, undevelopable, material. Scale bars represent 1 µm.

While care must be taken to minimize dose overlap, underdosing is just as problematic and must also be avoided. If spot steps are much greater than the beam spot size, while the total integrated dose of the pattern may be properly exposed, locally, areas will be overdosed or underdosed, as seen in figure 3a. In this exposure, residual polymer was left after development, resulting in poor film adhesion and continuity. Conversely overdosing will result in loss of fine feature resolution and should also be avoided, and eventually. Significant overdosing can cause cross-linking of the polymer and will also prevent removal during development, an example presented in figure 3b. Slight overdosing generally results in regular arrays of dots where the beam overlap was strongest.

During development, scissioned PMMA polymer of reduced molecular weight, relative to unexposed resist, is solubilized and removed. This involves intercalation of developer into the polymer matrix, reducing developer solubility limits solvent intercalation to only surface layers and prevents longer polymer chains from dissolving and ensures that only areas of high dose will develop and minimizes partially dose edges. A co-solvent solution of 7:3 IPA:H$_2$O, both of which PMMA is insoluble in, offers high contrast while keeping total threshold doses reasonably low.$^1$
Similar to minimizing development to low molecular weight material, increasing total molecular weight of the polymer to begin with increases range of polymer masses post exposure\(^2\). This will raise threshold dose and contrast between short chain, developable, polymers and unexposed material. As lateral dose profile drops off quickly outside of exposed regions, this limits the removal of partially exposed edges.

To further reduce dissolution of mid-weight polymer during development, processing at low temperatures (0\(^\circ\) C) decrease thermal motion at the interface, preventing partially and unexposed material from conformationally rearranging to allow solvent to absorb into the film\(^3\). To assist in development at low temperatures sonication will induce mixing of the solvent assist in removal of soluble materials. Of all the parameters discussed, Temperature of development has the strongest effect on resolution of fine features. The effect of increasing contrast in exposure processes not only facilitates higher resolution patterning, but because of slight vertical dose variations, high contrast development processes produce slight undercuts in developed layers, beneficial to lift off processes.

![Figure 4: Possible modes of pattern failure.](image)

(a) Partial development of the channel gap resulting in failed lift off due to reduced film thickness and partial shorting of the channel. (b) PMMA that has partially collapsed. (c) De-anchoring of the fin at one end, allowing it to move during development. Scale bars all represent 200nm.

Material concerns must be taken into account when patterning fine features. The PMMA itself is not a rigid or structurally robust material and will collapse if the aspect ratios of lift off patterns are too extreme. With short source-drain gaps, a narrow fin of material separates two patterned rectangles. If the height of this fin is much more than it’s with (observationally, about 2:1), the PMMA will collapse onto itself. Strong capillary forces can also cause the fin to break away at one or both edges and so development must be performed delicately. Similarly this limits channel widths because longer fins are more flexible and susceptible to damage. Thinning of the PMMA layer will reduce the prevalence of resist failure, but also places upper limits on the evaporated layer thickness for lift off. Some examples of failure modes are presented in figure 4.

The final variable to control for in patterning is the mechanics of the instrument itself. During exposure the electron beam is scanned/rastered along the fast axis, and is stepped along the slow axis. To form a rectangle, a common shape of an electrode, the beam may either be rastered horizontally or vertically to fully pattern the rectangle, and because steps between raster lines is slow tools will generally program pattern exposures to minimize raster stepping. However, because each swept line is quickly swept, the edge roughness parallel to the fast axis is less than the roughness parallel to the slow axis, so raster alignment must be forced to sweep parallel to narrow gaps. An illustration of the
roughness of an exposed pattern is presented in figure 5a. The difference in sweep patterns is 1-2 nm shorter channel widths, 1-2 nm in extra width variation, and 10% more dose leeway before sub-20 nm channel gaps overdevelop and short. A resultant short channel gap is presented in figure 5b.

![Figure 5](image)

**Figure 5: Raster control of pattern exposure.** (a) Illustration comparing sweep direction on edge roughness. Edge roughness is reduced parallel to the sweep direction. (b) SEM micrograph of a resultant 100 nm wide, short channel gap. The measured gap in this device was 16 nm. (c) Bowtie contact with measured gap of 6 nm. Scale bars represent 100nm.

When these variables are controlled and processing is properly implemented source drain gaps of less than 20 nm can be easily achieved in 100nm wide electrodes, with gaps as low as 15 nm possible. By employing more constrained patterns, even higher resolutions are attainable. By tapering the edge of each contact to a point, gaps as small as 5 nm, an example of which is shown in figure 5c, between to points is possible, although variation in these patterns is large. Bowtie patterns are used to produce plasmonic structures, but can also be used to fabricate ultra-narrow channel gaps due to the sharp angle of contact.

**Evaporation**

Once patterned and developed, metal contacts are then deposited. Generally this is carried out via e-beam evaporation. An electron beam is aligned to bombard a metal source, causing it to heat at the point of impact to until it begins to melt and evaporate, and in some cases sublimating due to the vacuum environment. This process is alternative to thermal evaporation, in which heat is applied through joule heating with a high current source.

E-beam evaporation is advantageous for a few reasons. First, the point of applied heat is confined. This keeps the point of evaporation confined to a very narrow region and increases directionality of the evaporation source. Directionality is important to minimize sidewall deposition. The heat transfer is also much more focused and so less overall energy is required, reducing heating of the target substrate. Finally, there is no heating of a thermal evaporation boat that may or may not contaminate evaporation source and sample. Second, heating via the electron beam allows for greater process control as the thermal mass of the active area is much less than in a thermal evaporation chamber. Finally, the separation physically of the heating mechanism from the source
enables multiple sources to be easily manipulated and evaporated within the same process.

Evaporation of thin films requires extra attention to detail. As previously discussed, PMMA must be kept very thin to produce fine features. This limits metal thickness to one third, at most one half, the PMMA layer, so for the highest resolution features, metal layers are limited to about 10 nm. This same limitation applies to films evaporated using a bilayer optical process, limiting layers to a few hundred nm.

Evaporation rate will also affect film quality. Chamber heating will cause a steady temperature rise over time regardless of evaporation rate. If deposition occurs too slowly the substrate heats up causing deposited material mobility to increase. In thin layers this causes formation of larger rough aggregates, which may be discontinuous, instead of a smooth film. Water-cooling of the substrate chuck partially ameliorates this issue, however the thermal gradient across a wafer and heated chuck in vacuum can be non-negligible. Conversely, evaporation too fast is difficult to control, especially with very thin layers. To evaporate thin, continuous, films, an evaporation rate of 3Å/s is generally a good starting point.

**Self aligned gaps**

Patterning of narrow gaps between two contacts is possible with resolutions comparable or better than deliverable through e-beam lithography by self-alignment of the source and drain. Generally self-alignment occurs through either a combination of differences in material properties (sidewall etch passivation), an anisotropic etch, deposition, or implantation process (spacer lithography), and a controlled growth process (oxidative fin narrowing). These processes can be used to form sub 10 nm source drain gaps in lieu of precise dose calibration with thicker final metal films, at the cost of multiple e-beam lithography steps.

**Figure 6: Overview of the overlap self-alignment process.** (a) Specific film thicknesses known to successfully lift off are included. (b) SEM micrograph of self-aligned gap produced via this process, with a measured gap of approximately 10 nm. Scale bar represents 100 nm.
Self-alignment is performed via a four-step process, presented in figure 6a. First, a metal stack of X/Al is evaporated and lifted off to form the source, where X is a metal etch resistant to TMAH. Second, the sample is annealed in air to oxidize the Al. Third, the drain is patterned overlapping the source and a metal layer of metal X half as thick as the source layer is deposited. Fourth, the Al layer is etched away in TMAH, causing the part of the drain overlapping the source to be lifted off. Because Al expands a few nm as it oxidizes, the aluminum oxide layer will shadow a few nm of the oxide substrate between the source and drain. This process relies upon oxidative expansion of Al, directional evaporation of the overlapping layer, and etch resistance of the contact metal to Al.

This process yields source drain gaps between 9-14 nm, as demonstrated in figure 6b. However, it is subject to similar constraints as high-resolution e-beam lithography. Because the drain must be lifted off the source in a manner similar to a bilayer lift off process, this limits the thickness of the drain to a third of the source. This necessitates a source layer of at least 30 nm to allow for a continuous drain of 10 nm. Additionally, minimizing edge roughness is crucial to ensure proper Al lift off and optical lithography is insufficient, e-beam lithography is necessary. The e-beam resist layer, then must also be sufficiently thick, as rabbit earing will also cause a gap through evaporation shadowing and render the self-alignment process useless.

Even with perfect processing, this technique is prone to failure if Al lift off is not optimal. A thick Al layer lift off is easier than a thin layer, but correspondingly shadows more and produces wider gaps. Additionally the source and drain must be aligned to prevent edge overlapping that will inhibit Al release. The drain pattern should be narrower than the source to assist in cases of unreliable alignment. Finally, over long ranges inevitably there are points of lift off failure. To prevent this, drain contact widths should be less than 300 nm, which is slightly wider than achievable through single step e-beam lithography.

**Conclusion**

In this and the previous chapters the individual steps in device fabrication have been discussed in great detail. CNTs of a variety of sources are either transferred or dispersed in solution and deposited onto an insulating substrate. Contact patterns are then defined lithographically and metals are evaporated on top of CNTs, forming three terminal devices of back-gate, source, and drain electrodes. Secondary processing steps, such as gate deposition, are performed via the same methods and are subject to the same preparation concerns. Once fabrication is finished, devices can be studied.
Chapter 6

Comparative studies of thin film transistors utilizing purified solutions of carbon nanotubes

While transistors utilizing single CNTs exhibit outstanding electrical properties\(^1\), issues with placement\(^2\), alignment, and electronic type present large roadblocks for large-scale integration. For different applications, however, thin film networks of CNTs can serve as a high-performance channel in thin-film field effect transistor (TFTs) and other device applications\(^3\)-\(^8\). These films benefit from the high mobilities of CNTs, over other organic semiconducting materials, while eliminating the need for precise control over placement of individual CNTs. Although these thin films generally exhibit degraded performance relative to a single CNT device, their strong TFT performance and low cost of deposition\(^9\)-\(^11\) makes these CNT thin films a potentially disruptive channel material.

CNT thin films have their own shortcomings as a channel material, however, that must also be addressed. Such films may have a lower mobility than single CNT devices because CNT-CNT crossings inhibit current flow from source to drain, especially when the channel length is longer than average CNT length\(^12\),\(^13\). Additionally, the presence of metallic CNTs in the film may lead to shorted channels or fully metallic percolation pathways, which is especially problematic for short channel lengths and wide devices. Because of this, while increasing the network density may increase current, it may also lead to shorted devices\(^7\).

The co-existence of metallic and semiconducting CNTs can be addressed to some extent by using purified semiconducting enriched CNTs produced, for example, by density gradient ultracentrifugation\(^14\). However, it is very difficult to produce a 100% semiconducting CNT solutions due to process variability and cost concerns, and so even the most purified of solutions contains some metallic CNTs. To date, research based on pre-enriched semiconducting CNTs (i.e., over 95% semiconducting nanotubes) has demonstrated promising results in producing micron-scale TFT devices\(^15\),\(^16\). Nevertheless, many issues remain to be unsolved, including degradation in on/off ratio as devices are scaled down due to metallic shorts. Other open questions include whether CNT purification actually improves device performance, and how does the topology of the film itself affect transport\(^17\).

In this chapter, \(\mu\)-scale devices, fabricated using thin films of CNTs of 90% and 99% semiconducting purity, to study the effects of density, electronic purity, and alignment of the thin film network on device performance. Contrary to expectations, the use of 99% enriched semiconducting CNTs did not improve device performance over 90% enriched
CNTs, because of both the continued presence of some metallic CNTs as well as purification specific material degradation. Additionally, device performance can be significantly improved by depositing semi-aligned CNT films instead of forming random CNT networks.

**Experimental Design**

Figure 1a presents an illustration of a solution-processed SWNT thin film transistor. Fabrication begins by cleaning a silicon substrate with a 55-nm oxide layer (Si/SiO₂) in O₂ plasma (30mT, 50W, 1 min.) to make it hydrophilic. Next, the cleaned substrate is immersed in a poly-L-lysine solution (0.1% w/v in water; Sigma Aldrich, 10 min.) followed by a deionized (DI) water rinse to form an amine-terminated adhesion layer⁹,¹⁰. The substrate is then immersed in a commercially available solution (0.01 mg/mL) of enriched semiconducting nanotubes (NanoIntegris Inc.), produced via ultracentrifugation, followed by DI water and isopropanol rinses. After deposition, 30-nm Pd source-drain electrodes were deposited using e-beam evaporation followed by a lift-off process. Finally, each device was isolated utilizing photolithography and O₂ plasma, fixing the channel widths and eliminating extraneous shorting pathways.

**Figure 1: CNT TFT devices.** (a) Device schematic for a back-gate solution-processed CNT thin-film transistor. (b) SEM micrograph of a network channel of CNTs deposited randomly on a SiO₂ substrate.

In all devices, the gate width and length were fixed at 3 μm and 4 μm, respectively. 144 devices were fabricated for each deposition condition. Although the transistors exhibited some hysteresis, as is typical for devices of this type¹⁸, the current values and on/off ratios, the central focus of this study, remained robust and independent of the directional history of the voltages applied to the gate. Figure 1b presents micrographs of a representative device. Devices utilizing two different solutions of varying purity, 90% semiconducting and 99% semiconducting, were studied. Electrical measurements of the
TFTs were carried out in air, at room temperature, with no further passivation or annealing treatments.

**90% semiconducting device measurements**

For the 90% semiconducting solution, substrates were incubated for 1 and 3 minutes. The resultant CNT density were measured via afm and found to be 28-38 tubes/µm² and 42-52 tubes/µm², respectively, and are presented in figure 2a. Evidently, the density CNTs deposited onto the poly-L-lysine-modified SiO₂ strongly depends on the deposition time. These deposition parameters were sufficient to produce samples that exhibit network transport, even at a relatively low density. The transfer characteristics of devices fabricated using the two deposition processes are presented in figure 2b and 2c.

Devices utilizing films formed via a 1-minute deposition (figure 2b) exhibited 100% semiconducting performance with high on/off ratios and an average on current of 360nA/µm. Importantly, previous reports regarding of devices utilizing random CNT have only demonstrated on/off ratios of factor of 2-3 for a relatively short gate length of 4 µm, even with a 95% semiconducting nanotube solution. In comparison, devices produced with a 1-minute incubation time possess an average on/off ratio of almost 10⁶. In transistors with tube densities greater than the network percolation threshold, there are many random metallic nanotube paths that may short between the source and drain. By limiting channel width to 3um these metallic pathways are reduced in the case of dense films (fig. 2c) or even eliminated (fig. 2b) for lower density films. Striped etching of channels has been used previously in macroscopic devices to increase on/off ratios in 100um channel length devices by limiting lateral metallic pathways while relying upon long channel lengths to limit the incidence of fully metallic source to drain pathways. Here, however, the use of enriched semiconducting material eliminates the long channel length requirement, enabling devices to be fabricated with short channel lengths that possess better drive current and on/off ratios.

Unfortunately, for devices with higher density channels produced via 3-minute deposition, while average I₉ₑ₉ increased to 810nA/µm, on/off ratios varied over 6 orders of magnitude, with yield of the devices with high on/off ratios were lower than those of the devices fabricated with a 1-min deposition time (Figure 3c). This is consistent with prior reports. Given that 10% of SWNTs in the solution are metallic, the most straightforward explanation for the observed deterioration of on/off ratio is that the probability of metallic interconnections between the source and drain electrodes increases with higher CNT density. Therefore, this deposition method entails an inherent tradeoff between high I₉ₑ (with a corresponding high mobility) and low I₉ₑ/I₉ₑ ratios.
Figure 2: 90% semiconducting enriched CNT films. (a) AFM images of random, 90% semiconducting enriched CNT networks formed via 3 and 7 min. depositions lengths. Scale bar is 1 µm. (b) Transfer characteristics and $I_{ON}/I_{OFF}$ distribution variation of the lower density film, at source-drain bias of $V_D = -0.5$ V. Subthreshold swing extrema are inserted in the graph (unit: V/dec). (c) Similar data for the higher density film.

Figure 3: 99% semiconducting enriched CNT films. (a) AFM images of random, 99% semiconducting enriched CNT networks formed via 3 and 7 min. depositions lengths. Scale bar is 1 µm. (b) Transfer characteristics and $I_{ON}/I_{OFF}$ distribution variation of the lower density film, at source-drain bias of $V_D = -0.5$ V. Subthreshold swing extrema are inserted in the graph (unit: V/dec). (c) Similar data for the higher density film.

99% semiconducting device measurements

To determine if this tradeoff can be mitigated through further enrichment of the solution, devices fabricated using 99% semiconducting CNT solutions were also investigated. For the 99% semiconducting CNT solution, substrates were incubated for 3 and 7 minutes, and are presented in figure 3a, with resultant densities of 46-54 tubes/µm$^2$ and 60-76 tubes/µm$^2$, respectively, and are again presented in figure 3a. For the 99% solution, a 1-minute incubation was found insufficient to produce network transport in deposited films, most likely due to the decreased length of the 99% enriched CNTs, relative to the 90%
CNTs, due to secondary purification. These shorter CNTs are less likely to overlap for a given density, and thus the probability of a complete source to drain pathway is unlikely at low densities.

Because the densities of the 3-minute deposition are similar for both solutions, the similarities and differences between the two solutions are obvious. As shown in figure 3b, the average $I_{ON}$ of the 99% solution, at 74 nA/µm, is more than a factor of 10 lower than devices produced with the 90% solution. Decreased CNT length necessitates network paths between the source and drain consist of more inter-CNT overlapping contacts, resulting in higher resistance and lower on-currents. While the maximum off-current leakage is reduced by more than two orders of magnitude, the devices still exhibit large variations in on/off ratio. Increasing semiconducting purity to 99% did eliminate most metallic shorting, their presence still results in off-state variation.

This observation is corroborated by higher CNT density devices, produced with a 7-minute long deposition, which are presented in figure 3c. Again, the increased density results in an almost four-fold increase in average on-current, 283nA/µm, while on/off ratios are greatly reduced. This time variation in $I_{OFF}$ is also reduced, but only because metallic paths are prevalent enough to begin to dominate device performance. Unequivocally, the higher density, 99% semiconducting CNT TFTs perform worse than the lower density, 90% semiconducting CNT TFTs. Their $I_{ON}$ is lower their on-off ratios are worse.

**Spin Aligned CNT films**

This experiment shows that there is an inherent tradeoff in $I_{ON}$ and on/off ratio for networks of randomly deposited CNTs where metallic CNTs are present. Additionally, it demonstrates that materials concerns inherent in the purification process itself result in performance degradation that offset many of its perceived benefits. The question then becomes, is it possible to improve device performance further by engineering film properties other than CNT density and purity?

One such parameter is the alignment of the CNTs within the conducting film. This can be carried out in a number of ways, the simplest and most controllable of which is through spin-alignment. In this technique, the substrate is spun as the CNT solution is deposited31. The centrifugal shear force on the CNT induces radial alignment macroscopically, but is essentially linear for micron-scale devices. Spin-alignment has been be used to increase CNT density without significantly increasing the number of network junction points and it is well known that density and alignment directly influence device behavior35. To determine if CNT alignment can indeed improve device performance, direct comparison between spuncast and random network CNT TFTs is necessary.

Devices are prepared in a similar manner to those previously discussed, but instead of incubating in a CNT solution, substrates are spun at 3,000 rpm and 7,000 rpm, while a constant volume (200 µL) of 90% semiconducting nanotubes is dropped onto the
spinning substrate. Again devices were fabricated with channel lengths of 4µm and widths of 3µm.

Figure 4a presents afm micrographs of the spin-assembled films. While the density of the two films is similar, the difference in CNT alignment is pronounced. The higher fluidic shear force of the 7,000 rpm spun sample leads to enhanced alignment, consistent with previous reports\textsuperscript{21}, while there is still some lateral orientation of CNTs in the 3,000 rpm sample.

Figure 4: Spin-aligned CNT TFTs. (a) AFM images spin-aligned CNT networks using the 90% semiconducting nanotube solution under two spin speeds: 3000 and 7000 rpm. Scale bar is 1 µm. Because the spin-aligned method results in the radial alignment from the center of the substrate, only upper parts of the chip showing the same direction of the alignment were used for device fabrication. (b) Transfer characteristics (ID-VG) both 3000 and 7000 rpm alignment speeds, measured at V\textsubscript{D} = -0.5 V. The subthreshold swing value is inserted in the graph (unit: V/dec). (c) I\textsubscript{ON}/I\textsubscript{OFF} ratio distributions.

Both sets of spin-aligned devices exhibit higher I\textsubscript{ON} values than those with random network CNT films (Figure 4b and 4c). Comparing devices fabricated from 90% semiconducting CNTs with 3-min drop-coating deposition and those spin-assembled at 3,000 rpm, although the density of the spin-aligned film is much lower than the random film, average I\textsubscript{ON}, at 1.3±0.2 A/µm, is higher by a factor of 2. This is due to the random orientation of CNTs in the incubated sample, leading to more CNT-CNT contacts that add to channel resistance. Conversely, the semi-alignment of the spun-cast sample results in a more linear source to drain pathway with fewer CNT-CNT junctions. However, the on/off ratio varies over roughly 6 orders of magnitude. At 3,000 rpm, a large amount of nanotubes adsorb nonspecifically, similar to drop-coating, and connect other semi-aligned pathways, potentially forming one that is fully metallic.
In contrast to the large variation in on/off ratio of the 3,000 rpm spun-cast sample, the uniformity of the on/off ratio is significantly improved in the 7,000 rpm spun-cast sample (Figure 4c). The highest normalized $I_{\text{ON}}$ value obtained, with an $I_{\text{ON}}$ of 1.2 $\mu$A/$\mu$m and an on/off ratio of almost $10^3$, stands among the best-reported CNT TFT devices to date. The narrowed distribution of on/off ratios is the result of enhanced alignment effectively reducing percolation of metallic nanotubes across multiple semi-linear pathways. Therefore, these results suggest that the spin-assembly technique can be further optimized to extend beyond the random nanotube network formation observed with the drop-coating deposition technique.

It is worth noting that at faster spin speeds (greater than 9000 rpm with the same volume of nanotubes), network formation was inhibited by a lack of CNT-CNT junctions because the alignment was too strong. Some misalignment is necessary to create percolation pathways between the source and drain.

**Conclusion**

Preventing the formation of fully metallic pathways is critical to forming semiconducting CNT thin film transistors. When CNTs are deposited randomly, the presence of these metallic CNTs adds variability and limits the density, channel width, and/or the channel length. While it would seem reasonable to assume that reducing the proportion of metallic CNTs would thus result in increased performance, quite the opposite is true, due to material degradation that occurs during purification. On the other hand, alignment of the CNTs within the network results in better performance and lowered variability, indicating the development of scalable, reliable processing techniques to align CNTs out of solution are critical in the fabrication of high performance solution-processed CNT TFS. It should be noted, however, that alignment only partially mitigates the issue of metallic shorting, limiting channel length scaling in order to prevent a single of few CNTs from directly bridging the source and drain. Elimination of metallic CNTs is critical for future advances in CNT device performance.
Chapter 7

Thin film transistors produced from highly purified, solution processed carbon nanotubes

In the previous chapters, thin film transistors made from networks of CNTs deposited from 90% and 99% semiconducting chirality enriched solutions were shown to exhibit high drive currents or semiconducting behavior, but with an inherent trade-off between the two properties. This was due to the residual presence of metallic CNTs. Further purification did not necessarily result in better device performance, rather, additional shortening of the CNTs during secondary purification resulted in reduced drive current regardless of on/off ratio for the 99% semiconducting solution when compared to the 90% solution. These limitations can be mitigated to a certain extent through the use of alignment or patterning techniques, but do not address the core issue and possess their own limitations as well. These results inevitably lead to one conclusion: higher purification is required to eliminate the presence of metallic CNTs in random networks of CNTs that lead to large variation and degradation in device performance.

In this follow-up experiment, thin film transistors (TFTs) with 99.9% semiconducting CNT enriched channel material, which was produced specifically for research purposes by multiple, repeated ultracentrifugation purifications, are compared to devices consisting of 90% semiconducting CNT enriched channels. These highly enriched devices are not only not subject to the same limitations that the less purified films are, but exhibit exemplary device characteristics, among the best TFT devices reported to date.

Experimental Design

Device fabrication is carried out in a manner similar to the devices in the previous chapter. First, a highly p-doped silicon substrate is used as the back-gate, with a thermally grown 55-nm-thick back-gate oxide (SiO$_2$). The substrate is incubated in a poly-L-lysine solution, to form an amine-terminated adhesion layer, and then rinsed in deionized water and isopropanol (IPA). The substrate is then immersed in a CNT solution for a fixed period of time, rinsed again, and then dried with nitrogen. Source and drain electrodes are formed by patterning and evaporating a 30-nm-thick Pd layer followed by a lift-off process. Lastly, the channel is defined by an additional photolithography step and O$_2$ plasma etch. This defines the channel width in addition to electrically isolating each device. In this study, solutions with 90% and 99.9%
semiconducting CNTs were used as channel material. Channel lengths and ranged from of 0.8 to 3 µm and 2 to 30 µm, respectively.

Figure 1a presents optical absorption spectra for the three solutions of varying purity. The strong reduction in the M_{11} peak, associated with the first metallic excitation transition energy, from the 90% solution (blue line) when compared to the 99% solution (green line) indicates removal of most, but not all, metallic CNTs. Absence of these peaks in the 99.9% solution (red line) suggests near, if not, complete removal of metallic CNTs.

![Figure 1: Characterization of CNT materials.](image)

Figure 1: Characterization of CNT materials. (a) UV-vis-NIR absorption spectra of the 90% (blue), 99% (green), and 99.9% semiconducting nanotube solutions (red). (b) AFM images (scale bar represents 1 µm) of random CNT networks of 90% and 99.9% semiconducting enrichment for varying deposition times.

AFM micrographs of deposited films used as channel material are shown in figure 1b and verify that unbundled CNTs are randomly oriented on the SiO2 surface. 1 and 3 minute depositions of the 90% solution resulted in average CNT densities of 9-14 tubes/µm² and 12-18 tubes/µm², respectively. In comparison to these short depositions times, deposition of the 99.9% semiconducting CNTs out of solution took 120 minutes to obtain a film with 32-41 tubes/µm². As previously seen, due to shorter CNTs in purer solutions¹, higher densities are required to effectively form percolation networks to enable source to drain connections. This longer deposition time may be the result of shorter CNTs interacting less with the substrate².
Device Measurements

Figure 2a presents the transfer properties of a single CNT TFT with a 1.5 µm channel length ($L_G$) and 2 µm channel width (W) with source drain bias $V_D$=0.5 V. Even with a relatively short channel length, with an on-state current ($I_{on}$) of 2.45 µA (1.22 µA/µm) at $V_G$ = -10 V, transconductance ($g_m$) of 0.84 µS and on/off ratio of $3 \times 10^5$, the electrical characteristics of this CNT TFT are excellent, compared with other reported devices. This is due to the high purity of CNTs employed in this study. With more metallic CNTs present, it is unlikely that a device this short, with a CNT film this dense, would be free of fully metallic shorted pathways.

Figure 2: Electrical Characterization of semiconducting enriched CNT TFTs. (a) Transfer characteristics ($I_D$-$V_G$) of a representative device, produced using 99.9% semiconducting nanotubes. (b) Output characteristics ($I_D$-$V_D$) of the same device. (c) Transfer characteristics ($I_D$-$V_G$) of the three sets of 90 devices produced with different solution purities and densities. (d) Statistical variation of on/off ratios for each set of devices.
Figure 2b shows the corresponding output characteristics of the same CNT-TFT. The linear response at small $V_D$ indicates good ohmic contact between the Pd metal electrodes and the nanotubes. The device also exhibits good saturation behavior at larger negative $V_D$, demonstrating reasonable field effect operation free of short-channel effects. From $g_m$, an extracted mobility ($\mu$) of the TFT of 73 cm$^2$/V•s is higher than previously reported values$^{23}$ because of the high network density of the CNTs. Previous works investigating CNT TFTs utilizing films containing only 1-2% of metallic CNTs report significantly decreased on/off ratios for $L_G=2$-4 $\mu$m.$^5$.$^6$ Higher purity semiconducting material is necessary to make devices with high mobilities and on/off ratios at short channel lengths.

Figure 2c aggregates the transfer characteristics of all 270 devices in three different sets (9-14 tubes/$\mu$m$^2$ and 12-18 tubes/$\mu$m$^2$ for the 90% semiconducting solution, 32-41 tubes/$\mu$m$^2$ for the 99.9% semiconducting solution). The CNT-TFTs produced from the 99.9% semiconducting solution have significantly higher on/off ratios compared with those obtained from the 90% CNT solution, especially at short-channel lengths.

Looking at on/off ratios for each set of 90 devices (figure 2d), for the denser film of 90% semiconducting CNTs the average on/off ratio of $10^{0.79\pm0.36}$ is poor compared to the average on/off ratio of the 99.9% semiconducting film at $10^{5.20\pm0.34}$. The less dense 90% semiconducting film, at $10^{1.53\pm0.92}$ exhibits larger variation overall, while still possessing a very small on/off ratio. Not only do devices that utilize the 99.9% semiconducting CNT film have larger on/off ratios, but the device-to-device variation is much lower as well.

Figure 3: Channel length and width scaling. (a) Average on-state current of devices with various channel widths measured at $V_D = -0.5$ V and $V_G = -10$ V. (b) Average on/off ratio ($I_{on}/I_{off}$) versus channel width for devices fabricated from 90% and 99.9% solutions. (c) On/off ratio ($I_{on}/I_{off}$) versus channel length for devices fabricated from 90% and 99.9% solutions.

Statistical data comparing the three sets of devices, as $L_G$ and $W$ are varied, further demonstrates the ability of the 99.9% semiconducting film to maintain favorable device characteristics throughout a broad range of device geometries. Figure 3a presents $I_{ON}$ as a function of channel width. TFTs produced with the 90% solution reach an on-current of 216 $\mu$A for channel lengths of 0.8 to 3 $\mu$m. For a width of 30 $\mu$m, this on-current is
higher by a factor of 3 to 12 than for devices utilizing the 99.9% solution at all channel widths. This is attributable to the shorter length of the highly purified CNTs and the higher density of the film, resulting in more CNT-CNT junctions\(^7\). Additionally, presence of metallic CNTs in the 90% solution also decreases channel resistance. While the current of the highly purified channels is lower, all devices exhibit similar decreases in current as \(W\) is reduced. Because of the higher density of the 99.9% film, it is less sensitive to scission of the edge percolation pathways, resulting in less drop-off in \(I_{\text{ON}}\) at small \(W\).

Despite lower drive current, the effect of \(W\) on on/off ratio (figure 3b) demonstrates the robust nature of the purified film. As previously demonstrated, devices using 90% semiconducting CNT films can exhibit large on/off ratios due to narrow device widths and channel lengths longer than the average CNT length. Here, devices utilizing the purified film maintain a constant on/off ratio of \(10^5\), regardless of channel width. This is in contrast to devices made with the unpurified material\(^8\), whose on/off ratio rapidly deteriorates from \(10^4\) to less than 10 as \(W\) is increased past a few \(\mu\text{m}\). Furthermore, as figure 3c shows, on/off ratio of the purified channel material devices remains essentially unchanged as \(L_G\) is scaled to the sub-\(\mu\text{m}\) regime.

**Conclusion**

Devices using the 99.9% purified material exhibit strong semiconducting behavior, not by mitigating the presence of metallic CNTs, but by not having them at all. By using this highly purified material, there is no more tradeoff between drive current and on/off ratio, as was previously observed in devices using 90% and 99% semiconducting solutions as channel material.
Chapter 8

Highly uniform carbon nanotube nanomesh thin film transistors

In the previous two chapters, devices utilizing enriched solutions of semiconducting CNTs demonstrated that one key limiting factor in device performance is the presence of metallic CNTs\(^1\). These metallic CNTs can overlap to create fully metallic pathways in the CNT network, limiting the maximum film density and thus the on-current. This density limitation subsequently results in large device variation. These factors can be mitigated through the use of highly enriched semiconducting CNT solutions. These solutions are both difficult to produce and exhibit reduced performance due to degradation in CNT length caused by secondary and tertiary purification.

In this study, very dense films of semiconducting enriched CNT films are shown to reduce device variability at the expense of semiconducting behavior. By etching these dense films with a mesh structure, direct source to drain percolation pathways are cut\(^2\), inducing longer network pathways around the mesh, reducing the likelihood of a metallic short. By varying the mesh parameters, the device properties can also be tuned in a manner similar to altering the density of a random network film\(^3\), with the distinct advantage that low variability is maintained across the entire range of devices.

Device Fabrication

Again, device fabrication is similar to that previously described. Before CNT deposition, a heavily doped silicon substrate with a 55-nm oxide layer (Si/SiO\(_2\)) is cleaned in an O\(_2\) plasma (30mT, 50W, 1 min.) to make the surface hydrophilic. Next, the cleaned substrate is immersed in a poly-L-lysine solution (0.1% w/v in H\(_2\)O; Sigma Aldrich) to form an amine-terminated adhesion layer, followed by a deionized (DI) H\(_2\)O rinse. Next, samples are incubated in a commercially available solution (0.01 mg/ml) of the 90% semiconducting SWNTs (NanoIntegris Inc.) for 1, 3, and 14 minutes to form dense CNT thin film networks of varying densities. The samples are rinsed with DI H\(_2\)O, followed by isopropanol, and finally blow-dried with nitrogen. After the networks are formed, 30-nm Pd source-drain electrodes are deposited using e-beam evaporation and lift-off. Finally, because the SWNT thin films cover the entire chip, device channel isolation is performed by photolithography and O\(_2\) plasma. In all devices, the gate width (W) and length (L) were fixed at 3 \(\mu\)m and 4 \(\mu\)m, respectively. Electrical tests of the fabricated devices were performed in air at room temperature, with no further passivation or annealing treatments.
Un-patterned thin film transistors

An illustration is presented of an ordinary CNT TFT, before mesh patterning, in figure 1. Randomly deposited CNTs overlap with each other to form CNT-CNT junctions that allow current to percolate from the source to the drain. The heavily doped substrate serves as a back-gate for field effect measurements. Figure 1a presents SEM micrographs of the high-density CNT film formed during a 14-minute deposition. For longer depositions, the density of CNTs saturate as the surface adhesion layer becomes completely covered. This results in a uniform high-density film over the entire substrate, in contrast to films of variable density produced via shorter deposition times (1-3 minutes), as shown in the set of AFM micrographs in figure 1b. Density variations will result in variation of device performance and should be minimized.

Figure 1: Dense CNT films (a) SEM images of the CNT film deposited on the SiO2 surface for a deposition time of 14 min at different locations on the substrate. (b) AFM micrographs comparing density variation for 1 and 3 minute deposition times at various locations on the substrate. (c) Device schematic of a CNT TFT constructed from a 90% semiconducting nanotube solution.

The transfer characteristics of the as-fabricated devices, illustrated in figure 1c, are presented in figure 2. For each CNT film (1 minute (a), 3 minute (b), and 14 minute deposition time (c)) 144 devices were fabricated. As the deposition time, and therefore CNT density, increases the average on-current (I_{ON}), defined at V_G = -10 V and V_D = -0.5 V, increases from 1.08 to 21.4 µA. In contrast, the on/off ratio, I_{ON}/I_{OFF} (the off-state current, I_{OFF}, is defined at V_G = 2 V and V_D = -0.5 V), exhibits the opposite trend, decreasing with increasing CNT density. This occurs because the probability of a totally metallic CNT connection between the source and drain electrodes increases at higher SWNT densities. This is consistent with prior reports\textsuperscript{1,4,5} of an inherent tradeoff between I_{ON} and I_{ON}/I_{OFF}.  

Figure 2: Effect of CNT film density on device performance. Transfer (I_D – V_G) characteristics for each deposition lengths of 1 (a), 3 (b), and 14 min (c), measured at V_D = -0.5 V. (d) Histograms displaying I_ON distribution for each set of devices. In all the devices, the gate width and length were fixed at 3 µm and 4 µm, respectively. More importantly, the distribution of I_ON values is significantly tighter for the high-density devices (Fig. 2d). Due to the statistical nature of the CNT film, variations in I_ON are expected because of variation in the number of connecting paths between the S/D electrodes. Lower density devices, with less connecting paths, are more strongly affected than higher-density networks. In higher-density networks, variation presumably is reduced by the averaging effect². It is worth noting as well the tight distribution in I_OFF, although the presence of metallic CNTs in the enriched solution has reduced the on/off ratio significantly¹.

Nanomesh thin film transistors

Figure 3 CNT nanomesh (a) Device schematic for the CNT nanomesh TFT. (b) SEM image of a nanomesh device. (Inset) AFM image of the nanomesh. The diameter of the holes etched into the CNT film is approximately 50 nm, the pitch between holes is approximately 212 nm.

Next, the channels of the high-density devices were patterned with a periodic two-dimensional mesh array. The devices were first coated with a thin layer of PMMA, in which holes were exposed using e-beam lithography. The pattern was then transferred into the CNT film via an O₂ plasma etch (100W, 30mT, 10s), resulting in a network of holes etched away from the otherwise continuous CNT film. The resultant device is illustrated in figure 3a with accompanying SEM and AFM images that verify the
formation of the mesh channel presenting in figure 3b. In this pattern, 50 nm holes are separated by 212 nm pitch.

Full electrical characterization of nanomesh TFTs is presented in figure 4. Comparing the transfer characteristics in figure 4a and 4b to the unpatterned TFTs, the average on/off ratio is greater than $10^5$, over three orders of magnitude in improvement. This indicates that fully metallic network pathways are effectively eliminated. Additionally, device uniformity is maintained post-patterning because of the high CNT density in the channel. Impressively, $I_{ON}$ ranged within 1uA of the median value (figure 4c), a much tighter distribution than the high performance CNT TFTs presented in the previous chapter$^4$. Output measurements of a single device (figure 4d) demonstrate both saturated behavior and linear response, indicating good ohmic contacts between the metal and CNT film.

![Figure 4](image-url)

**Figure 4 : Electrical characterization of CNT nanomesh TFTs.** Transfer ($I_D - V_G$) characteristics of nanomesh TFTs at $V_D = -0.5$ V in the log (a) and linear (b) scale. (c) Histogram of $I_{ON}$ distribution of the 144 devices. (d) Output ($I_D - V_D$) characteristics of a characteristic device. In all devices, the gate width and length were fixed at 3 µm and 4 µm, respectively

With the best devices, an estimated mobility, $\mu$, of approximately 20 cm$^2$/V•s, while less than the mobilities measured for the highly purified CNT channel material, is still impressive compared to other reported devices using similar CNT channel given their low variability and large on/off ratios$^{5,6}$. Additionally, gate capacitance, estimated using a simple parallel plate configuration, is overestimated due to the presence of the mesh, resulting in an underestimated mobility, which in reality is higher.
Figure 5: Resistance of a nanomesh. (a) Schematic of the thin film resistor with holes. Total resistance of the film can be approximated as the series additions of $R_1$, $R_2$, and $R_3$. (b) Calculated ratio of the resistance change due to hole etching, as a function of mesh pitch.

Despite the improvement in semiconducting performance and reduction in variability, $I_{\text{ON}}$ also exhibits a large drop post patterning. This is either the result of increased channel resistivity, an increase in the number of CNT-CNT junctions necessary to form a percolation network due to the elimination of a direct source to drain path, decreased mobility caused by extra scattering, or a combination of all three. By calculating the sheet resistance, it is possible to determine the proportion of the effect that is simply due to there being less channel material. Presented in figure 5a is a simple model of a nanomesh, with three separate regions defined. The total resistance is simply the sum of the three regions. $R_1$ is the resistance of a narrow strip in between each row of etched holes given as:

$$ R_1 = \frac{\rho L_{\text{total}} - 2rN_1}{t} W_{\text{total}} $$

where $t$ is the thickness of the strip and $N_1$ is the number of components in the film. $R_2$ and $R_3$ are defined:

$$ R_2 = \frac{\rho}{t} \frac{2r}{\int_0^{2r} W(x) dx} \cdot N_2 = \frac{\rho}{t} \frac{2r}{2r \left( 2r W_{\text{total}} - M \pi r^2 \right)} \cdot N_2 $$

$$ R_3 = \frac{\rho}{t} \frac{2r}{2r \left[ 2r W_{\text{total}} - (M - 1) \pi r^2 \right]} \cdot N_3 $$

where $W(x)$ the width of the film in $R_2$ or $R_3$ components, $M$ is the number of holes in $R_2$ components, and $N_2$ and $N_3$ are the number of $R_2$ and $R_3$ components in the film, respectively. The resistivity of each component is assumed to be the same.

Figure 5b presents the calculated increased resistance of a two-dimensional conductor, due to the nanomesh, as a function of hole spacing. For pitches greater than the hole diameter, the change in resistance due merely to removal of conductor is relatively small,
much smaller than the observed reduction in $I_{ON}$ of the fabricated devices. Therefore, it is much more likely that removal of metallic pathways, or increased network lengths are the cause of resistance increase in these devices.

![AFM images of nanomesh network channels of various hole pitch (142, 212, and 354 nm). The diameter of the holes in these nanomesh networks is approximately 50 nm.](a)

![Transfer ($I_D - V_G$) characteristics of the same nanomesh TFTs, measured at $V_D = -0.5$ V. In all the devices, the gate width and length were fixed at 3 µm and 4 µm, respectively.](b)

![Comparison of $I_{ON}$ to $I_{ON}/I_{OFF}$ for each set of patterned CNT TFTs are included for comparison.](c)

**Figure 6: Effect of nanomesh variation on device properties.** (a) AFM images of nanomesh network channels of various hole pitch (142, 212, and 354 nm). The diameter of the holes in these nanomesh networks is approximately 50 nm. (b) Transfer ($I_D - V_G$) characteristics of the same nanomesh TFTs, measured at $V_D = -0.5$ V. In all the devices, the gate width and length were fixed at 3 µm and 4 µm, respectively. (c) Comparison of $I_{ON}$ to $I_{ON}/I_{OFF}$ for each set of. Unpatterned CNT TFTs are included for comparison.

This conclusion is further supported by measurements of devices with varied nanomesh pitch, presented in figure 6. Figure 6a presents dense CNT films etched with three different hole spacing, 142 nm, 212 nm, and 354 nm. Their transfer characteristics are presented in figure 5b, including the unpatterned TFTs for comparison. As expected, reduction in $I_{ON}$ is much greater than is predicted by a purely resistive increase.

Average $I_{ON}$ vs. average on/off ratio, plotted in figure 6c, showing that for the smallest spacing on/off ratios of almost $10^6$ are achievable, at the expense of an approximately 20x reduction in $I_{ON}$. This is due to further reduction of metallic pathways. For the nanomesh with 354 nm spacing, the on/off ratio is increased significantly, but the largest marginal gain in on/off ratio, of over two orders of magnitude, is seen in the 212 nm nanomesh. Correspondingly, further spacing decreases to 142 nm results in less than half an order of magnitude, while $I_{ON}$ begins to drop precipitously. After initially cutting metallic pathways, further scaling only serves to increase the network path length further, and is non-optimal. Comparing the four sets of devices, yet again the trade-off between
$I_{ON}$ and on/off ratio places a limit on device performance, again due to the presence of metallic CNTs.

**Conclusion**

Despite this shortcoming, the advantages of the nanomesh patterned TFTs are numerous. The channel material utilized in this study is relatively easy to procure and can be produced at scale, meaning these CNT TFTs are as low cost as other semiconducting CNT TFTs. While in this study e-beam lithography was employed, it is easy to see that self-assembled materials, like block copolymers, could easily be substituted in during the mesh formation step. The high uniformity of these devices remains unchanged despite varying the nanomesh structure because it does not significantly limit the number of connected pathways in the device$^2$, and mobilities and on-currents already in line with other reported TFTs, even those that utilize highly enriched CNT solutions, make them compelling candidates for adoption in current TFT applications$^{5,6}$. 
Chapter 9

Short channel, solution processed, ballistic, carbon nanotube field effect transistors.

High-temperature growth of CNTs via chemical vapor deposition (CVD) is the most widely employed process used in reported high-performance SWNT devices\textsuperscript{1-3}. Field-effect transistors (FET) utilizing CVD grown CNTs typically possess mobilities ranging from 1,000 to 10,000 cm\textsuperscript{2}/V·s, depending upon CNT diameter\textsuperscript{4}, and conductances that approach the ballistic limit (G = 4e\textsuperscript{2}/h ~ 155 µS)\textsuperscript{2,5}. TFTs with channels of solution-processed CNTs generally exhibit effective mobilities between 20 and 300 cm\textsuperscript{2}/V·s\textsuperscript{6-12}, a figure that is generally taken to imply that solution processed CNTs are inferior to CVD grown CNTs for device applications, despite the fact that these two types of devices operate in the diffusive, and not quasi-ballistic, transport regime. Nevertheless, for short-channel transistors operating in the quasi-ballistic regime, where electron transport is primarily limited by the contacts, transistors made from solution-processed CNTs can be expected to provide high performance, assuming the CNT is relatively defect free within the channel and that metal contacts to these CNTs are of comparable quality to those with CVD CNTs\textsuperscript{12}.

In this chapter, we report 15 nm gate length (L\textsubscript{G}), short-channel, solution-processed CNT transistors in a top-gated structure utilizing a high-\(\kappa\) (ZrO\textsubscript{2}) gate dielectric layer. The objective of this work is to measure the electronic performance of solution-processed CNTs at similar gate lengths to ballistic devices utilizing CVD grown CNTs. These results demonstrate that the performance of scaled solution-processed CNT devices approaches the best p-type devices containing CVD CNT channels.

Experimental Fabrication

The devices presented here are composed of a purified, commercially available 90% semiconducting SWNT solution (0.01 mg/mL, average diameter ranging from 1.2 nm to 1.7 nm, determined by the commercial provider, NanoIntegris Inc.). CNTs were deposited onto a SiO\textsubscript{2} (55 nm)/p\textsuperscript{+}-Si substrate via spin-casting\textsuperscript{7} by spincasting at 7,000 rpm to ensure strong linear alignment and full extension of CNTs. To produce low-density films necessary to fabricate devices on isolated CNTs, 4 µL of solution was pipetted onto the substrate before spinning, in contrast to 200 µL used to create dense semi-aligned CNT arrays previously discussed. For the higher density films used to produce multiple-CNT/channel devices, the volume of solution was increased.
After depositing the solution-processed CNTs, a two-step source/drain (S/D) metallization (optical and e-beam lithography) of Pd separately defined probe pads and short-channel source and drain contacts. Devices were first measured electrically, with no passivation or annealing treatments, and then top-gated with ZrO\textsubscript{2} dielectric film (\(\kappa \sim 12\)), deposited via atomic layer deposition at 130 °C, and an evaporated Ti gate electrode. For single CNT devices, 15 nm of ZrO\textsubscript{2} was deposited, for multiple CNT/channel devices 10 nm was deposited.

![Figure 1: Device Geometry](image)

(a) Schematic of a top-gated solution-processed CNT transistor. A two-step metallization process first defines probe pads, using optical lithography, which are then connected to source and drain contacts separated by a short channel length, patterned via e-beam lithography. (b) Optical image of such devices fabricated on the chip.

A schematic of the final device structure with top-gate is shown in Figure 1a. The \(L_G\) of the bottom-gated device is the defined by the source-drain gap. The \(L_G\) of this top-gated structure is defined not by the distance between the S/D electrodes, but the gate electrode. The difference in the top- and back-gate \(L_G\) arises from the narrowing of the top-gated channel region by twice the thickness of the ALD dielectric layer, which grows laterally on the source and drain sidewalls in addition to growing vertically on the substrate. Note that our top-gated device differs from self-aligned CNT transistors\(^{14}\) in that this device has un-gated underlap regions on two sides of the S/D electrodes. Figure 1b shows a microscopic image of the fabricated top-gated transistors.

**Bottom-gated device measurements**

Representative transfer characteristics for a bottom-gated, 270 nm \(L_G\), FET at source-drain bias \(V_D = -0.5\) V are shown in Figure 2a. The on/off ratio, \(I_{ON}/I_{OFF}\), is in excess of \(10^6\) with an off-current, \(I_{OFF} = -36\) fA, (defined at the gate bias at which the drain current is minimal) and on-current, \(I_{ON} = -2.4\) \(\mu\)A (defined at \(V_G = -8\) V and \(V_D = -0.5\) V). AFM measurements (figure 2a, inset) confirm the channel of this device consists of a single CNT. Approximately 50 % of the devices characterized via AFM contained a single CNT within its channel (Figure 2b). No device contained more than 5 CNTs.

Figure 2c plots \(I_{ON}\) vs. the number of CNTs for the same set of devices. Note that some devices were excluded from this data set because one or more of the CNTs in their
channels were metallic. When packing numerous SWNTs into a device, $I_{\text{ON}}$ is often hampered by charge screening\textsuperscript{15}. Such screening is part of the reason why dense thin film transistors from solution-processed CNTs exhibit lower-than-anticipated on-currents\textsuperscript{6}. However, the modest CNT densities of these devices provide an excellent opportunity to observe direct current scaling. The trend in current seen in these devices demonstrates linear on-scaling for these low density devices, similar to previous reports for CVD CNTs\textsuperscript{16}, suggesting that previously reported devices suffered not from inferior CNTs, but from electrostatic effects not observable in low density CVD CNT arrays. Variation from the trend line can be ascribed to variation in CNT diameter, resulting in different band gaps and, thus, Schottky-barriers height at the contact. Ideally, further work in solution processing will tighten CNT diameter distribution and reduce device-to-device variability. This result also demonstrates a method for distributing solution deposited CNTs evenly.

**Figure 2:** Electrical characterization of bottom-gated solution-processed CNT FETs with $L_G = 270$ nm. (a) Transfer characteristics of a representative device at $V_D = -0.5$ V. (Inset) AFM image of the device. (b) Distribution CNTs per device channel for 4 µL CNT solution deposited at 7,000 rpm. (c) $I_{\text{ON}}$ versus the number of CNTs/channel under the same bias conditions ($V_G = -8$ V and $V_D = -0.5$ V).

**Top-gated device measurements**

Devices were then top-gated with 15 nm of ZrO$_2$, as previously described, and re-measured. The back-gate bias was floated in all subsequent measurements. Figure 3a shows the representative transfer characteristics of an as-fabricated, top-gated, 240 nm $L_G$, single CNT device in air at room temperature, with no further passivation or annealing treatments. Both the subthreshold swing and the transconductance drastically improve over the bottom-gated device because of the thinner, high-$\kappa$ gate dielectric of the top-gate. $I_{\text{ON}}$, however, did not significantly change for the device as-made (Figure 3a). Oxygen exposure (230 mT for 50 min, referred to as ‘oxygen doping’ ) substantially improved $I_{\text{ON}}$ (Figure 3b), resulting in a transconductance ($g_m = dI_d/dV_G|_{V_D}$) of 8.6 µS and $I_{\text{ON}} = -6.6$ µA (defined at $V_G = -2$ V and $V_D = -0.5$ V), almost three times higher than the bottom-gated measurement. The subthreshold swing, approximately 130 mV/decade and $I_{\text{OFF}}$ was relatively gate bias-independent (for $V_D = -0.1$ V to -0.5 V). The $I_{\text{ON}}/I_{\text{OFF}}$ remained constant at $\sim 10^5$. 

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Figure 3. Electrical characterization of a top-gated, single CNT device with \( L_G = 240 \) nm and 15 nm ZrO\(_2\) gate dielectric (EOT \( \approx 4.9 \) nm). Transfer characteristics for the as-made device (a) and after oxygen doping (b). The gate dielectric was used as a gate dielectric. (c) Linear transfer characteristics of the device before and after oxygen doping (red: as-made, blue: after oxygen doping). The black dotted lines serve as a visual guide for \( g_m \). (d) The calculated Y-function and 2\( R_C \) (inset) as a function of \( V_G \) (red: as-made, blue: after oxygen doping). The black dotted lines represent the linear fit estimating mobility.

The effect of oxygen on the electrical properties of the CNT devices has been reported previously\(^{17}\). Y-function analysis provides a framework to obtain contact resistance \( (R_C) \) and mobility \( (\mu_{FE}) \) values from transfer measurements\(^{12,18}\), providing insight into the physical origin of oxygen’s effect on the conductance modulation observed in these devices. The Y-function is defined as follows:

\[
Y = \frac{I_D}{g_m^{1/2}} \left( \frac{W}{L} C_{ox} \mu_{FE} V_D \right)^{1/2} \left( V_G - V_T \right) = \left( \frac{1}{L^2} C_G \mu_{FE} V_D \right)^{1/2} \left( V_G - V_T \right)
\]  

(1)

where \( \mu_{FE} \) is derived from the slope of Y versus \( V_G \), with the intrinsic \( V_T \) is directly identified by the x-axis intercept. From the known \( \mu_{FE} \) and \( V_T \), \( R_C \) can be acquired with the following equation:

\[
2R_C = \frac{V_G}{I_D} - R_{ch} = \frac{V_G}{I_D} - \frac{L_G^2}{\mu_{FE} C_G (V_G - V_T)}
\]

(2)
Linear-scale transfer curves of the device, before and after oxygen doping, are combined in Figure 3c. The two measurements yield very different $g_m$, which results in differing slopes. The Y-function plot (Figure 3d). However, reveals that the two devices have nearly identical $\mu_{FE}$ values of ~ 380 cm$^2$/V·s, as indicated by their similar slopes. This value is lower than the average $\mu_{FE}$ of CVD, single CNT, sub-µm devices, which is typically in the range of 1,500 – 3,000 cm$^2$/V·s$^{19-22}$. These results indicate that relative to CVD CNTs, solution-processed CNTs may possess some structural defects induced during the suspension and/or purification processes, limiting $\mu_{FE}$.

While the $\mu_{FE}$ of the device remained unchanged after oxygen doping, the $R_C$ of the oxygen-doped device are significantly lower than that of the as-made device. The inset of Figure 3d presents the calculated $2R_c$, as a function of $V_G$, according to eq. (2). Note that the contact resistance of the oxygen doped device ($2R_c = 20 – 34$ kΩ) are similar to those reported in previous studies of CVD CNTs$^{20,23}$. Therefore, solution-processed CNTs should perform similarly to CVD CNTs in scaled FETs, where the channel becomes transparent due to ballistic transport. The slightly higher $2R_c$ in this work, compared to the best-reported CVD CNT devices, is possibly due to residual surfactants on the CNT surface.

![Figure 3c](image)

**Figure 3c.** Linear-scale transfer curves of the device, before and after oxygen doping, are combined in Figure 3c. The two measurements yield very different $g_m$, which results in differing slopes. The Y-function plot (Figure 3d). However, reveals that the two devices have nearly identical $\mu_{FE}$ values of ~ 380 cm$^2$/V·s, as indicated by their similar slopes.

![Figure 4](image)

**Figure 4.** Short-channel devices with a single solution-processed CNT. In these devices, 10 nm ZrO$_2$ (EOT $\approx$ 3.2 nm) was used as the gate dielectric. (a) Top-view SEM images of two devices ($L_G = 15$ and 45 nm). (b) Transfer characteristics for a device with $L_G=15$ nm. (c) Output characteristics of the same device. (d) Output characteristics of a 15 nm, 45 nm, and 300 nm device at the same gate overdrive voltage ($|V_G-V_T| = 1.0$ V).

The physical process responsible for the change in device performance is well known. Exposure to oxygen results in an increase in Pd work-function that modifies the Schottky barrier at the metal-semiconductor interface and allows for more efficient carrier injection$^{24}$. Further supporting this conclusion, oxygen doping consistently results in a shift in $I_D-V_G$ curves toward a more positive $V_G$, indicating additional hole-doping in the CNT body. It is likely that oxygen molecules desorb from the CNT/contacts during ALD processing due to the high process temperature (130 °C) and low-pressure vacuum. Although these devices are capped with ZrO$_2$ dielectric layers, apparently these layers are permeable enough to allow oxygen molecules to escape from and penetrate into the device to some extent. Exposure to oxygen molecules in air itself is insufficient to reintroduce oxygen to the devices, as shown in Figure 3a. Oxygen doping, however, produces reliable improvement in these devices. Subsequent devices are oxygen doped post-fabrication.
To determine the scaling behavior of the solution-processed CNTs, top-gated devices with 15 nm, 45 nm, and 300 nm $L_G$ were fabricated, with gate lengths verified via SEM (figure 4a). For these devices, the ZrO2 dielectric layer was also reduced to 10 nm, an equivalent oxide thickness (EOT) of approximately 3.2 nm, to improve electrostatics at short channel lengths. Top-view SEM images of 15 and 45 nm $L_G$ devices are shown in Figure 4a. Transfer and output characteristics of a representative 15 nm $L_G$ device are shown in figures 4b and 4c. This device exhibited a high peak transconductance of 32 $\mu$S, $I_{ON}/I_{OFF} > 10^4$ at $V_D = -0.5$ V, and a subthreshold swing of $\sim 130$ mV/decade. Notably, its saturation current reached 17 $\mu$A at $|V_G - V_T| = 1.0$ V.

As seen in Figure 4d, the saturation current significantly improves as $L_G$ is scaled from 300 nm down to 45 nm. This is due to reduction of scattering within the channel due to scaling $L_G$ below the average linear defect density of solution-processed CNTs. Further scaling down to 15 nm does not significantly increase conductance, suggesting that these devices have nearly reached the ballistic transport limit. These devices are significantly better than previously reported solution-processed CNT transistors\textsuperscript{11,12,25}. Additionally, output response in the linear regime is essentially unchanged between the 15 nm and 45 nm $L_G$ devices, indicating that at low fields, scattering in the channel plays a negligible role in device performance. This is evidence of ballistic transport consistent with previous reports on CVD CNTs.\textsuperscript{14,20} The higher subthreshold slope, lower saturation current, and lower transconductance values of these devices, compared to the CVD CNT devices is not due to lower quality CNTs, but instead due to a thicker EOT and subsequent worse electrostatics.

Multiple CNT/channel scaled devices were also fabricated separately as part of this study. Increasing the volume of CNT solution deposited from 4 to 6 $\mu$L resulted in denser CNT films. From test structure AFM measurements, the average number of CNTs inside a device channel with 2 $\mu$m width is estimated as 3–4 (figure 5a, inset). These devices also used 10 nm of ZrO2 as the gate dielectric. Figure 5 panels a, b, and c present the transfer characteristics of 15, 45, and 65 nm $L_G$ devices with multiple CNT/channel, respectively. The $I_{ON}/I_{OFF}$ ratio for the 15 nm $L_G$ device is larger than $10^4$ at $V_D = -0.1$ V.
and larger than $10^3$ at $V_D = -0.5$ V. Moreover, for the 15 nm $L_G$ device, $g_m = 73 \, \mu S$. This device also exhibits current saturation around $V_D = -0.35$ V at $|V_G - V_T| = 1.5$ (figure 5d) indicating good electrostatic control, free of short channel effects. The slight increase in minimum current as $L_G$ decreases, primarily the result of back-injection of carriers into the conduction band from the drain, slightly increased subthreshold values, and $V_T$ roll-up for decreasing $L_G$ should be attributed to the somewhat thicker than optimal gate dielectric layer and may be addressed with a thinner EOT. Note that the $I_{ON}$ levels for the two set of devices that have $L_G \leq 45$ nm are almost identical ($\langle I_{ON} \rangle = 60 \, \mu A$ for 15 nm $L_G$ devices, $\langle I_{ON} \rangle = 61 \, \mu A$ for 45 nm $L_G$ devices, and $\langle I_{ON} \rangle = 36 \, \mu A$ for 65 nm $L_G$ devices at $|V_G - V_T| = 1.5$ V).

**Conclusion**

These measurements together indicate that indeed structural defects in solution processed CNTs, the result of suspension of purification processes, can act as localized electron-scattering centers and result in degraded electrical performance, relative to CVD grown CNTs. However, they do not significantly affect the quality of the contact between the CNT and metal electrodes. For devices shorter than the average defect density, these impurities become negligible, enabling devices consisting of solution-processed CNTs to perform comparably to devices that utilize CVD grown CNT channels.
Chapter 10

Bottom-up, Graphene Nanoribbon Field-Effect Transistors.

Graphene nanoribbons (GNRs) have been extensively investigated as a promising material for use in high performance, nanoelectronic, spintronic, and optoelectronic devices due to their unique physical properties\(^1\text{-}^{11}\). These properties, however, are critically determined by the precise geometry of the GNR and are degraded by rough edges. Bottom-up, chemical synthesis has been shown to produce GNRs *en masse* that, unlike GNRs previously studied, possess uniform width and precise edge structure\(^12\). Previously, the electronic structure of chemically synthesized GNRs has been studied on their Au growth substrate through Raman, photoemission and tunneling spectroscopy\(^12\text{-}^{17}\), but their short length and the metallic growth substrate has thus far prevented standard electronic device fabrication and transport measurements. Here we report layer transfer of chemically synthesized, atomically precise GNRs, enabling study of their physical properties regardless of substrate. Further, we demonstrate short channel field-effect transistors based on this material and report unique transport behavior characteristic of these extremely narrow, large band-gap GNRs.

Growth of GNRs, as previously reported\(^12\), occurs via a two step process in which the molecular precursor, 10,10'-dibromo-9,9'-bianthryl (DBBA) is thermally sublimed in ultrahigh vacuum (UHV) onto Au(111), where it is converted into a polymer chain. Thermal cleavage of the labile C–Br bonds induces a radical step growth polymerization to yield polymeric GNR precursors. Annealing these polymers on the surface leads to a stepwise cyclization/dehydrogenation sequence yielding fully conjugated GNRs with atomically defined armchair edges. GNRs synthesized with DBBA are exactly 7 carbon atoms across \((n=7, \ w=7.4 \ \text{Å})\) with a band gap on Au(111) of approximately 2.5 eV\(^13\text{-}^{15},^{18}\).

**Film transfer and Device Fabrication**

Synthesis takes place on the crystalline terraces of clean epitaxial Au films pre-deposited on cleaved mica substrates. Device fabrication requires the transfer of GNRs to an insulating substrate. Previously, transfer of these GNRs onto SiO\(_2\) was reported through mechanical contact of the growth and transfer substrate\(^12\), however, we found this method to be irreproducible. We have developed a reliable method of full layer transfer, illustrated in figure 1a and 1b. First, poly-methyl methacrylate (PMMA) is spun-cast onto the GNRs and baked \((180^\circ\text{C, 10 min.})\) forming a PMMA/GNR/Au/Mica stack. The stack is then floated on concentrated HF (40% wt.) and occasionally agitated, which induces the mica substrate to delaminate from the Au growth layer. The PMMA/GNR/Au film is
then rinsed twice in water and transferred to Au etchant. Finally, the PMMA/GNR film is rinsed twice again and drawn onto the target substrate surface, 50 nm thick SiO$_2$ thermally grown on heavily doped silicon in this study. Once the film is adhered to the substrate, it is baked (50°C for 5 min. followed by 100°C for 5 min.) to remove residual water and stripped of PMMA with acetone, leaving GNRs on an insulating surface.

Raman Spectroscopy performed on samples pre- and post-transfer verifies ribbon integrity is maintained throughout the transfer and device fabrication processes (figure 1c), confirmed by preservation of the radial breathing like mode (398 cm$^{-1}$) characteristic for n=7 GNRs. An observed increase in the D peak intensity (1343 cm$^{-1}$) and slight overall line-width broadening may be the result of reduced substrate screening effects or defects induced during transfer. This transfer process is also compatible with any substrate resistant to organic solvents such as acetone.

Next, three terminal transistor devices were fabricated (figure 2a). While our GNRs can be as long as 30-40nm, the average length is 10-15nm and so very short physical channel lengths are necessary to contact ribbons at both the source and drain. Therefore, to measure individual ribbons, a large array of source and drain contacts with nano-scale gaps, 100nm wide, were defined using e-beam lithography. First, probe pads (Pd 30nm thick) were fabricated via standard liftoff processing using optical lithography and e-beam evaporation. PMMA (1% wt. 950K M$_w$, 4krpm spin, 180°C bake for 10 min.) was exposed and developed at -4°C in a 7:3 H$_2$O:IPA co-solvent solution to pattern individual source/drain contacts. Pd (10nm thick) was again evaporated and lifted off in acetone. 300 devices were fabricated in total.

**Figure 1: Growth and Transfer of GNRs.** (a) Room-temperature STM image of n=7 armchair GNRs on their Au growth substrate, tunneling current $I_t$=0.10 nA, sample bias $V_s$=1.67 V. Inset: high resolution image of n=7 GNR acquired with a low-temperature STM (T=7K, $I_t$=0.26 nA, $V_s$=−0.40 V). A structural model of the GNR is overlaid on the STM image. For full details regarding STM characterization see ref. 18. (b) Illustration of transfer process. The PMMA/GNR/Au/Mica stack is first floated on HF to delaminate the mica substrate. It is then rinsed and placed on Au etchant to dissolve the catalyst layer. It is then rinsed again and pulled onto the target substrate. (c) Raman spectra of GNRs on growth substrate, after transfer on SiO$_2$, and after device fabrication (532nm excitation wavelength). Peaks characteristic of n=7 GNRs are labeled for reference.
Figure 2: Device Fabrication and Environmental Behavior  (a) Schematic illustrating device geometry. Because small channel lengths are necessary, a Pd layer forming source and drain contacts to the GNR, using e-beam lithography, is connected to optically defined Pd contact pads. The GNR spans both contacts with some overlap region, \( L_C \), between the GNR and contact. Below: Scanning electron micrograph (1keV EHT) of the device presented in fig. 3, 100nm wide with a 26nm source drain gap. (b) Electrical characterization of a typical device at \( V_{SD}=1 \)V in both air and under vacuum at 77K.

Electrical Characterization

Devices were first screened in air and then characterized in a cryogenic probe station. Devices with patterned source-drain gaps greater than 30nm do not show any conductance, implying that possible inter-ribbon charge transfer between any overlapping ribbons is negligible and that single GNRs did not directly bridge any source-drain gaps this wide. Several devices with smaller gaps between 20-30nm (14 out of 300 devices with source-drain gaps ranging 20-40nm) exhibit gate-modulated conductance with on-currents ranging from tens of pA to a few nA at 1V source-drain bias, \( V_{SD} \). Because ribbon orientation and position is random, the actual channel length and number of ribbons in each individual device is uncertain. We estimate that in each device there are zero to two GNRs long enough to potentially contact both the source and drain; GNR density is approximately \( 2 \times 10^4/\mu m^2 \) with less than 4% of ribbons longer than 30nm. Device yield is expected to increase significantly by further reducing the source-drain gap and/or increasing ribbon length during synthesis.

Figure 2b presents electrical characterization of a typical GNR transistor measured in ambient conditions (red) and under vacuum at 77K (blue). When measured in air, GNRs contacted with Pd exhibit p-type conduction. Immediately post-fabrication, transistors exhibit large random conductance variations and variable hysteresis due to adsorbed oxygen, water, and residual PMMA on the contact and GNR\textsuperscript{20,21}. Once annealed in vacuum (300°C, \( 3 \times 10^{-7} \) Torr, followed by a 80°C, \( 1 \times 10^{-6} \) Torr anneal in the probe station pre-measurement), device behavior switches to n-type conduction, caused by reduction of the contact metal work function due to molecular desorption\textsuperscript{22}, while hysteresis is also greatly reduced by desorption from the channel. About half of devices still display
hysteretic ambipolar behavior after vacuum annealing or re-exposure to ambient conditions. Further passivation with a hydrophobic monolayer, hexamethyldisilazane (HMDS), was found to nearly eliminate hysteresis and fully switch device polarity in all devices. Small residual hysteresis effects are attributed to trapped charges within the relatively thick back-gate dielectric and not from molecular adsorbates on the contact or channel\textsuperscript{23}.

Transport is largely dominated by the Schottky junction contacts. Full polarity switching through small shifts in contact work function\textsuperscript{24}, relative to the GNR’s \(\sim 2.5\) eV band-gap, suggests that band alignment of the Pd Fermi level falls close to mid-band-gap, a conclusion in agreement with simulations of \(n=7\) GNR/Pd interfaces\textsuperscript{25}. Previously published experiments measuring the electrical characteristics of unzipped, chiral Pd contacted GNR transistors 2-20nm wide, derived from CNTs through sonochemical induced ripping, demonstrate the presence of a relatively small Schottky barrier at the metal-GNR interface\textsuperscript{5,7}. We see much larger Schottky barriers, potentially as large as 1.25 eV, due to the increased band-gap of the much narrower (7.4 Å) GNRs.

Figure 3 presents full transport characterization of another typical device, with 26nm source-drain gap, as a function of back gate modulation (figure 3a) and source-drain bias (figure 3b). High series resistance is also presumed to limit on-current in our GNR devices due to the short contact overlap length (\(L_C\)) between the GNR and the source and drain. Even with our very short channel gaps, \(L_C\) is no more than a few to perhaps 10 nm long depending on GNR length and alignment. Conventional graphene and CNT transistors show large resistance increases as \(L_C\) is decreased past the electron mean free path (\(\sim 200\)nm)\textsuperscript{26,27}, suggesting very low transmission probabilities in short contacts for our smooth edged GNRs with low scattering. Despite this, we still see a large measurement limited on-off ratio of \(3.6 \times 10^3\) at \(V_{SD} = 1\) V, clearly demonstrating semiconducting transport in chemically synthesized GNRs.

![Figure 3: Electrical Characterization of a typical device post passivation, under vacuum, at 77K. (a) drain-current response with respect to gate voltage, \(I_D-V_G\), at different source drain bias, \(V_{SD}\), and (b) drain-current response with respect to drain voltage, \(I_D-V_D\), of same device at different gate bias, \(V_G\), inset: The same data presented in logarithmic scale.](image-url)
The observed device behavior is typical of a short channel Schottky barrier device. In the off-state, leakage is caused by holes tunneling through the drain barrier, which is therefore relatively temperature independent but strongly dependent on $V_{SD}$, as larger biases will narrow the width of the Schottky barrier substantially. Also strongly dependent on $V_{SD}$ is the threshold voltage ($V_T$) for turn-on, becoming negative for $V_{SD}>1$V, due to the strong coupling of the channel to the drain that the gate has to counteract for the device to remain off. The large electric field between the source and drain when the devices are gated on or aggressively biased is sufficient to induce tunneling through the barriers, causing field emission to dominate current flow. This results in unsaturated, nearly exponentially increasing on-current (figure 3b, inset), even at large $V_{SD}$, as the barrier continues to narrow and tunneling increases. From this, we can conclude that the resistance of the GNR channel is much lower than the Schottky barrier series resistance, but intrinsic GNR transport properties cannot be observed until these extrinsic factors are ameliorated.

Lowering of the contact work function would reduce the source conduction band barrier height and correspondingly increase the drain valence band barrier, resulting in both improved on- and off-state performance. Further improvement in band alignment should also arise through the use of wider GNRs such as those recently synthesized via similar methods with 1.4nm width and ~1.4eV band-gap. These are expected to show improved characteristics in a given device due to smaller Schottky barriers and lower effective mass that result from their smaller band-gap. Longer GNRs, through growth optimization, may also reduce contact resistance by increasing $L_C$.

The narrow width, chemically synthesized GNRs studied here appear to be more sensitive to their environment compared to graphene, CNTs, or significantly wider GNRs previously studied, possibly a consequence of a higher proportion of the exposed, current carrying edge region, relative to the chemically inert surface. Sensors with greater sensitivity than seen with graphene or CNTs might be achieved through GNR edge modification. Similarly, artificially induced edge states in graphene have been shown to be beneficial to graphene-metal contacts and may also be engineered to enhance GNR-metal electronic coupling. Electronic behavior might also be adjusted through local environment and edge modification in addition to precursor selection during synthesis.

**Conclusion**

By developing a method for layer transfer of chemically synthesized GNRs we have gained the ability to directly study, using techniques previously unavailable, the behavior of this bottom-up engineered, self-assembled electronic material. In addition to electronic transport measurements, other experiments using chemically synthesized GNRs are also now possible, including optoelectronic and spintronic studies, optical fluorescence measurements, or transmission electron microscopy of freestanding GNRs suspended over patterned membranes. This work highlights the materials development path toward future electronic devices with low series resistance and high intrinsic mobility expected of chemically synthesized GNRs with atomically smooth edges.
Chapter 11

Conclusion & Further Work

The work presented in this dissertation represents a concerted effort to advance the field of CNT electronics by developing processing techniques to address current limitations in solution-processed CNT devices, analyzing device performance as a function of semiconducting enrichment, and demonstrating unexpected electronic properties at short channel lengths. However, the field is by no means mature. Future work analyzing aligned arrays and short-channel devices with highly purified CNT channels will yield more information about device yield, variability, and device performance. This is achievable through the use of localized and linear deposition techniques. Furthermore, analysis of nanomesh devices with respect to film purity may show that fully unpurified CNT films may be sufficient to produce high performance, low variability devices when patterned.

Additionally, demonstration of electronic transport in chemically synthesized GNRs is the first step in developing new types of devices through bottom-up approaches. Because of their chemical nature, a menagerie of synthesizable GNRs has been developed since this work, with more being discovered every day. Electrical characterization of these materials will help develop a more robust understanding of their chemical and physical properties. This initial study has demonstrated that improving GNR-metal contact is critical to improved device performance, which is itself a complete area of study. Open questions as to the predicted and actual band-gap of these materials when in contact with insulating substrates should also be investigated through optical and electron transport measurement. Finally, polymeric growth processes may soon produce integrated molecular junctions within GNRs themselves; placement, alignment, and characterization of these junctions may form the basis of fully bottom-up integrated circuitry.

Each answer begets three more questions; the opportunities for further research based on these experiments are limitless.
References

Chapter 1

(11) Радушкевич, Л. В. О Строительстве Углерода, Образующегося При Термическом Разложении Окиси Углерода На Железном Контакте *1954*, 26, 88–95.
Chapter 2


Chapter 3


Chapter 4

(6) Cicoria, R.; Sun, Y. Nanotechnology 2008, 19, 485303.


**Chapter 5**


**Chapter 6**


**Chapter 7**


(7) Pimparkar, N.; Cao, Q.; Rogers, J. A.; Alam, M. A. *Nano Research* 2010, 2, 167–175.


**Chapter 8**


(2) Pimparkar, N.; Cao, Q.; Rogers, J. A.; Alam, M. A. *Nano Research* 2010, 2, 167–175.


Letters 2009, 9, 4285–4291.


Chapter 9


Chapter 10

(19) Jorio, A.; Fantini, C.; Dantas, M. S.; Pimenta, M. A.; Souza Filho, A. G.


