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Formation and Electrical Properties of
Solid State Nickel Disilicide Nanowires

A thesis submitted in partial satisfaction of the requirements for the degree of Master of Science in Materials Science and Engineering

by

Ya-Hsuan Chuang

2015
ABSTRACT OF THE THESIS

Formation and Electrical Properties of Solid State Nickel Disilicide Nanowires

by

Ya-Hsuan Chuang

Master of Science in Materials Science and Engineering
University of California, Los Angeles, 2015
Professor Yu Huang, Chair

In my research, there are two structures for silicidation by solid state reaction. The lateral structures and full coverage of NWs are utilized to study the formation and electrical properties of NiSi$_2$ NWs. By the lateral structure, we can know that NiSi$_2$ wins as the first phase, but the length of NiSi$_2$ is not long enough for electrical measurements. Therefore, a new structure is adopted for create long and pristine NiSi$_2$ NWs. Ni is global deposited onto the top of Si NWs, and an ALD Al$_2$O$_3$ shell is applied to confine the expansion of NWs during phase transformation. The thicker nickel film can provide more Ni source on all the
NWs, and thicker of oxide film can increase the compressive stress and confine the volume expansion during annealing process. The thickness of Ni and Al_2O_3 as well as the annealing temperature has been studied in this research. The long and pristine NiSi_2 NW can be formed successfully in a Si NW with 15 nm Ni and a 29 nm Al_2O_3 shell at 650 °C for annealing 30 min. The four terminal resistivity of a 52 nm NiSi_2 NW is 39.2 µΩ-cm, and the current density is 2.6×10^7 A/cm^2.
The thesis of Ya-Hsuan Chuang is approved

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2015
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In the semiconductor technology, the size of device shrinks by the time. When the size scales down, the response time, total power and cost can be decreased. Under Moore’s law, the semiconductor components have been scaled-down in every two years, but IC technology is approaching the limit on Moore’s law, such as the physical limits of photolithography, non-scalability of the MOS transistor, and so on.\textsuperscript{1,2} In interconnects, the problem as RC delay as well as electromigration also appear in the semiconductor manufacturing. Nowadays, the material of interconnects changes from aluminium (Al) to copper (Cu) because of low resistivity, and the inter-layer dielectric (ILD) layer utilizes low-κ material rather than the silicate glass. However, when the scale shrinks, the RC delay issue needs to be taking into consideration. Moreover, although Cu is widely utilized as interconnect material in integrated circuits, the increasing resistivity with size scaling has become an issue. Another problem of copper wire is electromigration when current density exceeds $10^6 \text{ A/cm}^2$.\textsuperscript{3,4} Therefore, the transition metal silicide can be a potential alternative in the semiconductor technology.

There are amounts of advantages of the metal silicide, including the low
resistivity, good ohmic contacts with p- and n-type semiconductors, high-thermal stability, and low cost. Most importantly, silicide is compatible with the Si device, and the direct transformation from Si to silicide can eliminate the fabricating processes. Additionally, in the nanoscale region, nanowires (NWs) have attracted considerable attention as one-dimensional (1-D) structures with high surface to volume ratio, and the 1D carrier transport to reduce phonon scattering. 1-D nanomaterials can be built into nanodevice successfully demonstrated in many electronic, photonic, and other functional devices.

Form the advantages of metal silicide and NWs discussing above, the metal silicide NW is a significant candidate in semiconductor technology, and especially in nanoscale interconnects. The bottom-up molecular technology can make silicide NWs with perfect surface unlike etched structure, and eliminate the number of processes.

The synthesis approaches to nanoscale silicides can be divided into three methods, endotaxy, chemical vapor deposition (CVD), and solid state reaction. The endotaxy means that the metal is deposited onto a heated Si substrate, and reacted with the substrate to form self-assembled silicide nanostructures. The method is direct and effective, but there is no effective method to control the growth length, diameter, and position of NWs. For the CVD methods, the transition metal source and silicon
are delivered simultaneous to the substrate, and reacted to grow as metal silicide. The reaction condition needs to be controlled strictly, such as the temperature zone, growth pressure, flow rate, and so on.\textsuperscript{10} The last method, solid state reaction, is the most controlled one. The metal is deposited as a thin film on tip of Si NWs, and diffuses into Si to form metal silicide by annealing process. By photolithography patterning and annealing period control, the epitaxial interface of silicide/Si heterostructures can be formed. The nanoheterostructure serves as an ideal electrical contact materials to the source, drain, and gate.\textsuperscript{11}

A resistivity study of nanowire and silicide phases is important to understand the fundamental electrical properties of silicides at low dimensions and to identify the best candidate for future interconnects. There are lots of transition metals, such as Ni, Co, Ti, Ta. In my research, nickel works as the candidate for discussing the formation and electrical properties of nickel silicides. Nowadays, NiSi is the most promising phase with its low resistivity and appropriate work function among nickel silicides. In 2004, Wu et al. reported the 29 nm NiSi with great resistivity down to 9.5 $\mu\Omega$-cm, and the high failure current density shows as $3 \times 10^8$ Acm$^{-2}$.\textsuperscript{12} Besides, there are some limitations other silicides, such as CoSi$_2$ and TiSi$_2$. The applicable line of TiSi$_2$ and CoSi$_2$ is over 90 and 50 nm, and the Si consumption or titanium silicide is 1.04 that is larger than the other materials. The formation temperatures are both higher than
Talking about the nickel silicide, there are totally seven phases, including NiSi, Ni$_3$Si, Ni$_{31}$Si$_{12}$, $\theta$-Ni$_2$Si, $\delta$-Ni$_2$Si, Ni$_5$Si$_2$ and NiSi$_2$. In all these phases, NiSi has the lowest resistivity about 9.5–18 $\mu$Ω-cm. For the crystal structure, NiSi$_2$ (space group 225, Fm3m, $a=5.416$ Å) has similar cubic structure with Si (space group 227, Fd3m, $a=5.43$ Å), and volume per Si atom of NiSi$_2$ and Si is almost the same as 19.75 Å$^3$ and 20.01 Å$^3$, respectively. For nanosize device, the volume expansion problem is significant, so NiSi$_2$ is a potential candidate.

In this research, it focuses on the formation and electrical properties of solid state NiSi$_2$ nanowires. Two different Ni and Si couple structure will be discussed, and also the growth conditions, such as the temperature and period for phase transformation, the thickness of Ni source. The electrical properties of long and pristine NiSi$_2$ NW are also measured.
Chapter II: Si NW Template Synthesis and Sample Preparation

2.1 Growth of Si NWs

For the growth of Si NWs, the catalysts are important for controlling the size and diameter of Si NWs. In our experiment, the Au nanoparticles are chosen as nanocatalysts which are prepared from the 1-10 nm sputtered Au film. After annealing at 550 °C, the Au sputtered film dissociates and reforms Au nanoparticles. Thus, the thickness of sputtered Au film and annealing time determine the size of Au nanoparticles. In the synthesis of Si NWs, the ordinary method is so called as vapor-liquid-solid (VLS) method with Au nanocatalysts as shown in Figure 2.1. The Si is supplied from the decomposition of SiH₄ under forming gas (95% N₂ and 5% H₂) at 450-550 °C for 10-40 min and cool down to room temperature in the furnace. The pristine Si NW of high resolution transmission electron microscopy (HRTEM) image is shown in Figure 2.2 (a), and Figure 2.2 (b) shows the diffraction pattern of [110] NW.
2.2 Preparation of TEM Membrane

In order to perform silicide process and to characterize the NWs under TEM, the TEM membrane should be prepared. The membrane with thin electron transparent silicon nitride windows provides a sample support that have the advantages of being chemically and mechanically strong insistence and can withstand temperature changes.
up to 1000 °C. In addition, TEM membranes are extremely stable and suitable to conduct a variety of nanotechnology experiments on the support films. The process flow of fabrication of TEM membrane is shown in Figure 2. Firstly, the <100> Si wafers rinse with buffer oxide etch (BOE) solution for few seconds and then wash by DI water in order to get rid of the native oxide. (Figure 2. (a)) Then, a 40 nm thick low stressed Si nitride is deposited on both side of Si wafers in a low pressure chemical vapor deposition (LPCVD) chamber at 550~650 °C for 10 min. (Figure 2. (b)). NH₃ and SiCl₂H₂ are used as precursors to form Si nitride thin film. After the nitride deposition, different sizes of windows are patterned on the backside of Si wafers through photolithography as shown in Figure 2.3 (c). The areas of windows as 100×100 µm, 300×300 µm, or 500×500 µm are exposed without photoresist covered, and then etched by reactive ion etcher (RIE) which presented in Figure 2.3 (d). Remove the photoresist by acetone clean, and the remaining silicon nitride film at back side works as hard mask when the wafer is etched by 35% potassium hydroxide (KOH) at 80 °C for hours.

The anisotropy etching of Si faces in KOH solution, the {111} facets remains as the slowest one to form as a wedge structure at the sides of the windows as shown in Figure 2.3(e). Then, the structure is rinsed by water to get rid of the remaining chemicals. The low stress Si nitrides film can work as the mechanical supporting
substrate for TEM observations, and the thickness of Si nitrite membrane is approximately 40 nm.

![Diagram](attachment:image.png)

Figure 2.3 Process flow of fabrication of TEM membrane. (a) Si substrate. (b) Si nitride deposited by LPCVD. (c) Photoresist patterned. (d) RIE etching. (e) Sample etched by the KOH solution, and the suspended Si nitride film can be the support membrane.

### 2.3 Preparation of Nickel / Si NW Diffusion Couple

The diffusion couples of nickel and Si form by the photolithography which allows NW been partially covered by metal pads and then metal can diffuse into NW
to form nickel silicide as shown in Figure 2.4(a). The pure Si NWs are sonicated into ethanol solution and dispersed onto suspended Si nitride film for TEM observation or other substrates for electrical measurement (Figure 2.4(b)). First, the whole sample is baked for 15 mins under 170 °C on a hot plate to get rid of moisture, and then two layers of photoresist are coated by the spin coating process which allows metal film to be easily lifted-off later. The MMA (MicroChem Corp. 8.5 MMA EL9) is coated firstly at 4000 rpm for 1 min and then baked for 2 min at 170 °C. Following, the second layer, PMMA (MicroChem Corp. 495 PMMA A4), is coated at 5000 rpm for 1 min and also baked for another 2 min. After the photoresist coating process, the patterned metal pads on Si NW are exposed by E-beam lithography, and developed in a mixed isopropanol solution (methyl isobutyl ketone: isopropanol = 3:1). Before the metal deposition, sample should be rinsed into buffer oxide etchant (BOE) solution few seconds and load into deposition chamber right away in order to remove the native oxide for the direct contact between metal and Si. The nickel film deposits in an e-beam evaporator under a vacuum order of 10^{-8} Torr, and then unloaded sample to lift off by dipping into acetone solution few hours. During these photolithography process, the metal pads as 80 nm thick and 2 µm width are patterned to serve as diffusion couples of metal and Si which is presented in Figure 2.4 (c).

Under the rapid thermal annealing process (RTA), the nickel can diffuse into Si
NW to form nickel silicide as shown in Figure 2.4 (d). HRTEM images and characterizations of silicides NW are performed with FEI Titan at 300 KV. The electrical properties are measured in a Lakeshore TTP4 probe station. The diameter of NW in device is confirmed by scanning electron microscopy (SEM).

Figure 2.4 (a) Schematics of typical heterostructure. (b) The pristine Si NW on SiN substrate for TEM characterization, (c) Ni pad deposition, and (d) after annealing, Si NW transfer to silicide NW.
Chapter III: Nickel Silicide

In previous research, the phase transformation sequence in different diameters has been discussed. Nickel diffuses into Si NW to form NiSi$_2$ successfully by the RTA process under lower temperature 300-650 °C with Si NW as templates with a diameter of 27-213 nm. NiSi$_2$ emerges as the first phase due to kinetic growth competition. In this chapter, the more growth conditions are discussed, including the temperature, annealing period, and with or without the oxide layers.

3.1 Annealing Temperature

The thickness of Nickel pad is 80 nm, and the width covered the Si NW is 2 µm. Annealing temperatures of silicide formation under 450 °C and 550 °C are presented in Figure 3.1 and 3.2, respectively, and the period keeps 2 min. In Figure 3.1, the diameter of template NW is 91.2 nm, and NiSi$_2$ works as the first phase during the process. The NiSi$_2$/Si interface keeps epitaxial relation of NiSi$_2$ [112] // Si [112] as shown in Figure 3.1(b). Also, under 550 °C annealing, the 83.0 nm as diameter NW grows as Ni$_{31}$Si$_{12}$ and NiSi$_2$ which still remains as the first phase during the process. In addition, the broken part can be seen at the interface of metal pads and Ni richer phase, because Ni$_{31}$Si$_{12}$ with a larger unit volume than Si faces stronger stress in the
phase transformation. The volume per Si atom for Ni$_{31}$Si$_{12}$, NiSi$_2$, and Si are 39.46 Å$^3$, 19.75 Å$^3$ and 20.21 Å$^3$, respectively.

Figure 3.1 TEM images of silicides formation sequence and silicide/Si interface in Si NW templates annealing 450 °C for 2 min. (a) Image of FFT patterns of NiSi$_2$ and Si. (b) Epitaxial interface between NiSi$_2$ and Si.

Figure 3.2 TEM images of silicides formation sequence and silicide/Si interface in Si NW templates annealing 550 °C for 2 min. (a) Image of FFT patterns of Ni$_{31}$Si$_{12}$, NiSi$_2$, and Si. (b) (c) HRTEM image of NiSi$_2$ and Si.
3.2 Annealing Period

In Figure 3.2, lengths of Ni$_{31}$Si$_{12}$ and NiSi$_2$ are 0.545 µm and 0.326 µm, respectively, so the total length of nickel silicide is 0.871 µm. In figure 3.3, the annealing period increases from 2 min to 10 min, and the total nickel silicide is 2.614 µm. The length of Ni$_{31}$Si$_{12}$ and NiSi$_2$ is 2.22 µm and 0.39 µm. Comparison the length from different annealing period, the longer annealing time can enhance the overall silicide growth length, but the length of NiSi$_2$ is not much improved rather than the Ni$_{31}$Si$_{12}$ phase. In order to inhibit the growth rate of Ni$_{31}$Si$_{12}$, a thick oxide shell around Si NWs can suppress the growth rate of silicide with larger unit volume than NiSi$_2$ by supplying a compressive stress.

HRTEM studies show that NiSi$_2$/Si heterostructure has clean as well as atomically sharp interface with an epitaxial relationship of NiSi$_2$[110]/Si[110] and NiSi$_2$(-111)/Si(-111) as shown in Figure 3.3(b).
Figure 3.3 TEM images of silicides formation sequence and silicide/Si interface in Si NW templates annealing 550 °C for 10 min. (a) Image of FFT patterns of Ni$_{31}$Si$_{12}$, NiSi$_2$, and Si. (b) Epitaxial interface between NiSi$_2$ and Si.

### 3.3 Confining Shell of Al$_2$O$_3$

A thick Al$_2$O$_3$ layer (200 cycles) is deposited by atomic layer deposition (ALD) on top of the wafer after the Ni pad patterned by photolithography fabrication.$^{18}$ The oxide layer serves as the confining shell, and it can suppress the volume expansion for the phase transformation from Si to silicide. In addition, oxide shell can inhibit the breaking interface by applying a compressive stress to the NW. The low magnification image of NW with 15 nm thick Al$_2$O$_3$ (200 cycles) shell is indicated in Figure 3.4(a), and the STEM and TEM images of the interface of NiSi$_2$ and Si are also indicated in Figure 3.4(b) and (c). The length of Ni$_{31}$Si$_{12}$ and NiSi$_2$ are 3.228 µm and 0.625 µm, respectively. The length percentages of Ni$_{31}$Si$_{12}$ and NiSi$_2$ by total silicide.
length are 84% and 16%, which is similar with the NWs without oxide shell presented in Figure 3.3 as 85% and 15%. Moreover, scanning electron microscopy (SEM) studies of a silicide/Si/silicide heterostructure obtained through partial silicidation of the silicon nanowire after 550 °C for 10 min without and with oxide shell as indicated in Figure 3.4 (a) and (b), and two arrows highlight two NiSi$_2$/Si interfaces. The silicon NWs can be converted into NiSi$_2$/Si/NiSi$_2$ heterostructures through controlled reaction between lithography defined Ni pad and Si nanowire. Without the thick oxide shell, a curved section near the contact due to strain resulting from volume expansion shows in Figure 3.4 (a). It demonstrates that the oxide shell can indeed suppress the volume expansion for the phase transformation, especially for the large unit volume Ni$_{31}$Si$_{12}$.

However, the lateral nickel diffusion structure is hard to form the long and pristine NiSi$_2$, so the new structure for Ni diffuse into Si NW should be take into consideration.
Figure 3.4 (a) TEM image of silicides formation sequence in 80 nm Si NW with a 15 nm thick Al$_2$O$_3$ shell as templates annealing at 550 °C for 10 min. (b) STEM and (c) TEM images of the NiSi$_2$/Si interfaces.
Figure 3.5 SEM images of silicide/Si/silicide NW (a) without and (b) with Al₂O₃ shell.

Scale bar: 1 µm.
Chapter IV: Full Coverage of NiSi\textsubscript{2}

In the previous chapter, the small region of NiSi\textsubscript{2} can be formed in Si NWs, but the resistance is hard to measure in such small region. Therefore, the longer NiSi\textsubscript{2} is needed for measuring the resistance by four terminal patterning. In this chapter, a new method, which nickel is fully deposited on the top of NWs, is used to grow fully silicide NWs. The growth conditions for long as well as pristine NiSi\textsubscript{2} NWs will also be discussed.

4.1 Process Flow of Full Coverage Si NW

Si NWs are dispersed on the Si nitride TEM membrane or substrate for characterization or electrical measurements. Before the Ni film deposition, the native oxide should be removed by the BOE etching, and then the sample sends into e-beam evaporating chamber directly for a 10-15 nm thick Ni deposition. A 15-30 nm (200~350 cycles) thick Al\textsubscript{2}O\textsubscript{3} film is also deposited on top of the metal films to serve as a protecting layer ALD process. Following, Ni would diffuse into Si NWs by heated under 550 °C for 30 min to form NiSi\textsubscript{2}. After reaction, Al\textsubscript{2}O\textsubscript{3} film is etched by reactive ion etching (RIE) and excess metal films are then etched in piranha solution (H\textsubscript{2}SO\textsubscript{4}:H\textsubscript{2}O\textsubscript{2}:H\textsubscript{2}O = 1:1:4) for 5 min. Ti and Au pads are patterned through e-beam
lithography to serve as contacts for electrical measurements under Lakeshore TTP4 probe station.

Figure 4.1 Process flow of full coverage growth of NiSi₂ NW.

Figure 4.2 shows a NW that is covered by 10 nm of Ni thin film as well as 16 nm (200 cycle) of Al₂O₃ shell, and then anneals at 550 °C for 30. NiSi₂ phase has been formed successfully, and it can be confirmed by the diffraction and EDX analysis. However, from the STEM image (Figure 4.2(b)) indicates the NW is non-uniform, and the edge of NWs maintain roughly (Figure 4.2(c) and (d)). Moreover, the four terminal measurements are presented in Figure 4.3(a). The areas between two contact
electrodes are also shown in Figure 4.3(b) and (c), in which the nanowire shows white and grey sections. It also demonstrates that the nanowire is not fully reacted as nickel silicide. In order to get the long and pristine NiSi$_2$ NWs, the growth condition should be modified.

Figure 4.2 (a) Low magnification TEM as well as (b) STEM images. Scale bar: 100 nm. (c) TEM as well as (d) STEM images at the end of NW. Scale bar: 50 nm (e) Energy-dispersive X-ray spectrometry of NiSi$_2$. Silicides formed in a Si NW with 10 nm Ni and a 16nm Al$_2$O$_3$ shell at 550 °C for 30 min.
Figure 4.3 (a) SEM image of four terminal NiSi$_2$ NW device. The top and down squares as shown in (b) and (c), respectively.

4.2 Thickness of Al$_2$O$_3$ Film

In order to confirm the Ni source enough for diffusion into Si to form the silicide, the thickness of Ni film increases from 10 nm to 15 nm. In addition, the thickness of oxide shell is also need to be confirmed. Increase the thickness of oxide film to enhance the compressive stress confined the phase transformation.

The ALD deposition cycles increases from 16 nm to 23 nm (200 to 300 cycles) as shown in Figure 4.4 and 4.5 in which the diameters of Si templates are 53 nm and 47 nm. Figure 4.4 (d) and (e) indicate that NiSi$_2$ and $\delta$-Ni$_2$Si co-exist in a single NW after anneal at 550 °C for 30 min. The diffraction patterns of NiSi$_2$ and $\delta$-Ni$_2$Si are presented in Figure (f) and (e), respectively. The smaller NW (47 nm) is fully reacted as NiSi$_2$. Thus, the 23 nm (300 cycles of ALD deposition) is not enough confined the
NW with larger diameters, so the thickness of oxide shell increases more up to 27 nm (350 cycles). Two NWs are characterized as shown in Figure 4.6 and 4.7 with Si templates as 40 nm and 23 nm. The low magnification TEM and STEM images indicate the uniform silicide nanowires are formed, and the diffraction patterns, HRTEM images, and EDX analysis confirm the phase as NiSi$_2$. However, some Al$_2$O$_3$ film remains on the NW, so the RIE etching recipe should be tuned to remove all the oxide shell in order to measure the electrical properties of pure NiSi$_2$ NW.

Figure 4.4 (a) Low magnification TEM as well as (b-c) STEM images. Scale bar: 250 µm. (d) Zoom in TEM as well as (e) STEM images at the end of NW. Scale bar: 50 nm. (f) (h) diffraction pattern, and (g) (i) Energy-dispersive X-ray spectrometry of NiSi$_2$ and δ-Ni$_2$Si part, respectively. Silicides formed in a Si NW with 15 nm Ni and a 23 nm Al$_2$O$_3$ shell at 550 °C for 30 min.
Figure 4.5 (a) Low magnification TEM as well as (b) STEM images, (c) diffraction pattern, and (e) Energy-dispersive X-ray spectrometry of NiSi$_2$ NW. Scale bar: 100 nm. Silicides formed in a Si NW with 15 nm Ni and a 23 nm Al$_2$O$_3$ shell at 550 °C for 30 min.

Figure 4.6 (a) Low magnification TEM as well as (b) STEM images, (c) diffraction pattern (d) HRTEM image and (e) Energy-dispersive X-ray spectrometry of NiSi$_2$ NW. Scale bar: 50 nm. Silicides formed in a Si NW with 15 nm Ni and a 27 nm Al$_2$O$_3$ shell at 550 °C for 30 min.
Figure 4.7 (a) Low magnification TEM as well as (b) STEM images, (c) diffraction pattern (d) HRTEM image and (e) Energy-dispersive X-ray spectrometry of NiSi₂ NW. Scale bar: 100 nm. Silicides formed in a Si NW with 15 nm Ni and a 27 nm Al₂O₃ shell at 550 °C for 30 min.

4.3 Annealing Temperature

Not only the Ni but also the Al₂O₃ shell thickness has been tried. From previous result, increase the Ni thickness can provide enough Ni source for phase formation. The thick of oxide film can increase the compressive stress and confine the volume expansion during annealing process. Moreover, increasing the annealing temperature can provide more thermal source for Ni diffusion into Si NW. A Si NW with 15 nm Ni and a 29 nm Al₂O₃ shell at 650 °C for 30 min is indicated in Figure 4.8. The whole NW transfers to NiSi₂ confirmed by the diffraction pattern and Energy-dispersive X-ray spectrometry.
Figure 4.8 (a) (b) Low magnification TEM as well as STEM images, (c) (d) diffraction pattern (e) Energy-dispersive X-ray spectrometry of NiSi$_2$ NW. Scale bar: 100 nm. Silicides formed in a Si NW with 15 nm Ni and a 29 nm Al$_2$O$_3$ shell at 650 °C for 30 min.

4.4 Electrical Properties of NiSi$_2$ NW from Four Terminal Measurements

From the two and four terminal measurement, the resistivity of 52 nm NiSi$_2$ NW is 242.8 and 39.2 µΩ-cm, respectively. The current density presents as $2.6 \times 10^7$ A/cm$^2$. The current-voltage (I-V) curve and the SEM image of NW are shown in Figure 4.9 (a) and (b). The width of NW is 52 nm, and the channel length is 1.3 µm.

Here, we assume all NiSi$_2$ NW are in cylinder shape by measuring the diameter of NiSi$_2$ NW from SEM top view image. The edge effect in SEM and the assumption of NiSi$_2$ NW diameter might cause over estimation. Thus, a sample should be sent to
focus ion bean (FIB) support to precisely approach real cross sectional area.

Figure 4.9 (a) I-V curve of a 52 nm NiSi$_2$ NW from two and four terminal measurements. (b) SEM image of the NW.
Chapter V: Conclusion

In my research, there are two structures for silicidation by solid state reaction. The first structure is the lateral structure in which we can know the first phase by kinetic competition. NiSi2 win as the first one during the annealing process. However, through different annealing temperature and period, the length of NiSi2 is not long enough for electrical properties study. Therefore, a new structure is adopted for create long and pristine NiSi2 NWs. Ni is global deposited onto the top of Si NWs, and an ALD Al2O3 shell is applied to confine the expansion of NWs during phase transformation. Besides, shell can prevent the silicide oxidation in silicidaiton. The thicker film can provide more Ni source on all the NWs, so it can get rid of the roughness issue. All the Si NW can covered by Ni for silicidaiton. The more thickness of Al2O3 confined shell, we can prevent the bending issue and extrusions of NWs. Also, the thicker of oxide film can increase the compressive stress and confine the volume expansion during annealing process.

To the end, a long and pristine NiSi2 NW can be formed in a Si NW with 15 nm Ni and a 29 nm Al2O3 shell at 650 °C for annealing 30 min. The two and four terminal resistivity of a 52 nm NiSi2 NW is 242.8 and 39.2 µΩ-cm, respectively. The failure current density is $2.6 \times 10^7$ A/cm². The resistivity of NiSi2 NW is similar with the
In the future, we can push the diameter of NiSi$_2$ down to 10-40 nm and study the electrical properties for small diameters. The small size of NW can be built into nanodevice or interconnects.
References


12. Wu, Yue, Jie Xiang, Chen Yang, Wei Lu, and Charles M. Lieber.


