Title
Sparse gallium arsenide to silicon metal waferbonding for heterogeneous monolithic microwave integrated circuits

Permalink
https://escholarship.org/uc/item/59v7p40c

Author
Bickford, Justin Robert

Publication Date
2008
Sparse Gallium Arsenide to Silicon Metal Waferbonding for
Heterogeneous Monolithic Microwave Integrated Circuits

A dissertation submitted in partial satisfaction of the
requirements for the degree Doctor of Philosophy
in
Electrical Engineering (Applied Physics)

by

Justin Robert Bickford

Committee in Charge:
Paul K. L. Yu, Chair
S. S. Lau, co-Chair
Peter Asbeck
William Chang
John Crowell
Vitali Nesterenko
Ivan Shubin

2008
The dissertation of Justin Robert Bickford is approved
and it is acceptable in quality and form for publication on microfilm:

___________________________________________________
___________________________________________________
___________________________________________________
___________________________________________________

___________________________________________________

Co-Chair

___________________________________________________

Chair

University of California, San Diego

2008

iii
Dedication

This dissertation is dedicated to my wife, Jamie, for all of her love and support throughout these difficult years. She accompanied me to San Diego, California immediately after graduating college, far from the comfort and support of our friends and family on the East coast, to help me pursue my dream of becoming a Ph. D. To this, I am eternally grateful. Although we have shared several wonderful experiences here in San Diego, we have also endured many emotional and financial setbacks.

Though we will miss all our friends here on the West coast, we are eager to return to home to become a more integral part of our family’s lives, as they have played a large role in supporting us both.
# Table of Contents

Signature page........................................................................................................ iii
Dedication............................................................................................................. iv
Table of Contents................................................................................................. v
List of Figures ..................................................................................................... xi
List of Tables ....................................................................................................... xvii
Acknowledgements............................................................................................. xviii
Vita....................................................................................................................... xx
Abstract ............................................................................................................ xxii

## 1 Introduction..................................................................................................... 1
1.1 General Microwave Integration Motivation .................................................. 1
1.2 Proposed HMMIC Implementation ............................................................. 1
1.3 Bonding Introduction.................................................................................... 2
  1.3.1 General Bonding Procedure................................................................. 2
  1.3.2 Types of Bonding.................................................................................. 3
1.4 Specific Motivation for the Metalbonded HMMIC Approach ....................... 5
1.5 Scope of the Dissertation............................................................................. 14
1.6 Writing Style............................................................................................... 16
1.7 References..................................................................................................... 17

## 2 Stress and Strain............................................................................................ 20

### 2.1 Introduction............................................................................................... 20
### 2.2 Stress and Strain Theory............................................................................ 20
  2.2.1 Definition of Strain................................................................................ 20
  2.2.2 Definition of Stress............................................................................... 22
  2.2.3 Uniaxial and Biaxial Stress..................................................................... 24
  2.2.4 Thermal Expansion Induced Stress....................................................... 26
  2.2.5 Definition of Strength.......................................................................... 31
  2.2.6 Defects.................................................................................................. 31
  2.2.7 Degradation and Failure....................................................................... 34
  2.2.8 Defect Nucleation and Critical Thickness.......................................... 35
### 2.3 Types of Integration Strain................................................................. 37
  2.3.1 Integration Borne Interfacial Strain...................................................... 38
  2.3.2 Integration Borne Bulk Stress.............................................................. 42
  2.3.3 Integration Method Comparison......................................................... 45
### 2.4 Conclusion............................................................................................... 45
### 2.5 Reference............................................................................................... 46

## 3 MOCVD Epitaxy......................................................................................... 49

### 3.1 Introduction............................................................................................. 49
### 3.2 MOCVD Basics...................................................................................... 49
### 3.3 MOCVD Growth at UCSD................................................................. 51
  3.3.1 Specifications of the MOCVD Machines at UCSD............................ 51
<table>
<thead>
<tr>
<th>Section</th>
<th>Title</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>5.5</td>
<td>Conclusion</td>
<td>125</td>
</tr>
<tr>
<td>5.6</td>
<td>References</td>
<td>126</td>
</tr>
<tr>
<td>6</td>
<td>Bond Interface Electrical Characterization</td>
<td>128</td>
</tr>
<tr>
<td>6.1</td>
<td>Introduction</td>
<td>128</td>
</tr>
<tr>
<td>6.2</td>
<td>Ideal Metal-Semiconductor Interface Theory</td>
<td>129</td>
</tr>
<tr>
<td>6.2.1</td>
<td>Band Alignment</td>
<td>129</td>
</tr>
<tr>
<td>6.2.2</td>
<td>General Non-Linear Behavior</td>
<td>131</td>
</tr>
<tr>
<td>6.2.3</td>
<td>Linear (Ohmic) Behavior</td>
<td>134</td>
</tr>
<tr>
<td>6.3</td>
<td>Real Metal-Semiconductor Interfaces</td>
<td>136</td>
</tr>
<tr>
<td>6.3.1</td>
<td>Fermi Level Pinning Examples</td>
<td>137</td>
</tr>
<tr>
<td>6.4</td>
<td>Practical Contacts</td>
<td>138</td>
</tr>
<tr>
<td>6.4.1</td>
<td>Effects of Annealing</td>
<td>138</td>
</tr>
<tr>
<td>6.5</td>
<td>Measurement of Bond Interface Electrical Behavior</td>
<td>140</td>
</tr>
<tr>
<td>6.5.1</td>
<td>Measurement Process Overview</td>
<td>140</td>
</tr>
<tr>
<td>6.5.2</td>
<td>Measurement Process Discussion</td>
<td>141</td>
</tr>
<tr>
<td>6.5.3</td>
<td>Discussion of Results</td>
<td>142</td>
</tr>
<tr>
<td>6.6</td>
<td>Bond Interface Contact Resistivity Measurement</td>
<td>143</td>
</tr>
<tr>
<td>6.6.1</td>
<td>Conventional Contact Resistivity Measurement Methods</td>
<td>144</td>
</tr>
<tr>
<td>6.6.2</td>
<td>Measurement Design</td>
<td>145</td>
</tr>
<tr>
<td>6.6.3</td>
<td>Kelvin Measurement Discussion</td>
<td>150</td>
</tr>
<tr>
<td>6.6.4</td>
<td>Measurement Process Overview</td>
<td>151</td>
</tr>
<tr>
<td>6.6.5</td>
<td>Measurement Process Discussion</td>
<td>152</td>
</tr>
<tr>
<td>6.6.6</td>
<td>Discussion of Results</td>
<td>152</td>
</tr>
<tr>
<td>6.7</td>
<td>Conclusion</td>
<td>154</td>
</tr>
<tr>
<td>6.8</td>
<td>Acknowledgment</td>
<td>155</td>
</tr>
<tr>
<td>6.9</td>
<td>References</td>
<td>156</td>
</tr>
<tr>
<td>7</td>
<td>Bond Interface Thermal Conductivity Characterization</td>
<td>158</td>
</tr>
<tr>
<td>7.1</td>
<td>Introduction</td>
<td>158</td>
</tr>
<tr>
<td>7.2</td>
<td>Measurement of Bond Interface Thermal Conductivity</td>
<td>159</td>
</tr>
<tr>
<td>7.2.1</td>
<td>Existing Measurement Methods</td>
<td>159</td>
</tr>
<tr>
<td>7.2.2</td>
<td>Investigated Method Introduction</td>
<td>163</td>
</tr>
<tr>
<td>7.2.3</td>
<td>Investigated Method Principle</td>
<td>164</td>
</tr>
<tr>
<td>7.3</td>
<td>Investigated Method Thermal Conductivity Extraction Theory</td>
<td>167</td>
</tr>
<tr>
<td>7.3.1</td>
<td>Analytical Spreading Resistance Calculation Approach</td>
<td>167</td>
</tr>
<tr>
<td>7.3.2</td>
<td>Empirical Spreading Resistance Approach</td>
<td>173</td>
</tr>
<tr>
<td>7.4</td>
<td>Measurement Overview</td>
<td>175</td>
</tr>
<tr>
<td>7.4.1</td>
<td>Sample Preparation</td>
<td>175</td>
</tr>
<tr>
<td>7.5</td>
<td>Measurement Discussion</td>
<td>178</td>
</tr>
<tr>
<td>7.6</td>
<td>Discussion of Results</td>
<td>179</td>
</tr>
<tr>
<td>7.6.1</td>
<td>Bond Interface Thermal Conductivity Estimates</td>
<td>181</td>
</tr>
<tr>
<td>7.6.2</td>
<td>Bond Thermal Conductivity Comparison</td>
<td>183</td>
</tr>
<tr>
<td>7.7</td>
<td>Conclusion</td>
<td>186</td>
</tr>
<tr>
<td>7.8</td>
<td>References</td>
<td>187</td>
</tr>
</tbody>
</table>
# 8 Bonded Device Microwave Characterization

8.1 Introduction ................................................................. 190
8.2 Basic Microwave Theory .................................................. 191
  8.2.1 Electromagnetic Wave Propagation ..................................... 191
  8.2.2 General transmission line circuit modeling .............................. 193
8.3 General Microwave Measurements ......................................... 198
  8.3.1 Scattering Matrix Definition .............................................. 198
  8.3.2 Transmission Matrix Definition ............................................ 199
  8.3.3 Measurement Procedure Overview ....................................... 200
  8.3.4 Extraction Theory ........................................................... 201
8.4 Finite Element Analysis .................................................... 204
  8.4.1 Ideal Lossless Situation .................................................... 205
  8.4.2 Realistic Lossy Situation .................................................. 206
8.5 Coplanar Waveguide Theory ............................................... 208
  8.5.1 CPW Definition .............................................................. 208
  8.5.2 CPW Supported Waves .................................................... 209
  8.5.3 CPW Quasi-TEM Theoretical Analysis .................................. 210
8.6 Microstrip Waveguide Theory ............................................. 213
  8.6.1 Microstrip Definition ....................................................... 213
  8.6.2 Microstrip Supported Waves .............................................. 214
  8.6.3 Microstrip Quasi-TEM Theoretical Analysis .............................. 214
  8.6.4 Analytical Estimations ....................................................... 215
8.7 CPW versus Microstrip Comparison ....................................... 217
  8.7.1 Design Freedom .............................................................. 217
  8.7.2 Ground Vias ................................................................. 217
  8.7.3 Cross-Talk ................................................................. 218
  8.7.4 Impedance ................................................................. 218
  8.7.5 Loss ........................................................................... 219
  8.7.6 Power Handling ............................................................. 219
8.8 Preliminary Bondmetal Microwave Propagation Investigation ......... 220
  8.8.1 Measurement Procedure Overview ....................................... 221
  8.8.2 Results and Analysis ....................................................... 222
  8.8.3 Discussion of Results ....................................................... 224
8.9 Bonded Device Microwave Propagation Investigation .................. 228
  8.9.1 Measurement ................................................................. 228
  8.9.2 Results and Analysis ....................................................... 228
  8.9.3 Discussion of Results ....................................................... 230
8.10 P-I-N Semiconductor Device Microwave Propagation Investigation .... 234
  8.10.1 TWEAM Definition ......................................................... 234
  8.10.2 Measurement ............................................................... 236
  8.10.3 Discussion of behavior ................................................... 236
  8.10.4 Modeling ................................................................. 237
8.11 Conclusion ....................................................................... 243
8.12 References ...................................................................... 245
9 Conclusions and Future Work .................................................. 247
  9.1 Summary of Dissertation .................................................. 247
  9.1.1 Robust Heterogeneous Integration .................................. 247
  9.1.2 Metalbonded HMMIC Evaluation .................................. 250
  9.2 Future work ...................................................................... 254
    9.2.1 Improving Measurement Methods .................................. 255
    9.2.2 Bonding Active, High-Power, High-Speed Microwave Devices .................................. 256
    9.2.3 Improving Yield ...................................................... 257
    9.2.4 Improving the Bond Alloy ............................................. 259
  9.3 References ...................................................................... 264

Appendix A: Heat Transfer and Thermal Conductivity Theory .......... 267
  A.1 Introduction .................................................................. 267
  A.2 Basic Heat Transfer Theory .......................................... 267
    A.2.1 General Thermodynamic System Theory .................. 267
  A.3 Heat Transfer System: Thermal Modeling ......................... 269
    A.3.1 Thermal Resistance Definition ............................... 273
  A.4 Thermal Conductivity .................................................. 275
    A.4.1 Theoretical Origins of Thermal Conductivity .......... 276
    A.4.2 Basic Thermal Conductivity Theory ...................... 277
    A.4.3 Simple Gas Formulation ....................................... 277
    A.4.4 Realistic Thermal Conductivity Formulations .......... 278
    A.4.5 Predicting Thermal Conductivity of Materials ...... 290
  A.5 Conclusion .................................................................. 295
  A.6 References .................................................................. 296

Appendix B: Fabrication Procedures .......................................... 297
  B.1 Epitaxial Growth Procedure .......................................... 297
  B.2 Post-Pattern Bonding Procedure ..................................... 298
  B.3 Pre-Pattern Bonding Procedure ...................................... 303

Appendix C: Measurement Procedures ...................................... 317
  C.1 Bond Interface Electrical Measurement Procedures ........... 317
  C.2 Bond Interface Thermal Conductivity Measurement Procedure .................................. 319
  C.3 Bonded Device Microwave Measurement Procedure .......... 322

Appendix D: Apparatus .......................................................... 323
  D.1 Sample Cleaving Setup ............................................... 323
  D.2 Bond Mask Patterns .................................................... 324
  D.3 Low-temperature Evaporation Assembly ....................... 327
  D.4 Evaporation Sample Mounting Tools ......................... 331
  D.5 Bonding Tools ......................................................... 333
  D.6 Bond Annealer ........................................................ 335
  D.7 Wicked Materials ...................................................... 337
  D.8 Etch-Thinning Apparatus ............................................. 342
D.9 Thermal Measurement Setup ................................................................. 344
D.10 HP4155 Semiconductor Parameter Analyzer ......................................... 346
D.11 HP8510B Network Analyzer ................................................................. 348

Appendix E: Software Source Code ................................................................ 350
E.1 Universal MOCVD Control Program ...................................................... 350
E.2 Circuit Parameters Extraction Program .................................................... 362
E.3 TWEAM Simulation Programs ................................................................. 371
List of Figures

Figure 1-1. Example illustration of the HMMIC scheme ........................................... 2
Figure 1-2. Illustrations of (a) CPW and (b) bonded-microstrip surface breakdown and (c) arbitrarily wide bonded-microstrip bulk breakdown .......................................... 13
Figure 2-1. Illustration of the normal and shear strains allowed in a unit body under (a) isotropic dilation and (b) rhombohedral distortion ........................................ 21
Figure 2-2. Illustration of the normal and shear stresses in a unit body creating (a) isotropic dilation and (b) rhombohedral distortion ........................................ 22
Figure 2-3. Illustrations of (a) a uniaxially strained cube and (b) a biaxially strained cube ................................................................................................................. 24
Figure 2-4. Illustrations of a heterogeneous lamination undergoing thermal stress: (a) un-bonded state at room temperature, (b) bonding at bond temperature, and (c) thermally strained at room temperature .................................................. 27
Figure 2-5. Illustration of the vertical stress distribution in a thermally stressed lamination ........................................................................................................... 28
Figure 2-6. Illustration of segments within a heterogeneous lamination undergoing thermal stress ........................................................................................................... 29
Figure 2-7. Illustrations of the two types of line defects: (a) an edge dislocation and (b) a screw dislocation ........................................................................................................... 32
Figure 2-8. Illustration of a planar defect .................................................................. 33
Figure 2-9. Illustrations of the three types of point defects: (a) a vacancy, (b) an interstitial atom, and (c) a substitutional atom ................................................... 34
Figure 2-10. Example plot of the critical thickness versus strain ......................... 37
Figure 2-11. Illustration of tetrahedral distortion during (a) pseudomorphic growth and (b) metamorphic growth ................................................................. 39
Figure 2-12. Illustration of the interfacial strain between two heterogeneously bonded materials ........................................................................................................ 40
Figure 2-13. Illustration of the interface between two mis-oriented homogeneously bonded materials ........................................................................................................ 41
Figure 2-14. Illustrations of thermally stressed laminations in bending: (a) a lamination prevented from bending via external forces, (b) a lamination freely bending, and (c) a lamination with negligible bending ........................................ 43
Figure 3-1. Illustration of a rudimentary MOCVD machine ..................................... 50
Figure 3-2. Picture of the metalorganic chemical vapor deposition (MOCVD) machine used at UCSD ........................................................................................................ 52
Figure 3-3. Nomarski interference contrast image of (a) organic and (b) particle pre-growth contamination ........................................................................................................ 57
Figure 3-4. Nomarski interference contrast images of crystal defects, including: (a) 'diamond' defects, (b) 'oval' defects, (c) ordering texture, and (d) teardrop-like hillocks (TDLH) ........................................................................................................ 58
Figure 3-5. Nomarski interference contrast images of (a) light ‘cross-hatch’ mismatch and (b) extreme metamorphic growth ........................................................................ 59
Figure 3-6. Picture of the high resolution x-ray diffraction (HRXRD) machine used at UCSD................................................................. 60
Figure 3-7. Example HRXRD rocking curve plots and illustrations of their physical construction: (a) a single strained epitaxial layer on a substrate and (b) a strained superlattice on a substrate. ................................................. 63
Figure 3-8. Illustration of a rudimentary photoluminescence measurement setup........ 68
Figure 3-9. Example photoluminescence plot of a III/V compound semiconductor epilayer.................................................................................................................. 69
Figure 3-10. Illustration of electron and hole movement within a compensated n-type semiconductor in a magnetic field giving rise to a net Hall field. ................. 72
Figure 3-11. Chart of the bandgap energy versus lattice constant for several common semiconductor materials................................................................. 74
Figure 3-12. Illustration (a) and image (b) of ‘bumps’ in a silicon-to-glass bond interface.................................................................................. 75
Figure 3-13. Pictures of a coated (a) reactor tube and (b) susceptor. ....................... 79
Figure 3-14. Microscope image of whisker growth................................................... 84
Figure 4-1. Illustrations of the ITS process depicting both the structural state and alloy state from (a) room temperature to the indium melting point, through (b) the alloying process to (c) the completion of the alloying process. (d) illustrates the solid behavior after bonding, below the alloy remelting temperature. 89
Figure 5-1. Microscope images of indium squeeze-out both (a) without and (b) with standoff implementation. .......................................................... 115
Figure 5-2. Microscope images of indium squeeze-out after etchstop removal both (a) without and (b) with PMGI implementation................................. 116
Figure 5-3. SEM images showing evaporated indium metal texture deposited while the sample was (a) un-cooled (+50°C), (b) cooled to dry-ice/acetone temperature (-80°C), and (c) cooled to liquid nitrogen temperature (-196°C). *Note that the magnification is identical for all images.................................................. 117
Figure 5-4. Microscope images of GaAs thermal expansion induced pattern shift of the (a) left-most and (b) right-most bonded epilayer mesaas. ...................... 124
Figure 6-1. Illustrations of an ideal metal-semiconductor contact band diagram depicting a high barrier metal coming in contact with a n-type semiconductor under zero external bias: (a) uninfluenced, (b) in proximity, and (c) in contact. 130
Figure 6-2. Illustrations of an n-type semiconductor (n-SC) Schottky barrier contact at different biases with associated I-V regions highlighted: (a) reverse bias (breakdown), (b) reverse bias (inversion), (c) reverse bias (normal), and (d) forward bias. ........................................................................................................ 132
Figure 6-3. Illustrations of ohmic contacts to n-type semiconductor (n-SC) with (a) a low barrier height metal and (b) a high surface doping concentration in reverse, mid, and forward biased states................................................................. 134
Figure 6-4. Illustrations of a realistic metal-semiconductor contact band diagram under zero external bias: (a) uninfluenced, (b) in proximity, and (c) in contact – empty circles indicate empty surface states while filled circles indicate filled surface states........................................................................................................ 136
Figure 6-5. Illustrations of the electron potential structure of (a) a single atom, (b) the edge of a semiconductor, and (c) the interior of a semiconductor crystal......... 137
Figure 6-6. Illustration of a metal-semiconductor spiking contact......................... 139
Figure 6-7. I-V plots of the bond interface electrical behavior showing the In-Pd ITS alloy’s universal ohmic contact behavior between GaAs and Si.................... 142
Figure 6-8. Illustrations of the surveyed contact resistivity measurement methods: (a) Cox and Strack disk method, (b) Kelvin method, (c) transmission line method (TLM) (collinear), (d) concentric ring method (axi-symmetric TLM), and (e) Kuphal collinear disk method................................................................. 144
Figure 6-9. Illustration of the bond interface electrical contact resistivity measurement structure........................................................................................................... 146
Figure 6-10. Illustrations of both the physical structure and equivalent circuit of an (a) traditional 2-wire measurement scheme and (b) Kelvin 4-wire scheme measurement scheme................................................................. 150
Figure 6-11. Plot of the residual resistance versus inverse bond contact area for n-GaAs/p-Si bonded structures (inset shows an example I-V electrical behavior plot of a typical structure)................................................................. 153
Figure 7-1. Illustrations of steady state thermal conductivity measurement methods. 160
Figure 7-2. Illustrations of transient thermal conductivity measurement methods. .... 161
Figure 7-3. Illustrations of non-contact thermal conductivity measurement methods. 162
Figure 7-4. Illustration of the bondmetal thermal conductivity measurement and equivalent circuit...................................................................................................... 165
Figure 7-5. Illustration of Loewen and Shaw’s isoflux heater on an infinite half-space. ................................................................................................................................. 169
Figure 7-6. Illustrations of the heater design revisions showing (a) older revision: temperature measured over only a portion of the heater’s length and (b) latest revision: temperature measured over entire length................................. 170
Figure 7-7. Microscope image of a void induced bonded epilayer warping .............. 180
Figure 7-8. Plot of In-Pd alloy thin film electrical conductivity versus alloy composition................................................................................................................. 182
Figure 8-1. Equivalent circuit schematic of a general microwave transmission line. 194
Figure 8-2. Block diagram of a two-port scattering matrix........................................ 198
Figure 8-3. Block diagram of a two port ABCD transmission matrix....................... 199
Figure 8-4. Illustrations and equivalent block diagrams of two lengths of measured waveguide: (a) short waveguide and (b) long waveguide............................ 201
Figure 8-5. Illustrations of a general ideal lossless two-wire waveguide cross section showing (a) the electric field and (b) the magnetic field, both with integration paths........................................................................................................... 205
Figure 8-6. Illustrations of a general ideal lossy two-wire waveguide cross section showing (a) the electric field (with voltage integration path) and (b) the magnetic field (with power flux integration)......................................................... 207
Figure 8-7. Illustrations of an ideal lossless coplanar waveguide cross section showing (a) the electric field and (b) the magnetic field........................................... 209
Figure 8-8. Illustrations of an ideal lossless microstrip waveguide cross section showing (a) the electric field and (b) the magnetic field....................................... 214
Figure 8-9. Microscope image (a) of a bondmetal coplanar waveguide test structure and SEM image (b) of a close up of the LN$_2$ as-evaporated center conductor cross section. 221

Figure 8-10. Example plots of a bondmetal CPW test structure’s measured S-parameters and extracted microwave characteristics. 223

Figure 8-11. Microscope images of bondmetal CPW test structures both before and after annealing of (a) un-cooled (+60°C) and (b) LN$_2$ temperature (-196°C) samples (inset illustrates the average height of the bumpy textured bondmetal). 226

Figure 8-12. Plots of the bonded-microstrip test structure’s measured S-parameters and extracted microwave characteristics with simulated results. 229

Figure 8-13. Illustrations of the finite element modeled cross section half of the bonded-microstrip test structure showing the log magnitude (intensity) and field flux (vector field) of the transverse (a) electric field and (b) magnetic field. 230

Figure 8-14. Illustrations of the finite element modeled cross section half of the ideal bonded-microstrip test structure showing the log magnitude (intensity) and field flux (streamlines) of the transverse (a) electric field and (b) magnetic field. 233

Figure 8-15. FEM results of the (a) loss, (b) microwave index, and (c) impedance for the ideal bonded-microstrip waveguide. 234

Figure 8-16. Illustration of the TWEAM structure cross section. 235

Figure 8-17. Plots of the TWEAM test structure’s measured S-parameters and extracted microwave characteristics. 236

Figure 8-18. Schematic diagram of the crude TWEAM equivalent circuit. 238

Figure 8-19. Plots of the crude TWEAM transmission line equivalent circuit calculation results. 239

Figure 8-20. Schematic diagram of the second generation TWEAM equivalent circuit. 240

Figure 8-21. Plots of the second generation TWEAM transmission line equivalent circuit calculation results. 242

Figure A-1. Illustration of the heat transfer in an arbitrary domain at steady state. 268

Figure A-2. Illustration of a unified heat transfer system domain (as seen from its exterior). 269

Figure A-3. Illustration of a subdivided heat transfer domain describing a heat source on a solid in air. 270

Figure A-4. Illustration of a simplified thermal conduction system with subdomain-2’s influence ignored (showing the further subdivision of subdomain-1 into three constituents). 273

Figure A-5. Illustrations of flow and accompanying equivalent circuits in a uniform body depicting: (a) the one-dimensional flow in a uniform cross section and (b) three constituent one-dimensional flows. 274

Figure A-6. Illustration of a resistance network and its characteristic terminal resistances. 275

Figure A-7. Plot of the thermal conductivity versus temperature of low defect density silicon. 292

Figure B.2-1. Illustration of post-pattern process: Si and GaAs sample preparation. 298
Figure B.2-2. Illustration of post-pattern process: after Si and GaAs bondmetal evaporation ................................................... 299
Figure B.2-3. Illustration of post-pattern process: after Si and GaAs bonding. .... 299
Figure B.2-4. Illustration of post-pattern process: Si and GaAs annealing. ............ 300
Figure B.2-5. Illustration of post-pattern process: GaAs substrate etching ............ 300
Figure B.2-6. Illustration of post-pattern process: after InGaP etchstop etching. .... 300
Figure B.2-7. Illustration of post-pattern process: high temperature ohmic contact metallization and annealing ................................................... 301
Figure B.2-8. Illustration of post-pattern process: GaAs topside contact metallization. ........................................................................................................ 301
Figure B.2-9. Illustration of post-pattern process: after GaAs mesa definition......... 302
Figure B.3-1. Illustration of pre-pattern process: after GaAs mesa photoresist definition and SEM cross sectional picture of the same ................................................... 303
Figure B.3-2. Illustration of pre-pattern process: after GaAs mesa definition and SEM cross sectional picture of the same ................................................... 304
Figure B.3-3. Illustration of pre-pattern process: after GaAs mesas after photoresist removal and SEM cross section picture of the same. ................................................... 305
Figure B.3-4. Illustration of pre-pattern process: after PMGI application and microscope picture of the same ................................................... 305
Figure B.3-5. Illustration of pre-pattern process: after photoresist dissolution and microscope picture of the same ................................................... 306
Figure B.3-6. Illustration of pre-pattern process: after PMGI/photoresist dissolution and photoresist removal and microscope picture of the same ................................................... 306
Figure B.3-7. Illustration of pre-pattern process: after PMGI reflow and microscope picture of the same ................................................... 307
Figure B.3-8. Illustration of pre-pattern process: after Titanium standoff photoresist definition and metallization and microscope picture of the same ................................................... 307
Figure B.3-9. Illustration of pre-pattern process: after bondmetal deposition and photoresist liftoff and microscope picture of the same ................................................... 309
Figure B.3-10. Illustration of pre-pattern process: after sample pair bonding ......... 310
Figure B.3-11. Illustration of pre-pattern process: sample pair annealing .............. 310
Figure B.3-12. Illustration of pre-pattern process: after sample pair wax wetting .... 311
Figure B.3-13. Illustration of pre-pattern process: after GaAs substrate S-etchant etch-thinning. ................................................... 311
Figure B.3-14. Illustration of pre-pattern process: after GaAs substrate etch S-etchant touch-up and composite microscope picture of the same ................................................... 312
Figure B.3-15. Illustration of pre-pattern process: after GaAs substrate C-etchant etch and composite microscope picture of the same ................................................... 313
Figure B.3-16. Illustration of pre-pattern process: after InGaP etchstop HCl vapor etch and composite microscope picture of the same ................................................... 314
Figure B.3-17. Illustration of pre-pattern process: after PMGI and wax dissolution and composite microscope picture of the same ................................................... 315
Figure B.3-18. Illustration of pre-pattern process: after chlorobenzened photoresist pattern definition and SEM cross section picture of the same ................................................... 316
Figure B.3-19. Illustration of pre-pattern process: after heater metallization and composite microscope picture of the same................................. 316
Figure D.1-1. Picture of vacuum chuck and deionized nitrogen cleaving setup. .... 323
Figure D.2-1. Contracted illustration of previous revision mask pattern. ............ 324
Figure D.2-2. Contracted illustration of latest revision mask pattern.................. 325
Figure D.2-3. Latest revision mask layout.......................................................... 326
Figure D.3-1. Illustration of low-temperature evaporation setup.......................... 327
Figure D.3-2. Picture of low-temperature evaporation setup. ............................. 328
Figure D.3-3. Close-up picture of cold finger assembly..................................... 329
Figure D.3-4. Picture of Molybdenum source boat for indium and illustration of its placement in the e-beam evaporator hearth............................................. 330
Figure D.4-1. Picture of low-temperature pronged copper sample mount and hooked tweezers................................................................. 331
Figure D.4-2. Picture of silicon pinching sample mount, extraction tool, and fork tool. ................................................................. 331
Figure D.4-3. Picture of evaporation shadow mask............................................. 332
Figure D.5-1. Picture of vacuum chuck bonder and keyhole tray. ....................... 333
Figure D.5-2. Pictures of transfer and pin plates, transfer fork, and metal carrier. .. 334
Figure D.6-1. Picture of previous revision bond annealer assembly.......................... 335
Figure D.6-2. Picture of latest revision bond annealer assembly............................. 336
Figure D.7-1. Picture of an example wax wetting two microscope slide gap test...... 337
Figure D.7-2. Pictures of (a) properly wet wax using latest mask pattern revision and (b) improperly wet wax (with bubbles) using old mask pattern...................... 340
Figure D.7-3. Illustration of wax wetting up side of silicon (in perspective).......... 340
Figure D.7-4. Illustrations depicting how edge wax traps bubble. ....................... 341
Figure D.7-5. Illustrations depicting how edge wax can be prevented from creating bubbles by using properly placed polypropylene beads. ...................... 341
Figure D.8-1. Pictures of the peristaltic jet etcher............................................. 342
Figure D.8-2. Pictures of the bubble etcher....................................................... 343
Figure D.9-1. Pictures of the thermal measurement setup................................... 344
Figure D.10-1. Pictures of the backside Kelvin connector apparatus (with and without sample)............................................................... 346
List of Tables

Table 1-1. List of typical semiconductor, metal, and insulator bulk thermal conductivities ................................................................. 8
Table 2-1. List of common compound semiconductor materials and their lattice constants, showing their relaxed misfit strain to silicon ........................................... 38
Table 2-2. List of thermal expansion coefficients of common semiconductors and their associated mismatch to silicon’s thermal expansion coefficient ......................... 42
Table 3-1. List of available precursor gas channels available in the MOCVD machine at UCSD .............................................................................................................. 53
Table 4-1. List of all elemental metals with low melting points ........................................... 93
Table 4-2. List of remaining common HMPM choices with respective alloy remelting temperatures ............................................................................................................ 94
Table 4-3. List of semiconductor ohmic contacts metallizations that use at least one metal from the narrowed down choices for LMPMs and HMPMs .......................... 95
Table 4-4. List of ohmic interface limited ITS alloy choices ............................................. 96
Table 5-1. List of measured bond alloy thermal conductivities ........................................ 179
Table 5-2. List of bulk thermal conductivities of typical heterogeneous bonding interface materials ............................................................................................................ 184
Table 5-3. List of measured DC resistivity for the bondmetal and gold CPW test structures both before and after annealing ................................................................. 224
Table 5-4. List of measured microwave loss and FEM loss for the bondmetal, gold, and calibration substrate CPW test structures at 40GHz both before and after annealing ........................................................................................................... 224
Table 5-5. FEM results of the TWEAM simulations .......................................................... 243
Table A-1. List of relevant metal Debye temperatures .......................................................... 285
Table A-2. List of thermal conductivity electron and phonon scattering events along with a brief description of each .................................................................................. 288
Table D7-1. List of Apiezon-W, W40, and 2:1 mix-wax properties ..................................... 338
Acknowledgements

I would first like to thank my advisors Paul Yu and S. S. Lau for the opportunity to work in their research groups, for the use of their facilities, and for acquiring funding to investigate this dissertation. I’d also like to thank the ECE department at UCSD for providing supplemental funding to complete my graduate work.

An initial feasibility demonstration of the indium-palladium bonding technique at UCSD was performed by Dongjiang Qiao, who created a functional metallization capable of bonding GaAs to silicon. The metallization recipes of this work stemmed from his early experiments. His assistance in introducing me to ITS metalbonding is greatly appreciated.

I would also like to thank Chris Niswander at Kyocera in San Diego for performing scanning acoustic microscopy tests to examine the voids in post-pattern metalbonded samples. The results of which were vital to refine metalbonding procedures.

I would especially like to thank my wife Jamie and our family for their support throughout the years, without which, I would have given up long ago.

I am very grateful to Philip Mages for training me how to grow using MOCVD and for introducing me to the world of waferbonding.

I am greatly indebted to Arthur Clawson for our endless discussions on MOCVD growth, bonding, and research in general. His knowledge in this area is vast, and his dedication to this field is inspirational. I can only hope to enjoy a future research topic as thoroughly as he has, throughout his career.
As a friend and mentor, Ivan Shubin was always willing to lend a hand, sharing many fruitful discussions on the topic of semiconductor fabrication.

Larry Grissom was always a friendly helping hand in the cleanroom. His vigilant maintenance to various cleanroom equipment, in addition to his assistance in new equipment creations, were essential to the successful execution of this dissertation.

I’d also like to thank past and present group members and fellow grad students for their theoretical and practical research assistance. Special thanks go to David Aplin, Clint Novotny, and Peng Chen for their insightful discussions on research in general.

This research was funded in part by National Science Foundation Grant No. ECS0307247 and by BAE/APTI, as well as an ECE Departmental Fellowship.

Vita

1999-2000
Research & Development Engineer
Branson Ultrasonics Corporation in Danbury, Connecticut

2000
Assistant Process Engineer
Texas Instruments in Dallas, Texas

2001-2002
Undergraduate Teaching Assistant
Rochester Institute of Technology in New York

2002
Bachelor of Science, Electrical Engineering
Rochester Institute of Technology in New York

2004
Master of Science, Electrical Engineering (Applied Physics)
University of California, San Diego

2004-2005
Graduate Teaching Assistant
University of California, San Diego

2005
Consultant
Maxwell Technologies, Inc. in San Diego, California

2008
Doctor of Philosophy, Electrical Engineering (Applied Physics)
University of California, San Diego

Publications and Presentations

Papers:


the IEEE International Microwave Photonics Topical Meeting, Victoria, BC Canada, pp.157-159 (2007).

Presentations:

Posters:
• “Electrical characterization of III/V-silicon metal waferbonding,” MRS conference (Spring 2006).
• “Travelingwave electroabsorption modulator RF design,” ANSOFT’s Leading Insight (Fall 2006).
• “Microwave design and analysis of a travelingwave optical modulator,” UCSD (2007).

Awards


Eagle Scout
Sparse Gallium Arsenide to Silicon Metal Waferbonding for Heterogeneous Monolithic Microwave Integrated Circuits

by

Justin Robert Bickford

Doctor of Philosophy in Electrical Engineering (Applied Physics)

University of California, San Diego, 2008

Paul K. L. Yu, Chair

S. S. Lau, co-Chair

Waferbonding is a technique that integrates different semiconductors together, in order to obtain hybrid structures that exploit the strengths of each material. Work was done at the University of California at San Diego to investigate the waferbonding of III/V compound semiconductors to silicon using a metal interface. GaAs and other III/V compound semiconductors surpass silicon in their ability to create high performance microwave devices, while silicon offers an inexpensive platform with a proven digital architecture that can interface with microwave devices and support
passive components and driver circuitry. Intimate integration of the two will be required, as mixed RF/digital and optical/digital systems for communications devices such as cell phones, wi-fi, and optical communications systems are pushed smaller, faster, and to higher power. The metalbonding implementation of a proposed heterogeneous monolithic microwave integrated circuit (HMMIC) system was investigated, and was shown to extend the capabilities of existing homogeneous monolithic microwave integrated circuit (MMIC) systems. The main goals of this work were two-fold; first to implement a robust heterogeneous integration technique, and second, to show that this approach uniquely improves upon existing microwave integration technology.

The metalbonding technique investigated sparsely integrated GaAs structures onto silicon, in pursuit of this HMMIC scheme. Both bottom-up and top-down fabrication methods were implemented. These approaches required the development of a myriad of meticulously designed fabrication procedures capable of avoiding the many incompatibilities between the compound semiconductor, bondmetal, and silicon materials.

The bondmetal interface, provided by these techniques, broadens the scope of existing monolithic microwave integrated circuit technology design possibilities. Essential bond interface properties were measured to establish the performance of this heterogeneous integration method. Passive bond test structures were designed, fabricated, and measured to extract the bond interface electrical behavior, electrical contact resistivity, and thermal conductivity. The In-Pd alloy, employed as the bondmetal interface between these GaAs/silicon test structures, provided a universal
ohmic contact between all doping combinations. The bond interface contact resistivity between n-type GaAs and p-type Si was found to be $1.03 \times 10^{-5}$ ohm-cm$^2$ and a bondmetal thermal conductivity of 2.51 W/m-K was also determined. In addition, passive un-bonded and bonded microwave waveguides were constructed to test the microwave propagation properties of the bondmetal. The characteristics of these test structures qualified the metalbonding technique for use in heterogeneous microwave systems. The successful fabrication of these structures demonstrated that this metalbonding method could be extended to active devices as well, which would be of similar size, form factor, and utilize the same fabrication methods. An un-bonded active microwave waveguide, similar to one which could become common in heterogeneous microwave systems, was investigated to illustrate its unique microwave properties. This un-bonded traveling wave PIN semiconductor waveguide propagated microwaves in a ‘slow-wave’ manner, as a consequence of its diode structure.
1 Introduction

1.1 General Microwave Integration Motivation

Microwave systems used to consist of expansive, bulky, waveguide based components; however, the majority of this architecture has now been replaced by Monolithic Microwave Integrated Circuit (MMIC) technology. This technology can reduce system size and weight, as well as provide an avenue to create more sophisticated systems at a lower cost.\textsuperscript{1} The size reduction yields smaller interconnects between devices which reduce parasitic reactances and allow higher bandwidths to be achieved.

1.2 Proposed HMMIC Implementation

An approach to providing the next step of MMIC system performance is proposed in the form of a heterogeneous monolithic microwave integrated circuit paradigm (HMMIC). A basic illustration of such technology is presented in Figure 1-1. High performance, compound, semiconductor microwave devices can be seamlessly integrated with silicon (Si) digital interpretation and control circuitry to form a heterogeneous monolithic microwave integrated circuit. This is accomplished by fabricating arrays of microwave devices on compound semiconductor wafers, while high-resistivity silicon (HR-Si) wafers are fabricated with the mating digital and analog support architecture. This can be done by using standard Bipolar/Complimentary Metal Oxide Semiconductor (BiCMOS) processing techniques. After completion, individual compound semiconductor microwave devices (or groups of devices) are tested and separated from
their host. Pick-and-place methods are used to populate the silicon host wafer with these microwave devices.\textsuperscript{2,3} The metalbonding techniques outlined in this thesis provide an optimal means to attach these devices without degrading their physical properties. Finally, traditional silicon metallization steps conclude the integration process and standard test, separation, and packaging completes the HMMIC devices.

Figure 1-1. Example illustration of the HMMIC scheme.

### 1.3 Bonding Introduction

The goal of bonding is to integrate two or more materials together, to obtain the advantages of both, without degrading either materials’ properties. This dissertation focuses on realizing HMMIC technology via a metal waferbonding technique.

#### 1.3.1 General Bonding Procedure

This generic bonding procedure is applicable to all forms of bonding.

1. Both samples are readied for bonding and cleaned thoroughly.
2. An optional interface material (or interlayer) may be applied to one or both of the mating samples’ surfaces.
3. Both samples are oriented to each other and placed in contact.
4. The sample pair is then heated while pressure is applied to create a permanent bond.
5. After cooling, processing continues to fabricate the hybrid device into its final form.

1.3.2 Types of Bonding

Bonding can take on several different forms within three basic categories, based on their interface material. These categories include no interlayer (direct bonding), insulating interlayer, and metal interlayer bonding, all of which will be introduced within this subsection.

1.3.2.1 No-interlayer Bonding (Direct Bonding)

Direct bonding is performed with no interlayer. Because bonding requires intimate contact between surfaces – with no interlayer to cushion any particle or defect contamination on the surfaces – obtaining a satisfactory yield from this type of bonding is challenging. This type of bonding supports heterojunction bond interfaces, but unless sample surfaces are prepared and bonded in an ultra high vacuum, surface states will significantly influence the band bending.\(^4,5\) This generally results in a non-linear, diode-like electrical behavior, even when not desired – such as when highly doped semiconductor surfaces are bonded, in an attempt to form ohmic connections.\(^6,7\) One bonus however, stemming from the lack of an interlayer, is this bonding technique’s superior heat dissipation. In bonded device situations, the thermal conduction is first limited by substrate and the interface materials, then by the bulk device material. The lack of an interface means that this contribution would be eliminated, giving direct
bonded devices the highest possible thermal performance. If the thermal conductivity of this interface can offset the poor thermal conductivity of directly integrated SiGe device material, then the bonding route would provide more efficient thermal conduction that traditional SiGe on silicon.

**1.3.2.2 Insulating-interlayer Bonding**

Insulator bonding is aptly performed with using an insulating interlayer, whether it be silicon-Oxide (SiOx), silicon-nitride (SiNx), or benzocyclobutane (BCB) (or other adhesive). Generally these materials can plastically deform around surface particles, or other protrusions, making it significantly easier to achieve higher yields than direct bonding. Due to the electrical properties of these materials, the interface will form an electrical barrier between the two bonded layers (with the exception of special adhesives containing metal suspensions). This insulating layer not only forms an effective electrical resistance, it is also a poor thermal conductor as seen in Table 1-1. This thermal insulation restricts the power handling capabilities of insulator bonded devices.

**1.3.2.3 Metal-interlayer Bonding**

Metalbonding is performed using a metallic interlayer, and depending on the specific properties of the metalbonding procedure, the bondmetal can deform around protrusions to achieve similar yields as insulator bonding. Generally, this metal will form either Schottky contact interfaces (which could be useful for MESFETs), or ohmic contact interfaces, both of which are discussed in the bond interface electrical behavior chapter. They could also form Schottky contacts on one side of the interface and ohmic contacts on the other. The electrical properties of metals would allow the interface to
spread or transfer current laterally, as well as normal, to the surface encompassing the traits of both interconnects and contacts. Metals typically have a high thermal conductivity which would provide efficient heat transfer across the interface. The metal interface would propagate DC, as well as high speed electrical signals. Although not investigated in this dissertation, the use of the metal interlayer as an optical reflector for optoelectronic devices is also a possibility.⁹

1.4 Specific Motivation for the Metalbonded HMMIC Approach

It is restricting to create entire transceiver systems using traditional MMIC. “[Traditional] monolithic microwave integrated circuits are not without some disadvantages, when compared with hybrid MICs or other type of circuitry. First, MMICs tend to waste large areas of relatively expensive semiconductor substrate [on passive components]… Because their small size limits heat dissipation, [traditional] MMICs cannot be used for circuits requiring more than moderate power levels.”¹ A heterogeneous monolithic microwave integrated circuit approach would provide a much wider design space for transceiver systems. These improvements may be categorized into three main groups: those gained by having the microwave devices fabricated on separate substrates, those gained by a heterogeneous system layout, and those gained by the unique opportunities afforded by the bonding process itself.

1.4.1.1 Advantages of Separate Substrates

There are several benefits to fabricating devices on separate substrates. Different substrate materials could be used to fabricate devices optimized for different purposes (i.e.: gallium arsenide (GaAs) for power and speed, gallium nitride (GaN) for maximum
power, indium-gallium arsenide (InGaAs) based on indium phosphide (InP) for maximum speed).\textsuperscript{10} High-speed, high-power microwave devices are generally needed in transceiver front-ends as transmit/receive switches, power amplifiers, mixers, and local oscillator sources. Today, GaAs based materials dominate high-speed, high-power, low-noise transceiver systems because of their unique properties and available high quality growth substrates. The most important and unique properties are their high electron mobility, large direct bandgap (in comparison to Si), and heterojunction device capability.\textsuperscript{11} Silicon-germanium (SiGe) is showing a promising future in the mm-wave frequency range as well, but suffers from higher noise and lower power gain as compared to GaAs and InGaAs/InP based devices – it will most likely never have the capability to exceed the speed of InGaAs/InP based devices.\textsuperscript{10}

The separate substrates idea extends to different structures grown on different substrates, using the same materials but optimized for different functions. Microwave compound semiconductor device performance depends on the material characteristics. Traditional, single substrate MMICs have a finite range of device materials, thickness, and doping, which limit the possible device outcomes.\textsuperscript{10} For example, in the HMMIC scheme heterojunction bipolar transistors (HBTs), Pseudomorphic high-electron mobility transistors (p-HEMTs), and metamorphic high-electron mobility transistors (m-HEMTs) could be made from the same starting material on different substrates and would require different processing optimizations for each. This cannot be accomplished in a standard MMIC process.

In addition, each microwave device may be tested before placing it into the circuit. One bad device would not ruin an entire circuit, as it would only waste the area
taken up by the footprint of that one device on the source substrate. The best devices could be relegated to systems requiring the most demanding specifications, with the remaining devices being used in more tolerant systems.

One final advantage of fabricating microwave devices on different substrates deals with process engineering. Given that all of the devices on the source substrate are identical, their fabrication could be optimized for device performance or yield, more so than traditional MMICs, which have a multitude of device architectures to balance.

### 1.4.1.2 Advantages of Silicon Architecture

High power compound semiconductor devices would benefit greatly if their heat dissipation could be improved. Table 1-1 lists the thermal conductivity of common semiconductor and bonding materials. The thermal conductivity of typical BiCMOS grade Czochralski (CZ) grown silicon is 148W/m-K, while the thermal conductivity of float-zone (FZ) grown HR-Si could be slightly higher due to their lack of impurities. This is in stark contrast to the thermal conductivities of GaAs and InP, at only 48W/m-K and 74W/m-K, respectively. The heat extraction of traditional MMIC is limited by the thermal conductivity of its substrate, but with the right integration technique, the high thermal conductivity of Si could improve the heat extraction from compound semiconductor devices. Although SiGe can be more or less directly integrated with Si, it suffers from a thermal conductivity much lower than GaAs at only 12W/m-K. This would be a severe disadvantage for high power SiGe-Si HMMIC devices.
Table 1-1. List of typical semiconductor, metal, and insulator bulk thermal conductivities.

<table>
<thead>
<tr>
<th>Material Type</th>
<th>Material</th>
<th>Thermal Conductivity (W/m-K)</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Metals:</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Ag\textsuperscript{12}</td>
<td>429</td>
</tr>
<tr>
<td></td>
<td>Cu\textsuperscript{12}</td>
<td>401</td>
</tr>
<tr>
<td></td>
<td>Au\textsuperscript{12}</td>
<td>317</td>
</tr>
<tr>
<td></td>
<td>In\textsuperscript{12}</td>
<td>81.6</td>
</tr>
<tr>
<td></td>
<td>Pd\textsuperscript{12}</td>
<td>71.8</td>
</tr>
<tr>
<td></td>
<td>Sn\textsuperscript{12}</td>
<td>66.6</td>
</tr>
<tr>
<td></td>
<td>Pb\textsuperscript{12}</td>
<td>35.3</td>
</tr>
<tr>
<td><strong>Semiconductors:</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Si (FZ)\textsuperscript{13}</td>
<td>168</td>
</tr>
<tr>
<td></td>
<td>Si (CZ)\textsuperscript{12}</td>
<td>148</td>
</tr>
<tr>
<td></td>
<td>Si (CZ)\textsuperscript{13}</td>
<td>156</td>
</tr>
<tr>
<td></td>
<td>GaAs\textsuperscript{14}</td>
<td>48</td>
</tr>
<tr>
<td></td>
<td>GaAs\textsuperscript{15}</td>
<td>44.5</td>
</tr>
<tr>
<td></td>
<td>GaAs\textsuperscript{16}</td>
<td>44</td>
</tr>
<tr>
<td></td>
<td>InP\textsuperscript{17}</td>
<td>74</td>
</tr>
<tr>
<td></td>
<td>InP\textsuperscript{16}</td>
<td>68</td>
</tr>
<tr>
<td></td>
<td>SiGe\textsuperscript{18}</td>
<td>12</td>
</tr>
<tr>
<td><strong>Insulators:</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>sapphire\textsuperscript{19}</td>
<td>46</td>
</tr>
<tr>
<td></td>
<td>SiOx bulk\textsuperscript{20}</td>
<td>1.37</td>
</tr>
<tr>
<td></td>
<td>SiOx bulk\textsuperscript{21}</td>
<td>1.23</td>
</tr>
<tr>
<td></td>
<td>SiOx thin film\textsuperscript{12}</td>
<td>1.29</td>
</tr>
<tr>
<td></td>
<td>SiOx thin film\textsuperscript{22}</td>
<td>1.1</td>
</tr>
<tr>
<td></td>
<td>nitrogen (air)\textsuperscript{12}</td>
<td>0.026</td>
</tr>
</tbody>
</table>

Relegating passive components and support hardware to the Si substrate would provide a big improvement in size reduction, and ultimately speed. Bonding compound semiconductor microwave devices to a completed Si host as a back-end process would mean that most of the transceiver architecture can be fabricated using the more mature, well controlled, and much cheaper Si processing technology.

The biggest disadvantage to using typical Si, as a microwave system substrate, is its associated loss. This loss comes from the poor background doping limit afforded by standard BiCMOS grade Si CZ growth process. Fortunately, this disadvantage can be curbed by using a Coplanar Waveguide (CPW) based circuit design instead of a
microstrip design, and adding an insulating layer between the coplanar lines and substrate to achieve lower loss.\textsuperscript{24} However, these insulating layers, whether silicon-oxide, nitride, or air, all drastically reduce heat transfer to the substrate, thus lowering the power handling capability of the microwave system. A better approach would be to choose a more highly resistive (HR) substrate such as sapphire or HR-Si. Unfortunately, sapphire has a poor thermal conductivity, slightly worse than GaAs. The silicon oxide used by reference 25 to bond silicon devices to sapphire, suffers from a very poor thermal conductivity, which would not be well suited to dissipate heat from high power devices. Silicon on sapphire technology is limited in device design by its silicon based device scheme. The sapphire substrate serves merely as a low loss microwave device support and cannot be used to add system functionality. Silicon’s low carrier mobility, in comparison to compound semiconductors, restricts device speed. In addition, the bandgap engineering capabilities of silicon are inferior to compound semiconductors as well. Therefore silicon based technologies cannot compete with a fully heterogeneous architecture. The added cost and minor system improvements provided by silicon on sapphire technology restrict its use to specialized applications.

Float-zone grown HR-Si substrates have already been introduced as a viable new MMIC substrate, capable of taking advantage of the long history of silicon technology without the associate microwave system loss.\textsuperscript{26} Their dielectric loss is comparable to GaAs if their resistivity remains above about 2.5kOhm-cm\textsuperscript{27} – modern HR-Si wafers are manufactured with resistivities greater than 10kOhm-cm\textsuperscript{28,29}.

Coplanar Waveguide and microstrip technology behave fairly similarly, with respect to both conductor and dielectric loss and impedance for similarly sized
conductors. CPWs have several advantages: less cross-talk, they do not require ground vias, and they also have no need for substrate thinning. Additionally, they have design flexibility, allowing them to change size while maintaining impedance.\textsuperscript{30,31,32} Shrinking the CPW to achieve smaller size comes at a cost of higher loss, but when increased in size, can have a smaller loss than microstrip designs. This means that the Si host can use traditional processing techniques without the need to add special microwave process steps and still maintain, or improve upon, standard microstrip MMIC performance.

Traditional MMIC real estate consists mostly of wasted space between devices, and between support hardware (as well as between devices and support hardware), which could be reduced using HMMIC. It should be noted that some of this space is necessary to reduce crosstalk, caused by the shared ground plane of traditional MMIC microstrip designs. A majority of this space could be reduced by switching to a CPW based architecture.\textsuperscript{24} If the silicon architecture were providing the microwave device biasing, traditional parasitic reactances caused by off-chip bias feeds would be eliminated. The same argument can be extended to the device level, where the unique bonding opportunities of HMMIC technology would allow microwave devices to be placed directly on top of, or immediately adjacent to, support devices.

If the bonding process and HR-Si substrates could be obtained at an affordable cost, HMMICs could enjoy a cost savings over traditional MMICs. Currently, 6-inch undoped GaAs wafers cost approximately as much as 6-inch HR-Si, while 3-inch InP are roughly 7 times more expensive.\textsuperscript{33} Barring excessive integration costs, this would translate into an obvious cost reduction for InP/HR-Si devices. It is unclear whether the cost of HR-Si will become significantly cheaper that GaAs in the future, though the trend
is heading in that direction. Traditional CZ grown non-HR-Si is currently about 5 times cheaper than that of HR-Si of comparable size. Another avenue for cost savings, of both InP/HR-Si and GaAs/HR-Si devices, stems from fabrication cost. It is more expensive to fabricate devices on GaAs or InP than it is on standard Si. Since this sparse integration technique requires fewer GaAs and InP wafers, due to the HR-Si architecture, the need for compound semiconductor fabrication would be equally sparse. That is to say, that with a sparse 10% of devices (or subsystems) coming from GaAs, a single GaAs 6-inch wafer could supply the needs of up roughly 10 6-inch silicon wafers – the term "roughly" is used to depict the slightly smaller available device area afforded by circular wafers. Since the cost of HR-Si fabrication would be comparable to that of standard CZ Si, if the cost of adding this metalbonding process to the queue can be kept low enough, the cost of manufacturing HMMICs could be comparable, or even better, than traditional MMICs. This is in addition to the added functionality afforded by HMMIC technology.

1.4.1.3 Novel Device Concepts

Using the metalbonding technique, described in this dissertation, to enable the HMMIC concept, allows for the inclusion of novel device concepts not technically feasible using ordinary monolithic fabrication techniques. Any design concept that requires, or would be improved by, a metal layer underneath a microwave or optoelectronic device, as well as, ready access to the topside, could be implemented using bonding. This is in stark opposition to traditional one-sidedness of monolithic fabrication techniques. With the advent of both topside and bond-side connectivity, metalbonded HMMICs technology could be extended to multiple stacked layers.
The combination of topside and bond interface contacts could allow novel connection schemes for transceiver systems, by providing otherwise unrealizable connections between microwave devices and support architecture. Bond-side contacts could efficiently connect microwave devices to Si support devices directly below. Topside contacts to bonded microwave devices would be possible using traditional monolithic metallization procedures, where wire-bonds or special metallization procedures would not be required.

The bonding technique implemented in this dissertation can easily be extended from singular bond contacts to multiple contact bonds – the metal bond contact need not be continuous. This would add connection functionality to microwave devices, such as simultaneously providing separate source, drain, and/or gate connections to underlying Si architecture, from a single bond-side of a transistor.
Having both topside and bond-side metal contacts means that bonded devices could support a bonded-microstrip waveguide design. The microwave properties of a continuum distributed pin structure (Traveling Wave Electroabsorption Modulator) are very similar to a bonded device design. The behavior of which is discussed in the bonded device microwave properties chapter. This design would be able to support higher breakdown fields than CPW device designs. Electronic devices breakdown first in their highest electric field regions. In CPW structures, this would typically be along the device surface, between the signal and ground lines. In bonded-microstrip structures, this would similarly occur along the signal to ground line surface path, before it occurred within the bulk device material itself as shown in Figure 1-2. The surface path of bonded-microstrip devices could be made arbitrarily long, by simply bonding devices wider than otherwise
necessary. The device breakdown mechanism of such wide devices would shift from a low threshold surface phenomenon, to a higher threshold bulk phenomenon, thus increasing the power handling capabilities of HMMIC microwave devices. It should be noted that this improvement would be pertinent to lumped element microwave devices with similar bonded-microstrip architecture as well.

With the advent of a CPW based Si architecture, a designer could easily transition back and forth, between CPW and bonded-microstrip circuit designs, to augment a typical layout scheme’s functionality.

Heterogeneous microwave integrated circuit implementations of this metalbonding technique have been illustrated thus far, but the same bonding technology would be immediately amenable to hybrid optoelectronic integration instead of, or in addition to, heterogeneous microwave integration.

1.5 Scope of the Dissertation

This introduction has thus far proposed the metalbonding HMMIC concept and described the motivation for expanding standard MMIC technology. The next several chapters describe topics related to bonded device fabrication, in order to illustrate the feasibility of this technique.

The first chapter titled ‘Stress and Strain’ introduces some general stress and strain theory, highlights what role they play in both forms of semiconductor integration (growth and bonding), and explains the reasons for choosing bonding over growth.

The ‘MOCVD Epitaxy’ chapter provides a glimpse into the art of Metalorganic Chemical Vapor Deposition (MOCVD). It introduces basic growth theory, noting the
capabilities and limitations of the MOCVD reactors at UCSD and discusses approaches to escape those limitations. In addition, the MOCVD epitaxial material metrics used at UCSD in the pursuit of growing bondable material, are described. The chapter also introduces the key growth effects that affect bonding and describes how the final recipe used produces bondable grown material.

Finally, the chapter titled ‘ITS Bonding Theory’ introduces the theory behind the specific type of metalbonding used in this dissertation. It will also describe the choice of metal alloy used, and the alloy formation behavior relevant to this type of bonding.

These introductory chapters are followed by the ‘Implementations of the ITS Bonding Technique’ chapter which chronicles both the top-down and bottom-up metalbonding approaches, investigated at UCSD, and describes the capabilities and limitations of each.

The final three chapters characterize the relevant physical properties of the bond interface. The beginning of each chapter presents some rudimentary theory before the details of each chapter’s focus are discussed. These theory sections also provide the reader with the context necessary to appreciate the discussion sections.

Bond interface electrical characterization is the first chapter in this section which introduces some basic metal-semiconductor interface theory and discusses the universal ohmic behavior of the bond interface. It then goes on to describe the measurement and analysis of the interface contact resistivity and its importance.

The second chapter in this section, ‘Bond interface thermal conductivity’ introduces some basic heat transfer theory, delves into basic thermal conduction theory, and discusses the thermal conductivity measurement and analysis of the bond interface.
Finally, the ‘Bonded device DC and microwave measurements’ chapter introduces some basic microwave waveguide theory and discusses the analysis of propagating microwave signals, in both CPW and bonded-microstrip configurations. In addition, detailed descriptions of both the preliminary DC and microwave characterization of an un-bonded structure, as well as the microwave properties of a bonded structure, are discussed. The chapter is concluded with a discussion of pin continuum loaded-line waveguide devices via the measurement and analysis of a similarly designed un-bonded Traveling Wave Electroabsorption optoelectronic Modulator (TWEAM) device.

The ‘conclusions and future work’ chapter recaps the relevant discoveries made in the pursuit of this dissertation and relates them to the main goal of providing a metalbonding approach for the proposed Heterogeneous Monolithic Microwave Integrated Circuit paradigm. Suggestions of future work are offered in the latter part of this chapter.

1.6 Writing Style

The diverse topics involved in bonding are very wide in extent and deep in breadth. So as not to get overloaded with unnecessary details, only the key points of those topics that relate to the bonding method will be discussed in the main body text. Extensive appendices are provided for the reader to refer to, where clarification is required, while references to external texts will articulate details beyond the scope of this dissertation.
1.7 References


25. Peregrine Semiconductor, San Diego, California, USA.


27. *ibidem* reference 18, chapter 8.

28. Siltronic AG, Munich, Germany.


33. Silicon Quest International, Santa Clara, California, USA.
2 Stress and Strain

2.1 Introduction

Defects caused by integration stress can adversely affect the electrical and structural properties of bonded HMMIC devices. Thus, the effects of stress and strain must be considered during heterogeneous integration processes. In order to choose the best integration method, the stresses involved with both growth and bonding must be understood.

This chapter introduces stress and strain background information integral to heterogeneous integration as a whole. Section 2.2 provides definitions and theory related to stress and strain, while section 2.3 discusses their relevance to common forms of integration.

2.2 Stress and Strain Theory

This section introduces the principles of the general stress/strain model to briefly familiarize the reader with the terminology used throughout this dissertation. Detailed discussion of the topic is deferred to textbooks dealing with the subject, such as reference 1.

2.2.1 Definition of Strain

Strains represent changes in geometry due to forces acting on a body. Figure 2-1 depicts the strain modes a body is allowed to have.
Figure 2-1. Illustration of the normal and shear strains allowed in a unit body under (a) isotropic dilation and (b) rhombohedral distortion.

A change in strain is defined by its associated change in length.

\[
d\varepsilon = \frac{dl}{l}
\]

Therefore, strain itself is defined as the sum of this, divided by the change in length

\[
\varepsilon = \frac{\ln \left( \frac{l_1}{l_0} \right)}{l} = \ln \left( \frac{l_1}{l_0} \right) = \frac{l_1 - l_0}{l_0}
\]

The logarithm term is the true strain, while the approximation is called the engineering strain. The approximation leading to the engineering strain representation is valid when the strains are small. For simplicity, this dissertation will use engineering strain. The general strain tensor is as follows:

\[
\varepsilon = \begin{bmatrix}
\varepsilon_{11} & \varepsilon_{12} & \varepsilon_{13} \\
\varepsilon_{21} & \varepsilon_{22} & \varepsilon_{23} \\
\varepsilon_{31} & \varepsilon_{32} & \varepsilon_{33}
\end{bmatrix}
\]

When the frame of reference is oriented to one of the principle directions, the strain tensor may be written with the more familiar look,
where $\varepsilon_{ii}$ are the principle strains and $\gamma_{ij} = 2\varepsilon_{ij}$ the shear strains.

### 2.2.2 Definition of Stress

Stress describes the forces acting on a body. Figure 2-2 illustrates the possible stress states a body may encounter.

Figure 2-2. Illustration of the normal and shear stresses in a unit body creating (a) isotropic dilation and (b) rhombohedral distortion.

The general stress tensor is as follows:

$$\sigma_{ij} = \begin{bmatrix} \sigma_{11} & \sigma_{12} & \sigma_{13} \\ \sigma_{21} & \sigma_{22} & \sigma_{23} \\ \sigma_{31} & \sigma_{32} & \sigma_{33} \end{bmatrix}$$

The tensor may be broken up into normal stresses $\sigma_{ii}$ and shear stresses $\sigma_{ij}$, similar to the strain tensor.

Stress is related to strain through the concept of elasticity, which may be described generally, by a fourth rank stiffness tensor.
\[ \sigma_{ij} = C_{ijkl} \epsilon_{kl} \]  

(2-6)

However, when considering the symmetry of tensor algebra, both the stress and strain tensors have unnecessary duplicate shear values \( \epsilon_{ij} = \epsilon_{ji} \) and therefore the density of the stress tensor may be drastically reduced. If the strains are relabeled, \( \epsilon_1 = \epsilon_{11} \), \( \epsilon_2 = \epsilon_{22} \), \( \epsilon_3 = \epsilon_{33} \), \( \epsilon_4 = 2\epsilon_{23} \), \( \epsilon_5 = 2\epsilon_{13} \), and \( \epsilon_6 = 2\epsilon_{12} \) and the stress tensor is replaced similarly (except without factors of 2), the giant stiffness tensor may be replaced by a much smaller stiffness second rank tensor (or matrix) transformation,

\[ \sigma_i = C_{ij} \epsilon_j \]  

(2-7)

or compliance matrix transformation.

\[ \sigma_i = S_{ij} \sigma_j \]  

(2-8)

Note that these new relations are more compact, but due to a loss of completeness, do not follow the general rules of tensor algebra.

Symmetry in the system will force many of the stiffness constants to be zero. When this occurs, the stiffness matrix becomes sparse. This sparseness, specifically for isotropic materials, yields the familiar stress/strain relations.

\[ \epsilon_1 = \frac{1}{E} \left[ \sigma_1 - \nu (\sigma_2 + \sigma_3) \right] \]  

(2-9)

\[ \epsilon_2 = \frac{1}{E} \left[ \sigma_2 - \nu (\sigma_1 + \sigma_3) \right] \]  

(2-10)

\[ \epsilon_3 = \frac{1}{E} \left[ \sigma_3 - \nu (\sigma_2 + \sigma_1) \right] \]  

(2-11)

and
\[ \varepsilon_4 = \frac{1}{G} \sigma_4 \]  
\[ \varepsilon_5 = \frac{1}{G} \sigma_5 \]  
\[ \varepsilon_6 = \frac{1}{G} \sigma_6 \]

where \( E \), \( \nu \), and \( G \) represent the elastic constants: Young’s modulus, Poisson ratio, and Shear modulus respectively.

Stress and strain are linked through materials properties alone. Stress may therefore only be controlled by altering the imposed strain or the material’s properties.

### 2.2.3 Uniaxial and Biaxial Stress

Uniaxial stress is a mode of stress whereby forces act to stress a body in only one direction, while the second and third directions are left to react. The forces are assumed uniform throughout the body and thus impart no shear. Figure 2-3b illustrates the strain state of a uniaxially stressed cube.

![Figure 2-3. Illustrations of (a) a uniaxially strained cube and (b) a biaxially strained cube.](image)

Equations 2-9 to 2-11 describe the strain state of a uniaxially loaded body as:
\[ \varepsilon_1 = \frac{1}{E} [\sigma_1] \quad 2-15 \]

\[ \varepsilon_2 = \frac{1}{E} [-\nu \sigma_1] \quad 2-16 \]

\[ \varepsilon_3 = \frac{1}{E} [-\nu \sigma_1] \quad 2-17 \]

Note how the Poisson ratio acts to strain the body in the unloaded directions.

Biaxial stress is a mode of stress whereby forces act to stress a body in two directions while the third is left to react. Just as with the uniaxial case, no shear stresses are involved. Figure 2-3c illustrates the biaxial strain state of a biaxially loaded cube.

Equations 2-9 to 2-11 describe the strain state of a biaxially loaded body as:

\[ \varepsilon_1 = \frac{1}{E} [\sigma_1 - \nu \sigma_2] \quad 2-18 \]

\[ \varepsilon_2 = \frac{1}{E} [\sigma_2 - \nu \sigma_1] \quad 2-19 \]

\[ \varepsilon_3 = \frac{1}{E} [-\nu (\sigma_2 + \sigma_1)] \quad 2-20 \]

Multiplying \( \varepsilon_2 \) by \( \nu \), and adding the result to \( \varepsilon_1 \) yields

\[ \varepsilon_1 + \nu \varepsilon_2 = \frac{1}{E} [\sigma_1 - \nu \sigma_2 + \nu \sigma_2 - \nu^2 \sigma_1] = \frac{1}{E} \left( \frac{\sigma_1}{1 - \nu^2} \right) \]

which may be rewritten in terms of \( \sigma_1 \) as

\[ \sigma_1 = \frac{E}{1 - \nu^2} (\varepsilon_1 + \nu \varepsilon_2) \quad 2-22 \]

similarly,

\[ \sigma_2 = \frac{E}{1 - \nu^2} (\varepsilon_2 + \nu \varepsilon_1) \quad 2-23 \]
2.2.4 Thermal Expansion Induced Stress

Temperature acts to dilate materials by changing their interatomic spacing via thermal expansion. In-depth descriptions of this phenomenon may be found in standard solid state theory texts.\textsuperscript{2,3,4,5}

Thermal expansion acts on bodies according to

\[ dl = \alpha dT \]

where \( \alpha \) is the material’s thermal expansion coefficient. This coefficient is generally a function of temperature,\textsuperscript{6,7} but if the material does not change phases, small changes of temperature may be approximated by a constant expansion coefficient.

Laminations composed of materials with differing thermal expansion coefficients produce internal loading upon changes in temperature. These loads may be represented by normal and shear stress distributions within the lamination. To understand how this comes about, a simplified version of a lamination is provided in Figure 2-4.
Figure 2-4. Illustrations of a heterogeneous lamination undergoing thermal stress: (a) un-bonded state at room temperature, (b) bonding at bond temperature, and (c) thermally strained at room temperature.

This specific representation depicts a waferbonding situation, but the general phenomenon is universal. Figure 2-4a shows the two bodies placed on top of each other, at rest, at room temperature. In Figure 2-4b, bond linkages are formed after the sample pair is raised to a bonding temperature. Figure 2-4c illustrates how these linkages become loaded when the structure is returned to room temperature. Note that the bodies themselves have attempted to shrink to their natural shape but are being pulled into a new equilibrium by the linkages. Also note that the center linkage has not changed while the exterior linkages have been elongated and bent. The fact that the center linkage behavior differs from the outer ones, indicate a non-constant stress distribution. If there were a
continuum of linkages connecting the two bodies and they had an infinite stiffness – corresponding to a bond – then the linkages would impart stress in the two bodies. Where the linkages try to elongate, a pealing stress is imparted. If this pealing stress becomes too great, the linkages (aka bond) will fail and the bodies will separate. Where the linkages try to bend, a shear stress is imparted. This shear stress radially pushes on one body and radially pulls on the other. These forces act to biaxially compress one of the bodies and biaxially tension the other. Note that at the center of the structure the bodies feel the influence of the entire radius of shear forces, while at the edges of the structure there are no radial forces acting on the bodies. This describes the inner and outer limits of biaxial stress in the system. Suhir has analyzed the two-dimensional stress distributions induced by a temperature change in a bi-metallic strip.\textsuperscript{8} The stress distribution behavior is illustrated in Figure 2-5. A stress calculation of a three dimensional axi-symmetric laminated disk would more accurately depict the real situation, but be less intuitive. Such a model would yield similar behavior.

![Figure 2-5. Illustration of the vertical stress distribution in a thermally stressed lamination.](image)

A crude model of the maximum biaxial thermal stress in each body may be found with a few assumptions. For simplicity, the bodies will be assumed to be well bonded and unloaded at a reference temperature $T_0$, and the system is increased to some
temperature $T'$ which is $\Delta T$ higher than $T$. Figure 2-6 illustrates the main forces acting on a biaxially loaded body, while the opposing body must appose these forces equally if the system is to stay in equilibrium.

$$F_a^\parallel + F_b^\parallel = 0$$ \hspace{1cm} 2-25

Figure 2-6. Illustration of segments within a heterogeneous lamination undergoing thermal stress.

Body-a is assumed to have a higher thermal expansion coefficient than body-b $\alpha_a > \alpha_b$. A region at the center of body-a experiences own body’s thermal expansion influence but is withheld by body-b’s mechanical influence such that its net expansion is,

$$\delta_a^\parallel = \delta_{a\_Thermal}^\parallel - \delta_{a\_Mechanical}^\parallel = \frac{1}{2} \alpha_a \Delta T_a' - \frac{F_a^\parallel l_a'}{2E_a w_a' h_a'} \hspace{1cm} 2-26$$

where $l_a'$, $w_a'$, and $h_a'$ are the dimensions of the body-a at temperature $T'$ and are defined as

$$l_a' = l_a + \delta_a^\parallel \hspace{1cm} 2-27$$
Since the length and width are identical, the material is assumed to have an isotropic thermal expansion $l'_a = w'_a$. Also, body-b may be defined in the same way, therefore, the biaxial expansion in each body is given by

$$\delta_a^\parallel = \frac{1}{2} \left( \alpha_a \Delta T l'_a - \frac{F_a^\parallel}{E_a h'_a} \right)$$  \hspace{1cm} 2-28

and

$$\delta_b^\parallel = \frac{1}{2} \left( \alpha_b \Delta T l'_b - \frac{F_b^\parallel}{E_b h'_b} \right)$$  \hspace{1cm} 2-29

In order for the two bodies to stay connected without sliding in reference to each other, their lengths and widths must remain the same. Thus

$$l'_a \equiv l'_b \rightarrow \delta_a^\parallel = \delta_b^\parallel \rightarrow \alpha_a \Delta T l'_a - \frac{F_a^\parallel}{E_a h'_a} = \alpha_b \Delta T l'_b - \frac{F_b^\parallel}{E_b h'_b}$$  \hspace{1cm} 2-30

Since the forces $F_a^\parallel$ and $F_b^\parallel$ must be equal and opposite, Equation 2-30 may be rewritten as

$$F_a^\parallel = \left( \frac{\alpha_a - \alpha_b}{E_a h'_a} \right) \Delta T l'_a + \frac{1}{E_a h'_a}$$  \hspace{1cm} 2-31

$F_a^\parallel$ may separately be written in terms of stress $\sigma_a^\parallel$ as

$$F_a^\parallel = \sigma_a^\parallel l'_a h'_a$$  \hspace{1cm} 2-32

Thus the biaxial stress in body-a $\sigma_a^\parallel$ may be written

$$\sigma_a^\parallel = \frac{(\alpha_a - \alpha_b) \Delta T E_a}{1 + \frac{E_a h'_a}{E_b h'_b}} \quad \text{and} \quad \sigma_b^\parallel = -\frac{(\alpha_a - \alpha_b) \Delta T E_b}{E_b h'_b + 1}$$  \hspace{1cm} 2-33

since $h'_a \approx h_a$ and $h'_b \approx h_b$. 

This brief derivation is quite crude and could be off by as much as a factor of two, from the real maximum biaxial stress in bodies-a and b, but their behavior is very enlightening. Then if the Young’s modulus of both bodies are approximately equal, the extreme cases may be evaluated as

\[
\sigma_u^\parallel = \begin{cases} 
(\alpha_a - \alpha_b) \Delta T E_a, & h_a \ll h_b \\
\frac{1}{2} (\alpha_a - \alpha_b) \Delta T E_a, & h_a = h_b \\
0, & h_b \gg h_b
\end{cases}
\]

Note that the biaxial stress in each body respectively becomes negligible – its thickness becomes very large while the thin body’s biaxial stress approaches a constant value. The zeroes are not meant to be deceiving, they simply represent a negligible state of stress.

2.2.5 Definition of Strength

Strength is generally defined as the capacity of a body to withstand influence. A specific definition must; however, reflect context. In this dissertation, strength will describe how much stress can be tolerated before bonded device performance degrades. The term ‘degrade’ is qualitative and may manifest itself both electrically and structurally. Any materials integration process that imparts strain can nucleate defects. These defects decay material properties that may be key to device operation. To understand this mechanism some basic background must be given.

2.2.6 Defects

Defects in this context are dislocations in the crystal lattice of semiconductor materials. All defects effect the movement of electrons in a crystal and may act as
electron donors or acceptors, as scattering sites, or recombination centers. Types of dislocations include point defects, line defects, and planar defects. Discussion of point defects is reserved for last.

2.2.6.1 Line Defects

Line defects are the manifestation of body dislocations. The dislocation direction and magnitude are described by the displacement vector (commonly known as the Burger’s vector). These defects originate and propagate via shear stresses. Line defects come in one of two categories: edge or screw. Examples of these are shown in Figure 2-7.

![Figure 2-7. Illustrations of the two types of line defects: (a) an edge dislocation and (b) a screw dislocation.](image)

Edge defects are defined as abrupt, one dimensional shear dislocations, perpendicular to a line of atoms – the Burger’s vector is perpendicular to the dislocation. Screw defects are defined by dislocations parallel to a line of atoms. Other line defects are simply compositions of the two. Line defects may extend to the edge of a material (where the dislocation is no longer defined) or connect to themselves or others via dislocation loops.
2.2.6.2 Planar Defects

Planar defects are compilations of line defects. An example of a planar defect is shown in Figure 2-8. They may exist at grain boundaries, twin boundaries, or domain and anti-domain boundaries. Though there are many types of planar defects, those that define grain boundaries are the most pertinent to this dissertation.

![Illustration of a planar defect.](image)

A grain is defined as a distinct crystal lattice, within a solid, with a single orientation. Neighboring grains may have different orientations and/or consist of different alloy compositions. The compilation of line defects that make up the grain boundaries depend on the orientation and composition of the neighboring grains.

2.2.6.3 Point Defects

Point defects come in several varieties within the three basic categories of vacancy, interstitial, and substitutional. Figure 2-9 illustrates two-dimensional versions of each of the three types of point defects. Vacancies are simply holes left by missing
atoms in a lattice, whereas interstitials are ‘extra’ atoms that reside within the lattice. Substitutional defects are atoms that have replaced existing atoms within the lattice.

Figure 2-9. Illustrations of the three types of point defects: (a) a vacancy, (b) an interstitial atom, and (c) a substitutional atom.

The movements of point defects are not directly influenced by bulk stresses, but interact with them through line defects. The movements of line defects are effected by nearby stress fields in the atomic lattice. Point defects create anomalies in the local atomic stress field, which effectively alter the energy required to move line defects. In addition, the collision of line defects can result in the creation or annihilation of point defects.

2.2.7 Degradation and Failure

The definition of degradation can take on different meanings depending on defect density. At a low density, defects impact the electronic properties of semiconductors.
Crystal lattice discontinuities scatter electrons leading to anomalies in semiconductor band structure. These anomalies manifest themselves as electrical states within the bandgap. Midgap electrical states can effectively lower mobility, reduce dielectric strength, and shorten carrier recombination lifetimes. The degradation of these properties is directly related to the defect density. Therefore, as the defect density increases, the performance of semiconductor devices worsen. In-depth explanations of how material properties are affected by defects, may be found in any of several common materials texts.\textsuperscript{3,4,5,9}

High defect densities structurally weaken the lattice, altering its stress response. Dislocations can move under the influence of stress. Dislocations that collide may either annihilate or proliferate. Since annihilation requires precise dislocation alignment, it is rather rare. It is much more typical for colliding dislocations to grow. This movement is collectively called plastic deformation and is the basis for the definition of mechanical yield strength.\textsuperscript{1}

As defect densities increase further, they begin to form fissures throughout the material. This defines the realm of mechanical failure.

### 2.2.8 Defect Nucleation and Critical Thickness

Defects nucleate when local strain energy exceeds the energy required to create a dislocation. Strain energy is defined as

\[
U = \frac{1}{2} \sigma_{ij} \varepsilon_{ij}
\]
where the lack of energy indices implies tensor contraction by addition. The energy required to create a dislocation depends on how it is made. People and Bean$^{10}$ define the required energy as

$$U_{\text{defect}} = \left( \frac{Gb^2}{4\pi nb} \right) \ln \left( \frac{h}{b} \right)$$

where the creation is defined by the shear dislocation of a few atoms $n$ by their Burger’s vector $b$. Here, it is assumed that a dislocation, only a few interatomic spacings long, is enough to create a stable defect.

If a strain field

$$f = (\alpha_s - \alpha_0) \Delta T$$

acts on a thickness of material to cause a defect to be born in this way, then a critical thickness associated with that field may be defined. This critical thickness for defect nucleation is defined by People and Bean as

$$h_c = \frac{b(1-\nu)}{32\pi(1+\nu)f^2} \ln \left( \frac{h_c}{b} \right)$$

Note that the critical thickness is a function of the material’s interatomic spacing and Poisson ratio $\nu$, as well as the applied strain field. Thus, for a specified strain field, the materials’ properties alone dictate the critical thickness.
A general critical thickness behavior is depicted in Figure 2-10. Below the critical thickness line, defects do not nucleate, and above this line, they are allowed to nucleate. Hence, thin layers can withstand much higher strains than thick layers. Because of the vague nature of the dislocation nucleation energy, this equation can predict defect nucleation behavior, but cannot predict their onset accurately. Other authors\textsuperscript{11,12,13} have published similar variations, but they all have the same end result.

2.3 Types of Integration Strain

Two main categories of strain are present in the realm of integration: interfacial strain and bulk strain. This section will define and describe both types, as well as illustrate their implications for both (growth and bonding) forms of integration.
Reference 14 provides additional information regarding the effects of stress on waferbonding.

### 2.3.1 Integration Borne Interfacial Strain

Interfacial strain can occur between different materials or identical materials. They exist in both growth and bonding, but the role of interfacial strain in growth is only non-trivial when integrating different materials. This sub-section’s discussion will chronicle the role of interfacial strain as it relates to heterogeneous growth. This is followed by a discussion of how it relates to heterogeneous and homogeneous bonding.

During growth, precursor material settles in the lowest energy region locally available. This typically correlates with the substrate crystal lattice. Generally, different materials have different lattice constants as evidenced by Table 2-1.

Table 2-1. List of common compound semiconductor materials and their lattice constants, showing their relaxed misfit strain to silicon.

<table>
<thead>
<tr>
<th>Material</th>
<th>Lattice Constant (Å)</th>
<th>Relaxed misfit strain referenced to silicon (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Si</td>
<td>5.431\textsuperscript{16}</td>
<td>-</td>
</tr>
<tr>
<td>GaAs</td>
<td>5.65315\textsuperscript{17}</td>
<td>4.09</td>
</tr>
<tr>
<td>Ge</td>
<td>5.658\textsuperscript{16}</td>
<td>4.18</td>
</tr>
<tr>
<td>InAs</td>
<td>6.05838\textsuperscript{17}</td>
<td>11.55</td>
</tr>
<tr>
<td>InP</td>
<td>5.8697\textsuperscript{18}</td>
<td>8.08</td>
</tr>
</tbody>
</table>

As the epitaxial material builds in thickness its desire to converge to its own natural lattice spacing competes with its desire to match the spacing of the substrate. As a result, the epitaxial layer’s crystal lattice distorts to accommodate both, as illustrated in two dimensions by Figure 2-11. Figure 2-11a illustrates an example of pseudomorphic growth, while Figure 2-11b illustrates metamorphic growth.
For three dimensional cubic crystal structures, this is called tetragonal distortion. Equations 2-33 may be used with the thermal strain field replaced by a lattice mismatch strain field

$$f = \frac{a_{\text{epilayer}} - a_{\text{substrate}}}{a_{\text{substrate}}}$$

Further discussion of this will be continued in the growth chapter. As long as the layer stays below its critical thickness, pseudomorphic growth is allowed to continue. Once the critical thickness is reached, the lattice gives way to defects, and the onset of metamorphic growth ensues. As the layer grows even thicker, these defects continue to propagate and more defects are born as strain energy is added.

Since these defects result in poor electrical behavior, epitaxial materials that are too highly mismatched cannot be grown to a usable thickness. This limits the variety of materials that can be integrated via growth. Compound semiconductor materials such as InP and GaAs cannot be grown on Si with a satisfactorily low defect density. Their
lattice constants are too highly mismatched, as evidenced by the misfit column of Table 2-1.

Besides a few tricks with non-traditional growth,\textsuperscript{21,22} it is currently very difficult to alter the stress situation, except to either stay below the critical thickness, or cope with the inevitable dislocations of metamorphic material. Both alternatives limit device performance.

During heterogeneous bonding, the materials involved are grown separately, without the complication of lattice mismatch. When they are joined, the interface absorbs all the lattice misalignment via local defects and dangling bonds in the interface, without affecting the bulk materials as illustrated in Figure 2-12.

![Figure 2-12. Illustration of the interfacial strain between two heterogeneously bonded materials.](image)

The bulk materials then maintain their typical materials properties, unimpeded by the integration.

It should be noted that while the material bulk maintains its native properties, the interface defects and point defect dangling bonds result in midgap states and locally bend
the band structure.\textsuperscript{23} A related electrical phenomenon is described in the metal-semiconductor contact theory of the bond interface electrical behavior chapter.

Interfacial strain is not limited to heterogeneous growth or bonding – it can also occur at the interface of two like materials. This occurs when the two materials’ crystal orientations are twisted, or tilted, in relation to each other, as illustrated in Figure 2-13, and can occur in both hetero and homogeneous bonding.\textsuperscript{21}

Figure 2-13. Illustration of the interface between two mis-oriented homogeneously bonded materials.

Interfacial strain in bonding does not profoundly affect bulk material properties due to its range of only a few monolayers. This is in stark opposition to heterogeneous integration by growth, where the defects propagate through the bulk material. Interfacial strain can also occur when bonding both dissimilar and similar materials.
### 2.3.2 Integration Borne Bulk Stress

Bulk strain can occur in integration during heterogeneous growth, but stems from interfacial strain caused by lattice mismatch. Bulk strain occurring in integration during heterogeneous bonding stems from a difference between the constituent materials’ thermal expansion.

GaAs or InP bonding to silicon represent situations that would be common during HMMIC fabrication. Microwave device materials would be grown on their respective substrates. These compound semiconductor materials’ thermal coefficients of expansion (TCE) are higher than that of silicon as shown in Table 2-2.

<table>
<thead>
<tr>
<th>Material</th>
<th>Thermal Expansion Coefficient (ppm/K)</th>
<th>Mismatch to Si (ppm/K)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Si</td>
<td>2.62(^6)</td>
<td>-</td>
</tr>
<tr>
<td>GaAs</td>
<td>6.03(^7)</td>
<td>3.41</td>
</tr>
<tr>
<td>InAs</td>
<td>5.20(^{24})</td>
<td>2.58</td>
</tr>
<tr>
<td>InP</td>
<td>4.56(^{25})</td>
<td>1.94</td>
</tr>
</tbody>
</table>

When bonding, the two materials are heated, joined, and cooled. This temperature schedule induces thermal stress into the bond lamination. The temperature difference between when they are joined and cooled produces a strain field that drives the thermal expansion induced stress, discussed in the thermal stress theory section.

For simplicity the thermal stress theory section ignored moments induced by the compression and tension body stresses \(F_{a}^{||}\) and \(F_{b}^{||}\). This assumption resulted in stress distributions that were constant throughout the lamination thickness. If the lamination is allowed to bend, the induced moments tend to redistribute the strain fields as the
lamination bows. The result is a non-uniform stress distribution along the lamination thickness. Chu\textsuperscript{26} has studied the bending of semiconductor wafers in response to loading.

Figure 2-14. Illustrations of thermally stressed laminations in bending: (a) a lamination prevented from bending via external forces, (b) a lamination freely bending, and (c) a lamination with negligible bending.

Figure 2-14 depicts a few results of these induced moments – the vertical axis represents the perpendicular distribution of lateral stresses. Figure 2-14a depicts a situation where bending is prevented by external body forces. This matches the assumption made earlier. In Figure 2-14b, the lamination is allowed to freely bend. If the structure survives being bent enough, the biaxial stress may flip sign within the material. The sign depicts whether the biaxial stress state is compressive or tensile. The regions where the stress passes through zero are called the neutral axes. The neutral axes may reside within the bodies as depicted in case-b or outside the bodies as depicted in the
The neutral axes for the extreme case of a are an infinite distance away. A real case would typically reside between the two.

When one of the bodies is thinned in comparison to the other, it cannot impose as much stress on the thicker one. When waferbonding, the samples start off un-bonded at room temperature. Once they reach the annealing temperature, the bond is formed. Only once the sample cools does the thermal stress become induced in the wafers. Thus, at room temperature (after bonding) the lamination is in equilibrium where the forces of each substrate are balanced by the other. If one of the bodies is thinned, the system must stay in balance via

$$F_a^{||} + F_b^{||} = 0 \quad \rightarrow \quad \sigma_a^{||} \frac{h_a'}{h_a} = -\sigma_b^{||} \frac{h_b'}{h_b} \quad \rightarrow \quad \sigma_a^{||} = -\sigma_b^{||} \frac{h_b'}{h_a}$$  \hspace{1cm} 2-40

Thus as body-a is thinned, its stress increases in comparison to body-b’s. As a result, the bending moment becomes negligible as shown in Figure 2-14c. Note that the lack of a strong bending moment yields a uniform distribution of stress, just as in case-a, but without requiring external forces. Note, also, that the thinning redistributed the stress within the lamination by shifting the stress from the thicker body to the thinner body. Thus the thinner body is experiencing a higher state of stress than it had originally, as evidenced earlier by Equation 2-33. Thin films can withstand this increase once they exist below the critical thickness; however, they may not necessarily survive the thinning process itself. The thermal stress involved in substrate bonding limits the bonding temperature of GaAs on Si to approximately 160-200° C.  \(^{14}\)

There are only two ways to reduce thermally induced bonding stress. Either the choice of materials must be restricted to those that share similar TCEs or the bonding
temperature must be lowered to lower the thermally induced strain. This dissertation focuses on the latter. The details of which will be discussed in the ITS theory chapter.

2.3.3 Integration Method Comparison

Integration by growth is inherently limited in its choice of materials by lattice mismatch. The material choices when bonding are less restrictive as the stresses involved follow Equation 2-33. This bonding stress is limited by the materials’ thermal expansion coefficients and the minimum bonding temperature. Thus, if the bonding temperature could be made arbitrarily small, then the variety of bondable materials would be arbitrarily wide.

2.4 Conclusion

Although interfacial stresses generally exist in semiconductor integration, the majority of stress issues associated with bonding are related to bulk stresses. Growth techniques are largely affected by interfacial stresses that cannot be avoided, whereas bonding techniques are more accommodating to the bulk stresses that may occur. Because the bonding process places fewer restrictions on the types of materials it can integrate, in comparison to growth, it is clear that integrating materials via bonding would be the more effective means of producing HMMIC.
2.5 Reference


3 MOCVD Epitaxy

3.1 Introduction

The metalorganic chemical vapor deposition (MOCVD) reactor used during this investigation has the capability to allow bondable semiconductor materials to be grown. It is essential to have a solid understanding of basic MOCVD theory and metrics, in order to properly control epitaxial growth. The growth of bond material requires more strict control than that of traditional devices. While it is acceptable for traditional device materials to exist with various defects, many of those same defects are not tolerable in bondable material.

Section 3.2 introduces the basic theory of the form of growth employed during this investigation, while section 3.3 highlights relevant topics associated with the particular MOCVD machine used at UCSD. Sections 3.4 and 3.5 discuss the characterization and subsequent control of growth parameters required to achieve bondable growth material. An overview of the resulting procedure followed to grow this material is presented in section 3.6.

3.2 MOCVD Basics

The acronym MOCVD stands for metalorganic chemical vapor deposition, although over the years, several names have been used (ie. OMVPE, meaning organometallic vapor phase epitaxy, or other such rearrangements). MOCVD growth proceeds from semiconductor source material that is provided by metalorganic gas phase
compounds. This source material is transported in gas-phase to the surface of a seed crystal at which point the vapor decomposes. These compounds react to form elemental semiconductor ions in the presence of a host seed crystal and proceed to attach to said crystal, thus growing an epitaxial film. A detailed introduction to MOCVD growth may be found in reference 1.

The advantage of this method lies in the fine control afforded by the gas nature of the growth precursor material. This control allows epitaxial layers to be grown with near atomic resolution. From a device perspective these layers are engineered well enough to control quantum effects in crystals, producing a wide design landscape.

Figure 3-1. Illustration of a rudimentary MOCVD machine.

Figure 3-1 presents a crude illustration of a rudimentary MOCVD machine with a computer controlling many (if not all) of the aspects of material growth. Carrier gas enters the system on the left and enters a bubbler, which picks up group-III precursor material, whose flow rate is controlled by a mass flow controller (MFC). This combination gas then proceeds to the mixing manifold. Gas from a bottle containing
group-V precursor material is sent through a separate MFC and into the mixing manifold as well. Carrier gas is then sent through a third MFC, directly into the mixing manifold for dilution. These routes are called channels and can be independently controlled. The mixing manifold combines the gasses from each of the channels and sends them either through a bypass line or into the reactor containing the sample. When the source gasses are passed over the sample, a heater heats a susceptor which the sample rests on. This raises the temperature of the nearby gas and initiates the decomposition of precursor gasses to commence the growth process. Unused gas residue is then sent to a vacuum pump to control the reaction chamber pressure. The noxious gasses are then fed through a scrubber system (not shown) that extracts the toxic components before the remaining gas is sent through a ventilation shaft. This describes the essential workings of an MOCVD machine, but in actuality there is a lot of supporting hardware not shown in the diagram. Also, a typical MOCVD machine would have several group-III and group-V channels, in addition to dopant lines, to give the system added functionality.

3.3 MOCVD Growth at UCSD

This sub-section describes the MOCVD apparatus used for bonding at UCSD. The capabilities and limitations of the machine are discussed as they relate to growing bondable material.

3.3.1 Specifications of the MOCVD Machines at UCSD

Figure 3-2 shows a picture of the MOCVD machine used to grow bondable compound semiconductor material at UCSD. The system was originally built by General Air, Inc. but has been heavily modified to suit growing needs. It is capable of growing
materials within the In-Ga-As-P system. Source materials include trimethyl-indium (TMIn), triethyl-gallium (TEGa), Arsine (AsH3), and phosphine (PH3) compounds as well as both diethyl-zinc (DEZn) and silane (SiH4) dopants.

Figure 3-2. Picture of the metalorganic chemical vapor deposition (MOCVD) machine used at UCSD. The reaction chamber is a single sample horizontal design. Samples up to 25mm x 20mm may be grown at a time; however, 1cm x 1cm pieces are favored. Susceptor heating is provided by a high intensity halogen lamp capable of heating the sample to about 700°C.
3.3.2 UCSD MOCVD Capabilities and Limitations

This machine has several advantages and disadvantages associated with its design, as outlined below. The ramifications of these are discussed in the final growth procedure and pre- and post-pattern bonding procedures.

3.3.2.1 Capabilities

Table 3-1 lists the available source gas channels. DEZn provides p-type doping, while SiH4 provides n-type doping. Doping is used in the manufacturing of bonding material for the interface contact resistivity measurements. Unused gas lines may be used to balance flows and pressures entering the reactor, to minimize turbulent flow.

Table 3-1. List of available precursor gas channels available in the MOCVD machine at UCSD.

<table>
<thead>
<tr>
<th>Precursor Type</th>
<th>Precursor Gas Channels</th>
</tr>
</thead>
<tbody>
<tr>
<td>group-III:</td>
<td>3x triethyl-gallium (TEGa)</td>
</tr>
<tr>
<td></td>
<td>2x trimethyl-indium (TMIn)</td>
</tr>
<tr>
<td>group-V:</td>
<td>3x arsine (AsH3)</td>
</tr>
<tr>
<td></td>
<td>1x phosphine (PH3)</td>
</tr>
<tr>
<td>dopants:</td>
<td>1x silane (SiH4)</td>
</tr>
<tr>
<td></td>
<td>1x diethyl-zinc (DEZn)</td>
</tr>
<tr>
<td>extra:</td>
<td>2x hydrogen (H2)</td>
</tr>
</tbody>
</table>

The computer control system and gas manifold can switch gasses in or out of the reactor with a resolution of about a tenth of a second. With growth rates typically on the order of 4-5Å/s this resolution is more than sufficient. The computer also controls the pressure and temperature in the reactor. TMIn channel composition verification is provided by an ultrasonic detector.

The computer control system was programmed via a universal text-based recipe writing and execution program developed by Justin Bickford and Dr. Clint Novotny. The
source code is provided in Appendix E.1. This program is much more user friendly and intuitive to use than its predecessor, and does not require the user to edit program code directly to make growth recipe changes. This avoids any coding errors that would otherwise lead to incorrect growths and inadvertent damage to the machine.

3.3.2.2 Limitations

The sample size is limited to a maximum of 20mm x 25mm and is considerably smaller if uniform material is desired – typically 1cm x 1cm. A further explanation of this will follow.

Repeatability of growth is limited by the cold-wall chamber design and the porous graphite susceptor material. Pre-growth conditioning runs are required to obtain repeatability. The cold-wall chamber design also limits the maximum epilayer thickness. Material growth on the walls builds up during growth, which flakes off after becoming too thick. These flakes limit the allowable thickness as they settle on the sample adding particle contamination.

Aluminum containing compounds could not be grown in this reactor. Without a moisture purging load-lock, it is impractical to provide an environment free enough of water vapor that would allow aluminum compounds to be grown. Aluminum precursors oxidize readily in an environment containing even a tiny amount of water vapor. Incorporation of this oxidized material in an epilayer results in electrical recombination centers and physical defects. Specifically, this eliminates the choice of AlGaAs alloys despite being the traditional etchstop material of choice in the GaAs system. Since it could not be acceptably grown in the MOCVD systems at UCSD during this
investigation, a lattice matched InGaP etchstop layer was chosen instead. The etch selectivity of known etchants – both wet and dry – are more selective between GaAs and InGaP\textsuperscript{2,3,4} than GaAs and AlGaAs\textsuperscript{5,6}. This turns out to be an advantage during the etch-back process after bonding. This assumes that the difficulties associated with growing InGaP are overcome. Considerable effort was expended to include this InGaP etchstop layer in the growth. InGaP grows in an ordered manner at typical growth temperatures – this ordering produces a texture which makes bonding difficult. This layer was grown at a low temperature to yield a smooth texture. Also, chemically abrupt interfaces at the InGaP-on-GaAs and GaAs-on-InGaP growth transitions improve crystal quality; gas interrupts were successfully used to improve these interfaces. Proper control of the InGaP composition lead to a closely lattice matched etchstop epilayer, which was required to grow a low crystal defect density GaAs epilayer.

Having no load-lock also means the loading environment is not clean. This presents a difficulty in supplying particle free growth substrates to the reactor, increasing the chances of pre-growth particle contamination.

Also, the mass flow controllers are not immune to temperature variations in the surrounding room air. Tight control of the room air temperature is essential to maintaining stable growth conditions. Temperature instabilities perturb the lattice matching condition as well as the growth rate.

\section*{3.4 Growth Metrics}

Several metrics are used to evaluate epitaxial material. These metrics provide valuable feedback to alter later growths. Several common metrics are discussed within
this subsection. The focus of which is to provide compound semiconductor source material capable of being bonded.

### 3.4.1 Nomarski Microscopy

The most valuable tool to qualify material is a well trained eye. Aided by a Nomarski microscope, the eye is capable of discerning minute surface variations via phase interference contrast. This allows the user to glean information about surface topography by seeing effects from particles and scratches, defects, and stress. Discussions of each category could fill multiple dissertations; however, identification and behavior are best provided by training and repeated growth trials. The study of how growth parameters affect surface morphology defines the art behind the science of MOCVD growth. It is important to minimize all causes of such defects, to grow material with the best opportunity to bond successfully. The next section will discuss the effects defects have on bonding.

A few key features will be highlighted below. For the sake of brevity, each particular feature category will be introduced by a minimal set of pictures and a short description of each.
3.4.1.1 Particles and Scratches

Figure 3-3. Nomarski interference contrast image of (a) organic and (b) particle pre-growth contamination.

Particles originate from external sources such as pre-growth contamination or chamber flaking. The example in Figure 3-3 shows one type of pre-growth contamination. Similarly, scratches may be discerned and can occur either before or after growth.
3.4.1.2 Crystal Defects

![Nomarski interference contrast images of crystal defects](image)

Figure 3-4. Nomarski interference contrast images of crystal defects, including: (a) 'diamond' defects, (b) 'oval' defects, (c) ordering texture, and (d) teardrop-like hillocks (TDLH).

Figure 3-4 presents just a few examples out of the plethora of possible crystal defects. Crystal defects may spawn from missing or extra compounds, memory effects, preexisting substrate dislocations, as well as many other sources.

3.4.1.3 Stress Dislocations

Stress induced dislocations can alter local growth rates leading to periodic undulating textures. Examples of these are shown in Figure 3-6. Typically these features are easier to see in person than in pictures. The effect can range from slight lattice mismatch ‘cross-hatch’ to extreme metamorphic growth.
Figure 3-5. Nomarski interference contrast images of (a) light ‘cross-hatch’ mismatch and (b) extreme metamorphic growth

3.4.2 X-Ray Diffraction

The second most valuable qualification tool is x-ray diffraction (XRD). XRD can yield important strain information about a sample. As stated in the stress and strain chapter, minor lattice mismatch leads to pseudomorphically strained epitaxial films. This strain can be measured using XRD. In-depth discussions on x-ray diffraction theory may be found in solid-state theory books such as references 7 and 8, while exhaustive discussions of measurement and analysis techniques may be found in references 9, 10, and 11.

3.4.2.1 High-Resolution X-Ray Diffraction

Figure 3-6 presents a picture of the Philips\textsuperscript{12} double/triple crystal x-ray diffraction machine used to qualify epilayers at UCSD. This machine provides high resolution x-ray diffraction (HRXRD) data.
Raw x-rays emanate from the copper target x-ray cathode ray tube source. The x-rays proceed through a network of x-ray diffractions, collectively called the collimator (the first crystal). These diffractions let only a highly collimated and narrow wavelength spectrum of x-rays pass through to the remainder of the system as a beam of x-rays. The beam may be cropped by a selection of beam forming slits to control its cross section. This refined x-ray beam may then diffract off of the sample (the second crystal). Any diffracted x-rays can be picked up by an x-ray detector. The detector may have an additional series of diffraction elements in front of it (the third crystal) to confine the detector’s angular view of the sample’s diffracted x-rays. Blocking slits may be used to narrow the angular view in place of or in addition to the third crystal.
X-rays will only diffract off of the sample’s epitaxial layer if the angle of the layer and the x-ray wavelength meet the diffraction criteria of the sample. A simplistic view of this may be provided by kinematic analysis using Bragg’s law

\[ n\lambda = 2d_{hkl} \sin(\theta) \]  

where \( d_{hkl} \) represents the reciprocal space diffraction plane spacing, corresponding to the plane orientation \( <hkl> \), which may be represented by

\[ d_{hkl} = \frac{a}{\sqrt{h^2 + k^2 + l^2}} \]

Here, an isometric crystal type is assumed – the representation of the reciprocal space plane spacing for a hexagonal or other crystal type may be found elsewhere.\(^9,10\)

Pseudomorphically strained layers lead to tetragonal crystal distortion which can be represented using

\[ d_{hkl} = \frac{1}{\sqrt{\frac{h^2}{a^2} + \frac{k^2}{c^2}}} \]

Where \( a \) is the lateral lattice constant and \( c \) is the normal – meaning perpendicular – lattice constant.

The Bragg condition represents only the minimum requirement for x-ray diffraction. The crystal’s atoms’ scattering potentials and the lattice’s structure factor must also support the diffraction at the investigated Bragg angle. This angle must also exist within the realm of measurable diffraction angles. The diffracted rays must emanate from the sample surface within the measurement plane without propagating into the sample. X-rays diffracted into the sample, rather than out, cannot be measured by the detector. The measurement plane is simply the plane coplanar to the source, the sample,
and the detector. This plane is the domain of the incident and diffracted x-ray beams measurable by the detector.

Thus far, the representation has been that of the kinematic theory of diffraction, where only the interaction of the incident x-rays and the individual lattice atoms have been included. This kinematic regime describes the basic diffraction that occurs in crystals whereas the more involved dynamical theory includes the interaction of incident and diffracted x-ray waves within a sample.\textsuperscript{14,15,16} The complexity of the entire dynamical theory is beyond the scope of this dissertation; however, a few key results do apply.

The intensity was left out of the kinematic discussion because growth analysis can typically get by with only a few rules about intensity, as discussed in the strain analysis section below. The dynamical theory, however, presents a much more accurate description of the intensity than would a kinematic theory approach, and gives way to rocking curve fringes and lobes.

The paths of the x-rays are affected by the different material layers in a finite crystal. These paths interfere, resulting in fringe patterns at the detector. They only become clearly noticeable if the epilayers have abrupt transitions. Smearred transitions result in poor x-ray wave reflection definition resulting in incoherent interference. The fringe pattern is essentially the Fourier transform representation of the physical strain structure of the sample.
3.4.2.2 Strain Analysis

A typical x-ray measurement technique used to analyze epilayers is a rocking curve measurement. The detector is trained on a single order of a particular diffraction while the sample is rocked through the Bragg angle. The resulting peak, or peaks, resolved in the plot, contain information about the strain structure of the sample.

Figure 3-7 shows two x-ray diffraction rocking curve plots of different sample structures. Figure 3-7a shows a substrate peak and a single mismatched epitaxial layer
peak. Figure 3-7b shows the substrate peak and several lobes associated with a mismatched superlattice. The insets illustrate simplified versions of the physical structure of the single epitaxial layer and superlattice.

Various publications have written about the analysis of x-rayed films. Fewster offers an instructive review of several techniques. Only a few of the more pertinent portions of the plots of Figure 3-7 are presented here. The first things to note about the single epitaxial layer plot are the differences between the two peaks. The most obvious is that the substrate peak and epitaxial layer peak do not overlap. This is due to the minor tetragonal distortion pervaded by the pseudomorphic lattice mismatch. The strain of the epitaxial layer may be deduced from this angular difference. The strain may either be calculated via the tetragonally distorted diffraction spacing directly or for small angles from a differential form of the Bragg condition,

\[ \epsilon_\perp = -\Delta \theta \cot \theta \]  

3-4

where \( \Delta \theta \) represents the angular difference between the two peaks. Note that the strain indicated here is the perpendicular strain of the tetragonally distorted lattice corresponding to

\[ \epsilon_\perp = \frac{c-a}{a} \]  

3-5

The relaxed representation of this stress is

\[ \epsilon = \frac{a_e - a_i}{a_i} \]  

3-6

where \( a_e \) represents the relaxed lattice constant of the epitaxial layer if it were not bound by the substrate, and \( a_i \) represents the relaxed lattice constant of the substrate. It is
assumed that the epilayer is much thinner than the substrate, such that the layer imposes a
negligible amount of stress on the substrate. $\varepsilon_\perp$ is related to $\varepsilon$ by

$$
\varepsilon = \varepsilon_\perp \left( \frac{1-n}{1+n} \right)
$$

The second observation of Figure 3-7a is that the substrate peak is intense and
narrow, while the epitaxial layer peak is broader and less intense. The width and
intensity are factors of the crystal quality, the diffractometer angular resolution, and the
layer thickness.

Crystal quality plays a big role in the resulting width and intensity of the
diffracted beam. The diffracted beam width is dependent on the sum of angles visible to
the input x-ray beam. A finite input intensity diffracted into a wide angle lowers the
maximum intensity of the distribution. In addition, any input intensity lost to regions that
do not meet the diffraction criteria, will be lost, reducing the output beam intensity
further. If the x-ray beam encompasses several crystal grains, each with different
orientations, the distribution of crystal orientations will be rather wide. A bowed crystal
could also create a distribution of crystal orientations.

Angular resolution also adds to the diffracted beam width by having a blurred
angular perception. The diffractometer has a minimum resolution limited by the ability
of the collimator to select a narrow wavelength of x-rays, as well as the emanating
beam’s angular dispersion. The x-ray spectrum bandwidth imposes a non-finite range of
wavelengths that, through the Bragg condition, yields a spectrum of diffraction angles.
Each detector receiving slit and/or third crystal collimator, adds its own influence to the angular resolution.

Layer thickness provides the final addition to the beam width and loss to intensity. The uncertainty in the layer’s angle is dictated by the thickness of the epitaxial layer. The less defined the layer position (ie the thinner the layer), the higher the angular uncertainty. A thinner layer has a smaller chance of defining the layer’s angle.

Fringes and ‘extra’ peaks (lobes) are a result of the wave nature of x-rays. Faint fringes can be seen in the tails of the peaks of Figure 3-7a, while strong lobes are seen in Figure 3-7b. These lobes are due to the repeating epilayer structure of the superlattice. The periodic nature of the superlattice structure coherently adds to the x-ray wave interference pattern, thus enhancing the intensity of the lobes. Poor periodicity, or defective layers, would lead to a loss of this coherence, resulting in a loss of lobe definition. Abrupt interfaces and high strain contrast of the layers, as well as the number of layers, dictate the strength of this coherence and thus the contrast of the lobes. A full dynamical approach would be required to fully understand the intensity pattern; however, a simple model relates the peak separation of the superlattice lobes to the period thickness.$^{18}$

The separation of the lobes is dominated by the period of they superlattice

$$
\Lambda = \frac{(n_i - n_0) \lambda}{2(\sin \theta_i - \sin \theta_0)}
$$

where index $n_i$ refers to any peak excluding the reference peak $n_0$. Since the separation of the peaks is the same, the most accurate way of determining the superlattice period is to use the ensemble average peak separation when calculating $\Lambda$. 


The center lobe (typically the highest intensity) can be used, just as the single epitaxial peak was, to extract the average strain of the superlattice structure. Since all the superlattice periods are identical, this also yields the average strain for a single superlattice period $\bar{\varepsilon}_\Lambda$. If the period $\Lambda$ and average period strain $\bar{\varepsilon}_\Lambda$ of a superlattice structure can be determined, then a series of test structures may be grown to extract individual layer quantities, such as the strain and thickness of each epilayer. To illustrate this technique a generic example is presented.

If a superlattice is grown using a thickness $t_A$ of composition $A$ for one layer and $t_B$ of composition $B$ for a second layer, four unknown quantities are presented: two thickness quantities ($t_A$ and $t_B$) and two strain quantities ($\varepsilon_A$ and $\varepsilon_B$). The x-ray rocking curve of this sample can provide two quantities which include the average strain and the superlattice period. If multiple samples are grown under identical conditions, except for the change of one variable – for example the thickness $t_A$ – then the resulting quantities extracted from the second sample’s x-ray rocking curve theoretically provides enough information to extract all four original unknowns. Typically, several runs are performed to create a more robust set of data. Knowing the thickness of each layer and the time to grow would yield the growth rate of each layer, and knowing the strain of each layer may determine the composition of each layer.

### 3.4.3 Photoluminescence

Photoluminescence (PL) is the third important tool available to characterize grown material and can offer another degree of compositional understanding. PL
measurements may be either time dependent or steady-state. Only steady-state
measurements of grown material were investigated for this dissertation.

Figure 3-8. Illustration of a rudimentary photoluminescence measurement setup.

Figure 3-8 depicts a rudimentary PL measurement setup. The laser provides
intense illumination at a wavelength corresponding to an energy above the bandgap of the
investigated semiconductor material. The wavelength of this laser radiation relates to the
photon energy by

$$E_\lambda = \frac{hc}{\lambda}$$

These photons project into the sample surface where they excite valance band electrons
into the conduction band. These electrons relax down to a region near the edge of the
conduction band where they emit a photon as they transit down to states near the valance
band edge. This process is very efficient for direct bandgap semiconductors, such as
most In-Ga-As-P compound semiconductors. This is why they are preferred when
designing high performance optoelectronic devices. The photons emitted by the sample
are then captured by an optical spectrum analyzer. If the received signal is weak and
noisy, an optical chopper and lock-in amplifier may be added to enhance the signal to noise ratio of the photoluminescence signal.

The emitted photons will have an energy that corresponds to the occupation of states near the band edges. This results in a photon energy distribution with a peak that is slightly higher than the bandgap of the sample. The significance of this effect is small, in most cases, and its role will be ignored to simplify the present discussion. Thus, the peak intensity wavelength may be approximated by the bandgap energy.

\[ E_g = \frac{hc}{\lambda_{\text{peak}}} \]

Figure 3-9 shows an example PL plot of a III/V compound semiconductor epilayer structure. Note the shape of the distribution is representative of the spectrum of transition energies allowed by the conduction and valance band energy states.

![Photoluminescence vs. Wavelength](image)

Figure 3-9. Example photoluminescence plot of a III/V compound semiconductor epilayer.
Care must be taken when constructing a sample for steady-state PL analysis, as steady-state PL measurements only record the information of the final response of the system. After the electrons are excited they relax down to the first band edge they come across. Some of the electrons may transit down to the valance band of that material resulting in a photon, while others will move to the lowest bandgap material in the sample before transiting. Most photons from the higher energy transition will be re-absorbed by the lower energy bandgap material to be emitted again as lower energy photons. The result is that only the lowest energy photons will be measurable from outside the crystal, therefore, the sample must be designed so that the layer of interest has the lowest bandgap. For InP based materials – which are typically lower in bandgap than the substrate – this is usually accomplished by adding a capping InP layer on top of the target layer. However, the measurement of a target layer on GaAs – which are typically higher in bandgap – dictate the removal of the absorbing lower bandgap GaAs substrate or the growth of an even higher bandgap barrier layer between the target layer and substrate.

Surface pinning can offer an alternative route for the excited electrons if the resulting band bending provides lower conduction band states. Discussion of surface pinning may be found in the metal-semiconductor contacts section of the bond interface electrical characterization chapter. Excited electrons, drifting or diffusing to the surface, will be presented with midgap surface states that allow the electrons to non-radiatively recombine, resulting in a degraded PL response. They may be prevented by providing a barrier material at the edge of the sample that presents a higher energy conduction band than the target layer.
The excited electrons must have enough energy to transition from the valance band to the conduction band, but not such a short wavelength that the light is absorbed very close to the sample surface. If the light is absorbed too close to the sample surface, the response of the emitted photon could be distorted due to the high density of excited electrons. If the density of excited electrons is too high, either from a low wavelength or strong intensity beam, they will fill the lower conduction band states and emit photons at higher energies. This results in a smeared response and must be accounted for during analysis or reduced during measurement.

The effects of heterojunction interface band bending must also be accounted for when performing PL measurements. Heterojunction interfaces may provide conduction band troughs that could affect emitted photon energies.

3.4.4 Photoabsorption

Photoabsorption may also be used to help determine a sample’s composition. Photons of various wavelengths impinge on the sample, while a detector behind the sample measures the spectrum intensity. The transmitted spectrum may be compared with the incident spectrum to yield absorption data. This absorption spectrum provides information about the bandgap. This technique was not used due to the similar sample data available from photoluminescence measurements which was readily available.

3.4.5 Hall Measurement

This last important measurement determines the doping of semiconductor materials. Doping density and mobility measurements are accomplished via Hall measurement. Doping density without mobility information may be determined by other
electrical means, such as capacitor or diode measurements, or directly, such as secondary ion mass spectroscopy (SIMS). The electrical measurement methods determine the net effect of activated donor or acceptors, while direct method determines the donor and acceptor atom densities without regard as to whether or not they are electrically active. The discussion below will focus only on Hall measurements.

The Hall effect describes the resulting perpendicular voltage induced by current flow, in a doped semiconductor, under the influence of a magnetic field. Figure 3-10 illustrates the electronic effect of placing a bar of semiconductor material in a magnetic field under the influence of a current.

An electrical current flowing through the sample moves carriers along the \( \hat{x} \) direction. In the presence of a magnetic field, these carriers move in response to the Lorentz force according to

\[
\vec{F} = q(\vec{v} \times \vec{B})
\]

This force causes the carriers’ paths to bend. The carriers accumulate on the bottom or top, dependent upon their sign and the direction of the magnetic field. The
accumulated charges create an electric field that is measured as a Hall potential. This potential has a field given by

$$E_H = -\frac{J_B}{Ne}$$

where $N$ represents the net density of available carriers. An added conductivity measurement without the magnetic field can yield the Hall mobility. This Hall mobility is affected by electrical defects in the sample and provides a measure of the electrical quality of grown epilayers.

### 3.4.5.1 Van der Pauw Measurement

Van der Pauw proposed a method to measure the carrier density in an arbitrarily shaped semiconductor. The method essentially performs a Hall measurement by mapping the electric fields in an arbitrary sample shape to that of an ideal sample. It was intended to measure bulk semiconductor samples without having to define a specifically contrived structure to perform precise Hall measurements. With the freedom to choose arbitrary sample shapes, doped epitaxial thin films on insulating substrates, in their as grown form, are then available for Hall measurement directly, without the need for device fabrication. This is the form of Hall measurement used to determine carrier concentrations and Hall mobility during the investigation of this dissertation. The details of this measurement are discussed in the bond interface electrical behavior chapter.
3.4.6 Composition Analysis

Knowing which precursors were used to grow each investigated material and having determined the strain, and or bandgap, information from the XRD and PL measurements the alloy composition of each target material can be determined.

Figure 3-11 shows plots of various semiconductor materials’ bandgap values versus lattice constant.\textsuperscript{21} This graph effectively maps the compositions of the compound semiconductor materials to their strain and bandgap information. Accurate equations of these relationships are available in the literature, and offer a grower the ability to determine the composition of their grown material. A detailed example of this process was described by Kuphal and Pöcker who published a method to determine the composition from XRD and PL measurements.\textsuperscript{22} Their approach also included the effects of strain dependent bandgap terms.
3.5 Growth Defects Affecting Bonding

Bonding demands a much lower density of imperfections than typical device material growth. The discussion of how to achieve such bondable material is presented in this section.

3.5.1 Bonding Requirements of Grown Material

The final sample surface must be uniformly flat and free from ‘bumps’ in order to assure bonding surfaces come into intimate contact – Figure 3-12 depicts an example of this.

Material must also be grown with a very low defect density. Defects cause electrical degradations in device performance and can also create avenues for the etchants used after bonding to essentially ‘leak’ into the bond region. These leaking etchants will attack bondmetal feverishly.

Figure 3-12. Illustration (a) and image (b) of ‘bumps’ in a silicon-to-glass bond interface.
3.5.1.1 Pre-Growth Artifact Induced Defects

Defects may stem from both pre-growth artifacts and growth conditions. The pre-growth artifacts can cause bumps and crystal defects in epilayer growth via latent particles, chemical residues, scratches, and pre-existing substrate defects.

Large latent particles, protruding from the sample’s surface, clearly present bonding obstacles, but even small pre-growth particles can affect bonding. Latent particles locally enhance precursor decomposition, thus increasing local growth rate. The enhanced growth rate creates mounds that may be detrimental to bonding. The epilayer is also forced to include several crystal defects when burying particles. Even when the enhanced growth rate is not enough to produce bond preventing bumps, the resulting cluster of defects could be preferentially etched after bonding.

Organic residues can locally inhibit growth just as particles enhance it. Holes in the epilayer will not typically prevent bonding but will leave behind voids that can provide a shortcut for etchants during post-bond processing. Variations in surface oxide thickness can also alter the local growth rate. The non-uniform growth can lead to crystal defects at the borders of such anomalies.

Scratches create low regions that cannot be bonded, leaving behind voids. The edges of scratches can grow faster than field regions creating another form of non-uniformity. In addition, the object that created the scratch could have induced a crystal defect that penetrates the sample surface just as a pre-cleave nick does during sample cleaving – see the sample preparation portion of Appendix B.1.

Crystal defects native to the substrate, prior to growth, will propagate through epitaxial layers during growth. These are typically rare when using high quality
substrates. The most common of these are screw dislocations. Under certain growth conditions and substrate offcut orientations, these screw dislocations preferentially grow locally, forming hillocks.\textsuperscript{23,24,25} Fortunately these hillocks tend to have a low aspect ratio of just a few 10’s of nanometers in height over a span of several micrometers. Bond substrates are typically compliant to bumps of this small an aspect ratio and do not usually affect bonding. The defects at the center of each hillock etch faster than non-defective field area; however, the rate tends to be much lower than more serious defects, like those caused by particles.

### 3.5.1.2 Growth Induced Defects

Defects are not just due to pre-existing artifacts – they can also be caused by growth parameters, such as excess mismatch strain, MOCVD system memory effects, high doping densities, and alloy ordering effects.

The primary effect that leads to flaws is lattice mismatch – growing strained material beyond the critical thickness, will result in dislocation defects. These defects grow faster than unstrained material, and if severe enough, can create topography that inhibits bonding. As noted before, any defect will act as an etching shortcut in post-processing, and these misfit dislocations are no exception. With proper strain analysis, the control of strained material is relatively straight forward. When growing test samples, it is possible to track a trend of lattice mismatch via x-ray analysis, to avoid growing highly strained material.

Inferior epilayer growth transitions can yield dislocations as well. Growth of abrupt transitions is non-trivial. Short term memory effects can lead to inferior
epilayer-to-epilayer transitions. These transitions can create defects or increase the likelihood of creating defects in later epilayers. Several growths may be required to understand the influence of growth parameters on these transitions. Susceptor and reactor wall desorption can cause this short term memory effect and can even create long term memory effects. Long term memory effects create variable growth conditions that affect growth-to-growth repeatability.

Memory effects are not straightforward to minimize. The sample isn’t the only object that absorbs growth material within the chamber. The susceptor that the sample lays on continually absorbs and desorbs growth material as well as the chamber walls. This absorption and desorption is what gives rise to the memory effect. Depending on the amount of absorbed material this memory effect can span from layer to layer within the same growth and from growth to growth.

The degree to which the susceptor absorbs material depends on its available surface area. High porosity susceptors have more surface area than low porosity susceptors. High density bulk graphite susceptors have been used at UCSD to grow bondable material; however, better alternative materials might be SiC coated graphite or ultra-high density pyrolytic graphite.26

The degree to which the reactor wall absorbs material depends on its temperature and surface composition. Starting from a clean reactor wall, where the surfaces are cold, the decomposed precursor will condense, leaving a residue similar to that shown in Figure 3-13. Material will build up faster on surfaces where this residue has already attached.
The upstream susceptor and coated reactor wall area, to sample area ratio, dictate how much the sample will be affected by the memory effect. When material from these regions desorb, the ‘memory’ of previously grown material is released into the gas stream and becomes available to absorb onto the sample. Even the upstream sample area itself can desorb material to be re-absorbed downstream on the sample, although the effect is minor. The memory effect is quite pronounced in the horizontal reactors at UCSD, due to their large desorbing area to sample area ratio, provided by the narrow reactor tubes, long nosed (large upstream area) susceptors, and typically small sample sizes. To further complicate the issue, the effect is not uniform across the reactor cross section due to its circular shape. This results in non-uniformly grown layers that can affect device performance and bond yield.
The layer-to-layer memory effect can be reduced via a lower surface area ratio or compensated for by gas switching techniques. The growth-to-growth memory effect can be dealt with between growths through proper cleaning and pre-growth chamber conditioning. Unchecked accumulation of material between growths can produce group-III rich growth defects such as the Ga defects shown in Figure 3-4a. Severe accumulation can flake off and add particle contamination during successive growths. Commercial vertical design MOCVD reactors are not as susceptible to this memory effect due to the vertical showerhead gas flow design, wide chamber, and minimized susceptor to sample surface area ratio.

Excessive doping can also lead to growth defects. When growing doped materials, the physical dopant concentration must remain below the solid solubility limit of the semiconductor. Beyond this limit, dopant atoms can cluster into crystallites, forming defects similar to particle contamination.\textsuperscript{27}

The last growth induced defect mechanism stems from an epitaxial material’s natural texture. Some materials may be grown under conditions that produce ordered alloys.\textsuperscript{28,29,30} These alloys have a texture that does not stem from defects but rather the ordering of the alloy itself. The resulting texture could potentially affect bonding.

### 3.6 Growth Procedure

Cleaning techniques and growth optimization is a never ending series of improvements throughout the bonding investigation. However, the procedure provided in the Appendix B.1 is the final, most refined method used to produce high quality grown material for bonding. Only explanations of key parts of the procedure, relevant to
growing bondable material, will be addressed here, allowing the reader to follow along with the bonding and growth procedure appendices at their discretion.

### 3.6.1 Procedure Overview

The high-level process steps required to grow bondable samples can be described in three phases. The samples are first prepared for growth by defining their size and cleaning them. Then the growth chamber and susceptor are cleaned and conditioned in preparation for the actual sample growth. Finally, the sample is grown and the chamber and next sample are prepared for the next growth.

### 3.6.2 Pre-Growth Sample Preparation

First, an appropriate substrate doping type must be chosen. N-type substrates tend to have fewer native defects than do p-type or semi-insulating, so n-type substrates are chosen whenever possible.

Next the samples need to be cleaved and cleaned into their final pre-growth form. To prevent unnecessary repetition here, most of the detailed discussion of these processes may be found in the post-pattern process discussion section. The process has been refined to minimize the addition of particles, as well as maximize the removal of latent particles.

After particle removal, the next step removes any chemical residues before growth. Test growths have shown that any attempt to remove chemical residues, prior to growth, only lead to non-uniformities in the epilayers. More uniform and less defective epilayers were grown from untreated samples, therefore, the exposure of the samples to chemical residues prior to growth, was simply avoided. As an example, hydrofluoric acid
(HF) can remove surface oxides, but subsequent growths showed that the native oxide reformed in splotches, creating non-uniform patterns in the growth. Another example stems from solvent exposure prior to growth. This was avoided because solvent residues could never fully be removed, ultimately resulting in non-uniform growth patterns as well. This is the main reason why photoresist was never employed prior to cleaving, to prevent particle contamination; the necessary solvents to remove the photoresist always affected growth.

3.6.3 Growth Chamber Preparation

The susceptor and tube are first cleaned by stripping them of old growth to prevent gallium droplet defects (in GaAs growth), flaking, and dopant poisoning, caused by the long term memory effect.

The reactor was conditioned with a chamber conditioning growth. This was performed to produce a consistent starting condition for each growth. The transient conditions at the beginning of a growth, without this conditioning, would impact sample growth. After the reactor was conditioned, the susceptor was cleaned again to prevent gallium droplet defects during GaAs growth.

Once a clean susceptor and ‘dummy coated’ reactor wall were provided, the sample was placed in the center of the susceptor to improve uniformity. Graphite shims, shown in Figure 3-13, were used to center the sample during growth. The chamber was then pumped and purged with nitrogen, to remove as much water vapor as possible to reduce oxidation during growth. The advent of these chamber preparation and loading procedures yielded consistent, high quality epilayer films every time.
3.6.4 Sample Growth

The recipe shown in Appendix B.1 was followed to create starting material for the pre-pattern bonding method. The older, post-pattern bonding method used a similar recipe, but included a doped GaAs epilayer.

The different layer’s gas flows were padded with extra hydrogen flows from spare lines, to reduce layer to layer transition gas surges. Vent/reactor switching surges were also minimized by padding the vent line with additional nitrogen. These surges would create turbulence in the gas flow, resulting in poor interface behavior. Furthermore, layer transitions included gas interrupts to minimize layer-to-layer memory effects. Optimization of InGaP growth was necessary to minimize interface roughness and compositional intermixing at both the InGaP-grown-on GaAs interface and the GaAs-grown-on-InGaP interface. Strain of the InGaP was minimized to prevent perturbation of the lattice-match and introduction of defects into the subsequent GaAs layer structure. The InGaP etchstop layer was kept below approximately 100 arcseconds of strain mismatch to GaAs, by controlling the TMIn to TEGa ratio. The InGaP ordering was minimized to reduce texturing by growing the etchstop layer at low temperature. 585°C presented the best growth temperature for this. Higher temperatures resulted in excessive ordering texture while lower temperatures resulted in whisker growth as shown in Figure 3-14.
3.7 Conclusion

The success of bondable material growth is made possible by careful control of the MOCVD recipe. This growth recipe is developed in order to circumvent the limitations imposed by this particular MOCVD machine. Several tools, including visual inspection, x-ray diffraction, photoluminescence and Hall measurement, offer valuable feedback to create the most effective recipe for material growth. The ITS Implementations Bonding chapter will verify the bonding capabilities of this material.
3.8 References


12. Philips, now PANalytical B.V., The Netherlands


26. Poco Graphite, Inc., Decatur, Texas


4 Isothermal Solidification Metalbonding

4.1 Introduction

Isothermal solidification (ITS) metalbonding is a method for bonding materials necessary to create the HMMIC architecture. When compared to other integration methods, the ITS method provides a low-stress metal interface form of waferbonding. Although similar methods may also provide a low-stress interface, ITS has fewer limitations and is more functional. In order to achieve the most effective interface, it is imperative that the proper alloy is chosen.

This entire chapter concerns ITS metalbonding theory. Section 4.2 introduces how the ITS method works; this is followed by section 4.3 which compares this form of metalbonding with other types. Sections 4.4 and 4.5 outline the method employed to decide which particular ITS alloy to use in this investigation and highlight the importance of ITS alloy formation behavior, respectively.

4.2 Isothermal Solidification Definition

Isothermal solidification\textsuperscript{1} is also known as Transient-Liquid-Phase (TLP) metallization\textsuperscript{2} or Diffusion Soldering\textsuperscript{3,4}. ITS is a novel metallurgical method of bonding at a low temperature to form an interface that remains solid at higher temperature.
Figure 4-1 correlates each of the structural process steps of ITS bonding techniques, with the metallurgical state of the bondmetal. Layers of high melting point metal (HMPM) and low melting point metal (LMPM) are deposited on the surfaces of a bond pair. The samples are brought into contact and heated above the LMPM’s melting point. The liquid LMPM diffuses into the HMPM layers to form an intermetallic alloy by
virtue of the peritectic nature of the bond alloy. The LMPM is completely consumed in this process, resulting in an alloy that remains solid, thus bonding the two samples. The bond pair can then be cooled to RT for further processing. Because the LMPM is completely consumed in the formation of the alloy, the new melting point of the system will be defined by the resulting alloy instead of the LMPM constituent.

4.3 ITS Metalbonding Comparison

This subsection introduces other metalbonding methods and highlights the advantages of the ITS technique. ITS metalbonding has the ability to bond at a low temperature of about 160°C-300°C yet form an alloy that melts at a significantly higher temperature of about 450°C-900°C.

4.3.1 Alternative Metalbonding Methods

This subsection discusses the two other metalbonding approaches: eutectic alloy and thermocompression bonding.

4.3.1.1 Eutectic Bonding

In this bonding approach, eutectic alloys are used to form a bond between two materials. Alloy constituent metals, or the alloy itself, is deposited at the interface of the two materials. The materials are brought into contact and may be pressed when heated beyond the alloy’s eutectic temperature. The materials bond when the alloy solidifies upon cooling. An advantage of this approach is that any eutectic system may be used – there are several options to choose from. Typically solders such as Pb-Sn (melting point
~180°C) or Au-Sn\textsuperscript{5} (melting point ~280°C) are used, but the Au-Si\textsuperscript{6} system (melting point ~360°C) is also common.

4.3.1.2 Thermocompression Bonding

This approach fuses metal coated samples under high temperature, and pressure, to form a bond. Thermocompression bonding differs from eutectic bonding in that no eutectic is required. When high temperatures and pressures are applied, the mating metal surfaces deform, to mate in intimate contact and fuse together – very similar to direct waferbonding. Pb-Pb thermocompression bonding was historically the oldest form of recorded bonding.\textsuperscript{7} Au-Au\textsuperscript{8} and Cu-Cu are common; however, other metals may be used.

4.3.2 ITS Metalbonding Advantages

The ITS bonding approach has several advantages over both eutectic and thermocompression bonding. Its low bonding temperature reduces the thermal stress induced, when bonding materials with different thermal expansions. This allows a wide variety of materials to be bonded. Eutectic bonding may share this same advantage if low temperature eutectic alloys are implemented. Thermocompression temperatures are much higher and are rather restrictive of the choice of materials that may be bonded.

Because the LMPM liquefies during the ITS bonding process, only modest bond-pressures are required. This low pressure reduces damage to fragile semiconductors, such as InP, InAs, etc. This melting behavior also serves to fill voids in the bond interface improving yield. Eutectic bonding shares this same property whereas Thermocompression does not.
The thermal budget of the ITS method is quite high, with remelting temperatures in the range of 450°C-900°C. This high melting point allows the sample pair joint to tolerate high temperature processing without melting. Thermocompression typically shares this ability while eutectic bonding does not. The eutectic alloys simply re-melt, when exposed to temperatures beyond their alloy’s low melting point.

If chosen correctly the ITS alloy can attain (or surpass) the variety of materials that may be bonded using the eutectic alloy approach and yet compete with (or exceed) the thermal budget afforded by the thermocompression bonding approach. In addition, the yield of the ITS method can be quite high due to the liquid behavior of the alloy during bonding.

4.4 Choosing the Bond Alloy

The choice of alloy system is key to achieving this ideal metalbonding behavior. Reference 1 has surveyed several alloy possibilities some of which are reviewed here.

4.4.1 Choosing the LMPM

Because of the ITS low temperature bonding ability, the search of LMPMs will be limited to those with low melting points. Table 4-1 lists all the metal elements with low melting temperatures.
Table 4-1. List of all elemental metals with low melting points.

<table>
<thead>
<tr>
<th>LMPM</th>
<th>Melting Point °C</th>
</tr>
</thead>
<tbody>
<tr>
<td>Hg</td>
<td>-38.8</td>
</tr>
<tr>
<td>Ga</td>
<td>29.8</td>
</tr>
<tr>
<td>In</td>
<td>156.6</td>
</tr>
<tr>
<td>Sn</td>
<td>232</td>
</tr>
<tr>
<td>Bi</td>
<td>271.3</td>
</tr>
<tr>
<td>Tl</td>
<td>304</td>
</tr>
<tr>
<td>Cd</td>
<td>320.9</td>
</tr>
<tr>
<td>Pb</td>
<td>327.5</td>
</tr>
</tbody>
</table>

In order to avoid processing complications, only those that are solid at room temperature may be used when ruling out Br, Hg, and Ga. Though Ga technically melts above room temperature, it is too close to be considered a viable LMPM. To take advantage of the low thermal stress afforded by ITS, a metal that melts below approximately 300°C should be chosen. Melting points above ~300°C severely restrict the choice of bondable materials. This rules out Cd, Pb, and any higher melting point metals. Low melting point alloys may also be considered as LMPM choices; however, they add undue complication to the alloy kinetics and may form undesirable parasitic eutectics.\(^1,3\) In the end, the choices are limited to only In, Sn, and Bi as highlighted in the table.

### 4.4.2 Choosing the HMPM

One might expect to be able to choose any high melting point metal to fill this need; however, the choices are narrowed drastically when considering their alloy behavior, and at the very least, must form stable peritectic intermetallic compounds.\(^9\) Many high melting point metals alloy with In, Sn, and Bi into peritectics, others may
create eutectics, and still others may simply form heterogeneous mixtures, rather than intermetallic compounds.\textsuperscript{1}

Further narrowing the choices are the resulting alloy’s re-melting temperature, which must be high enough to support subsequent high temperatures from contact annealing, interconnect metallization, packaging, and high temperature device operation. This limits the search to alloys that have melting points above about 450°C – although for reliability reasons, higher temperatures are preferred. The remaining choices of HMPMs, as well as their respective remelting temperatures, are highlighted in Table 4-2.\textsuperscript{1}

Table 4-2. List of remaining common HMPM choices with respective alloy remelting temperatures.

<table>
<thead>
<tr>
<th>In: HMPM</th>
<th>Remelt T (°C)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Mn</td>
<td>910</td>
</tr>
<tr>
<td>Pt</td>
<td>894</td>
</tr>
<tr>
<td>Ti</td>
<td>796</td>
</tr>
<tr>
<td>Pd</td>
<td>664</td>
</tr>
<tr>
<td>Ag</td>
<td>166 or 660</td>
</tr>
<tr>
<td>Au</td>
<td>454</td>
</tr>
<tr>
<td>Cu</td>
<td>310 or 440</td>
</tr>
<tr>
<td>Ni</td>
<td>420</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Sn: HMPM</th>
<th>Remelt T (°C)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Ti</td>
<td>1475</td>
</tr>
<tr>
<td>Nb</td>
<td>835</td>
</tr>
<tr>
<td>Ni</td>
<td>794</td>
</tr>
<tr>
<td>V</td>
<td>756</td>
</tr>
<tr>
<td>Mn</td>
<td>549</td>
</tr>
<tr>
<td>Co</td>
<td>525</td>
</tr>
<tr>
<td>Pt</td>
<td>522</td>
</tr>
<tr>
<td>Fe</td>
<td>513</td>
</tr>
<tr>
<td>Ag</td>
<td>480</td>
</tr>
<tr>
<td>Cu</td>
<td>415</td>
</tr>
</tbody>
</table>

4.4.3 Refining the Alloy List

Any alloy system that contains Au must be cautioned against when used near Si device active regions, as Au can form undesirable midlevel electrical traps in Si.\textsuperscript{10,11} Because this dissertation focuses on GaAs and Si, the list of alloys can be narrowed down significantly to obtain the best alloy system choice for these materials. This is done by considering the possibilities of ohmic contact interfaces and thermal expansion effects.
**4.4.3.1 Ohmic Contacts**

The alloy’s use as an ohmic electrical connection between GaAs and Si will be discussed first. The bond interface electrical behavior chapter discusses the details of what is meant by an ohmic contact and surface pinning. Table 4-3 provides a list of relevant ohmic contact metallizations used for both GaAs\(^{12}\) and Si\(^{13,14}\). The list has been limited to only those that contain at least one of the metals from the list of narrowed down alloys thus far.

Table 4-3. List of semiconductor ohmic contacts metallizations that use at least one metal from the narrowed down choices for LMPMs and HMPMs.

<table>
<thead>
<tr>
<th>Contact Metallization</th>
<th>Type</th>
<th>Contact Metallization</th>
<th>Type</th>
</tr>
</thead>
<tbody>
<tr>
<td>n-GaAs:</td>
<td></td>
<td>n-Si or p-Si:</td>
<td></td>
</tr>
<tr>
<td>Pd/In/Pd</td>
<td>low SBH</td>
<td>Al</td>
<td>spiking</td>
</tr>
<tr>
<td>Si/Pd</td>
<td>low SBH</td>
<td>Pt</td>
<td>silicide</td>
</tr>
<tr>
<td>Ag/In</td>
<td>low SBH</td>
<td>Pd</td>
<td>silicide</td>
</tr>
<tr>
<td>Ag/Ti</td>
<td>low SBH</td>
<td>Ti</td>
<td>silicide</td>
</tr>
<tr>
<td>Pt/In</td>
<td>low SBH</td>
<td>Ta</td>
<td>silicide</td>
</tr>
<tr>
<td>W/In</td>
<td>low SBH</td>
<td>Mo</td>
<td>silicide</td>
</tr>
<tr>
<td>Ni/Au/Ge</td>
<td>high doping</td>
<td>W</td>
<td>silicide</td>
</tr>
<tr>
<td>Au/Ge/Pd</td>
<td>high doping</td>
<td>Ti</td>
<td>silicide</td>
</tr>
<tr>
<td>Ge/Ag/Ni</td>
<td>high doping</td>
<td>Co</td>
<td>silicide</td>
</tr>
<tr>
<td>Ni/Au/Ge</td>
<td>high doping</td>
<td>Ni</td>
<td>silicide</td>
</tr>
<tr>
<td>p-GaAs:</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Pt/Ti</td>
<td>low SBH</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Au/Zn</td>
<td>high doping</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Note that due to Fermi surface pinning and the relative ease with which high GaAs p-doping may be achieved, many metallizations form reasonable contacts to p-GaAs. Ohmic contacts to n-type GaAs are much more difficult to obtain, requiring very specific metallizations. Note also that silicon’s Fermi surface pinning is more centered between n and p-type as compared to GaAs. Contacts to n-type Si yield slightly higher contact resistivities than p-type, however the same metals are commonly employed for both.
From this list – HMPMs available for bonding and capable of making ohmic contacts to both Si and GaAs – only Pt, Pd, Ni, and Ti remain. This limits the choice of ITS alloys to that shown in Table 4-4 although there is no guarantee that the ITS metallizations that simply contain these metals will produce reasonable ohmic contacts.

<table>
<thead>
<tr>
<th>In:</th>
<th>HMPM</th>
<th>Remelt T (°C)</th>
<th>Sn:</th>
<th>HMPM</th>
<th>Remelt T (°C)</th>
<th>Bi:</th>
<th>HMPM</th>
<th>Remelt T (°C)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pt</td>
<td>894</td>
<td></td>
<td>Ti</td>
<td>1475</td>
<td></td>
<td>Ti</td>
<td>1300</td>
<td></td>
</tr>
<tr>
<td>Ti</td>
<td>796</td>
<td></td>
<td>Ni</td>
<td>794</td>
<td></td>
<td>Pt</td>
<td>522</td>
<td></td>
</tr>
<tr>
<td>Pd</td>
<td>664</td>
<td></td>
<td>Pt</td>
<td>522</td>
<td></td>
<td>Pd</td>
<td>485</td>
<td></td>
</tr>
<tr>
<td>Ni</td>
<td>420</td>
<td></td>
<td>Pt</td>
<td>522</td>
<td></td>
<td>Ni</td>
<td>469</td>
<td></td>
</tr>
</tbody>
</table>

It is important to mention that Sn is an effective donor in Si\textsuperscript{10}, as well as Bi\textsuperscript{15}. Although bismuth’s impurity level is deeper than both Sb and As. Bondmetal contacts using Sn or Bi may compensate p-type Si layers. This could make achieving low resistivity ohmic contacts to p-Si difficult. Experimental tests would have to verify this claim.

4.4.3.2 Thermal Expansion

Although many compound semiconductors could benefit from being bonded to Si using this method, this dissertation focuses on GaAs. GaAs has the biggest disparity of thermal expansion to Si compared to other microwave and optoelectronic device compound semiconductors materials, as shown in Table 2-2. By extension, illustrating the successful ITS metalbonding of GaAs to Si validates its ability to bond materials more closely matched in thermal expansion. This suggests that the lowest bond temperature available should be chosen, which is dictated by the melting point of the LMPM. Low melting point alloys aside, indium represents the best single element choice
of LMPM for ITS bonding based on its low melting point, as evidenced by the melting points presented in Table 4-1. In addition, the In-Pd system is the most cited ohmic contact to n-type GaAs that contains both constituents of an ITS alloy. These reasons, together, dictated the decision to investigate this alloy system.

4.5 Alloy Kinetics

Alloys are not fully described by their steady state behavior alone, and consist of kinetic behavior in addition. Tradition metallurgy alloying processes typically involve mixing constituents, alloying for long periods of time, crushing the resulting material, and repeating the process several times. This ensures that the final product has had a chance to alloy completely. The bond alloy is not created separately in this manner, but is instead formed in place during the ITS bonding process. Therefore, the transient behavior of the alloy’s formation is an important factor to consider during ITS bonding. Another potential issue to consider is that the ITS alloy bonding process involves thin metal films. The alloy kinetic behavior of thin films is generally different from bulk behavior and must be accounted for. This subsection details the key factors that effect ITS bond alloy formation.

4.5.1 Alloy Diffusion

The transient nature of alloy formation is important in deciding the temperature and duration of the bond anneal. In$_7$Pd$_3$ is the first stable intermetallic compound formed by the In-Pd system. If other intermetallics form simultaneously and vie for dominance, the kinetic behavior would be much more complex and could result in a final alloy which remelts at a temperature that is too low for further processing. Studnitzky and
Schmid-Fetzer found the In-Pd system to be diffusion limited, but only performed reaction rate measurements on powdered bulk samples – the thin film behavior could be quite different. Quitoriano, *et al.*\textsuperscript{17} determined the diffusion rate at different temperatures of In-Pd thin films, allowing the alloy completion to be estimated by

\[
x = (Dt)^{\frac{1}{2}}
\]

where \( t \) is the diffusion time, \( x \) is the diffusion thickness, and \( D \) is the diffusivity given by

\[
D = D_0 e^{-E_A/kT}
\]

\( D_0 \) is the diffusion constant, \( E_A \) is the activation energy approximately equal to 0.63 eV, \( k \) is Boltzmann’s constant and \( T \) is the temperature.

### 4.5.2 Other Effects

Process effects may exist beyond the typical kinetics, induced by the fabrication process itself. A few of these effects are introduced here, while the details of their significance will be revealed in the next chapter.

Quitoriano, x, x, and x found that the exposed surfaces of their prepared bonding samples were affected either by oxidation, or other chemical residue, that acted as a diffusion barrier. This diffusion barrier resulted in a delay time, before which the alloy process does not take place.

A constituent films’ roughness would seem tolerable due to the liquid state that occurs during bonding. However, if the LMPM prematurely alloys with the HMPM during deposition, resulting in a rough textured, partially prematurely completed layer,
then the uneven alloy may prevent the remaining surface from coming into intimate
contact. This remaining area would not have the opportunity to form the bond alloy,
resulting in an un-bonded region.

4.6 Conclusion

In order to bond the GaAs and Si materials used in this investigation, an In-Pd
bondmetal was chosen. This alloy system is beneficial to the integration process by
providing a low-stress metal interface. This interface can also provide device
performance advantages as well, pertinent to the creation of metalbonded HMMIC
devices, including the possibility of low-resistivity ohmic interconnects. The realization
of which will be presented in the electrical characterization chapter.
4.7 References


5 Implementations of the ITS Bonding Method

5.1 Introduction

The ITS bonding method is implemented in two forms: a bottom-up approach and a top-down approach. The top-down approach demonstrates whether the ITS bonding method is capable of integrating GaAs with Si, while the bottom-up approach provides a more effective way to bond the two materials. It is important to choose an approach that is capable of sparsely bonding the two materials while producing a high yield, in order to be most beneficial to the HMMIC system.

Section 5.2 introduces the two types of patterned bonding investigated. The presentation of the, top-down, post-pattern bonding process is discussed in section 5.3, while the, bottom-up, pre-pattern bonding process is discussed in section 5.4.

5.2 Patterned Bonding Introduction

The ITS implementations were split into two types: post-pattern bonding and pre-pattern bonding. Post-pattern bonding is defined as a top-down approach where both sample halves are joined everywhere on their mating surfaces and the resulting heterogeneous sample is then etched and fabricated into devices. Pre-pattern bonding is a bottom-up approach where devices on one or both sample halves are fabricated to completion (or near completion), then patterned with the bondmetal, bonded, and etched back to reveal bonded devices. A few final metallization fabrication steps complete the integration process.
The post-pattern bonding process was technically easier to realize and was pursued first. However, the post-pattern bonding process yield was excessively low and the variety of bonded device configurations afforded by this method were substantially restrictive. The pre-pattern process was developed to surpass these limitations in both yield and capability.

5.3 Post-Pattern Bonding

This subsection illustrates the capabilities and limitations of this form of ITS metalbonding, details its fabrication procedure, and discusses its yield.

5.3.1 Capabilities and Limitations

The post-pattern bonding process bonds the entire interface with one continuous coating of metal. Thus illustrating that the ITS method can, in fact, be implemented to bond GaAs to Si and was used to test the electrical behavior of the bond interface. This electrical characterization is discussed in the next chapter.

Evaporating the bondmetal onto the entire sample, and bonding prior to fabricating individual devices, raises a few issues. The first is that having the metal over the entire surface severely limits the types of devices that can utilize this approach. Not all device designs can support having metal deposited everywhere. A fully functional HMMIC, as described in the introduction chapter, would not be easily realizable with this method. Another limitation is that it is not a back-end process. The bonding and patterning have to be done in the middle of the heterogeneous device’s fabrication rather than afterwards. This eliminates the possibility of testing the compound semiconductor
devices before they are bonded, as well as many of the advantages afforded by a sparse integration technique.

5.3.2 Fabrication Procedure

This procedure was used to fabricate devices that could determine the electrical behavior of the interface and extract the interface specific contact resistivity. 1cm x 1cm pieces of unpatterned GaAs were bonded to 8mm x 8mm pieces of unpatterned Si. Both bulk doped, and MOCVD grown doped epitaxial GaAs, were used.

5.3.2.1 Procedure Overview

For clarity, this procedure overview provides a high-level list of the basic process steps involved. The reader may refer to Appendix B.2 for specific process step details. The procedure was split into three basic parts; the first prepared the samples for bonding, the second actually bonded the samples together, and the third fabricated the devices out of the heterogeneous sample.

Part 1: Bonding preparation

First, the Si and GaAs were prepared for bonding. This included cleaving: to separate appropriately sized pieces from full wafers, cleaning: to remove debris that would prevent bonding, and epilayer growth: to later measure interface contact resistivity. The MOCVD epitaxy procedure of Appendix B.1 details the growth procedure.

Next, the samples were mounted and evaporated with appropriate bond-metallizations – after which the samples were demounted and readied for bonding.
Part 2: Bonding

The samples were aligned and bonded, using a few handheld tools (detailed in Appendix D.5), and transferred to an annealing station where they were annealed and cooled under pressure in a reducing atmosphere. The remaining steps fabricate the heterogeneous sample into their final bonded device form.

Part 3: Post-bond fabrication

The first part of this post-bond process was to etch-thin the GaAs substrate to a thickness suitable for monolithic processing. The bulk doped GaAs bonded samples – used for preliminary interface electrical behavior tests – were etched either to a thickness of a few 10’s of micrometers, without the aid of an etchstop, or simply left un-etched. Etch-thinning of the GaAs substrate with epitaxial etchstop, and doped layers, were performed in two stages. The first stage was a rapid GaAs etch, less selective to the etchstop, while the second stage consists of slower, more selective etch.

The etchstop layer of the epitaxial GaAs samples was then removed to reveal the bonded doped GaAs epilayer beneath. After which Si backside ohmic contact metallization was applied, and the sample annealed, to form the ohmic bond connect and backside contact.

Next, GaAs topside ohmic contact metallizations were defined. The topside contacts were additionally capped with a thick metal, to act as an ion milling mask. The sample was then annealed to form topside ohmic contacts. After this, the mesa structures were defined, via ion milling, to electrically isolate the devices.
After the devices were fabricated, they were electrically tested to determine bond interface electrical behavior and extract the interface contact resistivity. The bond electrical characterization chapter reveals the details of the measurement processes and reviews the results.

### 5.3.2.2 Procedure Discussion

This subsection discusses the process steps outlined in Appendix B.2. The cleaving and cleaning procedure outlined in Appendix B.2 produced samples with the lowest number of bond-preventing particles of all preparation methods tested. Numerous processes were tested before settling on this procedure. Cleaning particles off of a cleaved sample is no trivial task. The best cleaning procedure never involves cleaving the samples in the first place – to uphold the original particle count. This is most likely something that could be done in a manufacturing setting, but could not be realized during the investigation of this dissertation. Since this was not an option, various methods had to be devised to optimally clean the cleaved samples.

Each cleaning step has a probability of cleaning off particles a certain way. As a consequence, each step removes a certain percentage of particles. Cascading steps in the proper order can progressively clean the sample surface. The desire is to yield a bondably clean sample, with minimal effort. Generally speaking, the fewer process steps performed prior to bonding, the less chance of sample contamination.

Cleaving the samples on a vacuum chuck allowed the fine pre-cleave nicking to be done by hand. This lead to the production of less cleaving dust contamination and a neater cleaved edge. The purpose of the deionized nitrogen was to whisk away a large
portion of the pre-cleave nick produced dust, before it could even settle on the sample surface. Preventing contamination is preferable to cleaning, whenever possible. When the deionized nitrogen was blown after nicking, instead of during, the particle density was as much as 100 times higher. Cleaving polished side down, on AlphaWipe\textsuperscript{1} cloths, minimized the addition of particles during cleaving. Again, avoiding contamination is preferable to cleaning.

Cleaning the samples in buffered oxide etch (BOE) released much of the remaining cleave dust by etching the underlying oxide, which seemed particularly true for the silicon pieces. However, the BOE tends to leave some sedimentary particles behind. These along with remaining particles have a chance of being removed in the ultrasonic bath dips, which cavitates the water to agitate the particles free. This method provided satisfactory results for the proof-of-concept bonding runs required for this dissertation; however, megasonic agitation would be preferable in future applications. Megasonic agitation excites the water at frequencies as high as 3MHz in comparison to ultrasonics’ 40kHz. This type of agitation is capable of releasing smaller particles than ultrasonic cleaning is capable of.\textsuperscript{2}

The Si pieces were cleaved slightly smaller than the GaAs pieces to prevent the excess growth thickness that forms at the edges of the GaAs from allowing the bond surfaces from mating. This edge effect is a consequence of growing on cleaved samples and is due to the typical thin film MOCVD diffusion limited growth regime where the edges of samples grow faster, due to their enhanced precursor flux. The excess GaAs periphery also adds a convenient place for the GaAs evaporation chuck to hold the sample. The Si pinching evaporation mount allows the Si sample to be held upside-down
over the evaporation source, in the evaporator, without contaminating the topside surface – Appendix D.3 discusses this further. Also, the discrepancy between the crystal monitor measured thickness and the actual thickness on the sample was not known at the time the post-pattern process was being investigated. The thicknesses noted in the procedure were those seen by the crystal monitor.

A variety of specialized tools used to dismount, transport, and bond the sample were created to improve the reliability of performing these tasks by hand, Appendices C.4 and C.5 describes each ones’ function in detail. However, only the keyhole tray, plastic transfer plate, pin plate, and an older revision annealing pressure apparatus existed during the period the post-pattern bonding process was being investigated.

It should be noted that the pressure applied to the sample during annealing was applied throughout the annealing process as it was purged, heated, and cooled. In contrast, the pre-pattern bonding procedure applied pressure only when the sample was hot. The importance of this is discussed in the pre-pattern bonding procedure discussion.

Also, the sample was heated to 170°C for 2 hours; alloy kinetics was not well understood at the time and the duration was presumed long enough to complete the alloying process. It was only later realized that, although the bond probably had enough time to alloy, its completion was not assured after only 2 hours at 170°C.

The etching of the post-pattern bond material did not benefit from the uniform quality and rate afforded by the jet-etcher developed later. In fact several etching schemes were tried before settling on this particular etching approach including a form of bubble-etching\(^3\). The etchant compositions were chosen after testing numerous combinations to provide a high etching rate, uniformity, and selectiveness.\(^4\) Etching
proceeded from a faster, Sulfuric acid based etchant, to a slower, Citric acid based etchant, to improve the GaAs to InGaP etchstop selectivity.

No chemical etchant method (wet or dry) was ever found capable of etching the GaAs mesas without uncontrollably undercutting the bondmetal – the task of forming the mesa structures had to be accomplished via Argon ion milling. This was done by capping the mesa contacts with a thick Ni layer, capable of withstanding the required milling operation, essentially creating a self aligned etching process.

After fabrication was complete, the topside, backside, and bond interface were annealed simultaneously.

5.3.3 Yield

The yield of the post-pattern bonding process was very low, with maximum yield never exceeding about 10%. This was, in part, due to the fact that many of the procedures, tools, and apparatus’ were being developed at the time and the process was performed in the class 10,000 (and higher) environment of the old ITL cleanroom facility at UCSD. Regardless of process improvements discovered along the way, a few underlying difficulties could not be resolved using the post-pattern bonding method.

The explicit particle contamination was reduced through improved cleaning procedures but an unseen implicit source of particle contamination persisted. This discovery was made while investigating the pre-pattern bonding approach. The metal sources were spitting molten droplets of metal onto the sample surfaces in the electron-beam evaporator. These were large enough to prevent the bond surfaces from coming in contact in many areas.
Another major yield issue showed up during etching. Any defect in the growth of the epitaxial layers provided a shortcut for the etchants – even a single defect was enough to cause this issue. Wherever the GaAs etchants leaked through the etchstop, they would erode the GaAs epilayer underneath. As soon as it broke through this layer, it would start attacking the bondmetal. The bondmetal etched much faster than either of the semiconductor materials and would essentially unzip the bond. This was particularly true of the Hydrochloric acid etchstop etchant, which would etch the bondmetal extremely fast if it leaked through the GaAs layer. This problem turned out to be the most challenging to overcome, as it would be for any indium or tin based bond alloy.

5.4 Pre-Pattern Bonding

The pre-pattern bonding process was investigated, following the yield issues associated with the post-pattern bonding process, during its implementation to investigate the bond interface electrical behavior. The capabilities of the pre-pattern bonding process are much more suited to implementing HMMIC assemblies; however, they do not come without several formidable limitations. Luckily these limitations were surmountable and the pre-pattern bonding process gave a much higher yield than the post-pattern bonding process.

5.4.1 Capabilities and Limitations

Pre-pattern bonding differs from the post-pattern bonding method in that the compound semiconductor device fabrication is completed before bonding even begins allowing the bondmetal pattern to match the finished device. This supports a sparse
architecture where multiple bonds may populate the interface as opposed to the single
blanketing metal bond of the post-pattern bonding approach.

The bondmetal etching issue required the use of an atypical Argon ion milling
procedure to define the device mesas during post-pattern bonding. This is not required if
the devices and bondmetal are defined prior to bonding. However, implementation of
this approach requires careful treatment of the regions between devices to avoid etching
difficulties. Also, the special stress complications imposed by sparse bonding must be
addressed.

5.4.2 Fabrication Procedure

This procedure was used to fabricate devices which extracted the microwave
behavior of bonded-microstrip waveguides and bond interface thermal conductivity. This
procedure did not entail patterning and aligning the silicon in addition to the GaAs. That
general case would be a straightforward extension of this procedure and could be
implemented using existing technology.  

5.4.2.1 Process Overview

As with the previous post-bonding procedure overview, this review will offer a
high-level list of the process steps. The pre-pattern bonding procedure in Appendix B.3
provides a detailed account of each process step. The process was realized in five stages:
the first cleaned and prepared the samples for processing, the second actually fabricated
the GaAs devices, the third prepared the GaAs devices for bonding, the fourth bonded
them and removed all the extraneous material, and the fifth and final part completed the
hybridization with a metallization process.
Part 1: Sample preparation

Si and GaAs wafers were cleaved, cleaned, and prepared as before, except the GaAs epilayer remained undoped, rather than being doped highly n or p-type.

Part 2: GaAs device fabrication

The GaAs epilayer was patterned with both the bond mesa structures, as well as standoff mesa structures, using photoresist. The details of the mask pattern are described in Appendix D.2. These structures were aligned to exclude the maximum number of defects and the mesa structures were defined via dry etching. The etching was performed in two stages: a vertical side-wall rapid etch and a slower etchstop selective etch. This marked the end of this simple test structure fabrication – if this were an active device, the fabrication would be completed and the device tested, before continuing on to the pre-bond sample preparation.

Part 3: Pre-bond preparation

Polymethylglutarimide (PMGI) photoresist\textsuperscript{6} was then used to fill the gap regions between the GaAs mesas up to a height just below the top of the mesas. Next, metal was added to the tops of the standoff mesas. This metal was designed to be slightly thinner than the GaAs bond metal height requirement.

After the standoffs were completed, photoresist windows were opened where the bondmetal was to be deposited, and the samples were mounted for evaporation. Palladium was evaporated, similar to the post-pattern bonding process, while the indium
was evaporated on the GaAs sample at low temperature. Special precautions were taken to prevent both metal sources from spitting—the samples were then dismounted and prepared for bonding.

**Part 4: Bonding and post-bond preparation**

Bonding and annealing ensued much as they did before, but with the aid of more advanced fabrication tools and a few notable differences. The samples were placed in the hands-off style bonder and oriented with respect to one another. The sample pair was then transferred to the annealer and thoroughly purged. Pressure was applied remotely, only when the sample was hot and the alloy was allowed to form for a duration of 3 hours at 180°C, to be sure the alloy process had completed.

Before the sample was cooled, a wax filler material was wicked into the remaining void regions between the mesas. Wax was also used to encapsulate the topside of the GaAs ledge for later etching. The sample was then allowed to cool and attached to an etch mount before reaching room temperature.

From there the sample was jet-etched in the Sulfuric acid based etchant, touched up to remove the remaining bulge, and completed in the Citric acid based etchant. The etchstop was then immediately removed with Hydrochloric acid vapor. Immediately following the etching steps, the PMGI and wax were removed with a myriad of solvents that harmed neither the bond alloy nor semiconductor. Figure B.3-15 through Figure B.3-17 show composite pictures taken of the sample at each etching step. It should be noted that these pictures were taken of an earlier sample that was not immediately stripped of wax and PMGI, as the importance of this timing was unknown at the time.
Part 5: Metallization

The device fabrication was then concluded with a metallization step.

5.4.2.2 Procedure Discussion

Just as with the post-pattern process discussion, this subsection discusses the process steps outlined in Appendix B.3. It is assumed that the reader has familiarized themselves, or is following along during this discussion.

The GaAs epilayer grown for this process was left undoped, rather than highly n or p-type doped, to act as an electrical insulator for the thermal and microwave measurements. The two patterns DF-MESA_0 and DF-PMGIPAD_-9 were used to provide the bond mesas and standoff mesa definitions. The discussions of their designations are provided in Appendix D.2. Two patterns were used instead of a combined one, simply because the necessity of the standoff mesas were not known at the time the mask was developed. When combined with their metal caps, these standoff mesas reduced the amount of indium that squeezed out the sides of the bond mesas as depicted in Figure 5-1. Small amounts of oxidation and other forms of contamination could not be completely removed from the exposed bond-metallization surfaces. These resulted in a delay that occurred, prior to alloying after the indium melted. This delay prevented the indium from alloying by allowing it to, instead, escape the bond regions by squeezing out under pressure. The standoffs prevented the indium from escaping completely, thus allowing it to alloy after the delay.
A dry etching method was chosen over a wet etching method to reduce undercutting of the mesas. The dimensions of the mask were designed to cope with only a narrow tolerance in mesa width. This was particularly important for the narrow mesa devices required for the thermal and microwave measurements. It also showed that dry etching (a common device processing technique) can be utilized in device fabrication without affecting bond yield. Inductively Coupled Plasma – Reactive Ion Etching (ICP-RIE) was used to efficiently produce vertical sidewalls on the mesas. Just as with the back-side etch-thinning process, dry etching was achieved in two stages. The first provided a fast means of producing vertical sidewalls, while the second was more selective over the InGaP etchstop layer material. The etching was performed in bursts, with a long recovery time to prevent the plasma from overheating the photoresist used. Futurrex™ NR7 series resist was chosen over their NR9 series to provide better thermal protection during etching. This overheating issue could have been avoided if either the etching platen in the ICP-RIE were capable of staying cool during etching, or if another material were used as an etch-mask. This process would be more effectively controlled.
in a manufacturing setting, but this stop-start method was adequate to create bondable
devices during the investigation of this dissertation. Photoresist was chosen over a hard
etch-mask, such as metal or insulator, because it was feared these would be too difficult
to remove completely, making bonding more difficult.

![Figure 5-2](image)

The PMGI step was added to the process after it was noticed that the wicked wax
did not fully support the thin etchstop during etch-back and any voids in the wax
exacerbated the issue. The PMGI also acted as a barrier between the etchstop and any
stray indium that squeezed out. Wherever the etchants got through the etchstop, the
PMGI would be there to prevent it from reaching the stray indium as illustrated in Figure
5-2. Without this PMGI layer, the etchants always found ways to breach the etchstop and
attack the bondmetal severely affecting yield.
The low temperature indium evaporation provided two benefits: it prevented the indium from prematurely reacting with the palladium underneath, and two; it created a smooth indium surface. The effects of temperature on surface texture are shown in Figure 5-3. The first benefit occurs because indium's reactivity with palladium is much lower at low temperature. The reason for the second benefit may not be immediately clear. Because evaporation requires the source to be heated to increase its vapor pressure, the metal vapor arriving at the surface of the sample transfers heat to it. This is not the
only source of heat impinging upon the sample, nor is it the most dominant. The largest quantity of heat flux impinging on the sample surface comes from the thermal radiation emanating from the hot source.\textsuperscript{10} Similar forms of heating occur during sputtering as well. When indium is evaporated, or sputtered, onto samples at room temperature, the resulting film coalesces into droplets.\textsuperscript{11,12,13} These droplets are a consequence of the unique stress imposed onto the indium during deposition\textsuperscript{14,15} and the proximity of the sample’s surface temperature to indium’s melting point, resulting in a high surface mobility. As the metal condenses on the surface of the sample, it cools and shrinks slightly, due to thermal contraction inducing a stress in the film. At room temperature adatoms of the recently condensed metal are mobile enough to move around\textsuperscript{16} the surface and relieve stress by forming islands. This behavior can be quenched by depositing the metal onto a sample held at low temperature.\textsuperscript{17,18} This phenomenon is not limited to indium and occurs with tin as well.\textsuperscript{19} It is presumed that this would also be an issue with other low-melting point metals. These droplets are often higher than a micron tall and could be separated by a few micrometers. The film may become continuous if enough metal is applied to coalesce the droplets; however, this requires more than a micron of metal to be evaporated and the texture of the film still persists. This is true regardless of the composition of the underlying surface. The few indium surfaces capable of wetting to the underlying palladium layer actually prematurely alloy with it during un-cooled evaporation.\textsuperscript{20,21,22} The solid alloy cores at the center of each droplet are highly undesirable – they ultimately act as particle contamination, preventing the bond surfaces from coming into intimate contact and severely impacting yield. The spacing of the droplets limits the smallest bondable feature and presents the issue of metal interlayer
continuity, which degrades bondmetal interconnects. The effects of this texture were not understood at the time the post-pattern bonding process was being investigated.

Performing the evaporation at liquid nitrogen temperature requires all the materials on the sample to survive the cool-down and return to room temperature intact, including the photoresist that defines the bondmetal pattern. This can be achieved by keeping the materials below their critical thickness. In order for the lift-off process to work, the critical thickness of the photoresist must be taller than the indium thickness required for bonding. The presence of the PMGI seemed to increase the critical thickness of the photoresist, either by providing additional stress relief or by creating a photoresist bond strength that was stronger than that of the photoresist and semiconductor alone.

One minor issue that should be noted is that the difference in sample-to-source and source-to-crystal_thickness_monitor distance had to be accounted for to obtain accurate metal thicknesses. The values reflected in the pre-pattern bonding procedure Appendix B.3 are the real thicknesses at the sample surfaces. This was less of an issue for the post-pattern process as both the GaAs and Si halves of the sample pair were evaporated at the same distance from the source. Thus this crystal-to-source/sample-to-source distance issue equally affected both halves. However, the cold finger used to cool the GaAs half during indium evaporation was at a different sample-to-source distance than the Si half, and was unequally affected by the crystal-to-source/sample-to-source distance issue.

Both palladium and indium tend to spit semi-molten droplets out of their source crucibles during electron-beam evaporation. These spits then land on the sample and cool quickly to create hard droplets of metal that act as particle contamination.
Generally, electron-beam evaporators spit and splatter material during evaporation while thermal evaporators typically do not. Some source materials do this more than others and some never spit or splatter. This behavior is caused by turbulent flow in the melt during e-beam evaporation. When hot molten material pulls colder solid material into its flow and is suddenly heated by the e-beam, the rapid change in temperature causes it to rapidly expand and be ejected out of the crucible. The large temperature gradient is created in e-beam evaporators because the crucible is kept cool by a water chilled hearth, while heat is being focused on the top of the charge. This effect can be curbed slightly if the source is evaporated at a very slow rate and may be eliminated if the source is heated slowly and evenly enough. The indium spitting was completely eliminated by replacing the typical graphite e-beam crucible with a home-built Molybdenum sheet metal boat that was suspended in the hearth as shown in Appendix D.3. This allowed the charge to heat more evenly, thus mimicking the uniform temperature achieved by thermal evaporators. The result was the ability to evaporate indium quickly without spitting. Using this technique, indium could be evaporated up to 80Å/s without suffering spitting – higher rates were not tested. Since palladium alloys with the refractory metals that would normally be fashioned into evaporation boats, the suspended metal boat technique could not be used. After many experiments, it was found that palladium spitting could be reduced or eliminated if the e-beam’s sweep across the melt was extremely slow. This reduced the turbulent flow that normally picked up the solid metal causing it to spit out. The less thermal contact the crucible had with the cold hearth, the more uniform the melt’s temperature would be. A graphite liner that loosely holds the crucible in the hearth was used for this purpose.
The latest revision of the bond and annealing pressure plates were hung by chain in the bonder assembly. It allowed uniaxial pressure to be exerted down onto the sample with minimal lateral force being exerted. A well designed manufacturing machine could accomplish the same task on a larger scale; however, the chain apparatus was the most elegant embodiment on the small scale involved during the investigation of this dissertation.

It was found that oxidation during annealing affected the periphery of the bond regions of several samples. This was believed to be caused by insufficient annealor purging. The susceptor drying and thorough pumping and purging of the annealing chamber were used to combat this issue.

An important note about the applied annealing pressure should be clarified. The force exerted was not a scaled down percentage of the bond force used by the post-pattern method – this force was too low to achieve reliable bonds. The force would have been about 2-5% of the post-pattern bonding case to provide equal bond pressure due to the smaller total bond area provided by the sparse design. Higher force was required to deform the indium around latent particles, which persisted even after all the precautionary cleaning steps. This would not be necessary if the samples could be cleaned to a higher degree, as would be the case in an industrial setting. Megasonic agitation may more effectively clean samples for this purpose.

The wax filling the remaining void region during the wax-wetting process serves two purposes. The first was to act as a temporary bonding material, taking much of the thermal strain off of the sparse bond regions. The bond strength, afforded by the sparse bond area, was not enough to hold the sample together during the cool down to room
temperature, without the wax present. The second purpose was to fill all the voids to protect the bondmetal from being attacked by the substrate etchants. Appendix D.7 discusses the purpose for the polypropylene beads mentioned in the pre-pattern bonding procedure Appendix B.3 and their connection to the revised heater structure shape is discussed in Appendix D.2. The wax is not intended to be permanent and is removed after the etchback process. The wax and PMGI can absorb some of the etchant and leach it over time, which is why the etching processes are done in rapid succession and immediately followed by the wax and PMGI stripping steps.

In order to fulfill these two jobs, the wax must be able to wet every recess of the bonded pair without leaving voids, yet solidify at a high enough temperature to ease the thermal stress. The criteria for choosing wax are detailed in the Appendix D.7. Wax is also used to temporarily mount the sample on an etching mount. This etching mount only serves to hold the sample in place in the current of the jet-etcher.

Due to the small size of the sample, and the lack of feedback in controlling the makeshift jet-etcher, a bulge of material persisted in the middle of the sample just after breakthrough. If the sample were etched in the citric acid based etchant at this stage, the etchant would leak through several defects in the etchstop by the time the bulge was removed. To prevent this, the bulge was etched selectively by hand to reduce the overall thickness that the citric acid etchant had to remove.

The remaining processing was straightforward, but it was feared that the solvents may not have completely removed all of the wax and PMGI, so special photoresist processing was used to avoid any possible incident. This precaution was taken by choice,
with no evidence to the contrary. The effort expended to fabricate a sample to this point, justified the extra caution.

5.4.3 Yield

While only a maximum 10% of the post-pattern bonded devices survived to any capacity, 15% of the pre-pattern bonded devices survived 100% intact and 75% survived at least 90% intact. This pre-pattern yield is extremely high for an in-house, by-hand bonding investigation. This is in spite of the numerous process steps required prior to bonding in the pre-pattern bonding process.

The class 100-1000 environment provided by the Cal-IT2’s Nano3 cleanroom facility at UCSD played a big role in the yield of this process. This is in stark contrast to the class 10,000 (or worse) environment of the older ITL cleanroom facility at UCSD.

Etching through defects in the epilayers was the main cause of poor yield for both approaches. Ideally the growth and etching of devices would be implemented better in a manufacturing setting where a higher quality and thicker etchstop layer could be grown, and automated etching machines implemented to etch more evenly. The sparse bonding concept implemented in the pre-pattern bonding approach improved the yield dramatically over the post-pattern bonding approach. This is due to the fact that the probability of inadvertent etching through a sparse network of bonds is much lower than a single, large area bond.

The secondary cause of poor yield was due to thermal stress in the pre-pattern bonding implementation. Stress in the bonded substrate as it was etch-thinned, produced cracks for the etchant to get through. This was aggravated by the high thermal
contraction of the wax and PMGI materials used in comparison to the GaAs substrate being etched. The contraction of the wax and PMGI caused the etch-thinned GaAs substrate to bend in the regions between the bond mesas and standoff mesas. Tighter spacing between the two could improve this issue. The low ratio of sparse bond area to total GaAs substrate instills a large shear stress on the device bonds at the periphery of the sample caused by the bulk substrate thermal stress. Figure 5-4 shows the amount of displacement between the thermal expansions of the GaAs and Si substrates. A device from either side of the sample is placed side-by-side to illustrate the displacement of the topside metallization pattern with the bonded mesas. Note that the mesa and top metallization mask patterns should line up to within the tolerance of the mask (which is a 0.25 micron or less). A better choice of filler – beyond the simple wax formulation used here – would help reduce these stress issues.

Figure 5-4. Microscope images of GaAs thermal expansion induced pattern shift of the (a) left-most and (b) right-most bonded epilayer mesas.
5.5 Conclusion

This post-pattern bonding method successfully demonstrates that the ITS method is capable of bonding GaAs to Si, however it suffers from a few limitations. The top-down approach of this process is exceedingly vulnerable to defect etching, resulting in a low bonding yield. Having to bond the entire sample surface prior to patterning also made this approach more susceptible to latent particles; even a low particle density was enough to inhibit bonding. The pre-pattern bonding process was more resilient to these problems because it was sparsely laid out prior to bonding, effectively isolating each bonded structure during post-bond fabrication. Therefore an etchant breach of a single structure would not affect neighboring devices. The sparse design also minimized the necessary bond area of the sample, making it less susceptible to particle contamination. As a result, the pre-pattern bonding method has the advantage of being able to integrate completed device structures with a high yield in a back-end process.
5.6 References

1. AlphaWipe is a trademark of ITW Texwipe, Mahwah, New Jersey

2. ProSys, Inc., Campbell, California


6. MicroChem Corporation, Newton, Massachusets


8. Futurrex, Inc., Franklin, New Jersey


23. "Thin Film Evaporation Source Reference," R. D. Mathis, Long Beach, California

6 Bond Interface Electrical Characterization

6.1 Introduction

Understanding basic metal-semiconductor contact theory is important when discussing the electrical behavior of bondmetal interfaces. The properties of real-world contacts; however, require amendments to this basic theory which must be included in their design. The electrical behavior of the bond interface must be measured to determine whether it is ohmic or not. Although non-ohmic metal-semiconductor contacts are advantageous to certain microwave devices, ohmic behavior is typically sought after. If linear conduction has been established, the contact resistivity of bonded HMMIC devices must be characterized if efficient electrical connections are to be realized.

Sections 6.2 through 6.4 provide a theoretical introduction to the ideal and realistic electrical behavior of metal-semiconductor interfaces, as well as a brief introduction to the typical methods of obtaining ohmic contacts. Section 6.5 discusses the bond interface electrical behavior measurements, while section 6.6 deals with its contact resistivity. Section 6.6 starts with an introduction of several existing surface contact resistivity measurement methods, describes the measurement used to extract the sub-surface bond interface contact resistivity, and ends with a discussion of the measurement results.
6.2 Ideal Metal-Semiconductor Interface Theory

This section’s metal-semiconductor (MS) contact behavior discussion begins with the theory of ideal contact band alignment, as well as general non-linear and special linear (ohmic) behavior. The importance of ohmic contacts as they relate to electronic devices – particularly those involved in the implementation of HMMIC technology – are discussed as well. Reviews of contact theory may be found in common semiconductor physics texts.\textsuperscript{1,2} Another semiconductor theory review is also provided by X. Tung.\textsuperscript{3}

6.2.1 Band Alignment

Figure 6-1 illustrates an ideal MS contact band diagram, depicting an n-type semiconductor. When the electrons in both materials are allowed to interact (i.e.: when electrons are allowed to either traverse the interface gap or allowed to flow through an external circuit), thermal equilibrium states that their average electron populations must reach a steady state condition. Any mobile electron occupying a high potential energy state will move to its lowest available potential energy state. When all the mobile electrons do this, the net effect causes them all to settle to a mutual, average steady state energy. This average electron occupation energy is called the Fermi energy.
The metal has a work function $\phi_M$ representing the average energy required to strip a mobile electron from the metal lattice. The semiconductor has an electron affinity $\chi_s$ representing the respective energy for the semiconductor lattice. The only difference being that the average energy for mobile electrons (Fermi level) in the semiconductor is
not within the conduction band as it is for the metal. The crystal structure of both materials has not changed during the equilibration process, so the chance for a mobile electron to be striped from either material must remain consistent throughout the system, including the interface, resulting in a band alignment discontinuity. This is essentially the theory presented by Schottky\(^4\) and Mott\(^5\). The Schottky barrier height (SBH) is defined as the potential energy a mobile electron must acquire to traverse the interface barrier and is given by

\[
\Phi_{SB} = \phi_M - \kappa \nu
\]

6.2.2 General Non-Linear Behavior

When the MS junction is reverse biased – with the n-type semiconductor held at a higher voltage than the metal as seen in Figure 6-2c – the mobile electrons residing in the metal are presented with the full height of the SBH as they attempt to reach equilibrium by drifting toward the n-type semiconductor. Electrons would have to defy this barrier to reach equilibrium by thermionic emission. The probability of this happening to an electron is very low at room temperature and therefore would not happen often. The result would be little to no current flow during moderate reverse bias. However, when the bias is high enough to effectively thin the barrier as in Figure 6-2a, electrons will have a high probability of quantum mechanically tunneling through the barrier, resulting in a high current.
Figure 6-2. Illustrations of an n-type semiconductor (n-SC) Schottky barrier contact at different biases with associated I-V regions highlighted: (a) reverse bias (breakdown), (b) reverse bias (inversion), (c) reverse bias (normal), and (d) forward bias.
When the MS junction is forward biased – with the n-type semiconductor held at a lower voltage than the metal – the mobile electrons residing in the semiconductor will be presented with a barrier that is lower than the SBH dependent on the applied bias. The electrons could either be thermionically excited over this barrier, with a probability dependent on the bias lowered barrier height at room temperature, or could quantum mechanically tunnel through it. The likelihoods of this happening from both modes working together result in the voltage dependent current seen in Figure 6-2d.

Schottky junctions under reverse bias, deplete n-type semiconductors of holes at the MS interface, and under high reverse bias can invert the surface doping type, forcing it to pool all available electrons as shown in Figure 6-2b. This pool, if supplied with electrons from a source, can transfer them laterally to a drain forming an electron channel. Such is the design of MESFETs and similarly HEMTs. The speed with which this channel can conduct electrons is limited by the electron mobility in the material. The electron mobility in III-V semiconductors are typically much higher than Si, making Schottky contact MESFETs valuable compound semiconductor microwave devices. Higher speeds have been attained in intrinsically doped (higher electron mobility) channels made possible by heterojunction bandgap engineering. These high electron mobility transistors (HEMTs) have replaced MESFETs in high speed microwave systems due to their speed. However, MESFETs are cheaper to produce as they do not require compound semiconductor heteroepitaxy.
6.2.3 Linear (Ohmic) Behavior

Ohmic behavior MS contacts are just special cases of Schottky MS interfaces where the carriers can easily traverse the interface in both reverse and forward bias states. This is possible when either the Schottky barrier height is physically low or when the doping in the semiconductor is very high near the surface, as illustrated in Figure 6-3. When the barrier height is low, it is trivial to show that the carriers will easily be able to traverse the interface under both bias conditions. When the semiconductor doping is very high near the interface, the barrier will be very thin allowing carriers to tunnel through.

![Figure 6-3](image.png)

Figure 6-3. Illustrations of ohmic contacts to n-type semiconductor (n-SC) with (a) a low barrier height metal and (b) a high surface doping concentration in reverse, mid, and forward biased states.
The ease with which carriers can traverse the MS interface dictates the resulting current flux versus bias relationship which defines its contact resistivity. Specific contact resistivity is represented as the resistance density per unit area

$$\rho_c = \frac{R}{A}$$

which is typically expressed in $\Omega \cdot cm^2$. Since this resistivity typically dominates the electrical behavior near the MS contact interface, it is called contact resistivity, or specific contact resistivity (to emphasize that it is normalized to area).

### 6.2.3.1 Ohmic Contact Impact

Ohmic MS contacts are desirable for all electronics devices that do not depend on the non-linear behavior of the MS interface (i.e.: all non-Schottky diode based devices). Electronic device design is much less complicated if the only non-linear element to be designed is the device itself – non-linear contacts complicate device design. Some device designs simply aren’t practical if they have non-linear contacts; if the carriers are stuck or lost inside the device, they cannot interact with the outside world.

Low contact resistivity ohmic contacts are extremely important to these types of devices. Ohmic contacts contribute to on-state device resistance, thus to operate devices at a minimum of on-state resistance, this parasitic contact resistivity needs to be minimized. Generally, the contribution from the (non-depleted) doped semiconductor material itself is much smaller than the contact contribution. The qualifier ‘non-depleted’ is used to describe semiconductor material within a device that is not electrically in an ‘off-state’. The parasitic voltage drop from this contact resistance lowers external device efficiency. The external voltage required to obtain a specific internal device bias will be
higher if the contact resistance is high, so some of the voltage is simply wasted on the contact. Lower contact resistances also mean device input and output currents produce less heat.

6.3 Real Metal-Semiconductor Interfaces

Figure 6-4 illustrates a realistic MS contact band diagram. Everything is the same as the ideal case, except previously ignored semiconductor surface states are included. These surface states come from two sources. Intrinsic surface states are energy states allowed by the non-periodic shape of the electron potential at the edge of the semiconductor. Figure 6-5 illustrates a surface potential at the edge of a semiconductor lattice. The shape of the final well is reminiscent of one half of the electron potential of a single atom which has distinct energy levels. The distribution of these energy states at the edge of the crystal is entirely dependent on the surface atomic structure. If these intrinsic energy states reside within the bandgap of the bulk semiconductor, they will affect the MS interface. Extrinsic surface energy states may also exist depending on whether compounds reside on the surface of the semiconductor (not shown).

Figure 6-4. Illustrations of a realistic metal-semiconductor contact band diagram under zero external bias: (a) uninfluenced, (b) in proximity, and (c) in contact – empty circles indicate empty surface states while filled circles indicate filled surface states.
These surface states will be partially occupied, resulting in their own version of a Fermi level. Just as the metal carriers influenced the semiconductor band bending at the ideal MS interface, these surface carriers will influence the semiconductor band bending at this non-ideal interface. In fact in the non-ideal case, the metal influence is typically trumped by the large density of surface states already influencing the semiconductor, and is known as Fermi level pinning.

![Figure 6-5. Illustrations of the electron potential structure of (a) a single atom, (b) the edge of a semiconductor, and (c) the interior of a semiconductor crystal.](image)

### 6.3.1 Fermi Level Pinning Examples

Since MS junctions are majority carrier dominant structures, the position of the surface Fermi level pinning within the bandgap of each semiconductor dictates the relative ease with which n or p-doped semiconductor contacts may be made.

Silicon surfaces pin roughly in the middle, though skewed slightly closer to the valance band. As a result, n-type ohmic contacts are slightly harder to achieve than p-type contacts.

GaAs pins closer to the valance band than the conduction band make it particularly challenging to form n-type ohmic contacts. This also means that it is fairly easy to obtain Schottky contacts to n-type GaAs. This is the reason why GaAs MESFETs are relatively easy to fabricate, and thus very popular.
InP pins quite close to the conduction band make p-type ohmic contacts difficult. This explains why it is difficult to make good InP MESFETs; n-type InP may have a very high mobility, but typical contacts to n-type InP are ohmic, making Schottky contact based MESFETs unrealizable. InGaAs can be lattice matched to InP and has an even higher electron mobility and contact behavior similar to GaAs. However, the added costs of dealing with InP material and growing heteroepitaxial material on it tend to detract from any InGaAs MESFET speed improvement. Typically lattice matched InGaAs-InP based HEMTs can provide exceedingly high speeds via bandgap engineered heterojunctions; however, this comes at the cost of price.

6.4 Practical Contacts

Real contacts are generally annealed to improve their electrical performance, allowing lower ohmic contact resistivities to be achieved. This is typically the case because, more often than not, the natural Fermi surface pinning is not favorable.

6.4.1 Effects of Annealing

Annealing can rearrange the construction of an MS interface, as well as change its alloy composition or even remove surface oxidation and other contamination. These effects alter the behavior of interfaces and can potentially improve ohmic behavior and reduce contact resistivity. The two main alloyed contact categories are defined by their annealing behavior, and include spiking contacts as well as non-spiking contacts.
6.4.1.1 Spiking Contacts

The contact metal in spiking contacts form crystallites lodged within the semiconductor surface during annealing, as depicted in Figure 6-6. These metals may form ohmic contacts prior to spiking but they can increase the interface interaction surface area when they do spike. This increased surface area can essentially squeeze a bigger contact area into a smaller footprint, improving the contact resistivity which is always defined by the footprint area.

![Figure 6-6. Illustration of a metal-semiconductor spiking contact.](image)

The deeper these spikes extend into the surface of the semiconductor, the more the contact resistivity will improve. However, if the spikes burrow too deeply, they can reach the active layers of a device degrading their performance or shorting them out. The control over the depth of the spikes is critical, and is defined by the annealing temperature and duration, as well as the propensity each particular contact metallization has to spike. The spiking may also be a factor of passed current, changing the contact structure through electromigration.

The Al/Si\textsuperscript{7} system is a historically significant example of just such a spiking contact, while the Au/Ge/GaAs\textsuperscript{8} system is an example of a compound semiconductor spiking contact.
6.4.1.2 Non-Spiking Contacts

Non-spiking contact metallizations typically either alloy with the semiconductor or diffuse high levels of dopants into the semiconductor surface without spiking. Due to their lack of spiking, these contacts do not suffer from the related reliability issue.

Silicides are good examples of non-spiking contacts to silicon. Au/Zn/GaAs and In/Pd/GaAs are good examples of non-spiking contacts to GaAs. The Au/Zn/GaAs system creates ohmic contacts by heavily doping the semiconductor near to the MS interface, as depicted by Figure 6-3b, while the Silicide and In/Pd/GaAs contacts act to remove semiconductor oxides and alloy with the underlying semiconductor material. This not only alleviates the surface pinning, but also lowers the near surface bandgap of the semiconductor as depicted by Figure 6-3a.

6.5 Measurement of Bond Interface Electrical Behavior

The post-pattern bonding process was used to create devices capable of measuring the electrical behavior of the bond interface and its associated contact resistivity. This section introduces just the bond interface electrical behavior measurement, while the subsequent section addresses the bond interface contact resistivity measurement. A measurement process overview introduces the process as a whole. This is followed by a discussion of the measurement process details, as well as a discussion of electrical behavior results.

6.5.1 Measurement Process Overview

Appendix C.1 details the process used to fabricate the bonded devices that determine the electrical behavior of the bond interface. First, bulk doped samples were
bonded and etch thinned using the post-pattern bonding process. Next, ohmic contacts were defined and annealed – during which the bond interface itself was annealed as well. The current-voltage (I-V) characteristics of each completed sample were then measured.

6.5.2 Measurement Process Discussion

Due to the fact that the bulk doped samples were etch-thinned to several 10’s of micrometers without an etchstop, the typical etching failure mechanism of the post-pattern process did not affect yield.

Ohmic contacts needed to be made to the backside and topside to prevent any unwanted non-linear behavior from masking the bond interface electrical behavior. The backside metallization only covered the center area of the sample so as to prevent unwanted shunting of the interface via rogue metallization running up the sides of the sample. The backside and bond interfaces were annealed prior to the topside contact deposition. This order was required to be able to apply the high temperature backside and bond interface without affecting the topside contacts. The topside contact schemes used, required lower annealing temperatures.

The topside GaAs contacts were defined without the need for photoresist processing by using an evaporation shadow mask. These details are described in Appendix D.3. Their large size did not affect these measurements, as only the electrical behavior was being studied.
6.5.3 Discussion of Results

The results of these measurements showed a universal ohmic behavior of the In-Pd bondmetal interface between GaAs and silicon substrates. Plots of the I-V behavior are shown in Figure 6-7\textsuperscript{12}.

![Figure 6-7. I-V plots of the bond interface electrical behavior showing the In-Pd ITS alloy’s universal ohmic contact behavior between GaAs and Si.](image)

Although no attempt was made to measure the sizes of the topside contacts, they were all nearly identical in size. Note in the plots of Figure 6-7 how the slope changes from highest to lowest in the order p-GaAs/p-Si, p-GaAs/n-Si, n-GaAs/p-Si, n-GaAs/n-Si. Therefore, since the contacts were the same size, this order lists the contact pairs from lowest to highest resistivity. This follows the Fermi pinning influence on ohmic contacts discussion earlier, as low resistivity ohmic contacts are expected to be more easily obtained on p-type GaAs and p-type silicon than on n-type GaAs and n-type silicon. The relevance of this order will be made clear during the discussion of the measured bonded interface ohmic contact resistivity results.
Having an ohmic bond interface that is universal to all combinations of GaAs and silicon doping is a valuable asset of this In-Pd alloy bonding technique. Its universal nature means that this one alloy system is all that is required to obtain ohmic bond interfaces between all types of devices. A single bond can provide all the ohmic contact needs of an integrated system at once.

These results may also be relevant to InP based device integration. The ease of obtaining n-type InP contacts may include this In-Pd bond system, and although p-type contacts to InP are generally difficult, they are rarely used. The typical contact to p-type InP is actually through a heavily doped lattice matched InGaAs layer. The InGaAs Fermi pinning level is similar to GaAs and therefore would be relatively easy to form a contact to and might include this same In-Pd bond system. Therefore this same alloy system may provide a similar universally ohmic bond between Si and InGaAs/InP devices.

### 6.6 Bond Interface Contact Resistivity Measurement

The procedure highlighted in this section was used to measure the contact resistivity of the In-Pd GaAs to Si bond interface. Discussion begins with the introduction of several traditional topside contact resistivity measurement processes. This is followed by the discussion of the measurement design used to extract the buried bond contact resistance, as well as the relevance of the Kelvin measurement scheme. Finally, the actual measurement procedure is overviewed and discussed, along with a discussion of the results.
6.6.1 Conventional Contact Resistivity Measurement Methods

No means to measure the contact resistivity of a buried bond metal existed at the
time this dissertation was investigated, thus a method had to be created to do so.
Traditional methods of measuring topside contact resistivity were adapted to this purpose.
Traditional methods may be performed on either bulk samples or thin films as shown in
Figure 6-8.

![Figure 6-8. Illustrations of the surveyed contact resistivity measurement methods: (a) Cox and Strack disk method, (b) Kelvin method, (c) transmission line method (TLM) (collinear), (d) concentric ring method (axi-symmetric TLM), and (e) Kuphal collinear disk method.](image)

Cox and Strack\textsuperscript{13} used different sized contact disks on the topside of a sample
and a wide area contact on the back of the sample to measure the topside contact
resistivity. The bulk sample must be uniform and conductive enough to be able to
resolve the contact resistance from the small disks. The measurement is straightforward
and does not require any fabrication, beyond creating the contacts.
Often a uniform bulk sample of semiconductor is not readily available during the manufacture of semiconductor devices, as most processes focus on thin films – in these cases, thin film techniques must be used. In all of these methodologies, the thin films must be electrically isolated. A doped epilayer to be investigated is typically grown on an insulating substrate. The Kelvin method requires the etching, insulation, and metallization of a rather complex geometry device. A collinear series of pads are used in a transmission line measurement (TLM) to extract the contact resistance. The structure requires a strip of thin film material to be electrically isolated, where on, the contacts are defined. This TLM method has become very popular due to its ability to yield reasonably accurate results, without extensive analysis. Its popularity has prompted several extraction improvements that remove parasitic current spreading effects. A concentric ring design was proposed to remove the mesa isolation, necessary for the collinear TLM method. The concentric ring design is essentially an axisymmetric TLM and, due to its symmetry, can remove some of the parasitic current spreading effect adjustments needed for the collinear TLM method. Another method capable of extracting thin film contact resistivity, is that of Kuphal, which also does not require etching. Kuphal’s four contact method does; however, require the approximation of current spreading terms, and is more analytically involved and generally less accurate.

6.6.2 Measurement Design

An adaptation of Cox and Strack’s method was devised to measure the bond interface specific contact resistivity. This choice was mostly dictated by the fabrication simplicity of the adapted design. Uniform bulk silicon substrate bond material was more
readily available for bonding than was insulating substrate with highly doped Si epilayers.

This discussion will assume that a bonded device, in a form similar to that illustrated in Figure 6-9, can be produced by either post-pattern or pre-pattern bonding processes [the author investigated the contact resistivity using the post-pattern bonding process]. The details of how this structure was produced and measured are described in the next sub-section. Discussion here will focus on the measurement design methodology. It should be noted that the device depicted in Figure 6-9\textsuperscript{12} is not to scale and the mesa structure is very small in comparison to the substrate width and thickness. The real mesas are on the order of 10’s of micrometers in diameter, the epilayer is roughly a half of a micrometer thick, and the Si substrate is roughly a half of a millimeter thick.

![Figure 6-9. Illustration of the bond interface electrical contact resistivity measurement structure.](image)

Proceeding from the top to the bottom all the resistance contributions may be represented by
This equation is simply an extension of Cox and Strack’s method where \( R_{ctop} \) represents the contribution from the topside GaAs contact resistance and may be expressed by

\[
R_{ctop} = \frac{\rho_{ctop}}{A}
\]

where \( \rho_{ctop} \) is the specific contact resistivity of the top contact to GaAs and \( A \) is the footprint area of the mesa.

\( R_{epi} \) is the GaAs epilayer resistance dictated by its bulk resistivity and expressed by

\[
R_{epi} = \frac{\rho_{epi} h}{A}
\]

where \( \rho_{epi} \) is the thin film resistivity of the GaAs epilayer and \( h \) is the height of the epilayer thickness.

\( R_{cbond} \) is the term in question and contains the bond’s specific contact resistivity \( \rho_{cbond} \) represented by

\[
R_{cbond} = \frac{\rho_{cbond}}{A}
\]

\( R_{spread} \) is the bulk silicon resistance contribution that comes from the current spreading produced by the footprint of the mesa, and for now, will be assumed equal to

\[
R_{spread} = \frac{\rho_{Sibulk}}{4r} B
\]

where \( \rho_{Sibulk} \) is the bulk resistivity of the silicon substrate, \( r \) is the radius of the mesa footprint, and \( B \) is a constant close to one.
$R_{bottom}$ is due to the substrate backside contact which is common to all the device measurements on a single bonded substrate. Because it is common to all the measurements, it can be represented by an as yet undetermined constant value.

Guesstimating the values ahead of time shows, first: the term $R_{epi}$ is almost negligible and may be ignored if desired, second: the $R_{spread}$ and $R_{bottom}$ values dominate the total resistance, and lastly: the $R_{total}$ will only be a few ohms. The $R_{epi}$ term may be negligible, but for completeness, will be included. The second and third conclusions require special treatment. In order to extract such a small $R_{ccond}$ from an already small $R_{total}$ the resistance of the measurement leads (not included in Equation 6-3) must be removed as they are also on the order of a few ohms and variable from measurement to measurement. As discussed below, a 4-wire Kelvin measurement is capable of removing these lead resistances.

Assuming the terms $R_{ctop}$, $R_{epi}$, and $R_{spread}$ can be calculated and extracted from the measurement, and that $R_{bottom}$ is a constant, the residual resistance may be expressed by

$$R_{residual} = \frac{\rho_{ccond}}{A} + \text{const}$$  \hspace{1cm} (6-8)

Plotting this residual resistance versus the inverse of the footprint area results in a simple linear trend, with the slope indicating the $\rho_{ccond}$ and the constant $R_{bottom}$ term being ignored. The elegance of such a method is now clear. The calculation of $R_{ctop}$ and $R_{epi}$ terms are straightforward; however, the $R_{spread}$ term is more complicated.
Since the height of the test structure is small, in comparison to its width, any lateral current spreading within the mesa may be ignored. The current distribution flowing through the mesa may be assumed laterally constant (i.e. an equipotential top contact boundary condition) or assumed laterally variable (i.e. an isoflux top contact boundary condition). Because the lateral current spreading can be ignored, either lateral current distribution may be used without loss of generality, and the $R_{\text{top}}$ and $R_{\text{epi}}$ parallel plate approximation used in Equations 6-4 and 6-5 are valid. It may be argued that the top metal contact itself could be affected by lateral current spreading from the measurement probe tip; however, this second order effect is ignored in the present analysis due to the fact that the contact resistance is typically larger than the effective lateral contact metallization resistance.

Revisiting Equation 6-7 which describes $R_{\text{spread}}$, the correction term $B$ that was assumed to be one is not generally true. Cox and Strack proposed an empirical equation for $B$ as

$$B = \frac{2}{\pi} \arctan \left( \frac{2}{r/t} \right)$$

This empirical equation was determined, essentially with an equipotential boundary condition for the contact voltage leading to a constant lateral current. Gelmont and Shur$^{19}$ produced a rigorous analytical correction which behaviorally turns out to be fairly similar to the Cox and Strack equation, although slightly offset in value. The method of Gelmont and Shur was used to evaluate the $R_{\text{spread}}$ term in the measurements below. It should be noted; however, that the mesas were designed to be relatively immune to errors.
in the $R_{\text{spread}}$ calculations by virtue of their extremely small ratio of mesa radius to substrate thickness. This is the reason why $B$ can be assumed close to one.

### 6.6.3 Kelvin Measurement Discussion

The effect of the lead resistances may be removed during measurement if a Kelvin type connection is used. A Kelvin measurement uses four leads, instead of the typical two used, for current-voltage measurements. The two measurement types are schematically illustrated in Figure 6-10. R1 and R2 represent both the lead resistances, from the measurement probes to the measurement apparatus, including the resistance between the Device Under Test (DUT) and probe tips. The lead resistances are generally constant, from measurement to measurement; however, the probing resistances can vary depending on probe pressure, probe cleanliness, and probe/contact indentation. The probing resistances easily change from measurement to measurement.

![Figure 6-10. Illustrations of both the physical structure and equivalent circuit of an (a) traditional 2-wire measurement scheme and (b) Kelvin 4-wire scheme measurement scheme.](image-url)
If a driving current $I_d$ is passed from terminal-1 to terminal-2, and the voltage was measured at the same terminals in the 2-wire scheme, the voltage drops across resistors R1 and R2, caused by the driving current $I_d$, add to the total voltage seen at the terminals.

Note that the lead resistances, R3 and R4, in the Kelvin measurement schematic, are just as prevalent as resistances R1 and R2, yet are irrelevant. The driving current, $I_d$, is passed from terminal-1 to terminal-2 just as before but the voltage drop is measured across terminals-3 and 4 instead. The probing current required to obtain the voltage measurement, is exceedingly small in comparison to $I_d$, therefore, the voltage drops across resistors R3 and R4 are negligible, as if the voltage across terminals-3 and 4 were being measured across the DUT itself. The voltage drops across R1 and R2 are ignored as the voltage is no longer being monitored across terminals-1 and 2. With the voltage effectively measured across the DUT and the current $I_d$ flowing through it, the resistance $R_{\text{load}}$ can be measured without the influence of the lead resistances R1 to R4. Furthermore, the effects of the lead resistances R2 and R3 are also irrelevant and can be ignored.

### 6.6.4 Measurement Process Overview

Appendix C.1 details the procedure used to measure the bond interface specific contact resistivity. First, the samples were fabricated into their final measurement device form – the details of which may be found in Appendix B.2. Concurrently, bulk doped GaAs samples matching that of the grown epilayer, were fabricated with identical topside contacts and similar backside contacts. These fabrications included the same ohmic contact annealing treatments as the bond behavior measurement samples.
Next, the topsides of the devices, and backsides of the samples, were Kelvin connected to a semiconductor parameter analyzer, to measure the total resistance of each device. This was done for both the bonded samples and the reference samples.

The resistance contributions from the bonded epilayer were then calculated and subtracted from the total measured bond resistances. This residual resistance was plotted versus the inverse contact area from which the bond interface specific contact resistance was determined.

### 6.6.5 Measurement Process Discussion

The contact resistivity extraction followed the method outlined in the theory section without deviation. The most important step in the device fabrication was the mesa isolation. Without this step, the current would unpredictably spread throughout the bondmetal layer and continue into the bulk Si substrate. During tests, the error this spreading brought to the measurement was intolerably high. Unfortunately, due to the low yield of the post-pattern process, only the n-GaAs/p-Si sample survived to be measured. However, the remaining bond interface contact resistivities may be estimated from the relative slopes of the other dopant combinations (see Figure 6-7) in comparison to the n-GaAs/p-Si case.

### 6.6.6 Discussion of Results

Figure 6-11 shows the residual resistance plot versus inverse area for a set of devices on an n-GaAs/p-Si bonded sample. Both materials were doped to a concentration of approximately $1 \times 10^{18} / \text{cm}^3$. The slope of the line depicts a bond interface specific contact resistivity of $1.03 \times 10^{-5} \text{ ohm-cm}^2$ (±$4.6 \times 10^{-7}$). The inset illustrates the I-V...
behavior of a representative structure, showing that the linear behavior assumption made during the contact resistivity extraction was valid.

To validate this result, it is possible to compare it to an estimation of the expected results. To do this, let the contact resistivity be broken up into three contributions: the first from the GaAs-bondmetal interface, the second from the bondmetal itself, and the third from the bondmetal-silicon interface. The published contact resistivity of the first interface In-Pd/n-GaAs$^{11}$ is approximately $1–3 \times 10^{-6}$ ohm-cm$^2$, the published bondmetal resistivity is approximately 110 micro_ohm-cm$^{20}$ (which is actually quite negligible), and the published Pd/p-Si$^{21}$ contact resistivity is approximately $5–15 \times 10^{-6}$ ohm-cm$^2$. Adding these together will yield a range of $0.6–1.8 \times 10^{-5}$ ohm-cm$^2$ for the total bond resistivity, which matches well with the measured value of $1.03 \times 10^{-5}$ ohm-cm$^2$.

A bond contact resistivity of roughly $1 \times 10^{-5}$ ohm-cm$^2$ is reasonably low for many devices that may be implemented in an HMMIC scheme. If a smaller value were desired,
dopant layers may possibly be added to the bond metallization; however, the generality of the universal ohmic bond would be lost as the dopant layers would have to be selectively applied for n or p-type contact formation.

Based on the Fermi pinning discussion earlier, p-GaAs should yield a lower bond resistivity. The contact resistivity to either n or p-doped silicon should be roughly the same. Thus, this measurement is near the upper bound of all dopant combination bond resistivities, representing close to the maximum contact resistivity afforded by this alloy system. To estimate this, the relative slopes of the other doping combinations may be compared to the measured n-GaAs/p-Si case. This would yield bond interface contact resistivities of approximately $8.49 \times 10^{-6}$ ohm-cm$^2$ for the p-GaAs/p-Si, $9.08 \times 10^{-6}$ ohm-cm$^2$ for the p-GaAs/n-Si, and $1.37 \times 10^{-5}$ ohm-cm$^2$ for the n-GaAs/n-Si cases.

The accuracy of the analytical expression for $R_{\text{spread}}$ and its heavy dependence on radius, rather than area, worked well enough to resolve the bond contact resistivity for the case of small mesas on large substrates. It will be seen in the next chapter that a similar treatment for thermal resistivity extraction cannot use such a simple analytical model and must instead rely on a more involved experimentally verified empirical extraction technique.

### 6.7 Conclusion

The electrical behavior measurements show that the In-Pd alloy provides a universal ohmic contact between GaAs and Si. It is more advantageous to have ohmic contacts between HMMIC devices in order to produce more functional devices. Its
universal nature allows the process to be streamlined by integrating all doping types at once.

The contact resistivity of bonded materials is measured using the introduced metric. This measurement shows that the In-Pd alloy yields a contact resistivity of \(1.03 \times 10^{-5}\) ohm-cm\(^2\) between n-type GaAs and p-type Si. This would yield approximate bond interface contact resistivities of \(8.49 \times 10^{-6}\), \(9.08 \times 10^{-6}\), and \(1.37 \times 10^{-5}\) ohm-cm\(^2\) for the p-GaAs/p-Si, p-GaAs/n-Si, and n-GaAs/n-Si cases, respectively, based on the earlier ohmic nature I-V measured slopes. All of which are sufficiently low, to enable efficient connection between these HMMIC materials.

6.8 Acknowledgment

6.9 References


7 Bond Interface Thermal Conductivity Characterization

7.1 Introduction

High temperatures adversely affect HMMIC device operation. It is important to understand how heat is transferred in these systems if these temperatures are to be properly controlled. HMMIC systems are dominated by heat transfer via thermal conduction. Therefore, it is important to know the thermal conductivities of the materials involved, and understand their origins.

Many of the materials used to create HMMIC systems have thermal conductivities that are already known, however the In-Pd bondmetal alloy has not been characterized. The thermal conductivity of this layer must be determined if HMMIC device heat transfer is to be characterized.

This chapter describes the bond interface material’s thermal conductivity measurement. Section 7.2 introduces several existing thermal conductivity measurement methods, and describes the specific approach used to obtain the bondmetal thermal conductivity. Sections 0 through 7.5 detail how the method extracts the thermal conductivity from measurements. Section 7.6 reveals the results of the measurements, compares them to the expected results, and discusses how they relate to other forms of integration.
7.2 Measurement of Bond Interface Thermal Conductivity

Based on the discussion in Appendix A, it is asserted that the thermal conductivity of the bond alloy cannot be accurately theoretically calculated, therefore a measurement must be made. Just as with the electrical bond contact resistivity measurements, no bond interface thermal conductivity measurement methods existed at the time this dissertation was being investigated. Traditional conductivity methods were surveyed to determine a suitable method to adapt to this cause. A review of several thin film thermal conductivity measurement methods was published by Mirmira and Fletcher. Another review may be found in reference 2.

7.2.1 Existing Measurement Methods

A few representative methods are highlighted in Figure 7-1 through Figure 7-3 and discussed below. Most of the methods implement a monolithic heater of some kind, which is used to provide a measurable amount of heat, as well as measure the temperature along the heater. Knowing temperature of, and power provided to the system, completes the boundary requirements necessary to model the heat transfer in a system. Since the heat transfer in these systems is dominated by conduction, it is possible to extract their associated thermal conductivity values.

7.2.1.1 Steady State Measurement Methods Discussion

Steady state contact methods provide a constant heat source and evaluate the thermal conductivity based on steady state heat conduction. These methods require knowledge of the heater’s temperature and power output, as well as, a temperature reference either in the system boundary or elsewhere within the system. These types of
measurements are illustrated in Figure 7-. They are split into two categories: those implementing a boundary reference and those implementing an embedded reference.

**Boundary Reference:**

Baier and Völklein\(^3\) published a method to extract the vertical thermal conductivity of thin films by using samples with different thickness but with the same footprint. At least two thin film thicknesses are required to implement this technique.

**Embedded Reference:**

Swartz and Pohl\(^4\) published a method to extract the thermal conductivity of interfaces by implementing a probing structure in close coplanar proximity to a source heater on a uniform solid. At least two heater structures are required to implement this technique and the heat spreading in the substrate must be modeled.

Zhang and Grigoropoulos\(^5\) published a method to extract the lateral thermal conductivity of a free standing film by also using a coplanar heater near a probing structure. This method uses structures that require extensive fabrication.
7.2.1.2 Transient Measurement Methods Discussion

Transient contact methods use a time variant heat source to evaluate the thermal conductivity. These methods do not rely on steady state conduction and therefore may be ‘self-referencing’. They do not require a temperature reference. Due to their transient nature, they can evaluate heat capacity as well as thermal conductivity. These types of measurements are illustrated in Figure 7-2. They are split into two categories as well: those implementing continuous wave excitation and those implementing step excitation.

![Figure 7-2. Illustrations of transient thermal conductivity measurement methods.](image)

**Continuous Wave:**

Cahill and Pohl\(^6\) published a method to measure the thermal conductivity of a solid body by applying a continuously varying driving current to a monolithic heater strip and measuring its temperature response. This method assumes a 2D analysis and neglects the heat capacity of the heater. Multilayer models have also been created to estimate thin film thermal conductivity from a single measurement; however, most implementations require samples with several different thicknesses to be measured.\(^7\)

**Step Excitation:**

Okuda and Ohkubo\(^8\) have published a method to measure thin film thermal conductivities via a step impulse method. A strong step impulse current is driven through
a monolithic heater while a high speed system monitors its temperature response. The
heat diffuses in a very short time and this process requires nanosecond data acquisition
resolution. The heat capacity of the heater must be included in the analysis and has not
been adequately analytically modeled; the system must be simulated to obtain accurate
results.

7.2.1.3 Non-Contact Measurement Methods Discussion

Non-contact methods use an optical method to evaluate the surface temperature
distribution in a system. Heat may either be applied via traditional contact methods or by
intense laser radiation. These types of measurements are illustrated in Figure 7-3. They
are also split into two categories: those implementing thermoreflectance, and those
implementing local thermal expansion.

Figure 7-3. Illustrations of non-contact thermal conductivity measurement methods.

Thermoreflectance:

Dilhaire et al.\textsuperscript{9} published a method to measure thin film conductivity using a
monolithic heater as a periodic heat source using scanning thermoreflectance to measure
the surface temperature. Optically opaque materials must be employed to use this technique.

**Local Thermal Expansion:**

Bhusari *et al.*\(^{10}\) published a method to measure the movement of heat wave through a material. A modulating pump laser launches a traveling heat wave into the material, which causes the sample surface to ripple via local thermal expansion. A probe laser and detector system is used to measure the movement of the wave to determine heat capacity. This method requires optical absorption to occur in the sample in a very specific manner.

### 7.2.2 Investigated Method Introduction

Non-contact methods require excessive calibration and special equipment, and therefore would require considerable effort to realize. The \(3\omega\) and pulse/step transient methods are excellent at excluding the ambient environment from their evaluation, but require special equipment and modeling, and were therefore not investigated. It should be noted however, that these methods would be of use in the future if high accuracy thermal conductivity measurements were required, or if heat capacity needed to be measured.

Embedded reference methods are very accurate, and can require minimal calibration, but need extensive fabrication and special device geometries to be defined. Swartz and Pohl’s method was originally investigated, but it was feared that any excessive post bond fabrication might affect the yield of precious bonded samples and so was not investigated further.
External reference methods require the calculation of the entire structure and require analytical, simulation, or empirical methods to evaluate the structure, which present their own difficulty. However, these methods may be implemented using simple device structures in a bond evaluation setting, such as this dissertation’s investigation. Despite the analysis complications, this style of measurement was chosen to investigate the bond interface thermal conductivity.

7.2.3 Investigated Method Principle

Akin to the bond interface specific electrical conductivity measurement, this method also uses the idea of additive resistances. In this case, these resistance components are thermal resistances and reflect the new geometry of this monolithic heater method.

Figure 7-4 depicts a basic illustration of one of the measurement devices. The illustration is far from scale but provides an adequate qualitative description. The heaters and bonded mesas are either a millimeter or half millimeter in length and a few 10’s of micrometers wide, while the bonded mesa height is roughly 2 micrometers thick. The slender bond region of these bonded devices required the fine texture, high yield, and sparse nature of the pre-pattern bonding process.
Figure 7-4. Illustration of the bondmetal thermal conductivity measurement and equivalent circuit.

The sample was secured to a heatsink which was maintained at a constant temperature, regardless of the power input to the heater to provide the boundary temperature reference. The monolithic heater was heated by passing current along its length. In order to do this the bonded mesa epilayer was grown undoped, to act as an insulating layer, to prevent current from leaking out of the heater. This current provided power via Joule heating in the resistive heater. The voltage of the heater was monitored by voltage taps at either end of the heater to measure its resistance. Calibrations of the heater at various temperatures were used to calculate an empirical relationship between temperature and heater resistance. This relationship was used to calculate the resulting temperature of the heater. With the boundary reference temperature being held constant by the heatsink, all the requirements necessary to evaluate the thermal resistance of the system were fulfilled.

The total thermal resistance of the system may be broken up into its constituent resistances as

\[
R_{\text{total}} = R_{\text{mesa}} + R_{\text{bond}} + R_{\text{spread}}
\]
where $R_{\text{mesa}}$ is the thermal resistance of the bonded epilayer mesa, $R_{\text{bond}}$ is the sought after bond resistance, and $R_{\text{spread}}$ is the spreading resistance associated with the materials between the bottom of the bond and the heat sink temperature reference. The mesa contribution may be calculated using a parallel plate approximation and the known thermal conductivity of the epilayer material using:

$$R_{\text{mesa}} = \frac{WL}{h_{\text{mesa}} \kappa_{\text{mesa}}} \quad 7-2$$

The spreading term, however, is rather tricky to analytically calculate and, unlike the electrical resistivity measurement, is not easily separable from the contact resistance. During the electrical contact resistivity extraction the contact resistance term represented a large fraction of the total resistance and relaxed the accuracy requirement of the spreading term. In addition the radius and area of the electrical contacts dominated the contact resistance and spreading resistance terms respectively. Due to the high contrast of contact conductivities to bulk resistivities, the equipotential contact approximation for the electrical spreading resistance was valid. This is in stark opposition to the thermal situation, where the low contrast of the thermal conductivities of the heater and heatsink to that of the sample, make this approximation invalid. If the total resistance can be found, and the mesa and spreading terms determined, then the resulting bond resistance would yield the bond thermal conductivity via another parallel plate approximation:

$$\kappa_{\text{bond}} = \frac{WL}{h_{\text{bond}} R_{\text{bond}}} \quad 7-3$$
7.3 Investigated Method Thermal Conductivity Extraction Theory

This subsection details the theory behind the bond interface thermal conductivity measurement method used.

7.3.1 Analytical Spreading Resistance Calculation Approach

The width of the heater is small, in comparison to the substrate thickness, while its length is actually greater. This essentially means that the influence of the substrate thickness plays a non-negligible role in the evaluation of the heat spreading. Thus the spreading evaluation will contain terms that relate to the area of the heater in addition to its small width. The spreading resistance term used in the electrical contact resistivity extraction was dominated by the radius of the mesas with a minor correction factor added to enhance accuracy. The correction factor calculation was dependent on the radius, as well as the area and the thickness of the substrate, but its contribution was so minor that any error in its calculation would not affect the overall spreading calculation. Also, the position and distribution of the voltage at the bottom of the contact of the substrate was well defined, whereas the heatsink temperature reference position and distribution within the heat sink is not well defined and presents a problem. Therefore the simple extraction technique available in the bond electrical contact resistivity measurement has no analog in the bond thermal conductivity measurement and accurate calculations of the heat spreading term had to be made.

7.3.1.1 Equipotential versus Isoflux Heater Approximations

The lateral thermal resistance of the heater is not exceedingly small in comparison to the lateral thermal resistance of the substrate, as was the case with the electrical
resistance of the top contact and substrate in the electrical bond contact resistivity measurement. This means that the equipotential approximation used for the top electrical contact is not valid for the monolithic heater, and an isoflux approximation must be used.

Fortunately, the isoflux heater approximation aids the analytical evaluation of the problem. The boundary conditions of an equipotential heater are a very harsh condition to impose on the spreading formulation and would make its evaluation very complex.

7.3.1.2 Isoflux Heater Analyses

**Infinite Solid:**

If the substrate / thermal grease / heatsink combination were modeled as an infinite solid, some useful behavior may be gleaned. Loewen and Shaw\textsuperscript{11} solved for a patch of length $2m$ and width $2l$ imposing a constant heat flux on an infinite solid by analytically integrating the influence of a point of heat flux over the patch. The influence of the point of heat flux on the solid was given by Kelvin’s integration of the Fourier heat-transfer equation. Their solution for the average temperature of the heater patch was

$$T_{\text{ave}} = \frac{2q}{\pi \kappa m l} \left[ \ln^2 \sinh \left( \frac{L}{m} \right) + ml^2 \sinh \left( \frac{m}{l} \right) + \frac{1}{3} \left( m^3 + l^3 - (l^2 + m^2)^{\frac{3}{2}} \right) \right]$$

7-4

The equation is quite elegant and requires only hyperbolic signs with no series summations. Figure 7-5 provides a simple illustration of their isoflux heater on an infinite solid.
The original heater pattern used to investigate the thermal conductivity using this method (see Appendix D.2) measured the voltage across just a portion $2n$ of the heater length as illustrated in Figure 7-6a. This meant that the measured average temperature was only evaluated over a portion of the heater and Loewen and Shaw’s method – which evaluates the entire heater – had to be re-evaluated over this smaller portion. The resulting equation:

$$\begin{align*}
T_{ave} = \frac{2q}{\pi \kappa nl} & \left[ + l \left( \frac{m+n}{2} \right)^2 \sinh^{-1} \left( \frac{2l}{m+n} \right) \\
& - l \left( \frac{m-n}{2} \right)^2 \sinh^{-1} \left( \frac{2l}{m-n} \right) \\
& + \left( \frac{m+n}{2} \right) l^2 \sinh^{-1} \left( \frac{m+n}{2l} \right) \\
& - \left( \frac{m-n}{2} \right) l^2 \sinh^{-1} \left( \frac{m-n}{2l} \right) \right] \\
& + \frac{1}{3} \left( \frac{m+n}{2} \right)^3 + \left( l^2 + \left( \frac{m-n}{2} \right)^2 \right)^{\frac{3}{2}} \\
& - \frac{1}{3} \left( \frac{m-n}{2} \right)^3 + \left( l^2 + \left( \frac{m+n}{2} \right)^2 \right)^{\frac{3}{2}} \right] 
\end{align*}$$

7-5
was considerably longer. The calculation leading to this equation (omitted for brevity) was rather involved, but proceeded in the same manner as Loewen and Shaw’s formulation.

This prompted the design of the later revision heater described in Appendix D.2 and illustrated in Figure 7-6b. This revision measures the average temperature over a region containing nearly the entire heater area allowing the original Loewen and Shaw equation to be used.
A method by Leturcq *et al.*\textsuperscript{12} extended the analytical heat spreading solution for a general point of heat flux on an infinite half space into a point on a multi-layer substrate. The general point on an infinite half space was integrated along the entire heater patch in the Loewen and Shaw formalism. Starting with the equation for a point heat source on a composite half-space, as done by Leturcq *et al.* would allow the inclusion of different thermal conductivities for each of the substrate / thermal grease / heatsink layers to more accurately approximate the real situation. Their evaluation is very complicated and requires numerical integration which is tedious and yields a less intuitive result.

*Finite solid:*

The effects of the finite size of the substrate are also important factors in the accurate evaluation of the spreading term. The closer the heater gets to the edge of the substrate, the greater this effect becomes. Linsted and Surty\textsuperscript{13} used Fourier series expansion techniques to solve a uniform bulk finite substrate but the series requires an enormous number of terms when the scale of the heater is tiny, in comparison to the solid – such was the case of the investigated heater measurement structure. Lindsted and Surty’s formulation was expanded to multiple layers as well, by Kokkas\textsuperscript{14}, which yielded an even more involved formulation.

Pallisoc and Lee\textsuperscript{15} derived a double Fourier series expansion technique to solve bulk finite substrate problems which converged much faster than the Lindsted and Surty series, but required numerical integration due to their extreme complexity.

Karmalkar *et al.*\textsuperscript{16} used the notion of spreading symmetry in a finite solid to split eccentric heaters into four concentric heater quarters. The concentric heaters may be
evaluated using other finite techniques and stitched together to evaluate the eccentric heaters. This allows generic concentric heater formulations to be generally applied to eccentric heaters.

### 7.3.1.3 Accuracy of Analytical Expressions

All of the improvements to the simple analytical approximation of Loewen and Shaw can improve the accuracy of the thermal spreading resistance evaluation and their results match full three-dimensional finite element models within just a few percent or less. There are other issues that conspire to ruin the validity of all of the previous approaches, including the full three-dimensional finite element modeling approach.

All of the methods so far, assume that the thermal conductivity of the materials involved are well characterized when in fact agreement on thermal conductivities from different authors typically span a range of about 5-15% for most materials. This is caused by the variation between samples, sample preparation, and thermal conductivity measurements techniques used in each investigation.

Another factor that affects the error is the poorly defined position of the reference temperature within the body of the heatsink. This effect introduces uncertainty in the substrate boundary condition, required by the analytical approaches, and complicates the finite element modeling.

Also, the edge effects of the sample boundary of such a tiny ratio of heater width to substrate size, eclipses the accuracy of simple finite element models, requiring the use of the previously mentioned, very involved, finite solid analytical models.
The thermal conductivity spreading resistance calculation is directly affected by these uncertainties. When compared to real world values, the calculated spreading resistance inaccuracies can be on the order of 10-15%. Spreading resistance term errors of this magnitude lead to extracted bondmetal thermal conductivity errors on the order of 50-100% – this level of error is unacceptable.

As a result it is far better to empirically determine the spreading resistance term by measuring similar heaters on reference samples. This can be accomplished with much higher accuracy than any of the analytical or simulation models.

7.3.2 Empirical Spreading Resistance Approach

The empirical spreading resistance approach endeavored to accurately model the thermal spreading resistance term of each device using an identical substrate / thermal grease / heatsink stack. The heaters were electrically insulated from the silicon substrate during measurement, by a thin layer of PECVD silicon oxide. The effect of this oxide layer was extracted from the measurements, to yield the substrate spreading term. Heaters that matched the size and placement of the to-be-measured bonded sample heaters were used to remove any edge effect variations. Any discrepancy between the reference heater dimensions, and bonded heaters, were accounted for to attain highest accuracy. This was accomplished by applying an empirically fitted function to the reference heater measured dimensions. A series of differently dimensioned reference heaters in similar proximity to an edge of the substrate were used to develop the empirical model.
Loewen and Shaw approximated the average temperature of the heater in their isoflux heater patch on an infinite half space formulation from the general Equation 7-4 by

\[
T_{ave} = \frac{2ql}{\pi \kappa} \left( \ln \left( \frac{2m}{l} \right) + \frac{1}{3} \frac{l}{m} + \frac{1}{2} \right) \tag{7-6}
\]

valid when the heater aspect ratio is greater than about 20. The actual heaters used in experiments had aspect ratios on the order of 25-85 and 50-170 (for 0.5mm and 1mm heaters respectively) – both higher than the required value.

This equation was shortened to the empirical formula

\[
T_{ave} = a \ln (l) + b \tag{7-7}
\]

separately for each of the two heater lengths (recall that \(2l\) was defined as the overall width of the heater, not its length). The constants \(a\) and \(b\) encompass all the effects of width variation for each heater length. The common Carslaw and Jaeger\(^{17}\) equation,

\[
T_{C&J} \approx \frac{q}{\pi \kappa m} \ln \left( \frac{4m}{l} \right) \tag{7-8}
\]

stems from the validity of the Loewen and Shaw approximation. Carslaw and Jaeger approximated a similar isoflux patch on an infinite half space, but chose to approximate the result when the width and length of the heater were approximately equal. The approximation under such a condition obliterates any previous distinction between the evaluation of the heater’s average temperature and its maximum temperature. Therefore, it is vague enough to allow an isoflux heater to be approximated as an isothermal heater and is typically quoted for such use in many textbooks, without caution.
7.3.2.1 Accuracy of Empirical Method

The measurements used to produce the constants $a$ and $b$ fit the model of Equation 7-7 with an error of less than a few percent. With the spreading resistance term accurately determined by the empirical method, the only term left to solve was the thermal resistance of the bonded mesa insulator epitaxial layer. This term’s error stems directly from the range given in the accepted value of its material’s thermal conductivity, which is on the order of a 5 percent for GaAs. The error in extracting the bond resistance term is limited by the epitaxial layer’s thermal conductivity uncertainty and spreading resistance empirical fitting error. The extraction of the bond conductivity requires accurate knowledge of the bond thickness which is achievable to within a few percent. Therefore an individual bond thermal conductivity value may have an accuracy error on the order of about 5-10 percent, which is comparable to the range in thermal conductivity values of many common semiconductor materials.

7.4 Measurement Overview

The bond interface thermal conductivity measurement procedure Appendix C.2 details the measurement procedure. This process overview illustrates the basic process steps involved.

7.4.1 Sample Preparation

First, the bond samples were fabricated into their final measurement device form, using the pre-pattern bonding process – the details of which may be found in the pre-pattern bonding process section of the ITS bonding implementations chapter. The GaAs bond epilayer was grown without intentional doping to act as an electrical insulator.
for the monolithic heater. Bulk silicon samples, matching that of the bond substrate, were fabricated separately with a thin PECVD silicon oxide layer to act as a similar electrical insulator, upon which identical monolithic heaters were fabricated.

**Setup Calibration and Sample Mounting:**

Next, the temperature stage (heat sink) was calibrated to within an accuracy of 0.1°C using a calibrated thermistor. The temperature of the heat sink was controlled by a thermoelectric cooler and matching controller.

After stage calibration, the silicon reference sample was mounted using a minimal amount of thermal grease, the electrical probes were attached to a structure’s heater contact pads and the whole measurement setup was shrouded with a clean cloth to remove environmental air currents.

**Break-In:**

The heater was then ‘broken-in,’ to stabilize its resistance, by applying a current for a long period of time – this period of time was higher than would be used during measurements. After the ‘break-in’ period, the heater’s resistance was measured with a small probing current to estimate the resistivity when the stage was at 75°C and at room temperature – this provided the upper and lower resistance bounds for the measurement.

A high current is then applied to heat the heater to achieve roughly the 75°C tested resistance, while the heatsink was maintained at room temperature – this provided the upper bound for the heating current used in the test.

**Heater Power and Temperature Measurement:**

After the bounds of the test were established, several heating currents were applied to the heater while the heat sink was maintained at room temperature and their
associated resistances recorded. A quadratic distribution of currents later yielded an evenly spaced distribution of input power.

When the heating test was complete, the temperature-resistance relationship was accurately mapped by applying a small probing current as the stage temperature was incrementally increased. The entire process was repeated for the remaining reference heater structures on the reference sample, as well as the test structures on the bonded sample.

**Thermal Resistance Extraction:**

Once the temperature-resistance and heating current-resistance relationships were established, the temperature of the heater and input power at each heating current were determined. These relationships could be combined into a single input power-heater temperature relationship. Plotting this as heater temperature, versus input power, the slope of the line at any given temperature yields the total thermal resistance of the system. In the case of the reference sample, this would be the sum of the oxide layer term and the spreading resistance term.

**Bond Interface Thermal Conductivity Extraction:**

Once the total thermal resistances for all the relevant reference and bonded test structures were made, the oxide layer and epitaxial layer terms were subtracted from the totals to yield residual thermal resistances. The residual resistance of the reference sample was the spreading resistance, and any dimensional differences in the reference sample were fitted using the empirical spreading resistance equation – sets of structures commonly separated from the edge of the sample were modeled together. This spreading resistance term was then subtracted from the residual resistances of each of the bonded
structures to yield each one’s bond resistance. The measured bond thickness was then used to calculate the bond thermal conductivity from the bond resistance for each structure.

7.5 Measurement Discussion

The oxide thickness was chosen to yield a thermal resistance approximately equal to that of the bonded epitaxial layer to minimize any unaccounted for errors. PECVD oxide provided the lowest defect density insulator attainable.

The temperature stage (heat sink) was experimentally verified to maintain a set temperature to within about 0.08°C variation over the long term. The error evoked by this variation was subdued by calculating an empirical trend for the array of heating current measurements taken over a long period of time.

Samples were pressed into the thermal grease with similar pressure for each sample. Several attempts showed that the thickness was repeatable to within a few percent and the resulting thermal resistance values were repeatable within one percent. This was important, as any systematic variation between the reference and bonded sample would carry through to the resultant bond interface thermal conductivity value.

During the heater break-in period, the resistance stabilizes, presumably as the polycrystalline grain structure of the as-evaporated nickel heater film electromigrates into a more stable configuration. The resistance changed by no more than a half of a percent during this process; however, if left undone, would add to the overall error.

The empirical fitting error of the thermal resistance measurements for each structure rarely exceeded half of a percent. The limiting error in the entire thermal
conductivity extraction was mostly due to the error in the known thermal conductivity of the GaAs epilayer material and to a lesser degree the fitting error of the spreading resistance empirical model.

### 7.6 Discussion of Results

Table 7-1 lists representative thermal conductivity values extracted from the measurements. The average thermal conductivity for the bond alloy was 2.51 W/m-K with a standard deviation of 14.2%. The actual bond alloy thermal conductivity error for this measurement would be a combination of this standard deviation and the thermal resistivity confidence errors. This error includes both the GaAs thermal conductivity literature value uncertainty and the spreading resistance empirical model fitting error, totaling about 10%. Therefore, the extracted bondmetal accuracy is on the order of about 25%.

<table>
<thead>
<tr>
<th>Test Structure Designation</th>
<th>Measured Thermal Conductivity (W/m-K)</th>
<th>Measurement Uncertainty (stdev/mean)</th>
<th>Total Sample Accuracy</th>
</tr>
</thead>
<tbody>
<tr>
<td>B3l</td>
<td>2.22</td>
<td>14.2%</td>
<td>~ 25%</td>
</tr>
<tr>
<td>A5l</td>
<td>1.90</td>
<td></td>
<td></td>
</tr>
<tr>
<td>A2s</td>
<td>2.61</td>
<td></td>
<td></td>
</tr>
<tr>
<td>A4s</td>
<td>3.30</td>
<td></td>
<td></td>
</tr>
<tr>
<td>mean</td>
<td>2.51</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

The scatter in data was most probably due to variations in the way indium squeezed out during annealing. The variation in squeezed out would affect bond
thickness, as well as bond alloy composition. A more ideal pressure plate and more closely spaced standoffs might improve this variation in the future. In a manufacturing environment, residual contamination particles would be much smaller than those involved in this investigation, allowing a lower pressure to be applied during bonding, ultimately improving uniformity.

Another factor leading to the measurement disparity, may be due to unseen thermal measurement error in the apparatus, or experimental method. Judging from the exceptional empirical fitting error of the reference sample structures, on the order of a percent or two, this source of error was likely very small.

The reader may first point to hidden bond voids as the root cause of the variation; however, due to the stress involved, any voids warp the epilayer. This warping is easily detected under a microscope, as shown in Figure 7-7, and the results from such structures were discarded. As an example, one bonded structure was tested that had two patches of warped area, covering approximately 5-10% of its area.

![Figure 7-7. Microscope image of a void induced bonded epilayer warping.](image-url)
7.6.1 Bond Interface Thermal Conductivity Estimates

The initial guesstimate for the thermal conductivity was about 5-10 times worse than the bulk thermal conductivities of either indium or palladium, based on the behavior of many different material alloys. No thermal conductivity of similar metal alloys had been reported, thus, the guesstimate was based on other material systems which were highly crystalline. The measured value was about 30 times lower than either bulk value. This introduced a potential question as to why the thermal conductivity was so much lower than either of its constituent bulk values.

The difference was presumed to come from the grain structure and poor thermal conductivity of the alloy itself. The ITS alloying process was never expected to yield a single crystal alloy. The thermal conductivity of similar alloys had yet to be reported, therefore, no comparison could be made.

As alluded to earlier, there is the possibility of using the Wiedemann-Franz law if the electrical conductivity of the alloy were known. Grebennik and Tsimbal\textsuperscript{18} did happen to measure the electrical resistivity of In-Pd alloy system thin films. Their annealed alloy electrical resistivity results are plotted versus alloy composition in Figure 7-8 -- an atomic percent palladium scale has been utilized rather than Grebennik and Tsimbal’s original mass percent palladium scale. Note, as they did, that the resistivity is not a smooth function of the alloy composition as might be expected, but varies sharply depending on the alloy composition. The variations follow the intermetallic alloy phases as shown. Note that the alloy resistivity at 30 atomic% palladium, representing the expected In\textsubscript{7}Pd\textsubscript{3} bond alloy, is about 1.20x10\textsuperscript{-6} ohm-m.
Let the In$_7$Pd$_3$ resistivity, as calculated by a linear average of its known bulk constituent values, be $1.02 \times 10^{-7}$ ohm-m, and the linearly averaged thermal conductivity value, based on its known bulk constituent values, be 78.7 W/m-K. Using the Wiedemann-Franz law, the linear average Lorentz value for the alloy at room temperature, is calculated to be $2.702 \times 10^{-8}$ W-ohm/K$^2$ – note that this matches fairly well with the standard value of $2.4453 \times 10^{-8}$ W-ohm/K$^2$. Applying this calculated Lorentz value to Gebennik and Tsimbal’s experimentally measured electrical resistance yields an expected electronic thermal conductivity component value of 6.71 W/m-K. This value does not include the added thermal resistivity of the lattice contribution and assumes the Lorentz value of the alloy is accurately predicted by its constituent’s average value.

Normally, in metals, the lattice contribution may be ignored, but when the metal is a poor electrical conductor, this contribution could be of a comparable value. The
lattice conductivity is likely to suffer from grain boundary scattering (phonon-boundary relaxation) as well as phonon-phonon relaxation within the alloy itself. Keyes’ approximation yields a rough lattice contribution estimate of 0.2 W/m-K for the In$_7$Pd$_3$ alloy based on data from Flandorfer.\textsuperscript{19}

The total thermal conductivity is expected to be the sum of the electronic and lattice thermal conductivities based on the discussion earlier. However, when the effects of grain boundary scattering are taken into account, the total thermal conductivity is expected to be lower than this ideal total, as evidenced by Matthiessen’s rule. The expected value (below 6.71 W/m-K) matches favorably with the average experimental value of 2.51 W/m-K.

It should be noted that the bond annealing was assumed to be in a reducing atmosphere. If this was not the case, and the bond metal was allowed to partially oxidize, then the thermal conductivity could suffer. Some of the measured value discrepancy could be due in part to this effect.

### 7.6.2 Bond Thermal Conductivity Comparison

No experimental values of the thermal conductivity of different bonds were available at the time this dissertation was being investigated. To compare this metal bonding technique to other forms of wafer bonding, the thermal conductivities of several materials, that are used to bond III/V to silicon reported in the literature, are shown in Table 7-2. The right column of which compares each particular bond material with the average experimental In$_7$Pd$_3$ bond alloy thermal conductivity.
Table 7-2. List of bulk thermal conductivities of typical heterogeneous bonding interface materials.

<table>
<thead>
<tr>
<th>Bond Material</th>
<th>bulk / thin film</th>
<th>Thermal Conductivity (W/m-K)</th>
<th>Comparison to In$_7$Pd$_3$</th>
</tr>
</thead>
<tbody>
<tr>
<td>polyimide</td>
<td>thin film</td>
<td>0.22$^{20}$</td>
<td>11.4x</td>
</tr>
<tr>
<td>BCB</td>
<td>thin film</td>
<td>0.24$^{20}$</td>
<td>10.5x</td>
</tr>
<tr>
<td>SiO2</td>
<td>thin film</td>
<td>$1.1^{21}, 1.26^{20}, 1.29^{22}$</td>
<td>2.1x</td>
</tr>
<tr>
<td>In$_7$Pd$_3$ bondmetal</td>
<td>thin film</td>
<td>2.51</td>
<td>1x</td>
</tr>
<tr>
<td>Pb$<em>{63}$Sn$</em>{37}$ solder</td>
<td>bulk</td>
<td>55$^{23}$</td>
<td>1/21.9x</td>
</tr>
<tr>
<td>Sn</td>
<td>bulk</td>
<td>66.6$^{24}$</td>
<td>1/26.5x</td>
</tr>
<tr>
<td>Pd</td>
<td>bulk</td>
<td>71.8$^{24}$</td>
<td>1/28.6x</td>
</tr>
<tr>
<td>Sn$<em>{95.8}$Ag$</em>{3.5}$Cu$_{0.7}$ solder</td>
<td>bulk</td>
<td>73$^{23}$</td>
<td>1/29.1x</td>
</tr>
<tr>
<td>In</td>
<td>bulk</td>
<td>81.6$^{24}$</td>
<td>1/32.5x</td>
</tr>
</tbody>
</table>

The In$_7$Pd$_3$ bond alloy outperforms all bulk insulator bond materials but does not compare well with bulk metal bond materials. The reader should be reminded that the remelting limitation of solder, indium, and tin bonding, as well as the stress limitation of non-ITS palladium bonding, must be kept in mind.

From a thermal resistance standpoint, the thermal conductivity must be accompanied by a bond layer thickness. The thickness of the bond layer could severely impact the comparison. To quantify this statement, the thickness of flip-chip solder bonds are typically on the order of several micrometers, as opposed to the roughly half a micron In$_7$Pd$_3$ ITS bond alloy. Thus the thermal resistance of the In$_7$Pd$_3$ ITS bond alloy would be close to that of solder bonding.

Another important difference between flip-chip solder (bump-bonding) and this In-Pd ITS metalbonding method should be highlighted. Bump-bonding, as its name implies, bonds materials using a series of bumps. Its purpose is to scale IC packages by replacing wirebonds with bump-bonds. The individual bumps cannot support bonded waveguides as easily or as compactly as the ITS metalbonding approach. The bump size
Large sized bumps result in excessive parasitic reactances which adversely affect microwave propagation.

Other metal ‘bonding’ methods do exist which simply place devices with metal contacts onto hosts with similar metal contacts using van der Waal forces; however, these contacts are generally inferior to chemically bonded contacts, such as ITS metalbonds. These weak van der Waal bonds do not connect the contacts optimally across their interface and can leave tiny gaps between the contacts. These gaps result in a thermal contact resistance, similar to the electrical analog, except their reduction of thermal conductivity is generally not as severe as its electrical counterpart. None-the-less, this thermal contact resistance does unnecessarily add to the net thermal resistance when compared to ITS metalbonding.

The total system thermal resistance would include effects from the device layers, bond layer, and substrate. This entire system thermal resistance is what matters, as a whole, to a bonded device. The substrate generally presents the largest contribution to the total system thermal resistance, therefore, a comparison should be made between un-bonded and bonded devices which use different substrates. The total system thermal resistance of GaAs devices grown on native GaAs substrates versus GaAs devices In$_7$Pd$_3$ ITS metal bonded to silicon should be compared. In$_7$Pd$_3$ ITS metal bonded structures on the order of the size of the measured heater structure would provide roughly a 2 times improvement in total system thermal resistance. Therefore, this metalbonding method would provide a marked improvement in device performance in spite of the mediocre bondmetal thermal conductivity.
7.7 Conclusion

The thermal conductivity theory was unable to predict the thermal conductivity of the bond alloy. In order to obtain an accurate value, a bond conductivity measurement was necessary. Several existing measurement methods were surveyed and an adequate measurement method was highlighted. This determined a bondmetal thermal conductivity of 2.51 W/m-K. This result was compared to other bond materials in order to evaluate its effectiveness. Although the bond thermal conductivity value was lower than anticipated, it would still provide a two-fold improvement in system heat conduction, when compared to an un-bonded GaAs case.

The Wiedemann-Franz law, that was capable of closely matching the measured value for this bondmetal, may be applied when searching for a higher thermal conductivity bondmetal in future investigations.
7.8 References


23. L. Kehoe, G. M. Crean, “Thermal conductivity and specific heat determinations of a set of lead-free solder alloys,” Proceedings of the 4th International

8 Bonded Device Microwave Characterization

8.1 Introduction

A solid understanding of microwave propagation is required to properly design HMMIC systems. Not only of general microwave systems, but also of specific structures relevant to the HMMIC architecture. Certain structures are better suited for HMMIC than others. It is important to choose the type which can provide the most optimal design. Theory may guide a designer, but measurements are needed to extract actual device behavior. Understanding how to extract microwave propagation data from these measurements and how to analyze the results are both essential to realize peak performance systems. This analysis may be performed analytically and/or via computational modeling.

This chapter is divided into three parts: the first part (sections 8.2 through 8.4) discusses the theory and measurement analysis of microwave propagation, the second part (sections 8.5 through 8.7) provides a theoretical analysis and comparison of the two most common waveguide geometries used in microwave integrated circuits, and the last part (sections 8.8 through 8.10) describes the microwave propagation in three forms of waveguide relevant to metalbonded HMMIC systems.

Section 8.2 introduces a brief overview of the relevant topics of general microwave propagation theory that relate to HMMICs. Section 8.3 introduces the theory required to analyze microwave propagation in actual structures, including scattering and transmission matrix definitions, as well as the extraction of microwave propagation
properties from measured waveguide structures. Section 8.4 adds a description of the specific nuances associated with finite element model analysis to this discussion.

Sections 8.5 and 8.6 provide the basic analytical theory of coplanar and microstrip waveguide propagation as well as refer to relevant, more complete, analytical treatments. Section 8.7 compares two common types of waveguide and discusses which one best suites HMMIC systems.

Sections 8.8, 8.9, and 8.10 each describe the measurement, results, and analysis of bondmetal CPW, bonded-microstrip, and un-bonded PIN diode waveguides, respectively. Each section is concluded with a discussion of the results which includes a description of what each device would add to an HMMIC system.

8.2 Basic Microwave Theory

This subsection illustrates some basic microwave theory, including an introduction to electromagnetic wave propagation and general transmission line circuit modeling. A detailed theory of microwave propagation and transmission line modeling may be found in reference 1.

8.2.1 Electromagnetic Wave Propagation

Electromagnetic (EM) waves are defined by their transverse and longitudinal electric and magnetic field components, as well as by their time dependence and their propagation constant via

\[
\vec{E}(x, y, z) = \left[ \hat{x} \cdot E_{x}(x, y) + \hat{y} \cdot E_{y}(x, y) + \hat{z} \cdot E_{z}(x, y) \right] e^{i\omega t - j\gamma z}
\]

and
where the propagation constant $\gamma$ contains real and imaginary components

$$\gamma = \alpha + j\beta$$

where $\alpha$ is the wave’s attenuation constant and $\beta$ is a value related to its propagation. In general, these waves propagate in a particular direction—defined as $\hat{z}$—with two transverse and one longitudinal field components according to Maxwell’s equations

$$\nabla \times \vec{E} = -j\omega\mu\vec{H}$$

and

$$\nabla \times \vec{H} = j\omega\varepsilon\vec{E}$$

These EM waves propagate in three varieties: transverse electric (TE), transverse magnetic (TM), and transverse electromagnetic (TEM). They are defined by their lack of a longitudinal electric field, magnetic field, and electric and magnetic fields respectively.

### 8.2.1.1 TE and TM Waves

TE and TM waves have longitudinal components and must conform to Maxwell’s equations, where the eigenvalue solutions must be non-trivial if the wave is to propagate. Therefore, these eigenvalues define the wave’s propagation and are labeled $k_c$ and described by

$$\gamma = \sqrt{k_c^2 - k^2}$$

The real component of $\gamma$ leads to wave attenuation, while the imaginary component leads to wave propagation. Gamma must maintain a positive imaginary component if the
wave is to propagate forward. This can only be done if the wavenumber \( k \) is greater than the cutoff wavenumber \( k_c \). For TE and TM waves, this cutoff wavenumber defines a cutoff frequency according to

\[
\omega_c = \frac{k_c}{\sqrt{\mu \varepsilon}}
\]

below which the wave cannot propagate. The TE and TM waves require at least one conductor to propagate, and can exist in systems with multiple conductors.

### 8.2.1.2 TEM Waves

TEM waves have only transverse field components which satisfy Laplace’s equations

\[
\nabla^2 \vec{E}_\perp = 0
\]
and

\[
\nabla^2 \vec{H}_\perp = 0
\]

This means that their electric and magnetic fields are identical to the static fields allowed to exist in a system. Therefore, TEM waves are allowed to propagate at all frequencies, including DC, and as such do not have a cutoff frequency. This also means that TEM waves can only exist where the static electric and magnetic fields are non-trivial, which requires at least two conductors.

### 8.2.2 General transmission line circuit modeling

Figure 8-1 illustrates a general distributed circuit model of a transmission line corresponding to a waveguide capable of propagating a TEM wave. \( L \) and \( C \) are the series inductance and shunt capacitance values, per unit length of the transmission line,
and \( R \) and \( G \) are the series resistance and shunt conductance per unit length. \( L \) and \( C \) represent the reactive components that allow a wave to propagate, and \( R \) and \( G \) represent the loss components that attenuate the wave.

![Figure 8-1: Equivalent circuit schematic of a general microwave transmission line.](image)

The transmission line’s voltage and current follow a set of one-dimensional equations similar to Maxwell’s, given by

\[
\frac{dV(z)}{dz} = -(R + j\omega L) I(z) \quad 8-10
\]

and

\[
\frac{dI(z)}{dz} = -(G + j\omega C) V(z) \quad 8-11
\]

The solutions to which follow as

\[
V(z) = \left[V^+ e^{-\gamma z} + V^- e^{+\gamma z}\right] e^{j\alpha z} \quad 8-12
\]

and

\[
I(z) = \left[I^+ e^{-\gamma z} + I^- e^{+\gamma z}\right] e^{j\alpha z} \quad 8-13
\]

where the terms on the left propagate in the positive \( \hat{z} \) direction and the terms on the right propagate in the negative \( \hat{z} \) direction. Their temporal components are allowed to contain separate phase offsets for each of the propagating directions. The equivalent circuit relates these two as
\[
I(z) = \frac{1}{Z_0} \left[ V^+ e^{-\gamma z} - V^- e^{+\gamma z} \right] e^{j \omega x}
\]

8-14

via a constant \( Z_0 \) called the characteristic impedance of the line which is related to the circuit parameters by

\[
Z_0 = \frac{\sqrt{R + j \omega L}}{G + j \omega C}
\]

8-15

and should not to be confused with the wave impedance \( \eta \) given by

\[
\eta = \frac{j \omega \mu}{\gamma}
\]

8-16

The propagation constant \( \gamma \) is also related to the circuit parameters and given by

\[
\gamma = \sqrt{(R + j \omega L)(G + j \omega C)}
\]

8-17

It should be noted, that in general, the characteristic impedance and propagation constant are complex. However, when the transmission line has a low loss (i.e.: the loss components \( R \) and \( G \) become small) the real component of the characteristic impedance and imaginary component of the propagation constant become dominant. In the extreme case, the loss components become negligible, and the impedance and propagation constant take on the forms

\[
Z_0 = \frac{L}{C}
\]

8-18

and

\[
\gamma = j \omega \sqrt{LC} = j \beta
\]

8-19

When the transmission line’s loss components are small, the characteristic impedance is typically approximated by Equation 8-18, while a loss term is added to the propagation
constant. It is important to note that this approximation is only valid when the transmission line’s loss components are small, otherwise the full Equations 8-15 and 8-17 are necessary.

The time average power of the forward moving wave, at position $z$, is given by

$$P_z = \frac{1}{2} \Re \left\{ V(z) I(z)^* \right\}_{\text{forward}} = \frac{V^+ e^{-\gamma_z}^2}{2Z_0} = \frac{|V^+|^2 e^{-2\alpha z}}{2Z_0}$$  \hspace{1cm} 8-20

The reactive component of the propagation constant is dropped, since only the loss component is necessary to define the power. A power loss may be defined by dividing the power found at two different locations along the line. Due to the extreme range of this loss factor, and the ease with which logarithmic quantities may be added to cascade these quantities, the logarithm of this value is used and multiplied by a factor of ten to express loss in terms of decibels (dB) as

$$\text{loss} = 10 \log \left( \frac{P_{z+L}}{P_z} \right) = 20 \log \left( \frac{V^+_{z+L} e^{-\alpha(z+L)}}{V^+_z e^{-\alpha z}} \right)$$  \hspace{1cm} 8-21

Along a uniform transmission line, the forward voltage terms $V^+_{z+L}$ and $V^+_z$ would be identical and the loss would collapse to its simple form, given by

$$\text{loss} = 20 \log \left( e^{-\alpha L} \right) \approx -8.686 \alpha L$$  \hspace{1cm} 8-22

Note that the loss is defined as negative, if the propagation loss term is positive. From here, a loss per unit length may be defined as

$$\frac{\text{loss}}{L} = -8.686 \alpha$$  \hspace{1cm} 8-23

The unit length is typically either meters or millimeters, thus, the units would be dB/m or dB/mm. Equation 8-23 could also be written without the constant term 8.686 to yield
units of nepers (Np) per unit length. From these equations, it is clear to see the
dependence of the microwave loss on the propagation loss term.

The wave moves along the transmission line with a phase velocity \( v_p \) defined as

\[
v_p = \frac{\omega}{\beta}
\]

The group velocity \( v_g \) is defined as

\[
v_g = \left( \frac{d \beta}{d \omega} \right)^{-1}
\]

The group velocity is important when investigating transient phenomena, while the phase velocity is important when investigating steady-state phenomena. This dissertation will deal with steady-state situations alone, and thus only the phase velocity will be needed. Note that these velocities are only valid for TEM waves.

From the phase velocity, a wave index \( n \) may be defined via

\[
n = \frac{v_p}{c}
\]

which describes the phase speed of the wave in comparison to the speed of light in vacuum. If the relative permeability of the structure is one, then the index may be given by

\[
n = \frac{\sqrt{\mu_r \varepsilon_0}}{\sqrt{\mu_0 \mu_r \varepsilon_r \varepsilon_0}} = \frac{1}{\sqrt{\varepsilon_r}}
\]

Note that because this expression has been derived from the group velocity above, it is only truly valid for TEM waves.
8.3 General Microwave Measurements

Microwave measurements, taken using a microwave network analyzer, are examined to extract the loss, index, and impedance of transmission lines. These characteristics fully describe the microwave’s propagation properties within the transmission lines. This subsection introduces the definitions of scattering and transmission matrices used during measurement, as well as the extraction procedure and its related theory.

8.3.1 Scattering Matrix Definition

A microwave circuit may be described using scattering parameters (S-parameters) that relate the ingoing and outgoing voltage phasors $V^+$ and $V^-$ at each port within a system via

$$V_i^- = S_{ij}V_j^+$$  \hspace{1cm} (8-28)

These are the parameters that a network analyzer measures.

Figure 8-2 illustrates a general two port system, described by a matrix of S-parameters, called an S-matrix. This S-matrix is defined as

![Figure 8-2. Block diagram of a two-port scattering matrix.](image-url)
The total voltage is defined at each port as
\[ V_i = V_i^+ + V_i^- \]

while the current going into the system at each port is defined as
\[ I_i = \frac{1}{Z_i} \left( V_i^+ - V_i^- \right) \]

### 8.3.2 Transmission Matrix Definition

It is difficult to cascade S-matrices when designing systems from multiple subsystems, instead a transmission matrix (T-matrix) is preferred for this task. In the case of two-port systems, an ABCD T-matrix may be defined. Figure 8-3 illustrates such a two port network, defined by an ABCD matrix.

Note that the current \( I_2 \) is defined as emanating from port-2, rather than impinging on the system, as with the S-matrix. This definition allows the ABCD matrix to be cascaded, using standard matrix algebra. The ABCD matrix for this system is defined as
\[
\begin{bmatrix}
V_1 \\
I_1
\end{bmatrix} =
\begin{bmatrix}
A & B \\
C & D
\end{bmatrix}
\begin{bmatrix}
V_2 \\
I_2
\end{bmatrix}
\]

![Figure 8-3. Block diagram of a two port ABCD transmission matrix.](image-url)
In this matrix notation, it is trivial to show that the inverse matrix $T^{-1}$ essentially equates to a rearrangement of the port designations, and therefore describes the system in reverse. This inverse matrix $T^{-1}$ is defined as

$$T^{-1} = \begin{bmatrix} A & B \\ C & D \end{bmatrix}^{-1} = \begin{bmatrix} A & -B \\ -C & D \end{bmatrix}$$

8-33

If the exterior systems connected to the ABCD matrix were identical, and their impedance $Z_o$ known, then the transmission matrix may be written in terms of the S-matrix as

$$T = \begin{bmatrix} A & B \\ C & D \end{bmatrix} = \begin{bmatrix} \frac{(1+S_{11})(1-S_{22}) + S_{12}S_{21}}{2S_{21}} & \frac{Z_o(1+S_{11})(1+S_{22}) - S_{12}S_{21}}{2S_{21}} \\ \frac{1}{Z_o}(1-S_{11})(1-S_{22}) - S_{12}S_{21} & \frac{(1-S_{11})(1+S_{22}) + S_{12}S_{21}}{2S_{21}} \end{bmatrix}$$

8-34

8.3.3 Measurement Procedure Overview

Measurement procedure details are provided in Appendix C.3; however, the general procedure is described below.

First, at least two devices of different length, uniform construction, and identical cross section are fabricated and prepared for measurement.

Then, a full 2-port calibration of the network analyzer is performed, being sure the microwave probes are properly seated, to yield identical characteristics.

Next, both the amplitude and phase of all of the S-parameters, for both the short (not to be confused with the microwave term ‘short’) and long device, are measured and recorded as data files. [A labview program written by a former student (GuoLiang Li) was used during this investigation.]
Finally, the microwave extraction program is run to automatically extract the transmission line’s propagation constant, index, and impedance from the S-parameter data files. The extraction program’s source code is provided in Appendix E.2.

### 8.3.4 Extraction Theory

Figure 8-4 depicts the two lengths of measured waveguide in terms of two pad-containing transmission matrices, $P_1$ and $P_2$, as well as an embedded waveguide-only transmission matrix $T_w$. The pad-containing transmission matrices are identical, except $P_2$ is the reverse of $P_1$.

![Illustration of waveguide](image)

Figure 8-4. Illustrations and equivalent block diagrams of two lengths of measured waveguide: (a) short waveguide and (b) long waveguide.
The short transmission line may be described by

$$T_S = P_1 P_2$$  \hspace{1cm} 8-35

while the long transmission line may be described by

$$T_L = P_1 T_W P_2$$  \hspace{1cm} 8-36

Both of which may be determined from the measured S-parameter data using Equation 8-34. Looking at the systems in the reverse direction, yields

$$T_S^{-1} = P_2^{-1} P_1^{-1}$$  \hspace{1cm} 8-37

and

$$T_L^{-1} = P_2^{-1} T_W^{-1} P_1^{-1}$$  \hspace{1cm} 8-38

where the ABCD T-matrix of a general lossy waveguide of length $L$ is given by

$$T_W = \begin{bmatrix}
\cosh \gamma L & Z_w \sinh \gamma L \\
\frac{1}{Z_w} \sinh \gamma L & \cosh \gamma L
\end{bmatrix}$$  \hspace{1cm} 8-39

The inverse of which would be

$$T_W^{-1} = \begin{bmatrix}
\cosh \gamma L & -Z_w \sinh \gamma L \\
-\frac{1}{Z_w} \sinh \gamma L & \cosh \gamma L
\end{bmatrix}$$  \hspace{1cm} 8-40

Adding these two matrices together yields

$$T_W + T_W^{-1} = \begin{bmatrix}
2 \cosh \gamma L & 0 \\
0 & 2 \cosh \gamma L
\end{bmatrix}$$  \hspace{1cm} 8-41

while subtracting them yields

$$T_W - T_W^{-1} = \begin{bmatrix}
0 & 2Z_w \sinh \gamma L \\
\frac{2}{Z_w} \sinh \gamma L & 0
\end{bmatrix}$$  \hspace{1cm} 8-42

Thus
\[ T_w + T_w^{-1} \bigg|_{11,22} = 2 \cosh \gamma L \]  
8-43

while

\[ T_w - T_w^{-1} \bigg|_{12} = 2Z_w \sinh \gamma L \]  
8-44

and

\[ T_w - T_w^{-1} \bigg|_{21} = \frac{2}{Z_w} \sinh \gamma L \]  
8-45

Both of which may be determined using the measured transmission matrices \( T_S \) and \( T_L \) via

\[
T_w + T_w^{-1} = P_1 P_1^{-1} \left[ T_w + T_w^{-1} \right] \cdot P_2 P_2^{-1} \\
= P_1 T_w P_2 \cdot P_2^{-1} P_1^{-1} + P_2^{-1} T_w^{-1} P_1^{-1} \cdot P_1 P_2 \\
= T_L T_S^{-1} + T_L^{-1} T_S \\
\]
8-46

and

\[
T_w - T_w^{-1} = P_1 P_1^{-1} \left[ T_w - T_w^{-1} \right] \cdot P_2 P_2^{-1} \\
= P_1 T_w P_2 \cdot P_2^{-1} P_1^{-1} - P_2^{-1} T_w^{-1} P_1^{-1} \cdot P_1 P_2 \\
= T_L T_S^{-1} - T_L^{-1} T_S \\
\]
8-47

Therefore, knowing \( L, \gamma \) may be found via

\[
\gamma = \frac{1}{L} \cosh^{-1} \left( \frac{1}{2} \left[ T_L T_S^{-1} + T_L^{-1} T_S \right] \right) \\
\]
8-48

Similarly, knowing \( L \) and \( \gamma, Z_w \) may be found via

\[
Z_w = \frac{\left[ T_L T_S^{-1} - T_L^{-1} T_S \right]_{12}}{2 \sinh \gamma L} \\
\]
8-49
It is important to note that this procedure may be used to extract the transmission characteristics from any uniform, reciprocal waveguide. However, it only works if the network analyzer ports are symmetric, have a known impedance $Z_o$, and have been correctly calibrated all the way down to the microwave probe tips.

The results of this extraction depend on the fact that the microwave has traveled along the waveguide without incident. Radiation losses are indistinguishable from other forms of loss in this measurement and must be negligible if the measurement is to accurately portray the real situation. Also, at very low frequencies, the microwave structure may be only a small fraction of a wavelength. In this situation, the accuracy of the measurement is compromised due to its assumption that the wave is propagating along the transmission line. Therefore, the measurement suffers a lower accuracy at these frequencies. If the waveguide loss is high, then the signal received at the end of the waveguide will be small. Inaccuracies in the measurement of this small signal also lead to extracted result error.

8.4 Finite Element Analysis

Full, three dimensional field solvers that break models up into finite elements, such as ANSOFT’s HFSS and COMSOL’s Multiphysics, can provide the most accurate field descriptions within a structure. The descriptions of these systems are quite lengthy and cannot be explored here. The basic idea stems from a similar argument, used earlier, to describe the thermal resistance of a system. Essentially, the model is broken up into very small domains, where the fields in each are calculated and matched at their boundaries. This matrix of domains is analyzed from different perspectives (ports) to
yield the system’s overall characteristics. Their only draw back is that they do not
directly build an intuitive feel for how model variables affect the system’s properties.
The relationships must be found by incrementally changing one model variable at a time
while tracking trends in the solutions. This process can be very tedious and time
consuming, but necessary if accurate results are to be obtained.

An important note should be made about determining the finite element model’s
(FEM) characteristic impedance, which in general, may be defined in a few ways. To
illustrate this, two different cases are discussed: an ideal lossless situation and a more
realistic lossy situation.

### 8.4.1 Ideal Lossless Situation

Figure 8-5 illustrates a cross section of a general two-wire waveguide, consisting
only of perfectly conducting conductors and perfectly insulating dielectrics. Such
structure supports a lossless quasi-TEM microwave. Note that the electric and magnetic
fields do not penetrate the perfect conductors.

![Figure 8-5](image.png)

Figure 8-5. Illustrations of a general ideal lossless two-wire waveguide cross section showing (a) the
electric field and (b) the magnetic field, both with integration paths.
Its characteristic impedance may be measured as a function of the microwave voltage and current exchanged between the two conductors given by

\[ Z_{\text{c}, \text{ij}} = \frac{V}{I} \]  

8-50

This voltage and current stem from the electric and magnetic fields between the two conductors. The voltage may be obtained by integrating the electric field along a path from one conductor to the other, via

\[ V = \int_{\text{II}} \vec{E} \cdot d\vec{l} \]  

8-51

as depicted in Figure 8-5. The current may be obtained by integrating the magnetic field, along a closed path, encompassing one of the conductors via

\[ I = \oint_{\text{I or II}} \vec{H} \cdot d\vec{l} \]  

8-52

also depicted in Figure 8-5. The voltage between the conductors, and the current flowing through them, is well defined, thus the resulting impedance characterizes the system adequately.

### 8.4.2 Realistic Lossy Situation

Figure 8-6 illustrates the same structure, except here, the imperfect conductors have an associated resistance and the imperfect dielectric has an associated conductance. Note that the fields are allowed to penetrate the conductors due to their resistive nature.
Figure 8-6. Illustrations of a general ideal lossy two-wire waveguide cross section showing (a) the electric field (with voltage integration path) and (b) the magnetic field (with power flux integration).

A voltage may be defined by Equation 8-51 between the two electric field vertices defined by the highest and lowest electric potential regions within the conductors, rather than their boundaries. However, the current definition of Equation 8-52 is somewhat hard to define as the dielectric that separates the ‘conductors’ is also able to conduct current and must also be considered a conductor. Therefore, a path that fully encircles just one conductor cannot be rigidly defined.

There is, however, a way around this issue involving the wave’s power, defined as

\[
P = \frac{1}{2} \int_{S} \vec{E} \times \vec{H} \cdot d\vec{s}
\]

where the surface of integration is the entire waveguide cross section (including the ‘conductors’). When this power is expressed in terms of voltage and current:

\[
P = \frac{1}{2} VI
\]

The characteristic impedance may be defined as

\[
Z_{o}\bigg|_{PV} = \frac{V^2}{2P}
\]
therefore, avoiding the difficulty associated with defining the current based on a magnetic field loop.

8.5 Coplanar Waveguide Theory

Coplanar waveguide (CPW) microwave structures were used to test the microwave propagation characteristics of un-bonded bondmetal. These structures were not the same as the bonded microwave devices, but were capable of determining if microwaves could propagate using the bondmetal, without having to endure the intense fabrication required to achieve bonded microwave structures. It was also possible to verify the link between bondmetal conductivity and microwave propagation behavior, using these preliminary CPW test structures.

The theoretical analysis of CPW microwave lines is directly applicable to HMMIC passive circuits as well as these preliminary bondmetal characterization microwave measurements.

8.5.1 CPW Definition

Coplanar waveguides consist of three coplanar conducting strips on an insulating material, as illustrated in Figure 8-7. During operation, the electric and magnetic fields between these strips propagate a microwave signal. The inner conductor is called the signal line and the outer conductors are called ground lines – this convention is by tradition only, as the microwaves make no distinction between the conductors.
8.5.2 CPW Supported Waves

If the CPW ground lines are electrically common, then the structure may be thought of as a two-wire system. Such two-wire systems can support TE, TM, and TEM waves as previously discussed. The environment around the wires is not uniform, and the dielectric underneath the wires generally has a higher permittivity than the surrounding medium (typically air). The phase velocity of a TEM wave in the air would be different from its phase velocity in the dielectric. A single TEM wave cannot support such a condition, and strictly speaking the CPW does not propagate a pure TEM wave, but rather, a hybrid TE-TM wave.

In general, the conductors involved are not perfect, and their resistance allows longitudinal electric and magnetic field components to exist within the wires. Also, the conductors are on a dielectric, which generally has a finite resistance, where longitudinal electric and magnetic fields may also exist. The effects of the hybrid TE-TM wave, and its attenuation due to conductor and dielectric losses, can usually be approximated as a quasi-TEM wave that behaves similar to a pure-TEM wave but with loss.
8.5.3 CPW Quasi-TEM Theoretical Analysis

A detailed analysis of CPW propagation may be found in reference 2; however, only a basic introduction will be given in this section. Since the transverse field components in the quasi-TEM are dominant, and behave as they would in a static system, the analysis is vastly simplified by estimating behavior based on electrostatic analysis. The frequency dependence of the structure may be reflected in a static framework to extend the analysis to all frequency.

If the quasi-TEM mode is assumed to approximate a pure-TEM mode, then the CPW may be thought of as existing in a uniform dielectric, described by an effective dielectric constant. The effective dielectric constant may be derived by essentially spatially averaging the electric field lines in both materials. Since the fields in these regions exist in parallel to the propagating wave, the system’s capacitance may be modeled as a sum of parallel capacitances in each of the regions. This effective system capacitance yields the effective dielectric constant.

Assuming a non-magnetic dielectric, the magnetic fields experience a uniform permeability throughout the entire structure. If the electric fields experience an effectively uniform environment, and the magnetic fields experience a truly uniform environment, and they are both dictated by the same conductors, then they will be related by a single constant that replaces the effective dielectric constant with the permeability of freespace. In this way, the electric and magnetic fields may be derived from a single solution to Laplace’s equation. This is the same argument discussed in the thermal analysis chapter, relating electrical conductivity and electrostatics solutions to thermal conductivity.
A set of CPW conductors lying on an infinite dielectric has half of its electric field contained within the air, and half contained within the dielectric. Therefore, the effective dielectric constant may be approximated by

$$\varepsilon_{r_{\text{eff}}} = \frac{\varepsilon_{r_{\text{dielectric}}} + 1}{2}$$ \hspace{1cm} 8-56

The overall capacitance of the CPW is given by

$$C = 4\varepsilon_0\varepsilon_{r_{\text{eff}}} \frac{K(k)}{K(k')}$$ \hspace{1cm} 8-57

where the right most terms represent the distribution of the electric fields amongst the two regions and are a ratio of the complete elliptic integrals of modulus $k$ and $k'$. These elliptic integrals stem from an electrostatic conformal mapping analysis technique. Modulus $k$ and $k'$ are dictated by the conductor spacing via

$$k = \frac{S}{S + 2W}$$ \hspace{1cm} 8-58

and

$$k' = \sqrt{1 - k^2}$$ \hspace{1cm} 8-59

where $S$ is the width of the center conductor and $W$ is the gap spacing between the conductors, as shown in Figure 8-7. The ratio of the complete elliptic integrals may be approximated using

$$\frac{K(k)}{K(k')} = -\pi \left\{ \ln \left[ \left( \frac{m_1}{16} \right)^2 + 8 \left( \frac{m_1}{16} \right)^4 + 992 \left( \frac{m_1}{16} \right)^8 + \cdots \right] \right\}^{-1} \text{ for } 0 < k \leq 1/\sqrt{2} \hspace{1cm} 8-60$$

and

$$\frac{K(k)}{K(k')} = -\pi \left\{ \ln \left[ \left( \frac{m_1}{16} \right)^2 + 8 \left( \frac{m_1}{16} \right)^4 + 992 \left( \frac{m_1}{16} \right)^8 + \cdots \right] \right\}^{-1} \text{ for } 1/\sqrt{2} \leq k < 1 \hspace{1cm} 8-61$$
where \( m \) and \( m_i \) are related to modulus \( k \) by

\[
m = k^2
\]

8-62

and

\[
m_i = 1 - k^2
\]

8-63

The inductance may then be written as

\[
L = \mu_0 \varepsilon_0 \frac{\varepsilon_{r_{\text{eff}}}}{C}
\]

8-64

If an effective relative dielectric loss constant could be determined, then the dielectric loss term could be represented in terms of \( C \) via

\[
G = \varepsilon_{r_{\text{eff}}}^\prime \frac{1}{C}
\]

8-65

although more direct approaches are typically used.

Crude approximations for the series resistance \( R \) may be obtained by calculating the resistance per unit length of the conductors, using the Wheeler incremental inductance rule. The Wheeler approximation is only valid when the conductor thickness is much greater than its skin depth, given by

\[
\delta_s = \sqrt{\frac{2}{\omega \mu \sigma}} \approx 5.03 \times 10^{-3} \sqrt{\frac{1}{\sigma}}
\]

8-66

where the latter approximation yields the skin depth in units of meters. This condition is typically met with large transmission line structures; however, the size of conductors in HMMICs would typically warrant a more involved full wave analysis.

Thus far, the conformal mapping has been described for infinitely thin conductors. When conductors with non-negligible thickness are involved, the solutions become unwieldy and the loss and characteristic impedance may be approximated
analytically. These equations are too lengthy to present here, and the reader is directed to
the references for clarification.

8.6 Microstrip Waveguide Theory

Microstrip structures are used in most traditional MMIC designs and an
introduction to HMMIC design would not be complete without their discussion. Microstrip structures operate differently from CPWs and their basic analysis must be
understood to effectively compare both. The ITS metalbonding technique allows for
bonded-microstrip structures, which could be important HMMIC elements. Understanding their basic behavior would aid integrated system design.

8.6.1 Microstrip Definition

Microstrip waveguides consist of two parallel conducting strips separated by an
insulating material as illustrated in Figure 8-8. During operation, the electric and
magnetic fields between these lines propagate a microwave signal. The upper conductor
is called the signal line, and the lower conductor is called the ground line. Just as with
the CPW case, this naming convention is by tradition, as the microwaves make no
distinction between the two.
8.6.2 Microstrip Supported Waves

Similar to the CPW structure, the microstrip structure has two conductors with fields that pass through both air and dielectric, thus supporting a quasi-TEM mode, as well as TE and TM modes. The cutoff frequencies for these TE and TM modes depend on the dielectric permittivity and the size of the microstrip. If the microstrip’s signal line is wide, and the dielectric thick enough in comparison to the wavelength, then the TE and TM modes will begin to propagate. For standard MMIC substrate microstrip waveguides, this could occur at 200-400GHz, for a bonded-microstrip, this wouldn’t occur until the frequency reached a few 10’s of THz or higher, at which point other effects would likely dominate. The following discussion will focus only on quasi-TEM modes.

8.6.3 Microstrip Quasi-TEM Theoretical Analysis

This subsection describes several analytical models of microstrip structures from the most crude to the most practical.
8.6.3.1 Crude Lossless Model

The most rudimentary model that may be applied to a microstrip structure is that of a parallel plate estimation. The permittivity that the wave sees is shown to be equal to the dielectric’s permittivity $\varepsilon_r$ directly; however, it is more likely to be between this value and one.

The reactive circuit elements are given by

$$L = \frac{\mu_r h}{w}$$  \hspace{1cm} 8-67

and

$$C = \frac{\varepsilon_r w}{h}$$  \hspace{1cm} 8-68

for a parallel plate of width $w$ and height $h$ as shown in Figure 8-8.

8.6.4 Analytical Estimations

The fields; however, penetrate both the surrounding air, as well as the dielectric. Just as with the CPW design, an effective dielectric constant may be determined by solving for the capacitance. Pozar$^1$ determined the capacitance to be

$$C = \left[ \sum_{n=1, \text{odd}}^{\infty} \frac{4a \sin(n\pi w/2a) \sinh(n\pi h/a)}{(n\pi)^2 w \varepsilon_o \left( \sinh(n\pi h/a) + \varepsilon_r \cosh(n\pi h/a) \right)} \right]^{-1}$$  \hspace{1cm} 8-69

by giving the microstrip arbitrary conducting walls at

$$x = \pm \frac{a}{2} \gg h$$  \hspace{1cm} 8-70

Therefore, the effective relative dielectric constant may be defined as
Once the capacitance is known, and the effective permittivity is known, then the inductance $L$, conductance $G$, and impedance $Z_o$ may be found using the same arguments used when describing the CPW structure. It should be noted that this method requires series summation, which is not very intuitive and whose convergence is slow for large $a$.

Wheeler\textsuperscript{7} analyzed the microstrip structure using conformal mapping techniques, similar to those used to analyze the CPW structure. However, by making several approximations of the structure during his analysis, he was able to create a simpler analytical approximation that did not require elliptic integrals. Reference 8 presented Wheeler’s analytical formulas for effective relative dielectric constant and characteristic impedance, as well as treatments by other authors. All of these equations are quite lengthy and are beyond the scope of this dissertation.

Reference 1 presented Bahl and Trivedi’s\textsuperscript{9} and Gupta, et al.’s\textsuperscript{10} approximations of the effective relative dielectric constant as

$$\varepsilon_{r_{\text{eff}}} = \frac{\varepsilon_r + 1}{2} + \frac{\varepsilon_r - 1}{2} \frac{1}{\sqrt{1+12h/w}} \tag{8-72}$$

and characteristic impedance as

$$Z = \begin{cases} \frac{60}{\sqrt{\varepsilon_{r_{\text{eff}}}}} \ln \left( \frac{8h}{w} + \frac{w}{4h} \right) & \text{for } w/h \leq 1 \\ \frac{120\pi}{\sqrt{\varepsilon_{r_{\text{eff}}}}} \left[ w/h + 1.393 + 0.667 \ln \left( w/h + 1.444 \right) \right] & \text{for } w/h \geq 1 \end{cases} \tag{8-73}$$
These equations are much easier to deal with, and are accurate over most practical width to height ratios. Corrections have been made that include conductor thickness variation. However, the deviation is rather small when the thickness to width ratio is small and the substrate dielectric constant is high.

8.7 CPW versus Microstrip Comparison

Since both CPW and microstrip transmission lines are common in MMIC, it is important to note how they compare in terms of design flexibility, loss, and breakdown. The advent of bonded-microstrip transmission lines provides higher circuit design flexibility, with the ability to switch freely between the two to improve the performance of HMMIC devices and architecture.

8.7.1 Design Freedom

Microstrip structures, being the first to be implemented, pervaded MMIC design for so long because of how well understood their characteristics were and the great diversity of passive components that were available. However, CPW structures now have an equally impressive list of passive components with characteristics that are just as well understood. System designers need no longer be restricted to microstrip designs because of CPW device diversity and analysis limitations.

8.7.2 Ground Vias

Microstrip circuits have their ground on the underside of the substrate. When microwave devices require access to this ground, large substrate vias must be created, adding fabrication cost and complexity. A typical circuit may require one or more vias.
per microwave device, which is wasteful of the precious real estate. Also these vias must be included during analysis, as they produce parasitic reactances, adding to design cost.

CPW circuits do not require ground vias, as the ground is coplanar and readily available at the top surface for microwave devices.

### 8.7.3 Cross-Talk

Microstrip circuits are plagued by cross-talk, just as CPW circuits are; however, it is easier for microstrip fields to couple, due to their large substrate interaction, while CPW fields terminate in coplanar grounds. In order to minimize cross-talk, microstrip circuitry must be spread out to weaken the field coupling, while CPW circuitry may be densely packed without difficulty, due to the coplanar ground lines that already exist between structures. This results in more efficient use of substrate real estate and leads to smaller system designs.

### 8.7.4 Impedance

CPW structures are more flexible than microstrip in terms of impedance design. CPW impedance is governed by coplanar conductor width and separation, whereas microstrip’s is dictated by substrate thickness and signal line width. In order to maintain a fixed impedance, as circuits become smaller, CPW conductor widths and separations may be altered without having to change the substrate thickness. This allows circuits to shrink without having to deal with thinner, more delicate substrates as microstrip must. It also provides more flexibility in circuit design to allow multiple impedances to be included in a single design, without having to create large signal line width variations.
8.7.5 Loss

The size reduction of CPW structures does; however, increase conductor loss, but it should be noted that for standard MMIC substrate thicknesses the conductor losses from equivalently sized microstrip lines are about the same as those of CPWs. Increasing the conductor thicknesses for either CPW or microstrip can provide lower loss, although this is more apparent when the thickness is below approximately three times the skin depth. On the other hand, this means that CPW transmission lines may be made larger to provide lower loss to subsystems that require it, without having to deal with the different impedance that would accompany an equivalent change in microstrip width.

The dielectric losses from CPW are comparable to microstrip for similar widths on the same substrate material and therefore do not require special treatment.

8.7.6 Power Handling

Waveguide power handling capability is dependent on the loss in the structure as well as any effects associated with heat removal; however, the ultimate limit for any structure depends on where its highest electric field is and what the breakdown field is in that location. CPW structures are limited by surface leakage, as the highest electric fields exist between the coplanar signal and ground conductors. Microstrip structures are typically limited by bulk leakage, as the highest electric fields exist underneath the signal conductor. Generally, surface leakage paths tend to breakdown before bulk paths, therefore, microstrip designs would be better at withstanding higher electric fields. However, this general rule does not directly apply to bonded-microstrip designs, which may be surface leakage dominant if narrow bond mesa structures were used. If these
bonded mesas were made wide enough, and thick enough, then the bonded-microstrip design could withstand higher electric fields than CPW structures.

The highest ultimate power handling would come from high bandgap bonded materials as the breakdown field increases with bandgap. This assumes that the semiconductor material has a low defect density – something that the ITS metalbonding process can provide.

8.8 Preliminary Bondmetal Microwave Propagation Investigation

Preliminary tests were performed to determine if the bondmetal could support microwave propagation, and to test the extraction ability of the measurement process outlined earlier. In order to accurately predict microwave behavior, the electrical characteristics of the test structures must be known. The substrate was chosen to be semi-insulating GaAs which provided a very low dielectric loss platform on which to isolate the microwave properties of the bondmetal. With the structures so highly dependent on metal behavior, the link between DC electrical resistivity and microwave loss could be made clear.

These tests were performed on un-bonded samples, in an attempt to simplify microwave analysis. Figure 8-9 shows a top view microscope image and a close-up SEM cross sectional image of one of the tested devices. Bondmetal test structures were compared alongside gold test structures, and calibration substrate structures, to help verify the microwave model analysis.
Figure 8-9. Microscope image (a) of a bondmetal coplanar waveguide test structure and SEM image (b) of a close up of the \( \text{LN}_2 \) as-evaporated center conductor cross section.

8.8.1 Measurement Procedure Overview

*Microwave measurement:*

Microwave measurements were performed first, using the standard method outlined in the general measurement section above.

*DC resistivity measurement:*

The bondmetal and gold test structures were measured at DC to evaluate their electrical resistivities. These were done using four terminal Kelvin measurements similar to those used to measure the heater resistances during the thermal measurements. These tests were performed after the microwave measurements were finished, as they left marks that could have affected the microwave measurements.

*Anneal:*

The structures were then annealed to evaluate the DC and microwave electrical changes caused by annealing.

*Microwave measurement of untested structures:*
After the anneal, microwave measurements of separate, untested structures were performed, to avoid any discrepancies due to the probe marks caused during the first series of DC resistivity measurements.

**DC resistivity measurement of untested structures:**

This was followed by DC resistivity measurements of the post-anneal microwave measured test structures as previously.

### 8.8.2 Results and Analysis

Figure 8-10 shows one set of measured data, including the S-parameters and extracted transmission line characteristics, of one of the CPW test structures. Since the portion in the middle of the measured frequency band (10 GHz – 30 GHz) trivially links the lower frequency (0.5 GHz – 10 GHz) to higher frequency regions (30 GHz – 38 GHz), this portion was omitted from the measurement. The dashed line shown connecting the two regions does not represent data and is there solely to serve as a visual aid. The high frequency portion was measured in an attempt to realize a higher loss resolution (as the loss is higher at higher frequency) even though this region was prone to a bit more error due to calibration difficulties.
Analysis was performed at high frequency to illustrate the modeling capability and establish the link between DC resistivity and microwave loss. Table 8-1 lists the measured DC resistivity while Table 8-2 lists the measured microwave loss for both pre-annealed and post-annealed cases of both LN$_2$ and room temperature deposited bondmetal structures at 40GHz – as well as those of the gold test structure and the calibration substrate – alongside the finite element modeled loss. The losses shown in Table 8-2 result from FEM modeling at 40 GHz assuming the same conductivities as those measured in the DC experiment.
Table 8-1. List of measured DC resistivity for the bondmetal and gold CPW test structures both before and after annealing.

<table>
<thead>
<tr>
<th>sample</th>
<th>pre-anneal resistivity (Ω·m)</th>
<th>post-anneal resistivity (Ω·m)</th>
</tr>
</thead>
<tbody>
<tr>
<td>LN$_2$ bond alloy</td>
<td>$1.32 \times 10^{-7}$</td>
<td>$1.81 \times 10^{-7}$</td>
</tr>
<tr>
<td>un-cooled bond alloy</td>
<td>$4.49 \times 10^{-7}$</td>
<td>$2.87 \times 10^{-7}$</td>
</tr>
<tr>
<td>Au</td>
<td>$2.91 \times 10^{-8}$</td>
<td>-</td>
</tr>
</tbody>
</table>

Table 8-2. List of measured microwave loss and FEM loss for the bondmetal, gold, and calibration substrate CPW test structures at 40GHz both before and after annealing.

<table>
<thead>
<tr>
<th>sample</th>
<th>pre-anneal measured loss (dB/mm)</th>
<th>pre-anneal FEM loss (dB/mm)</th>
<th>post-anneal measured loss (dB/mm)</th>
<th>post-anneal FEM loss (dB/mm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>LN$_2$ bond alloy</td>
<td>$2.62 \pm 0.13$</td>
<td>$1.97$</td>
<td>$2.95 \pm 0.11$</td>
<td>$2.55$</td>
</tr>
<tr>
<td>un-cooled bond alloy</td>
<td>$5.57 \pm 0.05$</td>
<td>$5.41$</td>
<td>$3.85 \pm 0.09$</td>
<td>$3.70$</td>
</tr>
<tr>
<td>Au</td>
<td>$1.34 \pm 0.28$</td>
<td>$1.06$</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>calibration substrate</td>
<td>$0.16 \pm 0.37$</td>
<td>(0)</td>
<td>-</td>
<td>-</td>
</tr>
</tbody>
</table>

8.8.3 Discussion of Results

Analytical calculations based on equations from reference 5 that account for conductor loss matched the finite element analysis results for all of the structures fairly closely – only the FEM results are shown for brevity. The analytical and FEM analysis of the microwave index and impedance matched the measured results within just a few percent. These quantities are less affected by metal loss and are omitted from Table 8-2 as they are ancillary to the DC-resistivity/microwave-loss comparison. The measured loss error is due to the noise of the microwave measurements – low losses are particularly difficult to resolve for these sub-millimeter length waveguides. Note that the measured loss is generally higher than the expected loss based on the DC resistivity data. This may be due to the metal surface roughness and radiation losses.
The calibration substrate’s transmission line is quoted as having zero loss, but this is not strictly true and was expected to have a low loss. The DC resistivity measurements left marks in measured transmission lines, so the calibration substrate was spared this treatment. As a result, these structures were assumed lossless, thus the modeled loss shown in Table 8-2 for these structures is depicted as zero in parentheses.

Figure 8-11 shows the surface texture of the LN$_2$ and room temperature bondmetal structures both before, and after, annealing. The bumpy texture of the room temperature bondmetal relaxed slightly during the anneal, as the indium droplets alloyed a bit with the palladium layer in between. The wide area texture shown in the annealed LN$_2$ structure was caused by water vapor that was trapped between the palladium and indium layers during deposition. These structures were fabricated before the water vapor removing process step had been implemented in the procedure, and is part of the reason why it was later created. The SEM images of Figure 5-3 (in the ITS implementation chapter) shows more clearly the effects of deposition temperature on bondmetal texture prior to annealing.
The pre and post-anneal room temperature bondmetal structures were very bumpy and average thicknesses and resistivities had to be used in the model estimates. This average thickness was based on the evaporator’s crystal monitor thickness values for each layer. The modeled impedance characteristics for the various structures matched the measured results less accurately for the more bumpy structures, although overall the match was fairly accurate.
The models used the measured DC resistivity during their calculation and matched fairly well with the measurement results showing that the conductor resistivity could be successfully accounted for.

Note that after annealing, the alloy resistivity increased for the LN\textsubscript{2} structures and decreased for the room temperature structures. As the room temperature structures alloyed, their roughness decreased while the LN\textsubscript{2} samples’ roughness increased. The texture effects for the room temperature structures offset the increase in resistivity due to alloying. As shown in Figure 7-8 (in the thermal conductivity characterization chapter), the electrical resistivity of the bond alloy is expected to increase as the structure is annealed. The large change in resistivity was not entirely seen in these structures and was attributed to incomplete alloying.

The LN\textsubscript{2} metallization procedure did not remove water vapor for these test structures, as the importance of such process steps were not known at the time. The alloy kinetics were also not well understood at the time and the anneal was presumed long enough, and high enough, to completely alloy the bondmetal. These structures were; however, not fully alloyed due to diffusion barrier effects caused by trapped water vapor and insufficient anneal temperature and duration.

Overall, the CPW measurements showed that accurate microwave measurement and extraction could be performed, and that the bondmetal could propagate microwaves. It is important to note that these results show that bondmetal is not the best choice of conductor wherever low loss CPW metallizations are required. Higher conductivity metals such as copper or gold should be used in those situations. With the knowledge gained from these measurements, bonded devices could be investigated with confidence.
8.9 Bonded Device Microwave Propagation Investigation

It is essential to understand how bonded structures operate at microwave frequencies, if the investigation of HMMIC systems is to be complete. Bonded-microstrip transmission lines were investigated to illustrate that microwaves could propagate in such structures.

For convenience, the bonded thermal conductivity test structures were used to test the microwave propagation characteristics. The nickel heaters of the thermal tests were used as signal lines, and the palladium coated field silicon and bondmetal formed the ground. Since these structures were used directly for microwave measurements without modification, the microwave structures were not optimized for peak performance.

8.9.1 Measurement

Microwave measurements followed the standard method outlined in the general measurement section above. The only difficulty was finding matched microwave probes, with sufficient signal to ground spacing and vertical compliance, to measure the bonded mesa structures.

8.9.2 Results and Analysis

The modeled results are shown along with the measured values in Figure 8-12. The high loss of these structures did not require measurement beyond about 20GHz. As shown, the loss becomes quite high at higher frequencies and starts to affect the extracted results. Since the extraction process requires knowledge of transmitted microwave signals, if these signals are small due to high loss and low input power, then the extracted results are prone to error.
The non-negligible conductivity of the ground (bond metal) conductor and unusual mesa structure did not allow for accurate analytical calculations and analysis was deferred to finite element modeling. Only half the structure was modeled to improve analysis speed, as shown in Figure 8-13, using COMSOL. Symmetric analysis was accomplished by using a perfect magnetic conductor boundary condition to mirror the half structure.
The modeling environment was capable of including the longitudinal field components using a two dimensional perpendicular modal analysis. Therefore, computationally intensive three dimensional models were not required. The integration of the electric field between the conductor potential maxima could yield the voltage directly, as described earlier; however, integrating the half-structure’s cross sectional power yielded only half of the total power in the structure, thus Equation 8-55 was modified to include this half-structure power as

$$Z_o = \frac{V^2}{4P_{\text{model}}}$$  

8.9.3 Discussion of Results

The nickel conductivity was calculated based on the measurements from the thermal conductivity tests, while the palladium conductivity was known from previous measurements. The bondmetal electrical conductivity was based on the thermal
conductivity results using the Wiedemann-Franz law, as there was no direct way of measuring the bond alloy electrical resistivity after the structures had been bonded. The silicon substrate and unintentionally doped GaAs epilayer conductivities were measured via Van der Pauw resistivity measurements.

The width of the signal line and bonded epilayer thickness were never specifically designed for any particular characteristic impedance, as the structure’s first use was to measure the bond interface thermal conductivity and no attempt was made to provide a low loss, high frequency, high power, 50ohm bonded-microstrip transmission line. However, even though the tested structures were designed primarily to test thermal conductivity, this measurement shows that it was still capable of propagating a microwave signal.

The nickel signal conductor and mixed bondmetal/palladium ground resistances resulted in high conductor losses, and because nickel is a magnetic material, it has a high permeability, thus increasing its conductor loss further. The unintentionally doped GaAs epilayer conductivity was also rather high, and lead to additional dielectric losses. Future designers are expected to take these considerations into account to yield higher efficiency transmission lines.

It should be noted that the simulations never included any loss due to radiation, which could account for some of the loss discrepancy seen in Figure 8-12 at higher frequencies.
8.9.3.1 Ideal Bonded-microstrip Structure Simulations

The FEM simulation matched the measured bonded-microstrip waveguide microwave propagation characteristics fairly well. In order to illustrate how the microwave propagation may be improved with proper design, the same basic structure was simulated with more ideal materials. The simulated electric and magnetic fields are shown in Figure 8-14, which also depicts various design improvements. The high resistance nickel signal line of the measured structure has been replaced with a more conductive, 5 micrometer thick by 3 micrometer wide gold metallization. The poor background doped, roughly 2 micrometer tall GaAs epilayer has been replaced by a more insulating GaAs mesa which is 3 micrometer tall by 10 micrometer wide. These new dimensions improve the impedance, bringing it closer to 50ohms. The bondmetal was kept the same thickness and conductivity, as reducing the thickness would only serve to increase the loss and it is difficult to predict an accurate value for a future higher conductivity bond alloy. The doped silicon substrate from the measured structure has been replaced with a minimum high-resistivity silicon resistivity of 10kohm-cm. Finally, a 1 micrometer thick gold metallization has been added on top of the existing palladium field metal to provide higher conductivity ground lines.
Figure 8-15 plots the simulated microwave characteristics of this ideal bonded-microstrip test structure versus frequency. The loss is significantly lower at only about 0.56 dB/mm versus the test structure’s simulated loss of 15.93 dB/mm at 15 GHz and the phase velocity is much higher with an index of 2.91 as compared to the test structure’s simulated index of 8.46 at 15 GHz. Also, the impedance is significantly less reactive (less imaginary) and closer to 50ohms showing a simulated result of 41.3+6.0i ohms as compared to the tested bonded-microstrip structure’s simulated result of 31.8-11.9i ohms at 15 GHz. An impedance of 50ohms could have been obtained by either increasing the bonded GaAs thickness or reducing the gold signal line width; however, a 3 micrometers thick GaAs epilayer is already fairly thick, and reducing the signal line width is less practical and would increase loss. These results illustrate how an ideal version of the bonded-microstrip structure can compactly propagate microwaves with a favorable loss, index, and impedance.
8.10 P-I-N Semiconductor Device Microwave Propagation Investigation

This section discusses the microwave behavior of an un-bonded continuously capacitively loaded p-i-n semiconductor microwave waveguide device. The specific structure discussed is that of a traveling wave electroabsorption modulator. This structure is similar to one that could be implemented in HMMIC using sparse ITS metalbonding and as such it is important to discuss its special microwave properties. The bonded version would have the p-i-n structure reversed and a large portion of the current n-layer replaced with bondmetal.

8.10.1 TWEAM Definition

The traveling wave electroabsorption modulator (TWEAM) is a high speed optoelectronic device used to amplitude modulate an optical carrier with a microwave signal – such a device plays a key role in optical communications systems. Figure 8-16 shows a cross sectional illustration of such a device. The illustration is not to scale, to highlight its key features. The bonded version would look very similar, but with two key differences. The first being that this structure is a mixture of CPW and microstrip, while
the bonded version would be purely microstrip – with much of the n-layer replaced with bondmetal to form a higher conductivity bonded-microstrip ground. The second major difference would be the reversal of the p-i-n structure, where the n-layer would be on top (with a smaller signal line contact area), and the p-layer would be on bottom (with a larger area in contact with the bondmetal). This latter change would reduce the contact resistance per unit length along the waveguide for the p-type layer, as its contact area would be much larger. Contact resistance would play a smaller role in bonded InP based device behavior, compared to the investigated un-bonded TWEAM. This is true because contacts to n-type InP typically have much lower specific contact resistivities than p-type (roughly 10 times lower). If the device were to be used as a bonded optoelectronic waveguide device, then the optical properties of the bondmetal must be included in the design – the most important being any scattering loss that may occur.

Figure 8-16. Illustration of the TWEAM structure cross section.
8.10.2 Measurement

Microwave measurements were performed using the standard method outlined in the general measurement section above, with no special considerations for this particular structure.

8.10.3 Discussion of behavior

Figure 8-17 shows example measurement results including example S-parameter plots and extracted waveguide characteristics. Again, two frequency ranges were tested as the mid-frequency range trivially connects the two.

![Graphs of S-parameters and microwave characteristics](image)

It should be noted that the thin intrinsic semiconductor layer and highly conducting n and p-type layers of the p-i-n structure yields a high junction capacitance.
This capacitance is in addition to the capacitance given by the signal and ground conductors while the inductance of the structure is due to the signal and ground conductor configuration, without regard to the semiconductor doping. Therefore, the capacitance and inductance are not reciprocals of each other characterized by a simple effective dielectric constant, but have a much more complicated relationship. The structure is effectively a capacitively loaded waveguide, where the junction capacitance continuously loads the waveguide along its length. This results in a slow-wave phenomenon where the microwave index is higher than the effective dielectric constant the structure would traditionally yield. The loss of the structure is also affected by this slow-wave phenomenon, and is higher than would be expected otherwise, and the impedances are lower than traditional ones as well.

8.10.4 Modeling

This slow-wave phenomenon has been modeled by several researchers using various equivalent circuits.\textsuperscript{14,15,16,17,18,19}

8.10.4.1 Crude Model

The crude model used to investigate this structure is shown in Figure 8-18, where each of the transmission line values are constant with frequency, with the exception of the series resistance which changes as a function of the skin depth in the structure.
Many of the previous models in the literature simply fit their measurement results to this circuit; however, here the dissertation author derived simple approximations for the values, based on the physical structure and properties of the waveguide, in an attempt to distill the microwave behavior using closed form equations.

The results of this analysis are shown in Figure 8-19. The impedance and loss depend on circuit parameters through this model; however, they did not match closely to the measurement results directly and a few constants (close to one) had to be factored onto the approximated circuit elements to more closely match the measurement behavior.
These factors were required due to the poor assumptions made when estimating the circuit elements from the physical parameters of the waveguide. The capacitance was assumed to be dominated by the intrinsic layer’s thickness, and was calculated based on a parallel plate calculation that included fringing fields. The contact resistance was imposed by the high resistance of the narrow p-type semiconductor contact metallization. The inductance was based on a simple microstrip assumption of the center conductor, assuming that the n-type epilayer formed an effective ground. A simple version of Wheeler’s incremental inductance rule was assumed, to provide the frequency dependent resistance of the signal conductor, assuming that its contribution dominated over the n-type epilayer ground.
The resulting capacitance value used was $x \text{ F/m}$ and the inductance value was $x \text{ H/m}$. The contact resistance value used was $x \text{ ohms/m}$ and the series resistance changed with frequency according to the approximate skin depth as $x \text{ ohms/m} \cdot f^{1/2}$.

The method to extract impedance directly from measurement data was not known at the time, and the only way to estimate it was via the equivalent circuit. Thus, the circuit model parameters were matched to the microwave loss and index only, and the impedance was calculated from the resulting equivalent circuit. Hence, the model matches well for the loss and index, but not the impedance.

**8.10.4.2 Advanced Model**

Once the impedance could be extracted directly from the measurement, the large disparity was discovered. A second, more advanced, model was created to simultaneously match the measured loss, index, and impedance. This equivalent circuit is shown in Figure 8-20. Most of the circuit elements of this structure were frequency dependent and changed according to the skin depth in the conductors.

![Figure 8-20. Schematic diagram of the second generation TWEAM equivalent circuit.](image-url)
The center conductor metal resistance was accompanied by a large parallel p-layer resistance, as well as a series ground conductor resistance with parallel n-layer resistance. The inductance was estimated as before, assuming a microstrip configuration, using the metal signal line and n-layer contact metallization ground. Although assuming the n-layer was the ground conductor was still a poor assumption, there was no other simple alternative model. The junction capacitance and contact resistance were accompanied by a parallel capacitance, due to the large metal signal conductor coupling to the ground in addition to the i-layer coupling. The contact resistance had an added series component due to the n and p-layer perpendicular resistance. Also, a finite junction resistance was included in parallel with the junction capacitance, which was quite high due to the reverse bias of the p-i-n diode and low-light absorption during the measurement.
This new equivalent circuit model was able to roughly match the loss, index, and impedance with all correction factors close to one as shown in Figure 8-21. It presented a much more realistic interpretation of the physical structure of the TWEAM, but still made several crude assumptions that lead to its mismatch with measured data.

### 8.10.4.3 Finite Element Modeling

Finite element models were expected to correct for all of these assumptions to create a model that more closely matched the actual case; however, due to limitations in defining the model in ANSOFT (which was the only modeler available at the time) the resulting loss, index, and impedance were just as, or even more mismatched, than the analytical calculations. Table 8-3 shows the results of the FEM modeling that matched...
the structure with measurements shown in Figure 8-17. The largest discrepancy was the loss where the finite element model predicted lower values than the measurement results. It was not possible to model a lossy dielectric intrinsic region, and a perfectly resistive layer had to be assumed. Also, the model had no ability to include the effect of contact resistance, and the complicated structure could not be populated with a course network of finite elements, resulting in long solution times.

<table>
<thead>
<tr>
<th>Frequency (GHz)</th>
<th>Loss (dB/mm)</th>
<th>Impedance</th>
<th>Index</th>
</tr>
</thead>
<tbody>
<tr>
<td>5</td>
<td>1.348</td>
<td>21.89 - j3.42</td>
<td>8.15</td>
</tr>
<tr>
<td>10</td>
<td>1.899</td>
<td>21.53 - j1.97</td>
<td>7.90</td>
</tr>
<tr>
<td>15</td>
<td>2.513</td>
<td>21.45 - j1.52</td>
<td>7.77</td>
</tr>
</tbody>
</table>

8.11 Conclusion

A discussion of HMMIC systems would not be complete without an introduction to microwave theory. Microwave transmission line measurements and theoretical analysis are required to understand HMMIC operations. Finite element modeling provides an additional means to analyze microwave propagation.

Coplanar and Microstrip Waveguide Theory are common circuit architectures in traditional MMIC systems. They were compared to one another, in order to conclude which was most appropriate for HMMIC. It was then determined that, due to their design flexibility, Coplanar Waveguides are better suited for HMMIC systems.

The Preliminary Bondmetal Microwave Propagation Investigation showed that the bondmetal was capable of propagating a microwave. It also illustrated the connection between bond conductivity and microwave loss.
The Bonded Device Microwave Propagation Investigation measured the microwave characteristics of a bonded-microstrip waveguide design. Although the structure tested was not optimized for this purpose, it was capable of showing how microwaves propagate in such a structure.

The un-bonded PIN structure investigated, illustrated the unique microwave properties of a continuously loaded line structure. The slow wave nature of this type of waveguide should be considered when designing similar bonded devices.
8.12 References


9 Conclusions and Future Work

9.1 Summary of Dissertation

Densely integrated heterogeneous microwave systems will soon be required, as mixed RF/digital systems are pushed smaller, faster, and to higher power. A metalbonding approach to achieving a heterogeneous monolithic microwave integrated circuit system architecture has been established. The investigation of which, has yielded a means of heterogeneously integrating an indispensable microwave compound semiconductor material (GaAs) with silicon. This combination was assessed to demonstrate how the metalbonded HMMIC can provide a more functional microwave system design, than currently exists. The performance of the metalbonding technique, used to achieve this integration, has been verified by examining its unique characteristics.

9.1.1 Robust Heterogeneous Integration

Sparsely integrated heterogeneous structures have been implemented using both a top-down and bottom-up approach. The top-down approach was achieved by waferbonding whole samples and fabricating structures from resulting heterogeneous samples, using the post-pattern bonding method. This method was the first to be investigated and provided a means of illustrating the viability of the metalbonding technique. The post-pattern bonding method was plagued by a low yield and minimal performance. This led to the investigation of a bottom-up approach, where both microwave device and silicon system fabrication could be completed, prior to integration.
– this provided a ‘back-end’ process. The pre-pattern bonding bottom-up technique offered a more practical high yield sparse integration method.

Many difficulties associated with the incompatibility of heterogeneous materials were overcome, to successfully create an integrated system, and are summarized below.

9.1.1.1 Lattice Mismatch

Misfit stress presented an obstacle to the heterogeneous growth of compound semiconductor materials on silicon. Lattice mismatch leads to metamorphic growth. This metamorphic material has a high density of dislocations which spoil the electronic properties desired by compound semiconductor heterogeneous integration.

With the exception of SiGe growth, the only viable method of integration is bonding. SiGe is a low stress material, in comparison to other compound semiconductors, and may be used to make heterogeneous microwave systems. However, it suffers from a few drawbacks, including: heat dissipation, speed, and noise performance, which prevent it from surpassing alternative compound semiconductor integration methods.

Waferbonding is capable of avoiding this fundamental lattice mismatch dilemma, yet still provides a means of integrating arbitrary compound semiconductors with silicon – this was the investigated method of choice.

9.1.1.2 Latent Debris

The removal of surface contamination was paramount to successful waferbonding and thorough cleaning procedures were necessary to minimize latent debris. Meticulous MOCVD growth procedures were devised as well, to minimize hillock defect formation
which would otherwise prevent bonding. The unique liquid state of the ITS bonding technique allowed for the compliance of any remaining ‘bumps’ at the bond interface.

### 9.1.1.3 Thermal Stress

Thermal stress reduction, between heterogeneous materials, can only be controlled by material choice or bond temperature. Since the electrical properties of the materials involved dictated the materials choices, only the bond temperature could be adjusted to curb thermal stress. The low bonding temperature ability of the ITS metalbonding technique was exploited to minimize this stress, by careful selection of the bondmetal alloy. The resulting process was capable of bonding the highly thermal expansion mismatched GaAs-Si system. The same alloy would be capable of bonding other relevant, less mismatched, compound semiconductors to silicon such as InP-Si or InAs-Si, etc.

The implementation of the wax underfill process was capable of relieving some of the thermal stress from sparsely bonded structures, and was crucial to the successful implementation of the sparse pre-pattern metalbonding process.

### 9.1.1.4 Chemical Incompatibility

Many chemical incompatibilities exist between the bondmetal, compound semiconductor, and silicon materials involved. The principle incompatibility, affecting integrated device fabrication, concerned etching. The etchants required to form the final device structures affect each material differently. Most GaAs etchants do not affect silicon, but demolish bondmetal. This difficulty was evaded by careful development of the fabrication procedure.
The bottom-up approach minimized the impact of this incompatibility. The sparse nature and implementation of wax and PMGI filler materials reduced the probability of etching the bondmetal through material defects during substrate etch-thinning. Patterning the devices prior to bonding allowed the pre-pattern bonding method to eliminate the need to etch GaAs devices in the presence of the bondmetal.

Optimized MOCVD growth procedures reduced the defect density, minimizing substrate etch-thinning leakage.

9.1.2 Metalbonded HMMIC Evaluation

Evaluation began with a review of existing microwave integration technology limitations, and an assessment of the unique capabilities afforded by the metalbonded HMMIC approach.

With the successful sparse integration capability of the metalbonding process achieved, bonded device properties could be evaluated to qualify its use in the HMMIC scheme. Several important measurements of the bond interface were made, as well as the microwave properties of a bonded transmission line. In addition, a relevant un-bonded active waveguide device was also characterized to illustrate the implications of its unique microwave properties.

9.1.2.1 Existing MMIC Limitations

The best material choice for creating microwave integrated circuits is one that has a high mobility, a large bandgap, and can be suitably manufactured on readily available substrates. Compound semiconductors combine all these with the ability to form unstrained heterojunctions, widening their design possibilities. The drawback to standard
monolithic microwave integrated circuits is their reliance on lattice matched substrate materials. These materials are expensive to obtain, costly to fabricate, small in size, and delicate to handle. Devices grown on these substrates are limited in variety and restrictive in operation.

Existing MMIC systems typically use a microstrip waveguide architecture. The use of this design is perpetuated by its vast knowledge base, but a coplanar design would provide more design flexibility and capability. Therefore, the CPW structure became the design of choice in the new HMMIC architecture.

9.1.2.2 Metalbonded HMMIC Capabilities

The hybrid nature of the HMMIC design provides many design advantages. Integrating devices from different substrates allows for a wider device variety and allows them to be tested, prior to integration, to improve quality control. Having separate substrates for each type of device allows them to be individually engineered, for either maximum yield or maximum performance.

High resistivity silicon combines an existing digital architecture with the low loss characteristics of semi-insulating compound semiconductors to provide an ideal platform for HMMIC designs. All of the digital functions of a hybrid RF/digital system and interconnect and support hardware can be provided by one material. The sparse nature of the pre-pattern metalbonding process can efficiently distribute the cost of compound semiconductor device manufacturing by integrating microwave devices into a customary silicon fabrication process as a ‘back-end’ process. Completed, tested, microwave components may be fully integrated into the silicon architecture using standard
metallization techniques. The metal bond interface provides a higher thermal conductivity than other bonding methods allowing for lower noise and higher power operation.

The bonding process itself allows novel device concepts to be introduced. Any device that would benefit from the use of a buried metal structure could be implemented using this technology. The example of a bonded-microstrip structure was characterized to demonstrate its effectiveness. It would be trivial to expand the pre-pattern bonding process to include multiple bond interface interconnects which could benefit multiple contact devices, such as transistors, by directly connecting them to underlying coplanar circuitry. The LN$_2$ temperature process improved bonded device scaling, as compared to a room temperature process. The LN$_2$ process limits the smallest bondable feature size to the minimum grain-size that can be created (on the order of a 10’s of nanometers), while the room temperature process limits the feature size to something larger than the droplet dimensions (on the order of 10’s of micrometers or larger). This represents a scaling improvement factor of one thousand.

9.1.2.3 Test Structure Characterization

Innovative test structures were implemented, to extract the physical properties of the In-Pd alloy bond interface, in order to validate its use as an appropriate HMMIC bondmetal. This alloy formed a universal ohmic contact between all doping combinations of GaAs and silicon, streamlining the integration interconnect process.

The electrical bond interface contact resistivity between n-GaAs and p-Si was tested, yielding a resistivity of $1.03 \times 10^{-5}$ ohm-cm$^2$ – matching well with the expected
result based on available contact resistivity data. Contact resistivities of x, x, and x, for the p-GaAs/p-Si, p-GaAs/n-Si and n-GaAs/n-Si cases were estimated from the electrical behavior I-V measurement slopes relative to the n-GaAs/p-Si case. These are low enough to form effective contacts between the two materials.

The bondmetal thermal conductivity was also tested and found to be 2.51 W/m-K. This was lower than originally expected, yet seemed sensible after analyzing the alloy using the Wiedemann-Franz law. It may be higher than anticipated, but still represents an approximate two-fold improvement over the next highest thermal conductivity heterogeneous bond interface material. Analysis shows that bonding to silicon using this alloy can improve bonded device heat transfer by a factor of two, as compared to an un-bonded GaAs case for similar sized devices. The total thermal heat transfer may be improved further by choosing either a higher thermal conductivity substrate than silicon (such as silicon carbide, aluminum nitride, metal, or diamond) or by improving or replacing the bondmetal alloy. The latter is discussed in subsection 9.2.4.3.

Pre-bond coplanar and bonded-microstrip microwave waveguides were characterized to establish that the bondmetal could support a propagating microwave and to demonstrate the role of bondmetal conductivity in transmission line loss. The index and impedance of the waveguides were reasonable, although not specifically optimized. The loss of the bonded-microstrip waveguide was high, but this was attributed primarily to the high resistance of the thin magnetic nickel signal metal and to a lesser extent the high resistance of the bondmetal and field metal. However, the investigated structure was not designed to yield optimal loss and could be better designed in the future.
An un-bonded traveling wave PIN diode structure was investigated to illustrate the importance this relevant active device structure’s unique properties. The PIN structure artificially loads the transmission line with a capacitance per unit length that affects its microwave behavior. This results in a ‘slow-wave’ phenomenon that is challenging to model in a standard finite element environment, and can be addressed using an analytical approach. The index of the ‘slow-wave’ waveguide is higher than would be initially expected, as well as the loss, and the impedance is lower. These unusual properties would have to be accounted when implementing similar devices in an HMMIC design.

9.2 Future work

This dissertation has taken the initial steps necessary to demonstrate the viability of the ITS metalbonding technique, as a means of achieving the proposed HMMIC paradigm. If the technology is to become a commercial success, rather than remain an idle curiosity, it must be carried over to a manufacturing setting. The investigation thus far has already addressed many of the fundamental concerns which would be raised during this process. However, a few notable details need to be elaborated upon.

Several bond evaluation metrics have been introduced, some of which could be improved. As yet, no active microwave devices have been bonded using this method. The yield of the pre-pattern bonding process is significantly higher than the post-pattern process; however, further exploration is necessary. The In$_7$Pd$_3$ bondmetal was an adequate starting alloy; however, better alloys may exist and need to be investigated.
9.2.1 Improving Measurement Methods

Improving the accuracy and efficiency of the measurement methods would yield a better physical understanding of the bond interface and increase manufacturing throughput.

The contact resistivity measurement method was adequate for laboratory testing; however, the entire substrate thickness was used during testing and was required to be uniform – such a structure would be wasteful in a manufacturing environment. A real HMMIC substrate would likely consist of various shallow doped patches on a HR-Si substrate. The contact resistivity structure would have to reflect this layout. Concentric metal contacts surrounding bonded mesas on conducting patches on the HR-Si substrate could be used to de-embed the contact resistivity without having to use special contact resistivity substrates. These structures could be located near the devices of interest at the edge of the Si circuits. These structures could be placed next to traditional Si test structures, which are positioned within the alignment mark/dicing rows and columns to save die real estate.

The current microwave waveguide test structures can be used directly without change, as they are self-contained and require no special substrate.

Bondmetal thermal conductivity measurements should be improved. The study of thermal conductivity is a study of defects, and accurate measurements would provide a quick test of bond alloy defect structure. The ability to consistently test conductivity in a production environment would allow variations to be detected. A drop in thermal conductivity would indicate an increase in alloy defect density, providing valuable feedback to process engineers. Improved accuracy would allow designers to alter layouts
accordingly, and let researchers find alloys with higher thermal conductivity. Although untested, thermal measurement structures using periodic bondmetal patterns might provide a method of extracting higher thermal conduction accuracy. By creating a situation where the spreading resistance of different structures would be identical, due to their similar footprint, the bond layer, which would consist of less bondmetal, could be used to de-embed the bond thermal conductivity more accurately. Other methods of achieving the same could be implemented, such as using different thicknesses of bondmetal. However, different thicknesses would require additional metal deposition steps which would slow production. A transient method such as that of Gustafsson and Karawacki\textsuperscript{1}, or Cahill and Pohl\textsuperscript{2}, may be adapted in the future to determine the heat capacity of the bond layer, if it were necessary to understand transient thermal behavior.

9.2.2 Bonding Active, High-Power, High-Speed Microwave Devices

Active semiconductor devices should be metalbonded in the future, to determine which, if any, significant consequences arise. Only then will all of the advantages associated with metalbonded HMMIC be realized.

In order to meet the demands of manufacturing, the scale on which the process is performed will have to increase from the small sample sizes illustrated here, to full wafer production. Much of the technology already supports such a move; however, existing pick-and-place methods will have to be incorporated into this technology to orient and bond the compound semiconductor structures onto completed silicon wafers. Also throughput would have to be improved as alloy diffusion currently limits the bond anneal
duration. Thinner bondmetal thicknesses, or faster alloy kinetics, will have to be implemented.

Another method to achieve faster alloying speed would be to locally heat the bondmetal without affecting the semiconductor substrates. Although as yet untested, intense light from a heat lamp or other source could, if properly filtered, pass through both semiconductors and be absorbed by the bondmetal. This could assist or replace the existing bond alloying techniques to effectively increase the bondmetal anneal temperature without imposing further substrate thermal stress.

Although much of the microwave loss of the bonded-microstrip waveguide was attributed to resistive conductor losses and conductive dielectrics, there is another loss mechanism that was not discussed. Metal roughness also plays a role in loss\textsuperscript{3,4,5} This is generally studied in high Q microwave resonator structures (typically air filled cavities). Much of the work in this area is focused on these systems because the loss due to surface roughness is generally small and only experimentally verifiable in high Q systems where even small losses have a big impact. Although its effect is minor in bonded device resistive conductor losses, its role could become more important as conductor resistances are improved.

### 9.2.3 Improving Yield

The pre-pattern process significantly improved the bond yield beyond that of the post-pattern process. However, further improvement must be made if the process is to become a commercial success. Many of the issues associated with this laboratory
investigation stem from the minimal amount of mechanization involved; most work was performed by hand, or with minor support from specialized equipment.

Cleanliness will likely improve with the advent of automation, as much of the debris stems from human interaction. The implementation of megasonic, rather than ultrasonic, agitation might yield cleaner bond surfaces, as well.

Defect density reduction would improve bond quality, as well as etch-thinning yield; superior MOCVD machines would be capable of achieving such a feat. Pre-growth cleave debris would be eliminated as entire growth substrates could be grown, and cleanliness could be maintained using a cleaner growth chamber and proper load-lock.

Advanced etch-thinning techniques would improve bond integrity by reducing the probability of etchant leaking through to the bondmetal. Enhancing this would, by far, have the biggest impact on yield, as the laboratory investigations thus far have all been plagued by this problem. An automated jet etching apparatus would be able to more uniformly thin the samples, especially if they had some sort of thickness monitoring system that could provide feedback. A more uniform etch would reduce the selective etch duration, improving etch yield. Also the wax and PMGI etchant barrier materials employed in this investigation may be adequate starting materials but would be improved by the investigation of advanced materials.

Reduced indium squeeze-out would also lower the likelihood of bondmetal etchant attack. This would be improved through better standoff design and layout, as well as improved cleanliness. Cleaner bond surfaces would allow taller standoffs to be implemented. Taller standoffs would reduce the collapse of the bond region, thus
reducing indium squeeze-out. This would improve the bonded structure packing density by minimizing the separation governed by the squeeze-out dilation of the structure footprint.

9.2.4 Improving the Bond Alloy

The In-Pd alloy successfully bonded GaAs to Si; however, other alloys may be used. The lower thermal stress between other compound semiconductor and silicon could allow alloys with better properties to be implemented. Thermal stress is also governed by the bond anneal temperature which is decided by the initial metallization and final alloy composition. The contact resistivity of the In-Pd alloy between GaAs and Si is adequate, but could be improved to increase electrical efficiency. Bondmetal thermal and electrical conduction is dictated by alloy composition and defect density. A higher conductivity alloy would improve heat transfer and microwave waveguide loss.

9.2.4.1 Finding Lower Bond Temperature Alloys

The process of finding lower bond temperature alloys consists of searching for bond alloys that have a high enough remelting temperature and lower LMPM melting temperature. Unless gallium can be prevented from prematurely melting during the bonding process, by keeping the samples below room temperature, the only hope for a low LMPM melting temperature would come from alloys.

These alloys would have to either be deposited in their completed or constituent form. The alloy kinetics of the LMPM must not compete with the peritectic alloying process if the ITS bond method is to be successful. The Au-In-Sn alloy examined by Schmid-Fetzer, and the Ag-In-Sn alloy examined by Jacobson and Humpston, did meet
the first criterion of having a low LMPM melting temperature, but ended up interfering with the ITS alloying process. Much trial and error investigation would be needed to determine what alloys would be best suited for this purpose, as ternary alloys are not well studied. Ternary systems are more difficult to study as some alloy processes may not be easily discernable from external behavior. Also, ternary systems add an additional axis of composition complexity which vastly increases the number of permutations.

When investigating new bondmetal alloys, it is important to keep other properties in mind. An alloy that lowers the bond temperature will not generally improve electrical/thermal conductivity, as alloys with more constituents tend to lower conductivity. Contact resistivity may also have to be sacrificed to achieve lower bond temperatures.

### 9.2.4.2 Finding Lower Contact Resistivity Alloys

The study of metal-semiconductor contact behavior is complicated by Fermi surface pinning and metal-semiconductor alloy behavior. The search for lower resistivity contacts tends also to be one of trial and error, and focuses mainly on finding alloys that lead to either lower Schottky barriers or high surface doping.

Restricting the search to ITS alloys limits the possible combinations considerably, and is necessary if they are to be used to metal bond. In some situations, the universal nature of the bond alloy may be sacrificed to create lower contact resistivity bond alloys. The easiest way to do this would be to add dopants to the bond metallization that would increase the surface doping level of the adjacent semiconductor, without adversely affecting the ITS bonding process.
### 9.2.4.3 Finding Higher Electrical and Thermal Conductivity Alloys

Finding alloys that have higher thermal conductivities is, for the most part, the same as finding alloys that have higher electrical conductivities. This is due to the Wiedemann-Franz law that relates the electronic thermal conductivity, which is dominant in good conductors (such as metals), to the electrical conductivity through the Lorentz constant.

It is difficult to analytically calculate the electrical (or thermal) conductivity using quantum mechanics of unknown alloys with any accuracy. This process becomes even more difficult if the conductivity is dominated by defect scattering mechanisms and impossible if the structure of the alloy is unknown. However, the Wiedemann-Franz law may be used to provide a higher accuracy for high thermal conductivity if the electrical conductivity can be measured. If the electrical conductivity can be assessed using a simple test structure, then the W-F law approach could severely reduce the time required to empirical search for alloys. Simply applying the constituent metals to an arbitrary insulating substrate, and annealing the sample uncovered, may not lead to the correct result, but would likely yield a value similar to the real bonded case. This is due to the removal of any substrate effect which might affect the alloy and the inclusion of any surface texture that result from annealing.

It is important to emphasize that the intermetallic crystal structure, and resulting ITS bonding grain structure, dominate electron transport, leading to conduction. Therefore, the bulk conductivity of the constituent materials, which have a different crystal structure, do not dictate the electrical and thermal conductivity of a resulting alloy. The only exception to this is dilute alloys where the main constituent dominates.
the alloy crystal structure. This case is unfortunately not relevant, as high conductivity alloys must support the ITS bonding process. Also, since the conductivity depends on the crystal structure, the melting point may be determined by an abrupt drop in resistance as the alloy temperature is increased. This may expand the type of data that may be recovered during resistance measurements, allowing phase behavior to be mapped.

A search for such alloys should start from published electrical resistivity or thermal conductivity alloy data. The electrical resistivity of In-Pd alloys has been investigated by Grebennik and Tsimbal.\textsuperscript{8} Farmakovskii and Karasik\textsuperscript{9} measured the electrical resistivity of several Cu binary alloys, of which Cu-Sn is, and Cu-In might be an ITS alloy. Parretta and Rubino\textsuperscript{10} also examined the Cu-In alloy system and described the instability of the Cu-In ITS intermetallic. Uemura and Satow\textsuperscript{11} measured the electrical resistivity of Ag\textsubscript{3}In, which is a possible ITS alloy. Horo \textit{et al.}\textsuperscript{12} also measured the electrical resistivity of two Ag-In alloys. A few other authors\textsuperscript{13,14,15} have measured the liquid phases of a few ITS alloys, but this data has little relevance to solids.

Several authors\textsuperscript{16,17,18,19,20,21,22,23,24,25} have presented either electrical or thermal resistivities of alloys composed of the same constituents as ITS alloys, but of non-ITS alloy intermetallics or dilute metals, both of little relevance. Authors\textsuperscript{26,27,28,29,30} all published data for low melting point eutectic alloys, but not for any ITS alloys.

Another major factor that contributes to the alloy conductivity is its defect structure and density. Alloys with lower defect densities suffer from fewer grain boundary scattering events, leading to higher conductivity. Methodical metallurgy may reduce these scattering events by adding dilute materials, capable of changing the crystal
structure without severely impacting the ITS alloying process, to more closely pack alloy grains or fill voids between grains.

The implementation of higher conductivity alloys may sacrifice other relevant characteristics, such as ohmic behavior or contact resistivity.
9.3 References


Appendix A: Heat Transfer and Thermal Conductivity Theory

A.1 Introduction

This appendix introduces heat transfer theory relevant to HMMICs. Section 0 provides a brief introduction to general heat transfer. Section 0 discusses a general thermal model for HMMIC systems and describes its simplification to a simpler conduction dominated model. Section 0 presents a brief introduction to the origins of thermal conductivity in materials, and details how to theoretically approximate the thermal conductivity of unknown materials. The first several subsections of which, 0 to 0, provide a sound depiction of the aspects that control the thermal conductivity in materials, while the last subsection, 0, specifically addresses how to accurately predict the thermal conductivity of unknown materials.

A.2 Basic Heat Transfer Theory

This section will discuss basic heat transfer theory as it relates to HMMIC devices. Discussion begins with the first subsection introducing the general thermodynamics theory involved, while the second subsection details methods to model heat transfer.

A.2.1 General Thermodynamic System Theory

This subsection provides a basic introduction to the thermodynamics involved in a general heat dissipation system. The reader is encouraged to refer to the many textbooks that have been written on the subject to gain a more in-depth understanding.
Conservation of energy dictates that energy may enter or exit a domain, but the net loss must be zero. This statement as it relates to thermodynamic systems essentially means that the total energy entering a domain’s boundary must be stored or converted within. Domains of interest to this dissertation will be assumed finite in size and operating at a steady state condition. In a finite domain, the storage of energy must be finite lest its temperature increase. The steady state condition prevents the temperature from increasing indefinitely, thus the storage of energy must drop to zero at steady state. As a result the domain is left to balance its incoming energy with its converted energy. Energy is allowed to move through the domain. The energy leaving the domain through its boundary must balance the energy conversion within and the energy entering the domain elsewhere on its boundary. A simple model describing this generic thermodynamic domain at steady state is illustrated in Figure A-1. A thermodynamic system is defined by at least one of these domains; however, the system may be divided into any number of subdomains.

![Figure A-1. Illustration of the heat transfer in an arbitrary domain at steady state.](image)

Energy conversion may occur on the domain’s bounding surface, or within its volume, and may be converted in many different ways (i.e.: Joule heating, imposed...
stress, friction, chemical reaction, electromagnetic radiation, evaporation, etc). Heat may transit the interior of the domain via four mechanisms. Matter containing heat energy may transit through the domain at a particular velocity to kinetically transfer heat (convection) or may be conveyed via radiation or conduction.

A.3 Heat Transfer System: Thermal Modeling

The measurement section will describe different ways to measure heat transfer in semiconductor devices. In general, they all have some form of a heating structure on the surface of the semiconductor surrounded by air. This semiconductor is eventually connected to a boundary that sinks heat. This same description holds true for any heat source in the proposed HMMIC system as well, although the air may be substituted by a poor thermal conductivity packaging medium, with no loss of generality. For now, the simple heat transfer system illustrated in Figure A-2 will be adequate to describe the generation and flow of heat within these systems. It consists of a solid region, mostly surrounded by an air region, with a heat source acting on a small patch of area in the inner boundary.

Figure A-2. Illustration of a unified heat transfer system domain (as seen from its exterior).
Assume for the moment that the system, if viewed from the outside, is a single global domain. An energy conversion component is present and is acting within the system volume, while the outer boundary is free to pass heat. The system may therefore be described by

\[ Q_{S2} = \dot{S} \]

where \( Q \) represents the net rate of heat flow out of the system and \( \dot{S} \) represents the rate of work imposed by the heat source within the system.

Dividing the system into two subdomains, as shown in Figure A-3, it can be seen that not all of the heat transfer mechanisms are significant everywhere in the system. All parts of subdomain-1 are solid and stationary, and unable to kinetically transfer heat. The air in subdomain-2 will generally be allowed to flow and is capable of kinetically transferring heat. Heat transfer by radiation within the solid will be assumed negligible in comparison to its heat conduction component. In addition, only one source of energy conversion will be included in the system and will act on the boundary of subdomain-1.

Figure A-3. Illustration of a subdivided heat transfer domain describing a heat source on a solid in air.
The importance of each heat transfer component in the system must be understood in order to model it accurately. Conduction transfers heat by phonons and electrons within a medium and takes the form

$$q_k = \kappa \nabla T$$

which depends solely on the temperature gradient $\nabla T$ and the medium’s thermal conductivity $\kappa$. The origins of thermal conductivity in materials will be discussed in the next section. The conductivity of the air is negligible in comparison to the conductivity of the solid (as shown in Table 1-1), so the conductivity contribution from subdomain-2 can be ignored.

Convection transfers heat by the kinetic movement of a medium and is given by

$$q_u = \rho C_p (T - T_{ambient}) u$$

which depends on the density $\rho$ and heat capacity $C_p$ of the medium as well as its velocity $u$ and temperature $T$. The external boundary of the system, is assumed to be at room temperature, thus any incoming air is assumed to be at this temperature. Heat may be transferred by convection only if the heat source temperature is higher than the air temperature. During measurements, the setup is shrouded with a cover to reduce air drafts, the heat source for the system never exceeds 50°C above room temperature, and the hot surface area is small (less than one hundred micrometers wide and a millimeter or less in length). These conditions are not strong enough to evoke a stable, natural convection current in the immediate surrounding air and the cover damps any external air...
movement. The minimal air currents and small heater size lead to a negligible convection component for subdomain-2.

Radiation transfers heat by photon and require a transparent optical path to do so. Heat transfer by radiation is described by

\[ q_A = \varepsilon \sigma \left( T^4 - T_{\text{ambient}}^4 \right) \]

which is dependent on the temperature \( T \) and emissivity \( \varepsilon \) of the medium, where the Stefan-Boltzmann constant \( \sigma \) is equal to \( 5.67 \times 10^{-8} \) W/m\(^2\)K\(^4\). The emissivity of any material must lie between zero and one – the emissivity of air is essentially zero due to its high transparency. Therefore, radiation transfers heat directly from the surface of the solid to the outer boundary without being absorbed or re-emitted within the air region. The surface of the solid may have an emissivity as high as one, but its maximum temperature is kept below 50°C over ambient during thermal measurements – most of which only exist within a small area on the surface near the heater. The influence of all these factors, along with the exceedingly small Stefan-Boltzmann constant, yields a negligible radiation contribution for subdomain-2.

With all the heat transfer mechanisms negligible in subdomain-2, there is no need to be concerned with its thermal influence on the system as a whole, and heat flow through its boundaries may be considered negligible. The entire system may be simply modeled as one dominated by heat conduction, where heat flows from the surface heat source through subdomain-1, down to the bottom exterior boundary as illustrated in Figure A-4. The discussion of the specific model of the measurement system will be addressed in the measurement section.
A.3.1 Thermal Resistance Definition

The heat flow in a conduction system is fully described by Equation A-2 alone, which is just a specific example of a general gradient model. Gradients are prevalent in many physical system models, including electrical conduction and electrostatics. In the case of heat conduction $q$ represents heat flux and $T$ the heat potential (or temperature). These are akin to electrical conduction’s current flux $J$ and voltage $V$ and electrostatic’s electric field density $D$ and voltage $V$. The only difference between these systems are the meanings of their flux constants: thermal conductivity $\kappa$, electrical conductivity $\sigma$, and permittivity $\varepsilon$. Any solution to a system that uses a gradient relationship may be used directly in a related system simply by changing the flux constant to match.

If a thermal domain can be broken up into a set of incremental, one-directional flows, each flow may be represented by a thermal conductance or resistance. This is true because any gradient in one direction – regardless of its orientation in space – may be
represented by a one-dimensional gradient with a corresponding flux constant. In a general example of an anisotropic media, the rotated one-dimensional gradient would have a flux constant given by the culmination of the axial components. From a geometry perspective this describes the collapse of a three-dimensional tensor transformation into a single-dimensional unitary transformation.

If the one-dimensional flux exists in a body that can be described by a cross section (such as in Figure A-5) then the flux may be represented as a flow. In the context of thermal conductivity, this flow would be power $P$ (in electrical conduction it would be current $I$, and in electrostatics it would be electric field $E$)

Figure A-5. Illustrations of flow and accompanying equivalent circuits in a uniform body depicting: (a) the one-dimensional flow in a uniform cross section and (b) three constituent one-dimensional flows.

Once in the framework of a one-dimensional flow the uniform conduction constant means the flow has a linear potential distribution. The integration of the static component along the length of the flow path defines the flow’s potential. The measure of
this potential in relation to its corresponding flow yields another constant. In terms of thermal conductivity, this constant is conductance \( C \) (in units of \( \text{W/}^\circ\text{C} \)) or resistance \( R \) (in units of \( ^\circ\text{C}/\text{W} \)) (in electrical conduction it is conductance \( C \) (in Siemens) or resistance \( R \) (in Ohms) and in electrostatics it is capacitance \( C \) (in Farads)).

The idea of thermal resistance can be used to model systems via a network of resistances or conductances similar to an electrical circuit, as illustrated by Figure A-6. These networks may be described, as seen by their terminals, as characteristic system resistances. If the networks were made of a continuum of incremental components then they could adequately describe any three dimensional system. Therefore any general three-dimensional thermal conductivity structure may be described at its terminals by a characteristic resistance.

![Figure A-6. Illustration of a resistance network and its characteristic terminal resistances.](image)

### A.4 Thermal Conductivity

Bulk macroscopic thermal conductivities of several materials pertinent to HMMIC (at room temperature) are shown in Table 1-1. The use of the macroscopic thermal conductivity value in thermal conduction systems are valid when investigating the heat transfer at scales larger than the mean free path length of the dominant heat
transfer particle. For poor electrical conductors, the phonon contributions tend to be dominant (with mean free path lengths on the order of 10’s of nanometers) and for good electrical conductors the electron contributions are dominant (also with mean free path lengths on the order of 10’s of nanometers). With the exception of very thin layers, such as superlattices or very thin bondmetal interfaces, the macroscopic thermal conduction modeling treatment is sufficient when discussing HMMIC structures and will be discussed to the exclusion of smaller dimension treatments.

It is important to use high thermal conductivity materials throughout the construction of an HMMIC, or any electronic system for that matter, in order to efficiently extract heat from working devices. In general, the nominal operation of these devices is dependent on maintaining a cool temperature. To begin with, a high temperature creates excessive thermal noise which would be detrimental to electronic systems. This high temperature will ionize more carriers in a semiconductor material which will lower device breakdown. It may also affect device linearity if the device’s saturation mechanism is affected. A higher temperature might physically alter the electronic device by diffusing material throughout its structure (i.e.: dopants, contact metallizations, etc.). This diffusion will adversely affect device reliability if their active regions are affected. At extreme temperatures, the devices may even catastrophically fail.

A.4.1 Theoretical Origins of Thermal Conductivity

Maintaining an electrical device at its lowest possible temperature requires achieving the lowest possible characteristic thermal resistance between device and
heatsink. In order to achieve this, the thermal conductivities of the materials that make up the system need to be optimally high. Understanding the fundamental origins of thermal conductivity could help decide how effective an unstudied material might be.

### A.4.2 Basic Thermal Conductivity Theory

The macroscopic thermal conductivity of a material depends on how thermal carriers react with each other, in the presence of a material’s crystal structure and composition.

Electrons, holes, phonons, photons, and a few others are all examples of thermal carriers. In good conductors, electron contributions dominate and in semiconductors and insulators, phonon contributions dominate. Contributions from holes in semiconductors are small in comparison to electron contributions, both of which are small in comparison to phonon contributions.

### A.4.3 Simple Gas Formulation

The essential elements involved in calculating thermal conductivity may be understood by first discussing the contribution from a single thermal carrier by applying a simple ideal gas formalism.

Equation A-2 may be more formally written

\[
\bar{Q} = -\kappa \nabla T
\]

Assuming an ideal gas where each contributing thermal carrier may be modeled as a particle, each carrier would have a capacity to hold some quantity of heat (or heat capacity \(c\) per carrier). If each particle moves with its own velocity \(\bar{v}\) under the influence of a temperature gradient \(\nabla T\) then their energy would change at a rate given by
\[ \frac{\partial E}{\partial t} = c \vec{V} \cdot \nabla T \]  

Averaging the particle velocities over all possible directions and declaring a carrier scattering mean free relaxation time \( \tau \), then applying Equation A-6 to Equation A-5 yields

\[ \bar{Q} = -\frac{1}{3} n c \tau \nu^2 \nabla T \]  

where \( n \) is the number of carriers and \( \nu \) is the average scalar velocity.

Declaring a mean free path length \( l \) between scattering events according to

\[ l = \tau \nu \]  

and letting \( C \) represent the total heat capacity of the gas according to

\[ C = cn \]  

then the conductivity may be represented by

\[ \kappa = \frac{1}{3} C \nu l \]  

Summing up the contributions from each type of thermal carrier would yield

\[ \kappa_{\text{total}} = \sum_{a} \kappa_a = \frac{1}{3} \sum_{a} C_a \tau_a \nu_a^2 \]  

A.4.4 Realistic Thermal Conductivity Formulations

More realistic thermal conductivity formulations may be made using a similar approach as the simple gas model, but using statistics that describe the true nature of the thermal carriers. Discussion will begin with dominant electronic and lattice thermal conductivity contributions of simple solids. Until recently, temperature has simply been a measure of energy potential; however, a more realistic description must be adopted if its movement is to be better understood. A material’s temperature is actually a measure
of its relative atomic movement; the more the atoms are displaced the higher the
temperature. The movement of atoms in a crystal is quantized based on the number of
atoms within the solid – these quanta are called phonons and are characterized by their
modes of vibration. Therefore the movement of temperature within a solid is given by its
local behavior of phonons. The formalism outlined below follows that of Yang.³

A.4.4.1 Electronic Contribution

The electronic thermal conductivity contribution does not stem from electrons
transporting heat around a crystal as was the case in the simple gas model. Instead, the
electrons rise and fall in energy within the confines of a solid’s crystal.

Due to Pauli’s exclusion principle, electrons of the same wavelength
(wavenumber) and energy (as well as spin) are not allowed to exist in the same spot and
are therefore defined as fermions, which obey Fermi-Dirac statistics. As stated earlier,
the electron contribution in insulators and semiconductors is very small, so discussion
here will focus on degenerate metals. This approximation is only valid for certain metals, such as
Alkali metals and to some extent Noble metals, but is quite poor for transition metals and
very poor for polyvalent metals, such as alloys. When at thermal equilibrium their
average distribution is given by

\[ f_k^0 = \frac{1}{e^{(E_k - E_F) / k_B T} + 1} \]

where \( k_B \) is Boltzmann’s constant and \( E_F \) is the Fermi energy.
A departure of this distribution from its thermal equilibrium represents a change in energy in the system and as time passes will return to the thermal equilibrium with a release of energy. The measure of this energy change over time is analogous to Equation A-6 and may be represented by

$$\frac{\partial\overline{E}}{\partial t} = \frac{f_k - f_k^0}{\tau_k} = -\vec{v}_k \cdot \left( \frac{\partial f_k^0}{\partial T} \vec{\nabla}T + e \frac{\partial f_k^0}{\partial E_k} \overline{E} \right)$$  \hspace{1cm} \text{A-13}

The reason for leaving in the electric field contribution will be evident in a moment. This may be rewritten using the Boltzmann distribution:

$$\frac{f_k - f_k^0}{\tau_k} = -\vec{v}_k \cdot \left( -\frac{E_k - E_F}{T} \frac{\partial f_k^0}{\partial E_k} \vec{\nabla}T + e \frac{\partial f_k^0}{\partial E_k} \overline{E}_{\text{eff}} \right)$$  \hspace{1cm} \text{A-14}

where

$$\overline{E}_{\text{eff}} = \overline{E} - \frac{\vec{\nabla}E_F}{e}$$  \hspace{1cm} \text{A-15}

is an effective electric field that describes the Fermi surface movement. This may seem excessively detailed at this point, but is the only illustration of its kind and isn’t without good reason.

Some understanding of the nature of this equation can be gleaned when viewing definitions of electrical current density

$$\overline{J} = \int e\vec{v}_k f_k d\vec{k}$$  \hspace{1cm} \text{A-16}

and thermal flux

$$\overline{Q} = \int (E_k - E_F) \vec{v}_k f_k d\vec{k}$$  \hspace{1cm} \text{A-17}

By creating a general integral
the current density $\vec{J}$ and thermal flux $\vec{Q}$ may be rewritten as

$$\vec{J} = e^2 K_0 \vec{E}_{\text{eff}} - \frac{e}{T} K_1 \vec{Q}$$

A-19

and

$$\vec{Q} = e K_1 \vec{E}_{\text{eff}} - \frac{1}{T} K_2 \vec{Q}$$

A-20

These relations fully describe the thermal and electrical state of the system. As a result

the thermal conductivity and electrical conductivity may be separated into

$$\kappa_e \bigg|_{j=0} = \frac{1}{T} \left( K_2 - \frac{K_1^2}{K_0} \right)$$

A-21

and

$$\sigma_{|T=0} = e^2 K_0$$

A-22

After some manipulation the current becomes

$$J_{|T=0} = \sigma E_{\text{eff}}$$

A-23

and the conductivity becomes

$$\kappa_e \bigg|_{j=0} = \frac{\pi^2}{3} \frac{k_B^2 T}{e^2} \sigma$$

A-24

The ratio of which yields

$$L_0 = \frac{\kappa_e}{\sigma T} = \frac{\pi^2}{3} \frac{k_B^2}{e^2}$$

(A-25

(commonly called the Wiedemann-Franz law) where $L_0$ is the standard Lorentz number

and is equal to $2.4453 \times 10^{-8}$ W-ohm/K$^2$. As a side note, the contributions from Equations
A-19 and A-20, not including $\bar{J} = 0$ and $\bar{\nabla}T = 0$, describe the Seebeck and Peltier thermoelectric effects.

Note the subscript applied to the thermal conductivity of Equation A-24, this conductivity is called the electronic contribution to the thermal conductivity and includes the effects of all electron scattering contributions. This is better illustrated when Equation A-24 is written out as

$$\kappa_e = -\left. \frac{\bar{Q}}{\bar{\nabla}T} \right|_{J=0} = \frac{1}{3} \int_{-\infty}^{\infty} v_i \tau_k \left( E_k - E_F \right) \frac{\partial f_k^0}{\partial T} d\vec{k}$$

A-26

Note the similarity to Equation A-11 from the simple gas formulation. The portion of this equation:

$$\left( E_k - E_F \right) \frac{\partial f_k^0}{\partial T}$$

A-27

may be thought of as the total heat capacity that electron behavior has within a crystal for all scattering types and $\tau_k$ represents the total electron relaxation spectrum for all scattering types.

The Wiedemann-Franz (W-F) law relates the electronic component of thermal conductivity to electrical conductivity in pure metal crystals. This rule is pertinent whenever electrons elastically scatter – this is generally true at high temperatures (when the absolute temperature is much greater than the Debye temperature: $T \gg \theta_D$). The Debye temperature is defined as

$$\theta_D = \frac{\hbar \omega_D}{k_B}$$

A-28
where $\hbar$ is Planck’s constant, $k_B$ is Boltzmann’s constant, and $\omega_D$ is the Debye cutoff frequency. This cutoff frequency is defined as

$$\omega_D = v_s \frac{2\pi}{\lambda_{\text{min}}} = v_s \left(6\pi^2 n\right)^{\frac{1}{3}}$$  \hspace{1cm} \text{(A-29)}

where $v_s$ is the velocity of sound in the solid given by

$$v_s = \sqrt{\frac{Y}{\rho}}$$  \hspace{1cm} \text{(A-30)}

where $Y$ is the solid’s Young’s modulus, and $\rho$ is its mass density. The concentration of atoms $n$ is defined by

$$n = \frac{N}{V}$$  \hspace{1cm} \text{(A-31)}

which represents the number of atoms per volume in the solid. The Debye temperature is defined in this way to normalize the absolute temperature of a solid to its ‘cutoff’ temperature. This ‘cutoff’ temperature is not the absolute maximum that the material may experience, but instead defines the temperature at which the highest phonon frequencies are excited – defined by the Debye cutoff frequency $\omega_D$ in Equation A-29.

Typically electron-phonon scattering events dominate the overall relaxation time and provide the biggest contribution to electrical and thermal conductivity. The resulting ideal electrical and thermal resistivities may be approximated at high temperature by

$$\rho_i = \frac{1}{\sigma_i} = \frac{A T}{4\theta_D}$$  \hspace{1cm} \text{(A-32)}

and

$$W_i = \frac{1}{\kappa_i} = \frac{A}{4\theta_D L_0} = \frac{\rho_i}{L_0 T}$$  \hspace{1cm} \text{(A-33)}
The constant $A$ is given by

$$A = \frac{3\pi \hbar q_D^6 (G')^2}{4e^2 \left( m^* \right)^2 n_c k_B \theta_D k_F^2 v_F^2}$$

where $\hbar$ is Planck’s constant, $\theta_D$ is the Debye temperature, $m^*$ is the electron effective mass, $n_c$ is the number of unit cells per unit volume, $v_F$ is the electron velocity at the Fermi surface, $k_F$ is the electron wavenumber at the Fermi surface, $q_D$ is the phonon wavenumber, and $G'$ is a constant representing the strength of the electron-phonon interaction. At medium temperatures ($T \sim \theta_D$), Equation A-32 through A-34 are much more involved and yield values that are higher than at high temperatures. The ratio of these more complicated equations deviate from the W-F law; however, impurity scattering at medium to low temperatures tend to keep the total electronic contributions off by less than a factor of two from the standard W-F relationship. Thus the W-F law may be used as an approximation within the medium to high temperature regimes. This is useful at room temperature as the average Debye temperature of common semiconductor industry metals are centered just around 260K and deviate by little more than about 40% as shown in Table A-1. This means that the medium temperature approximation of the W-F law is valid near room temperature for most metals.
Table A-1. List of relevant metal Debye temperatures.

<table>
<thead>
<tr>
<th>Metal</th>
<th>Debye Temperature (K)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pb</td>
<td>87</td>
</tr>
<tr>
<td>Bi</td>
<td>116</td>
</tr>
<tr>
<td>In</td>
<td>129</td>
</tr>
<tr>
<td>Au</td>
<td>178</td>
</tr>
<tr>
<td>Ag</td>
<td>221</td>
</tr>
<tr>
<td>Pt</td>
<td>225</td>
</tr>
<tr>
<td>Sn</td>
<td>254</td>
</tr>
<tr>
<td>Pd</td>
<td>275</td>
</tr>
<tr>
<td>Cu</td>
<td>310</td>
</tr>
<tr>
<td>Ni</td>
<td>345</td>
</tr>
<tr>
<td>Fe</td>
<td>373</td>
</tr>
<tr>
<td>Ti</td>
<td>380</td>
</tr>
<tr>
<td>Al</td>
<td>390</td>
</tr>
<tr>
<td>V</td>
<td>390</td>
</tr>
<tr>
<td>mean</td>
<td>262.4</td>
</tr>
<tr>
<td>stdev / mean (%)</td>
<td>40.7</td>
</tr>
</tbody>
</table>

A.4.4.2 Lattice Contribution

Phonons are mechanical oscillations of atoms within a material – when atomic movement is small, the atoms may be described as harmonic oscillators. Multiple oscillations of the same wavelength (or wavenumber) in a crystal are allowed to exist within the same space, therefore, phonons are defined as bosons and therefore obey Bose-Einstein statistics. The same formalism as used above may be followed to examine the phonon interaction contributions to thermal conductivity.

In equilibrium the phonon distribution is given by

\[
N_q^0 = \frac{1}{e^{\frac{E_q}{k_B T}} - 1}
\]
The quantized boson nature of phonons allows the phonon energy to be expressed by its wavelength

\[ E_q = \hbar \omega_q \]  

(similar to photons of light: another boson). Equation A-35 may be therefore rewritten as

\[ N_q^0 = \frac{1}{e^{\frac{\hbar \omega_q}{k_B T}} - 1} \]  

A departure from this equilibrium represents a change in energy over time which may be represented by

\[ \frac{\partial \bar{E}}{\partial t} = \frac{N_q - N_q^0}{\tau(q)} = -\nu_q \cdot \frac{\partial N_q^0}{\partial T} \nabla T \]  

where \( \nu_q \) represents the phonon group velocity. The movement of phonons therefore represents a heat flux given by

\[ \bar{Q}_q = N_q \hbar \omega_q \nu_q \]  

Summing over the entire phonon spectrum, to include the influence of all phonon scattering events on the spectrum, and dividing by the temperature gradient, yields the lattice thermal conductivity

\[ \kappa_L = \frac{\bar{Q}_{\text{total}}}{\nabla T} = \sum_q \hbar \omega_q \nu_q^2 \tau_q \frac{\partial N_q^0}{\partial T} \]  

where \( \tau_q \) represents the total phonon spectrum relaxation time for all scattering types. Noting the similarity to Equations A-11 and A-26, the portion of this equation

\[ \hbar \omega_q \frac{\partial N_q^0}{\partial T} \]
may be thought of as being the total heat capacity that phonon behavior gives to a crystal for all scattering types just as Equation A-26 did for electron behavior.

Just as with the simple gas model Equation A-40 may be recast into

$$\kappa_L = \frac{\theta_D T}{\pi} \int_0^\infty C(x) \nu l(x) dx$$  \hspace{1cm} \text{A-42}$$

where the integration variable \( x \) is a unitless temperature \( \theta_D / T \). This is the Debye approximation model which represents the lattice thermal conductivity by a heat capacity and mean free path given by

$$C(x) = \frac{3k_B}{2\pi^2V^3} \left( \frac{k_B}{\hbar} \right)^3 T^3 \frac{x^4 e^x}{(e^x - 1)^2}$$  \hspace{1cm} \text{A-43}$$

and

$$l(x) = \nu \tau_q(x)$$  \hspace{1cm} \text{A-44}$$

where \( \tau_q(x) \) is the sum off all phonon interaction contributions:

$$\tau_q^{-1}(x) = \sum_i \tau_i^{-1}(x)$$  \hspace{1cm} \text{A-45}$$

The collisions included in this model do not conserve crystal momentum which lead to their additive nature and are called Um-Klapp processes (U-processes). Other processes called Normal processes (N-processes) do conserve crystal momentum and do not add to the thermal conductivity directly.\(^3\) The N-processes can; however, convert phonon motion from one mode of vibration to another. This conversion requires very long phonon-phonon interaction lengths present only in very pure, defect free crystals. They act to effectively lengthen the relaxation time of Um-Klapp scattering events, thus increasing the thermal conductivity rather than decreasing it.
A.4.4.3 Scattering Mechanisms Summary

Table A-2 lists the electron and phonon scattering events possible in a material, along with a brief description of their strength. The total thermal conductivity of a material is given by its electronic and lattice contributions according to

$$\kappa_{\text{total}} = \kappa_e + \kappa_L$$  \hspace{1cm} A-46

where the electronic $\kappa_e$ and lattice $\kappa_L$ contributions represent the total effect of their respective scattering events.

Table A-2. List of thermal conductivity electron and phonon scattering events along with a brief description of each.

<table>
<thead>
<tr>
<th>electron-phonon</th>
<th>electron-boundary</th>
</tr>
</thead>
<tbody>
<tr>
<td>most dominant contribution in good electrical conducting materials such as metals</td>
<td>non-negligible in amorphous solids</td>
</tr>
<tr>
<td>electron-electron</td>
<td>electron-dislocation</td>
</tr>
<tr>
<td>always very weak</td>
<td>non-negligible in defective solids (weaker than phonon-dislocation scattering contribution)</td>
</tr>
<tr>
<td>phonon-phonon (Um-Klapp process)</td>
<td>phonon-boundary</td>
</tr>
<tr>
<td>most dominant contribution in poor electrical conducting materials such as insulator or semiconductors</td>
<td>is typically small (at least for non-highly polycrystalline solids)</td>
</tr>
<tr>
<td>phonon-phonon (Normal process)</td>
<td>phonon-dislocation</td>
</tr>
<tr>
<td>usually very weak, requiring long uninterrupted phonon coupling</td>
<td>non-negligible in defective solids (stronger than phonon-dislocation scattering contribution)</td>
</tr>
<tr>
<td>phonon-electron</td>
<td>phonon-impurity</td>
</tr>
<tr>
<td>always very weak</td>
<td>non-negligible in dilute alloys, dominant in non-dilute alloys</td>
</tr>
</tbody>
</table>

In general, all electronic contributions (shown in the top half of Table A-2) to thermal conductivity are dominant in good electrical conductors, while lattice contributions (shown in the bottom half of Table A-2) are dominant in poor electrical
conductors. Contributions from interactions on the right left of Table A-2 act to improve thermal conductivity by increasing the net carrier relaxation time, while those on the right act to reduce thermal conductivity by decreasing the net carrier relaxation time. Thermal carrier interactions with stationary crystal defects (shown in the left half of Table A-2) are non-negligible in materials that have a high density of defects. Of these, boundary and dislocation scattering events are generally difficult to quantify, as all the possible directions of the thermal carrier motion and all the specific shapes of these defects must be accounted for during calculation.

The electron-phonon and phonon-phonon (both Um-Klapp and Normal processes) behavior has already been discussed, however a few important points about electron-electron and phonon-electron interactions should be highlighted. Both electron-electron and phonon-electron contributions are very small. Electron-electron scattering events are rare due to Pauli’s exclusion principle, which keeps them separated. Also, the only electrons available to interact are conduction electrons, as valence electrons are hardly mobile. In addition, any scattering events that do occur, do not release much energy, as the electrons are thermodynamically restricted to the lower portion of the conduction band. Phonon-electron scattering events are quite rare as well, as electron movement does not perceptibly impact atomic movement in solids.

A.4.4.4 Matthiessen’s Rule

The electron interactions with stationary defects in crystals are grouped in the top-right portion of Table A-2. The electron scattering events do not change with
temperature and thus may be considered constant additive terms, which may be grouped together in the definition of a residual electrical resistivity

$$\rho_0 = \rho_{k\text{-boundary}} + \rho_{k\text{-dislocation}} + \rho_{k\text{-impurity}}$$  \hspace{1cm} A-47

If all the electron scattering events are assumed elastic, then their thermal resistivity contributions would follow the W-F law and all be commonly inversely proportional to temperature. They may also be grouped together in the definition of a residual thermal resistivity

$$W_0 = W_{k\text{-boundary}} + W_{k\text{-dislocation}} + W_{k\text{-impurity}}$$  \hspace{1cm} A-48

These terms may be added to the ideal electrical and thermal resistivities of Equation A-26 (or Equations A-32 through A-34) and Equation A-40 (or Equation A-42) to yield Matthiessen’s rule.

$$\rho_{\text{total}} = \frac{1}{\sigma_{\text{total}}} = \rho_i + \rho_0$$  \hspace{1cm} A-49

and

$$W_e = \frac{1}{\kappa_e} = W_i + W_0$$  \hspace{1cm} A-50

Note that the electrical resistivity portion of Matthiessen’s rule will come up again in the next chapter.

A.4.5 Predicting Thermal Conductivity of Materials

Only a full quantum mechanical calculation involving the electronic and lattice contributions of electrons and phonons, within a real crystal structure, as well as a quantum mechanical treatment of all the scattering interactions, would yield a reasonably accurate thermal conductivity in a particular temperature regime. This involves the
determination of the true non-spherically symmetric Fermi surface, the true electrical carrier density, and an accurate depiction of all the scattering events within a crystal. This is simply unrealistic to use outside the study of just a few commonly used materials, due to the difficulty involved in tailoring a solution to each material. In fact, no single formalism has ever completely described the thermal conductivity in a material as common as Iron, let alone silicon. Typically, different quantum mechanical approaches attempt, instead, to describe key mechanisms separately, to create a combined formalism.

A.4.5.1 Predicting Thermal Conductivity Trends in Low Defect Density Solids

To make thermal conductivity theory more understandable, rules of thumb must be created to help gain an understanding, such as when electronic or lattice contributions dominate and which scattering events dominate each contribution – such is the origin of Matthiessen’s rule. It is possible, in the pursuit of this, to vary parameters in basic quantum mechanical formulations, noting their behavior, rather than calculate values for each material. In this way, the thermal conductivity theory calculations may be used to track trends, rather than obtain absolute values. This is the most prolific use of thermal conductivity theory – the most common of trend to track is that of temperature. Figure A-7 shows an example of a thermal conductivity plot versus temperature of low defect density silicon.¹
Figure A-7. Plot of the thermal conductivity versus temperature of low defect density silicon.

Thermal conductivity theory is typically used to probe the behavior of defects in solids. This is done over a broad temperature range from near absolute zero to beyond the melting point. Of which, the low temperature regime is focused on intently, as this is where the defect effects are generally dominant.

A.4.5.2 Predicting Thermal Conductivity Trends in Alloys

Alloy trend calculations are treated differently than pure solids. This is typically done using quantum mechanical perturbation theory, which is easier than solving the entire quantum mechanical problem directly. Unfortunately, because it requires the variations to be small, it can only be applied to very dilute alloys of about 1% or less. Less dilute alloys require individually tailored, full quantum mechanical treatments.
A.4.5.3 Absolute Thermal Conductivity of Solids at Room Temperature

From an engineering perspective, it is important to know an absolute value for the thermal conductivity near room temperature. However, many effects are occurring at the same time in this mid-temperature regime and cannot be distinguished from one another. The result is an extremely complex theoretical depiction of thermal conductivity in materials for which there is little hope of understanding beyond empirical formulations. Common materials behave similarly, making it possible to predict behavior of new materials based on common categories, but only if materials within the same category have been well studied.

The related theory of semiconductor electronics is possible, only because of the extreme purity of investigated materials and the use of just a few well characterized material systems. Once defective materials are included in semiconductor analysis, the difficulty escalates quickly.

A.4.5.4 Estimating the Thermal Conductivity of Good Electrical Conductors

One glimmer of hope stems from the large domain of the Wiedemann-Franz law (even if only approximate). This law allows at least the electrical conductivity of electrical conductors to be accounted for. If the electrical conductivity can be measured, then the W-F law may be used to calculate an approximate electronic thermal conductivity. In low defect, good electrical conductor materials, such as metals, the electronic component is dominant and this method can yield a basic total thermal conductivity approximation.
A.4.5.5 Estimating the Thermal Conductivity of Poor Electrical Conductors

In materials that are not good electrical conductors, such as semiconductors and insulators, the electronic contribution is not dominant and this approach cannot be used. Reference 8 discusses basic estimates of the lattice contribution in solids – excluding defect effects – from Leibfried and Schlömann\textsuperscript{9}, as well as, Dugdale and MacDonald\textsuperscript{10}, which share similar form of

$$\kappa_L \approx A \left( \frac{k_B}{h} \right)^3 \frac{MV^{5/3} \theta_D^3}{\gamma^2 T}$$ \hspace{1cm} \text{(A-51)}$$

where \( A \) is a constant (equal to 3.5\textsuperscript{9} or 8\textsuperscript{10}), \( M \) is the average atomic mass of the material, \( V \) is the average atomic volume, and \( \gamma \) is the Grüneisen parameter (roughly 0.5-2 at room temperature). Another formalism is described in reference 8 after Keyes\textsuperscript{11}, that approximates the lattice thermal conductivity without the need to know the Debye temperature. This is done (which is often not known of new materials) using:

$$\kappa_L \approx \frac{BT_m^{\gamma/6} \rho^{\gamma/6}}{TM}$$ \hspace{1cm} \text{(A-52)}$$

where \( T_m \) is the melting point of the material, \( \rho \) is the density, \( M \) is the average atomic mass, and the constant \( B \) is given by

$$B = \frac{R^{\gamma/6}}{3\gamma^2 \epsilon_m^3 N_A^{\gamma/6}}$$ \hspace{1cm} \text{(A-53)}$$

where \( R \) is the universal gas constant, \( N_A \) is Avogadro’s number. \( \epsilon_m \) is a constant that represents the ratio of lattice vibration amplitude to the interatomic distance required to melt the material (~1-10%) and is roughly constant for all materials that share the same type of interatomic bonding. It should be noted that these equations are best suited to
form trends of thermal conductivity within a group of common materials rather than being used to calculate explicit lattice thermal conductivities for new materials. As a rule of thumb, values obtained in such a manner could be off by as much as a factor of ~5-10 in either direction, depending on what is known of the new material’s behavior. Another word of caution should be offered at this point: these lattice thermal conductivity estimations are meant for defect free solids only, with no allowance for defect contributions.

A.5 Conclusion

The basic thermal conduction model accurately describes the heat transfer within HMMIC systems. This conduction model also emphasizes the importance of having a solid understanding of the thermal conductivity of all materials involved.
A.6 References


Appendix B: Fabrication Procedures

B.1 Epitaxial Growth Procedure

This is the final procedure used to grow starting material for the pre-pattern bonding method. The post-pattern bonding procedure was similar.

1. Susceptor cleaning
   a. red-orange active Aqua regia bath for 20m
      i. Fresh, vigorously boiling ruby-red will deposit too much chlorine, taking longer to remove than 40m. Yellow to clear is not active enough to remove growth material within 20m
   b. DIW rinse for 40m
      i. shorter and there will be residual chlorine, longer is a waist of time
   c. N2 blown dry
   d. 180°C bake in oven to dehydrate and drive off residual chlorine

2. Reactor tube cleaning
   a. Aqua regia bath for 20m
   b. several DIW rinses
   c. N2 blown dry

3. Chamber conditioning
   a. 600s AsH3 purge/bake-out at 700°C
   b. 400s AsH3 purge cool-down to 650°C
   c. 1000s GaAs at 650°C (~325nm)
   d. 400s AsH3 purge cool-down to room temperature

4. Device growth
   a. 600s AsH3 purge/bake-out at 700°C
   b. 400s AsH3 purge cool-down to 585°C
   c. 300s GaAs buffer at 585°C (~90nm)
   d. 25s PH3 purge to remove excess As at 585°C
   e. 250s InGaP at 585°C (~130nm)
   f. 35s GaAsP at 585°C [uses up any excess In on the sample or in the susceptor]
   g. GaAsP is used because the resulting (In)GaAsP is more closely lattice matched to GaAs than either (In)GaP or (In)GaAs alone
   h. 100s GaAs at 585°C (~30nm) [to ‘seal’ the InGaP before the long heat up to 650°C]
   i. 5700s GaAs at 650°C (1850nm)
   j. 400s AsH3 purge cool-down to room temperature
B.2 Post-Pattern Bonding Procedure

The sample preparation described here was used for both post- and pre-pattern bonding.

1. Pre-bond sample preparation
   a. Si preparation
      i. cleave and clean the Si wafer into 8mm x 8mm pieces
         1. Nick the polished edge using a SiC tipped scribe on the
            cleaving vacuum chuck shown in the Apparatus Appendix
            D.1. This is done while blowing high pressure deionized
            nitrogen on the surface to whisk away as much of the
            nicked off crystal dust as possible.
         2. Press on the reverse side of the wafer (with the polished
            side down, facing a set of Alphawipe cloths) above the
            nicked mark to cleave.
         3. BOE dip for 30s to 1m, then rinse with deionized water
         4. Dip in ultrasonic bath two times with three changes of
            water after each
      ii. mount on pinching evaporation mount in Apparatus Appendix D.4
   b. GaAs preparation
      i. same preparation as with Si except cleaved into (1cm)^2 pieces
      ii. the GaAs substrates are grown with an InGaP etchstop and a
          highly doped n or p-type epilayer. [see procedure appendix B.1]
      iii. the sample is then mounted on a tabbed mount similar to that
           shown in Apparatus Appendix D.4
   c. Bondmetal evaporation [see Apparatus Appendix D.3]
      i. 50Å Pd on GaAs
      ii. 2000Å Pd on Si
      iii. 8500Å In on GaAs
      iv. 50Å Pd on GaAs
   d. Sample dismounting [see Apparatus Appendix D.4]
      i. GaAs is removed from its mounting clamps via the hooked tool

Figure B.2-1. Illustration of post-pattern process: Si and GaAs sample preparation.
2. Bonding
   a. Bonding [see Apparatus Appendix D.5]
      i. Si half is placed on keyhole tray (being sure to touch only the bottom or corners of the sample)
      ii. Si half is vacuumed to conventional handheld vacuum tweezers
      iii. GaAs half is placed on transfer plate
      iv. samples are oriented to one another by hand and pressed into contact by hand

   b. Annealing [see Apparatus Appendix D.6]
      i. the sample is removed from its transfer plate via the pin plate
      ii. the sample can then be transferred to the graphite heater using the transfer tool
      iii. the sample is registered with the pressure plate
      iv. the pressure plate is pressed onto the sample with a force of about 1kg
      v. the carboy is put in place
      vi. the annealer is purged with forming gas for 15m to flush out water vapor
      vii. the sample is then heated to 170°C for 2hrs
      viii. after 2hrs the forming gas is turned off, the heater turned off, and is the sample allowed to cool
      ix. the carboy is removed once the sample has cooled to room temperature and the pressure released
3. Post-bond fabrication
   a. Peripheral wax wetting
   b. Substrate etching [the jet etcher had not been created by this time]
      i. etchant \( S \equiv (\text{H}_2\text{SO}_4:\text{H}_2\text{O}_2:\text{H}_2\text{O} - 3\text{mL}:30\text{mL}:3\text{mL}) \) is used first to etch the substrate. The sample is periodically removed from the etchant every 20m and rinsed with DI water to measure its etch progress using a digital caliper. The sample is then dipped in a 5% HF and water solution to remove any oxide and etching is resumed. This procedure is continued until the etchant first reaches the etchstop (breakthrough) [this will happen in the corners first].
      ii. the sample is removed from \( S \) and rinsed with DI water and another 5%HF with water dip is performed. The sample is then placed in etchant \( C \equiv (\text{Anhydrous Citric Acid:}\text{H}_2\text{O:}\text{H}_2\text{O}_2 - 7.5\text{g:7.5mL:1mL}) \) until the etching has completed.
   c. Etchstop etching
      i. undiluted hydrous Hydrochloric acid (HCl) is used to etch off the etchstop for about 5s or until the etchant stops bubbling
      ii. the sample is immediately rinsed in water to prevent the HCl from etching the bondmetal
      iii. wax removal

Figure B.2-4. Illustration of post-pattern process: Si and GaAs annealing.

Figure B.2-5. Illustration of post-pattern process: GaAs substrate etching.

Figure B.2-6. Illustration of post-pattern process: after InGaP etchstop etching.
d. Backside contact and ohmic contact annealing
   i. the backside of the Si substrate is evaporated with 2000Å of Pd
   ii. both backside and bond interface are annealed to 600°C in 15%FG with a GaAs cover sample to form ohmic contacts

![Figure B.2-7. Illustration of post-pattern process: high temperature ohmic contact metallization and annealing.](image)

[e. Contact disk window patterning](#)
   i. GaAs epilayer samples are patterned using PR, while bulk GaAs samples use a simple shadow mask [see Apparatus Appendix D.4]
   ii. spin NR9-3000PY at 4000RPM for 40s
   iii. bake on a hotplate at 150°C for 1m
   iv. expose dark-field circular disks mask for 15s [the disks are unremarkable in appearance and their illustration is not required]
   v. bake on hotplate at 100°C for 1m
   vi. develop in RD6 for 15s

![Figure B.2-8. Illustration of post-pattern process: GaAs topside contact metallization.](image)

[f. Topside ohmic contact metal evaporation](#)
   i. an appropriate low contact resistivity metallization is evaporated on either the n or p-type GaAs bonded epilayer
   ii. the metallization is then capped with a thick 2000Å of Ni to act as an ion mill mask
   iii. liftoff the unwanted metal with an acetone soak

[g. Mesa definition](#)
   i. the sample is then placed in an Ar ion mill to define the mesas
   ii. the ion milling was performed in bursts 1m long (to reduce heating) and periodically checked for milling rate. The milling was stopped just after the field bondmetal was removed exposing the Si substrate
Figure B.2-9. Illustration of post-pattern process: after GaAs mesa definition.

h. Topside ohmic contact annealing
   i. the topside contacts are annealed appropriately to complete the ohmic contact fabrication
B.3 Pre-Pattern Bonding Procedure

Many of the pre-pattern bonding procedure steps are similar to the post-pattern bonding procedure, but are repeated here for clarity.

1. Pre-bond device fabrication
   a. GaAs and Si samples are prepared as they were in the post-pattern bonding procedure, except the GaAs epilayer is left undoped.
   b. Mesa patterning
      i. spin NR7-1500PY at 5000RPM for 40s
      ii. bake on hotplate 150°C for 60s
      iii. expose DF-MESA_0 for 15s [see Apparatus Appendix D.2] (centering the pattern on the sample as much as possible as well as avoiding as many growth defects as possible)
         1. using MJB3 aligner with LP filter
         2. intensity set to 2.0 mW/cm² at 320nm (or 0.60 mW/cm² at 365nm)
      iv. bake on hotplate 100°C for 60s to reveal the DF-MESA_0 (device mesas) pattern
      v. repeat iii and iv with the DF-PMGIPAD_-9 pattern (to create the standoff mesas) being sure not to overlap the device mesas
      vi. develop in RD6 for 12s (do not agitate or PR film will delaminate)
      vii. rinse in flowing DIW for 20-30s
   c. O₂ + CF₄ descum in Trion ICP-RIE dry etcher for 15s (this removes any PR residue that may remain in the field area) using 50W RIE, 50sccm O₂ (setpoint 53), 2sccm CF₄ (setpoint 3), 50mT pressure, 40°C temperature, followed by a DIW rinse to remove any remaining etch residues (the additional CF₄ more completely removes the PR residue than does O₂ alone and does not damage the GaAs)
      
   ![Figure B.3-1. Illustration of pre-pattern process: after GaAs mesa photoresist definition and SEM cross sectional picture of the same.](image)

   d. Dry etch
      i. condition Trion for 15’ of continuous 300W ICP, 100W RIE etching as below
ii. Trion recipe A: 30s on, 2m off using 300W ICP, 100W RIE, 20sccm (setpoint 21) BCl$_3$, 10mT (setpoint 8) pressure, 15°C temperature

iii. 100W RIE yields straighter sidewalls than 50W RIE, but is not very selective to InGaP

iv. test etch thickness using test sample
   1. 5-7nm/min (when using fully anodized plate, rate can be ½ this amount when anodized coating is worn through [The lack of anodized coating means that some of the etchants are used up in reactions with the plate’s exposed Al])

v. repeat above until 0.25-0.5um away from etchstop, then switch to recipe B (to improve selectivity): 30s on, 2m off using 100W ICP, 50W RIE, 20sccm (setpoint 21) BCl$_3$, 8mT (setpoint 7) pressure, 15°C temperature
   1. continue checking the etch rate with the test sample (the etch rate of recipe B is about 50% less than A)

vi. repeat recipe B until you no longer see the GaAs substrate coloration in the field region of the sample (fillets of connecting GaAs epi may exist in several places: this is due to etch products leaving behind a liquid material that cannot be removed with recipe C.)

![Figure B.3-2. Illustration of pre-pattern process: after GaAs mesa definition and SEM cross sectional picture of the same.](image)

e. PR removal
   i. acetone rinse several times with ultrasonics until no ‘strands’ of PR residue remain
   ii. O$_2$+CF$_4$ plasma off residue for 5’, followed by DIW rinse
   iii. BOE dip and DIW rinse to remove any remaining residue
   iv. water ultrasonicate 2x to remove any particle contamination caused by BOE or any other source
2. Pre-bond sample preparation
   a. PMGI field patterning
      i. Bake samples at 200°C for 5m prior to applying PMGI resin (This dries off the sample surface and prepares it for PMGI deposition. Immediately apply the resin once on the spinner. Allowing the sample to cool down creates unwanted air gaps in the PMGI fillet regions. [Various experiments with spinning cyclopentanone first to fill the fillets without air gaps never worked as well as this procedure. This solvent pre-spin technique is typically used to help PR fill small vias.])
      ii. Spin dilute PMGI SF-13 (diluted in more of its native solvent cyclopentanone down to a viscosity of SF-9 [the required PMGI formulation was not available at the time]. The SF-# is actually the % of solid PMGI dissolved in cyclopentanone.) at 5500RPM for 45s (this speed has been optimized to yield a 0.5um layer of PMGI in the field region of the sample.)
      iii. Bake on hotplate 200°C for 5m (let cool 1m)
      iv. Spin S1827 on top of the PMGI at 5000RPM for 40s
      v. Bake on hotplate 115°C for 2m (this is about twice as long as a typical bake, the added time helps maintain the PR pattern during the longer developing time required for the PMGI)
      vi. Expose DF-PMGIPAD_-9 for 90s on the device mesa pads, DF-PMGIPAD_-9 for 90s on the standoff mesas using MJB3
aligner without LP filter (The goal is to create PR openings that are slightly wider than the mesas to allow the developer to remove the PMGI both on top of the mesas as well as part of the PMGI fillets.)

1. intensity set (with LP filter still engaged) to 2.0 mW/cm$^2$ at 320nm or 0.6 mW/cm$^2$ at 365nm

vii. develop the PR/PMGI stack in MF-321 for 150s, taking it out periodically and rinsing in DIW to inspect the progress. (MF-321 is the most dilute commercial version of the TMAH based developers. PR failure will occur if a MIB (metal ion bearing) NaOH based developer like 354 is used.)

viii. Once the PMGI is satisfactorily removed, strip the PR in acetone and propanol [Because the PR has only ever been in developer and

![Figure B.3-5. Illustration of pre-pattern process: after photoresist dissolution and microscope picture of the same.](image1)

![Figure B.3-6. Illustration of pre-pattern process: after PMGI/photoresist dissolution and photoresist removal and microscope picture of the same.](image2)
not exposed to a plasma treatment, the acetone and propanol rinses
will not leave any PR residue behind.], then post-bake/reflow the
PMGI on a hotplate at 280°C for 5m (this refloows the field PMGI
and re-fillets the mesa sidewalls without extending overttop of the
mesa, it also removes all of the solvent and readies it for the bond
anneal)

Figure B.3-7. Illustration of pre-pattern process: after PMGI reflow and microscope picture of the same.

ix. Finally the PMGI coated samples must be prepped for the
bondmetal evaporation with another O\textsubscript{2}+CF\textsubscript{4} etch to remove any
residue followed by a DIW rinse. [This replaces a BOE step that
occasionally lifted off the PMGI.]

b. Ti standoff fabrication
   i. Spin NR9-3000PY at 7000RPM for 40s
   ii. bake on hotplate 150°C for 60s
   iii. expose LF-HEATPAD_-7 for 13-15s using MJB3 aligner with LP
        filter
       1. intensity set to 2.0 mW/cm\textsuperscript{2} at 320nm or 0.60 mW/cm\textsuperscript{2} at
            365nm
   iv. bake on hotplate 100°C for 60s
   v. develop in RD6 for 11-12s
   vi. e-beam deposit 1000Å of Ti capped with 50Å of Ni [Without the
       Ni capping layer the bondmetal window PR tended to stick to the
       Ti surface.]
   vii. liftoff PR in acetone, rinse with propanol and DIW

Figure B.3-8. Illustration of pre-pattern process: after Titanium standoff photoresist definition and
metallization and microscope picture of the same.
c. Bondmetal window patternning
   i. spin NR9-3000PY at 6000RPM for 40s [NR7-1500PY at 3600RPM for 40s was required before the PMGI process was implemented.] (This speed was optimized to yield PR thick enough to allow the bondmetal to be deposited, yet thin enough to be below the point at which the PR would crack and peel away. This cracking and pealing was caused by cooling to LN2 temperature. This does not occur when NR9-3000PY is used on the PMGI.)
   ii. bake on hotplate 150°C for 60s
   iii. expose LF-BOND_-2_g for 13-15s using MJB3 aligner with LP filter (the _g allows the alignment T mesas to bond to the Si)
      1. intensity set to 2.0 mW/cm^2 at 320nm or 0.60 mW/cm^2 at 365nm
   iv. bake on hotplate 100°C for 60s
   v. develop in RD6 for 11-12s
   vi. O_2 descum in Trion using 50W RIE, 50sccm O_2, 50mT pressure, 40°C temperature for 15s, followed by a DIW rinse [The addition of CF_4 could have affected the bondmetal and was omitted. Without this step the alloyed bondmetal shows an ominous texture indicating that the bond alloy was affected by PR residue.]
   vii. mount on Cu evaporation mount [see Apparatus Appendix D.4. The sample must be held down on either side – holding it down on just one side does not adequately thermally couple the sample to the mount.]

d. Bondmetal evaporation [see Apparatus Appendix D.3] The discrepancy between the thicknesses is due to the different distances to the crystal monitor and sample from the source metal. The bag is used in conjunction with the Cu fin assembly to getter as much of the remaining water vapor as possible out of the chamber ambient preventing it from condensing on the sample surface where it would create bubbles of trapped water under the deposited metal. Once the residual water vapor is condensed (indicated by the saturation of the vacuum pressure down to ~2x10^-7 Torr), the sample can be safely brought down to LN2 temperature for evaporation by removing the bag and pouring LN2 directly into the Dewar. The pressure will lower further to ~9x10^-8 Torr once LN2 temperature is reached.]
   i. 50Å Ti on GaAs
   ii. 200Å Pd on GaAs
   iii. 1000Å Pd on Si
   iv. melt/degas the In before cooling down [The cool down process also pumps the chamber pressure down. If the In were not degassed prior then the outgassing would deposit water on the sample.]
v. cool down
vi. LN2 in bag to getter water
vii. LN2 in Dewar to lower GaAs temperature
viii. 4000Å In on GaAs
ix. 40Å Pd on GaAs [this layer prevents oxidation of the In]
e. Sample dismounting [see Apparatus Appendix D.4]
i. the GaAs sample is removed from its mounting clamps via the hooked tool
ii. Si is removed from its mounting chuck via the pedestal and fork tools (requiring only backside sample contact)
f. Photoresist removal
i. acetone liftoff of unwanted metal
   1. takes about 10m-20m to completely release (agitation is provided by jetting acetone with a pipette)
   2. peeled strips of metal are removed in solution by pipette
   3. ultrasonic agitation is avoided as it sometimes peels the PMGI off (side note: the ultrasonic agitation has never peeled the bondmetal off)
ii. follow-up with propanol rinses and DIW rinses to remove acetone residue
iii. O₂ descum and DIW rinse to remove PR residue

Figure B.3-9. Illustration of pre-pattern process: after bondmetal deposition and photoresist liftoff and microscope picture of the same.

3. Bonding
   a. Bonding [see Apparatus Appendix D.5]
      i. Si sample is placed on keyhole tray (being sure to touch only the bottom or corners of the sample) [Use conductive plastic tweezers for all manipulation of samples as the non-conductive Teflon tweezers impart static charge to the samples making them come apart after bonding. This is also the reason for the all metal tools and carrier.]
      ii. Si sample if vacuumed to bonder
      iii. GaAs sample is placed on transfer plate
      iv. samples are oriented to one another and lowered into contact
      v. vacuum source is turned off and replaced with compressed air (the air helps release the sample from the bonder)
b. Annealing [see Apparatus Appendix D.6]
   i. the annealing furnace is heated to 200°C to drive off any moisture in the susceptor, this is evacuated by repeatedly pump and purging the FG, then the system is then allowed to cool to 65°C while the sample is prepared
   ii. the sample is removed from its transfer plate via the pin plate
   iii. the sample can then be transferred to the graphite heater using the transfer tool
   iv. the sample is then registered with the pressure plate, the carboy is put in place, the pressure plate is lowered onto the sample with chains slack (to hold the sample pair motionless during the pumping and purging cycles), and the annealer is pumped/purged with forming gas several times to ensure that the entire bond surface is purged of air (Remaining air leads to oxidation affecting bond quality.)
   v. the sample is then heated to 120°C [the susceptor temperature was carefully calibrated to an accuracy of ±1°C]
   vi. the pressure plate then applies 1kg of uniaxial force and the temperature is increased further to 180°C for 3hrs [3hrs at 180°C ensures that the bond has fully alloyed]
   vii. after 3hrs the forming gas is turned off and the carboy removed

c. wax wetting [see Apparatus Appendix D.7]
   i. while the annealer is at 180°C the sample is slid onto a piece of Al foil to catch any stray wax
   ii. four 1mm$^3$ pieces of polypropylene are melted
iii. two 1mm$^3$ pieces of the mix-wax are applied to either of the ends of the sample on the GaAs ledge and allowed to wet across the front face and underfill the bonded pair’s void

iv. 1hr assures that the wax has wet across the entire sample (tests show that it typically completes in about 30m)

v. after the wax has finished wetting, W wax is used to build up fillets along the entire periphery of the sample.

vi. the sample is cooled to ~120°C and 3 dots of W wax are placed on the Si backside (already facing up)

vii. the etching mount is centered on the sample and the dots bond to the mount

viii. the annealer is allowed to cool to room temperature at its own natural rate

---

4. Post-bond fabrication
   a. Substrate etching [see Apparatus Appendix D.8]
      i. etchant $S \equiv (\text{H}_2\text{SO}_4:\text{H}_2\text{O}_2:\text{H}_2\text{O} – 3\text{mL}:30\text{mL}:3\text{mL})$ is used first to etch the substrate. The jet-etcher maintains a constant etch rate of about 6.2um/min until the etchant first reaches the etchstop (breakthrough) [this will happen in the corners first]

      1. because the etch rate is predictable with the jet-etcher there is no need to periodically remove it from the etchant and it can remain there until it first breaks through (not having to remove the sample and test it periodically significantly reduces the etching time)

      ii. the sample is removed from the jet etcher, quickly rinsed in deionized water, and immediately dipped in a 5% HF in water solution to clean off any chemical residue and oxide, then thoroughly rinsed in water

---

Figure B.3-12. Illustration of pre-pattern process: after sample pair wax wetting.

Figure B.3-13. Illustration of pre-pattern process: after GaAs substrate S-etchant etch-thinning.
iii. To make up for the slight bulge that occurs at the center of the sample due to its small size, tiny droplets of etchant S are deposited at the center of the remaining GaAs substrate bulge until it breaks through around the edges. The etchant is again DIW rinsed and HF dipped. This process is repeated until the bulge is satisfactorily reduced. [This speeds up the C etching process and more uniformly distributes the time any exposed etchstop region is in contact with etchant D.]

![Illustration of pre-pattern process: after GaAs substrate etch S-etchant touch-up and composite microscope picture of the same.](image)

iv. Without delay the sample is then placed in etchant C ≡ (Anhydrous Citric Acid:H\textsubscript{2}O:H\textsubscript{2}O\textsubscript{2} – 7.5g: 7.5mL:1mL) and allowed to completely remove the remaining GaAs substrate. Etchant C etches at approximately 0.3um/min. After which it is thoroughly rinsed in DIW.
b. Etchstop etching [This is performed as soon as the C etching is complete, otherwise festered C etchant will creep over time and end up destroying the GaAs mesas. If performed in time and the wax and PMGI are also removed right away then the C etchant will have no place to hide.]
   i. undiluted HCl vapor is used to etch off the etchstop (this should only take about 20-22s, if the sample is placed in the liquid HCl etchant the etching is too fast and can potentially undercut the bondmetal where unprotected)
   ii. the sample is immediately rinsed in water to stop the HCl vapor from etching further
c. PMGI and wax removal [This is performed immediately after HCl etching to reduce the chance of C etchant attack. Remaining wax residue used to adversely affect the Ni heater photolithography step, but with proper cleaning procedures and the use of Shipley positive PR with chlorobenzene treatment and using a process temperature below the melting point of the wax instead of Futurrex negative PR (who’s primary solvent was cyclohexanone: which attacks the wax residue) this problem can be averted.]

i. The PMGI is removed in 1165 PR stripper at 80°C for 20m

ii. The wax is dissolved with the addition of TCE to the 1165. This soaks for 5m then is rinsed several times in TCE to be certain the wax is removed.

iii. The sample is then rinsed in chlorobenzene to be certain there will be no reaction with any residual wax during the Ni patterning process.

iv. This is followed up by acetone, methanol, and propanol rinses before being N₂ dried

v. Any remaining residue is removed using an O₂ plasma treatment for 5m
d. Heater window patterning
   i. spin S1818 at 6000RPM [The ethyl acetate based solvent in the S1800 series resist does not attack the wax if any residue remained. This is in stark contrast to the Futurrex resist that uses cyclohexanone as its solvent, which after only a few seconds of exposure dissolved wax residue affecting PR development.]
   ii. bake on a hotplate at 60°C for 5m (this is well below the recommended bake temperature of S1800 series resists ~115°C, but is sufficiently long to remove enough solvent.)
   iii. expose DF-HEAT-2,4 for 30s [since the pattern is smaller than the mesas the DF obscures the mesas, so the bonded T mesas are used to align the pattern]
   iv. soak in chlorobenzene for 1m (This hardens the top layer of PR. The timing of which is critical; too long and the overhang will be too vertical, too short and it won’t form a substantial enough overhang to aid liftoff) [Many other solvents that were claimed to create the same ‘crusting’ of the PR were tested. They were tested because chlorobenzene readily dissolves the mix-wax. But these other solvents attacked the wax even faster.]
   v. develop in MF-321 for 1-2m (this is longer than what is typical because the chlorobenzene slows the development rate)
e. Heater metal evaporation
   i. evaporate 1000Å of Ni
   ii. liftoff the unwanted Ni with an acetone soak [acetone was tested not to dissolve the mix-wax at all, even after prolonged exposure, so there was no chance of wax residue redepositing on top of the Ni heaters.]

f. RF signal line pattern definition
   i. Optionally pattern the RF pads using the same chlorobenzene soaked S1818 PR procedure used for the heater patterning [Although the existing Ni heaters were used for testing purposes].
Appendix C: Measurement Procedures

C.1 Bond Interface Electrical Measurement Procedures

This measurement appendix section presents both the bond interface electrical characterization and specific contact resistivity measurement procedures.

1. Bond interface electrical behavior measurement
   a. After the doped bulk post-pattern bonded samples had been thinned, 2000Å of Pd was evaporated onto the Si backside.
   b. The sample was then annealed to 600°C to form the bond and backside ohmic contacts.
   c. Next traditional GaAs topside contacts were evaporated using a metal shadow mask.
   d. The GaAs topside contacts were annealed to form ohmic contacts. [These temperatures were considerably lower than the 600°C used to form the bond and backside ohmic contacts. Topside contact ohmic behavior was verified via pad-to-pad I-V characterization.]
   e. Current was passed vertically through the structure from topside to backside contacts using 4155 sweep measurements [see Apparatus Appendix D.10]. Several of the contact pads’ I-V characteristics were measured to verify the ohmic behavior of the bond interface.

2. Bond interface specific contact resistivity measurement
   a. After the doped epilayer post-pattern bonded samples had been etch-thinned to remove the GaAs substrate and etchstop, 2000Å of Pd was evaporated onto the Si’s backside and annealed to 600°D. Bulk doped GaAs reference samples were evaporated with typical ohmic contact metallizations and annealed for later use.
   b. From there the samples were fabricated into mesas using the post-pattern post-bond procedure described in the post-pattern bonding procedure appendix. Identical topside contacts were fabricated on the GaAs reference samples and annealed along with the bonded samples.
   c. After the structures were completed and the topside contacts annealed, the samples were placed on the backside Kelvin connector mount [see Apparatus Appendix D.10].
   d. Next two finely pointed probes were placed on each topside contact pad to provide a topside Kelvin connection.
   e. The HP4155 was used to pass current through the sample from one of the backside contacts to one of the topside contacts using a sweep measurement while the other two leads were used to record the pad
voltages. The total resistances of several devices were measured in this way. The GaAs reference samples were measured concurrently.
f. The GaAs epilayer resistance values for each bonded device mesa were calculated based on previous Van der Pauw resistivity measurements and their influence subtracted from the total bond resistances to yield bonded device residual resistances. [The resistance of this layer’s effect on the entire measurement is rather minimal.]
g. The residual resistances of the bonded samples were plotted versus the inverse of their contact area and the slope extracted to obtain the contact resistivity. This process was repeated with the GaAs reference samples.
h. The specific contact resistivity of the bond interface was found by subtracting the GaAs reference sample contact resistivities from the bonded sample values. (Alternately the GaAs reference sample’s resistivities could be used to calculate the expected bonded device topside contact resistances and subtracted from the total bond resistance values before plotting them.)
C.2 Bond Interface Thermal Conductivity Measurement Procedure

This measurement appendix section presents the bond interface thermal conductivity measurement procedure.

1. Measurement
   i. Si reference sample
      1. Cleave and clean an 8mm x 8mm piece of Si that matches the material used for bonding. Use the same method as described in the post-pattern bonding procedure appendix.
      2. Deposit 100nm of SiOx on Si via PECVD
      3. Measure the thickness using an ellipsometer.
      4. Pattern heater structure using the same process described in the pre-pattern bonding procedure appendix
      5. Deposit 100nm of Ni onto the sample and lift off the photoresist to reveal the Ni heater structure. (This does not need to match the thickness of the bonded sample exactly.)
   ii. calibrating the temperature stage
      1. use the resistance vs temperature chart of the 0.1°C accuracy thermistor (provided by the manufacturer) to calibrate the 1°C accuracy thermistor that controls the thermoelectric controller (0.1°C accuracy thermistor was temporarily only available in 2.5kOhm resistance, temperature controller requires 10kOhm resistance to achieve maximum control resolution)
   iii. mounting
      1. place sample on the Cu temperature stage with a small (2-3 mm³) bead of thermal paste (an AlN particle suspension called ‘Cool-Grease CGR7018’). (Higher thermal conductivity interface materials were not immediately available.)
      2. press down on the sample to squeeze as much of the paste out as possible
   iv. device break-in (next few steps are performed for each DUT without removing the probes; this allows high precision measurements to be made. A shroud is placed over the test setup to prevent room air currents from disturbing the measurement. A 25°C reference temperature is used for these measurements; however this is only valid if the room environment does not exceed this. A room warmer than the reference temperature will influence the measurement.)
1. use the HP4155C (with extender box) to measure the resistance of the DUT at roughly 25°C using a probing sweep of -100uA to +100uA
2. measure the resistance again at roughly 80°C
3. From these two data points estimate the heater resistance at 80°C
4. While the Cu heating stage is maintained at 25°C estimate by trial and error the maximum current for the heater not to exceed 80°C
5. apply that current until the heater’s resistance settles to a constant value (The value will theoretically never reach a constant value; an approximately steady state condition varying by less than 250ppm/min is adequate. This should take about 30-45m.)

v. Joule heating measurements
1. With the probes still contacting the sample and the Cu temperature stage maintained at 25°C, estimate by trial and error a current that will heat the DUT to about 75°C, call it I(75°C) (this will provide ample range for a high resolution measurement)
2. perform ‘sampling’ measurements of the resistance at several different currents (both positive and negative) that extend from I(75°C) to zero. These will require several minutes each to settle. (Using a parabolic heating current distribution will result in a more evenly spaced series of measurements than a linear distribution. This is due to the fact that the resistance value varies slowly with temperature while the joule heating power varies as a square of the applied current.)
   a. The noise in the resistance measurements are above the resolution limit of the semiconductor parameter analyzer, but with proper averaging the precision of each resistance measurement can be typically on the order of 50ppm.
3. Calculate the input power via joule heating by $P=I^2R$ for each temperature, and note the resistance

vi. Temperature calibration measurements
1. This section will measure the T(R) by selecting several stage temperatures and measuring the DUT’s resistance
2. With the probes still attached to the DUT and the stage raised to a series of temperatures perform low power (-100uA to +100uA) sweep measurements of the resistance at each test point (the temperature stage will require a few minutes to stabilize for each measurement)
3. Extract an empirical formula of T(R) from the resistance data

vii. Thermal resistance extraction
1. Use the T(R) formula to calculate a value named Tj from the resistance data measured during the joule heating procedure
2. Calculate an empirical formula by plotting the Tj measurement vs. input power results from the joule heating measurements
3. The slope of this formula at 25°C will indicate the thermal resistance. [The slight bow in the plotted data is due solely to the temperature dependence of the thermal conductivity. The influence of this effect approaches zero as the sample temperature approaches ambient.]

viii. Si spreading thermal resistance extraction
1. Using a parallel plate approximation for the SiOx layer between the heater and the Si substrate calculate the theoretical SiOx thermal resistance. Alternately, the entire test may be preformed with multiple thicknesses of insulator to extract its contribution.
2. Subtracting this thermal resistance from the measured total will resolve the Si spreading thermal resistance Rs. [This Si spreading thermal resistance will actually include influences from the thermal grease as well as Cu heater stage.]

j. Measure bonded sample
i. Measure the total thermal resistance of several of the bonded structures following the same method as used for the Si test sample. (Be sure to use structures at similar distances from the sample edges as tested in the Si test sample.)

2. Bond thermal conductivity extraction
a. Extract an empirical formula that relates each of the test sample structure’s Rs values to their heater dimensions Rs(dim).
b. Determine the bonded GaAs mesa thermal resistance contribution R_{GaAs} via a parallel plate approximation similar to that used in determining the insulator contribution on the Si test sample.
c. Subtract these Rs(dim) and R_{GaAs} contributions from the total measured thermal resistance of the bonded structures to reveal the bond thermal resistance contribution R_{bond}.
d. Use the same parallel plate approximation technique to extract the bond thermal conductivity k_{bond} from this residual thermal resistance R_{bond} and the measured bond thickness.
C.3 Bonded Device Microwave Measurement Procedure

This measurement appendix section presents the bonded device microwave characterization procedure.

1. Perform full 2 port calibration on HP8510 [see Apparatus Appendix D.11]
   a. Use 0dBm source power [too much will harm the calibration substrate load resistors]

2. Measure scattering parameters S11, S22, S21, S12
   a. Assuming the device is symmetric, S11 should be identical to S22, and S21 should be identical to S12

3. Extract circuit parameters loss, index, and impedance [see source code appendix E.2]
D.1 Sample Cleaving Setup

This apparatus appendix section describes the apparatus used to cleave samples from full wafers into bondable die.

1. Cleave Nicking Setup
   a. the vacuum chuck holds the sample steady during hand cleave nicking
   b. the deionized nitrogen blows away much of the cleaved dust
D.2 Bond Mask Patterns

This apparatus appendix section presents the pre-pattern bonding mask patterns. The post-pattern bond interface contact resistivity mask pattern consisted merely of different sized disk shapes and is omitted.

![Figure D.2-1. Contracted illustration of previous revision mask pattern.](image)

2. Previous Revision Mask Pattern
   a. Note the many crevasses that can harbor wax voids [see Apparatus Appendix D.7].
   b. The voltage taps do not reach the extent of the heater and therefore cannot resolve all of the heater’s temperature.
3. Latest Revision Mask Pattern
   a. Note the streamlined pattern to avoid wax void creation.
   b. The more rigidly connected contact pads deter bonded epilayer fractures.
   c. The variety of structure widths allow for more accurate property characterization.
   d. The patterns can universally provide both thermal and microwave measurements to be performed.
   e. The voltage taps of the heater are at the ends of the heater to resolve a bigger portion of the heater’s temperature.
4. Mask Pattern Cell Designations
   a. Several versions of the general shape shown in Figure D.2-2 produce a very flexible pattern design. Each version is created with a specific dilation or contraction radius to suit the needs of a wide variety of possible situations.

   b. Patterns used are highlighted in Figure D.2-3
      i. DF-MESA_0
      ii. DF-PMGI_+1
      iii. DF-PMGIPAD_-9
      iv. LF-BOND_-2_g
      v. DF-HEAT_-2.4
      vi. LF-HEATPAD_-7
      vii. General designation: FF-XXXX_NN_G (i.e.: LF-BOND_-2_g)
      viii. FF = DF, LF
           1. designates whether the pattern is Dark Field or Light Field
      ix. XXXX = MESA, PMGI, etc.
           1. designates the label corresponding to the function each pattern was originally designed for
      x. NN = -9, -2, -1, 0, +1, +1.5 etc.
           1. designates the dilation radius in micrometers of the pattern with respect to the MESA layer (+ denotes dilation, - denotes constriction)
     xi. G = null, g
           1. designates whether the pattern had the outer guide structures or not
           2. these were originally designed to remove the wax edge effect but did not work as designed
D.3 Low-temperature Evaporation Assembly

This apparatus appendix section describes the various parts of the evaporation assembly.

Figure D.3-1. Illustration of low-temperature evaporation setup.
1. low-temperature evaporation setup parts
   a. sample and mount
   b. cold finger, Dewar, and fin assembly
   c. sample carousel
   d. source
   e. crystal thickness monitor

* Note the difference between the source-to-sample heights as compared to the source-to-crystal monitor height. The thickness at a given distance from the source goes – as any radiating phenomenon from a point source would – as the inverse square of the distance (due to the surface area of the spherical shell surrounding the source). As an example if the ratio in distance for two items in the evaporation field were $d_1:d_2$ their thickness ratio would be $t_1/t_2 = d_1^{-2}/d_2^{-2} = d_2^2/d_1^2$. 

Figure D.3-2. Picture of low-temperature evaporation setup.
2. cold finger parts
   a. sample
   b. sample mount [see Apparatus Appendix D.4]
   c. Dewar and cold finger
      i. where sample mount attaches
   d. thermocouple and temperature gauge
      i. k-type TC gauge measures temperature down to -190°C (just 6°C away from LN2 boiling point)
   e. fin assembly
      i. Cu fins that increase surface area for water vapor collection in vacuum
   f. thin plastic bag
      i. to hold LN2 in fin assembly region of Dewar to freeze water vapor onto fin assembly before getting the cold finger cold, thus reducing water condensation on the sample surface
3. Molybdenum Source Boat for indium
   a. Boat rests on the e-beam evaporator’s hearth ledge restricting the heat from escaping the boat, thus allowing its temperature to be uniform
D.4  Evaporation Sample Mounting Tools

This apparatus appendix section describes the various tools used during evaporation preparation.

1. Low-Temperature Pronged Copper Sample Mount
   a. vice prongs affix sample to mount near their edges

2. Hooked Tweezers
   a. this tool lifts the vice prongs or releases the sample clamps efficiently with a low chance of operator slip

Figure D.4-1. Picture of low-temperature pronged copper sample mount and hooked tweezers.

Figure D.4-2. Picture of silicon pinching sample mount, extraction tool, and fork tool.
3. silicon Pinching Sample Mount
   a. wire clamps grip the sample like a vise – touching only their sides
      (adhesives may leave a residue and are prone to failure if the sample
      becomes too hot during evaporation)
   b. extraction holes are used to remove the samples touching only their
      backside
4. silicon Pedestal Extraction Tool
   a. used to extract Si samples via extraction holes in mount by touching only
      sample backside
5. Fork Tool
   a. pick and place tool that touches only the sample’s backside

![Figure D.4-3. Picture of evaporation shadow mask.](image)

6. Metal Shadow Mask
   a. used to evaporate large contacts onto bulk material
   b. the sample is affixed to the top of the shadow mask facing down
D.5 Bonding Tools

This apparatus appendix section describes the various tools used during bonding.

1. Vacuum Chuck Bonder
   a. simple apparatus that allows user to bond small samples remotely without applying undesirable shear forces
   b. description of parts
      i. Si sample mount assembly
         1. chain-link suspended sample mount
            a. gently places Si sample onto GaAs sample eliminating excessive shear force
         2. vacuum chuck
            a. holds Si sample up-side-down during alignment
      ii. positioning assembly
         1. lowering crane
            a. linear stage
            b. guide wire
i. isolates any unwanted stage movement from lever arm

2. rotation and x-y stages to align Si sample with GaAs sample

2. Keyhole Tray
   a. allows user to pickup sample directly from backside using vacuum chuck bonder

3. Metal Transfer and Pin Plates
   a. transfer plate and matching pin plate allow user to relocate sample by only touching sample’s backside

4. Transfer Fork
   a. used to pick and place sample from pin plate to bond annealer touching only the sample’s backside

5. Metal Carrier
   a. just a dust cover for transfer plate to transport and store sample
D.6 Bond Annealer

This apparatus appendix section describes two revisions of the bond annealer setup.

Figure D.6-1. Picture of previous revision bond annealer assembly.

1. Previous Revision Bond Annealer Assembly
   a. used during post-pattern bonding investigation
   b. very clumsy to operate
   c. could only apply pressure or remove pressure when cold (and not remotely)
   d. difficult pressure adjustment
   e. many samples at once (designed as a time saver, but turned out not to be very useful during investigation and difficult to keep multiple samples aligned at once)

2. Description of parts
   a. heater assembly
      i. polished graphite susceptor
      ii. thermocouple
      iii. temperature controller
   b. sample
   c. pressure applicator assembly
      i. spring plate
      ii. spring plate locking arms
3. Latest Revision Bond Annealer Assembly
   a. used during pre-pattern bonding investigation
   b. capable of being raised and lowered remotely (to allow pressure to be
      applied and removed at any temperature and from outside the chamber
      environment)
   c. easy to operate
   d. easily adjustable pressure
   e. only one sample at a time (serial sample throughput was tolerable during
      investigation)

4. Description of parts
   a. heater assembly
   b. sample
   c. pressure applicator assembly
      i. pressure-plate
      1. metal pressure point
      2. glass/silicone pressure spreader
      3. polished sapphire
         a. evenly applies pressure to sample
      ii. crane and spring
         1. applied (variable) uniaxial force onto the sample
      iii. lowering stage
         1. to remotely lower stage from outside the carboy
   d. pump and purge assembly
      i. carboy
      ii. forming gas purge
      iii. vacuum (building vacuum)
D.7 Wicked Materials

This apparatus appendix section describes the wax selection process and describes its wetting behavior. Wax was chosen based on its low melting point, low (melted) viscosity and its ability to be easily stripped in solvents, yet able to withstand harsh etchants. When at room temperature the wax was viscous enough to help take some of the thermal strain off of the sparsely bonded structures.

Waxes and other materials’ wetting ability were judged based on a split two-microscope slide gap test as described in the wax wetting reference given in the discussion section. Figure D.7-1 depicts how this setup works. A VdW bonded pair of glass slides are chosen; clamped at one end and split open at the other, then a known filler is slipped in as a separator (such as a simple piece of tape) and clamped at the other end. The glass slide pair essentially has a wedge shaped void within and the wax or other wicking material may be presented along one side and allowed to wet along the void. This test is an elegant method to compare and verify the wetting ability of different materials.

Figure D.7-1. Picture of an example wax wetting two microscope slide gap test.
Table D7-1. List of Apiezon-W, W40, and 2:1 mix-wax properties.

<table>
<thead>
<tr>
<th>Material</th>
<th>Melting Point (°C)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Apiezon-W</td>
<td>80-90</td>
</tr>
<tr>
<td>Apiezon-W40</td>
<td>40-50</td>
</tr>
<tr>
<td>W₂W₄₀, mix-wax</td>
<td>65-75</td>
</tr>
<tr>
<td>Polypropylene</td>
<td>~ 165</td>
</tr>
</tbody>
</table>

1. Materials
   a. Apiezon mix-wax
      i. my wetting wax is a 2:1 mixture of Apiezon-W and Apiezon-W40 wax (essentially a less dilute Apiezon-W40)
      ii. Table D.7-1 lists the properties of both standard waxes along with the melting point of the mix-wax
          1. the ‘melting point’ or ‘softening point’ is a vague term given to the material qualitatively based on its change in viscosity
          2. the molecular weight distributions of each are unknown
          3. according to Apiezon their Apiezon-W40 wax is simply Apiezon-W diluted in a heavy weight grease
   b. comparison to other types of waxes
      i. Apiezon W and W40 are microcrystalline waxes with no visible voids
      ii. other waxes such as carnauba, bee’s, and paraffin, and Crystalbond waxes are all macrocrystalline waxes each with large voids (on the order of 0.5um-5um) that make them permeable to etchants
      iii. the large grain size of the macrocrystalline waxes prevented their wetting into narrow gaps such as the bond void region
   c. comparison to solvent based glues
      i. solvent based adhesives consist of a polymer suspended in a solvent
      ii. these adhesives must release their solvent to harden, this requires evaporation or absorption into their substrates, however the only way to release solvents from between semiconductors is to escape to the edge
      iii. as experimentally verified the solvent nearest the edges evaporates first thus hardening and locking in the interior solvent preventing the it from hardening
   d. comparison to epoxies

\footnote{Apiezon Products is a business unit of M&I Materials Ltd.}
i. many epoxies do not release solvents or gasses during their curing process as they generally rely on polymerization although they do tend to shrink

ii. they cure faster when heat is applied, so an epoxy would have to match the bonding temperature to allow it to wick completely before curing

iii. all the commercial epoxies the author ever found had filler particles embedded in them that were much larger than the channel depth of the investigated samples (typically the fillers were on the order of 10’s of micrometers and larger), though this is not to say that an appropriate epoxy does not exist nor that a usable epoxy could be manufactured for this purpose

iv. epoxies are commonly used as filler materials in flip-chip integration technology, but who’s gaps are generally on the order of 10’s of micrometers

2. Wax Wetting
   a. Figure D.7-2a shows a picture of proper wax wetting using the new mask pattern
   b. Figure D.7-2b shows a picture of improper wax wetting, with bubbles (voids), using the old mask pattern
      i. The shape of the old revision mask pattern creates multiple voids due to its ‘non-aerodynamic’ shape
   c. Edge effects
      i. Figure D.7-3 shows an illustration of the wax wetting up the sides of the silicon sample (in perspective view)
      ii. Figure D.7-4 shows a series of illustrations depicting how the wax wicking up the sides of the silicon causes voids to form
         1. The wax that wicks up the sides of the sample wets along the edge faster than in the void region between the samples causing the void to eventually become enclosed with wax
         2. Once the bubble forms the wax can no longer wet to fill the void
   iii. Polypropylene beads
      3. Figure D.7-5 shows a series of illustrations depicting how the wax wicking up the sides of the silicon can be prevented from creating bubbles
         4. the polypropylene has a higher melting point and does not mix readily with mix-wax (although the grease in the wax does slowly displace the polypropylene over time) providing an edge wax barrier

e. comparison to UV curable adhesives
   i. These cannot be used for UV opaque materials such as most semiconductors and was not considered
Figure D.7-2. Pictures of (a) properly wet wax using latest mask pattern revision and (b) improperly wet wax (with bubbles) using old mask pattern.

Figure D.7-3. Illustration of wax wetting up side of silicon (in perspective).
Figure D.7-4. Illustrations depicting how edge wax traps bubble.

Figure D.7-5. Illustrations depicting how edge wax can be prevented from creating bubbles by using properly placed polypropylene beads.
D.8 Etch-Thinning Apparatus

This apparatus appendix section describes two etch-thinning apparatus revisions.

Rapid reaction rate limited etch-thinning etchants are less susceptible to agitation induced etch rate changes, but are effected enough to cause noticeable thickness variations over long-term substrate etching sessions. Simply placing a sample in a stir-bar agitated beaker results in highly non-uniform etch thinning. The etchant must either be uniformly agitated (such as by a laminar flow of a ‘jet etcher’) or randomly varied (such as by the random motion of rising bubbles in a ‘bubble etcher’).

The peristaltic jet etcher was the latest implementation of an etch-thinning apparatus. It could uniformly and rapidly etch-thin the GaAs substrate with a predictable and constant etch rate.

The bubble etcher presented was a previous implementation of an etch-thinning apparatus.

![Peristaltic Jet Etcher](image1)

Figure D.8-1. Pictures of the peristaltic jet etcher.

1. Jet etcher assembly
   a. peristaltic pump
   b. pump tube
   c. nozzle mount
   d. sample mount
   i. prevented the sample from moving in the jet stream
2. Bubble etcher
   a. Early attempt to uniformly etch thin the GaAs substrate
      i. the bubbles would ‘randomly’ flow etchant across the surface of
         the sample which was attached to the bottom of a floating bob
      ii. the bubbles tended to produce a uniform flow due to the small size
          of the bob and low volume of bubbles emanating from below
   b. Was clumsy and dangerous to operate
      i. the bubbles would dangerously aspirate etchant at the surface of
         the etchant reservoir
D.9 Thermal Measurement Setup

This apparatus appendix section describes various parts of the thermal measurement setup.

*Figure D.9-1. Pictures of the thermal measurement setup.*

1. **Description of parts**
   a. sample
   b. Cu sample mount (heat-sink)
      i. where the sample is mounted with thermal grease
   c. thermistors
      i. 0.1°C accuracy 2.25kohm calibration thermistor
         1. used to accurately calibrate the sample mount temperature
      ii. 1.0°C accuracy 10kohm controller thermistor
         1. higher resistance thermistor to operate the temperature controller more effectively
            a. this higher resistance yields a sharper temperature resolution
   d. thermoelectric element
      i. this device exchanges heat between the Cu sample mount and the water chilled Cu block
   e. thermoelectric controller
      i. this device controls the temperature of the Cu sample mount
         (measurements have shown stability of about 0.08°C standard deviation over long periods)
   f. water chilled Cu block
i. just a chunk of Cu with a water channel through it to convectively transfer heat from the thermoelectric element to a higher capacity compressor driven water chiller

g. water chiller
   i. absorb the heat from the thermal electric element

h. microscope
   i. to align the fine probes with the heater contact pads

i. probe stages and leads to connector box

j. BeCu probe tips
   i. these probes provided a consistent low electrical resistance contact to the heater pads capable of passing high amounts of current to the heaters
D.10 HP4155 Semiconductor Parameter Analyzer

This apparatus appendix section describes the parts of and use of the HP4155 semiconductor parameter analyzer used to perform electrical measurements throughout this dissertation’s investigation.

1. High Power SMU extender
   a. Use SMU extender box to provide high current output using HPSMU

2. Connector box
   a. An intermediate connector box is used to link the 4155 to the measurement leads
   b. This box:
      i. connects the force and ground of HPSMU to the input and output current leads
      ii. connects the sense of VMU1 and VMU2 to the input and output voltage leads
      iii. connects the ground of VMU1 and VMU2 to the box exterior (be sure to insulate the box from the measurement setup to prevent shorting)

3. Backside Kelvin Connector
   a. Conveniently removes the resistance of the backside lead wires from the resistance measurement

4. Sweep measurements
   a. Refer to the 4155 manual for details of how to setup a sweep measurement

Figure D.10-1. Pictures of the backside Kelvin connector apparatus (with and without sample).
b. options:
   i. select dvolt to reduce noise on the VMUs
      1. this reduces noise, but the voltage resolution remains the same as a non-dvolt setup
      2. the dvolt range for the VMUs is a maximum of ±2V

c. create an auto measure regression line that encompasses the entire sweep
d. the slope of the V-I regression line yields an ensemble resistance
e. average several of these resistances to remove any environmentally induced undulations over time

5. Sampling measurements
a. refer to the 4155 manual for details of how to setup a sampling measurement
b. user variable settings:
   i. variable name= R
   ii. data= (VMU1-VMU2)/I5
c. choose options:
   i. initial interval= 2s
   ii. # of samples= 128
   iii. total sampling time= nolimit
d. plot R vs time
e. apply current until steady state condition exists for 2-3m (repeat for opposite polarity)
f. extract time averaged R
   i. set cursor1 to R=1, t=70s (70s is typically the beginning of the steady state condition)
   ii. set cursor2 to R=1000, t=500s (beyond the range of data)
   iii. draw a regression line
       1. this regression line will average all the R data points from 70s-end
D.11 HP8510B Network Analyzer

This apparatus appendix section describes the settings of the HP8510B microwave network analyzer used to obtain microwave measurements in this dissertation.

Refer to the operation manual for details on how to setup, calibrate, and perform measurements using the 8510C.

1. Power settings
   a. the power is typically set to 0dBm on each port
   b. too high a power will damage the calibration substrate load resistors

2. Averaging
   a. averaging will lower the noise floor and is typically set to 256

3. Sweep type
   a. set the sweep type to step rather than ramp (ramp typically causes calibration issues and is typically noisy)

4. Calibration
   a. Define the calibration standard
      i. input the calibration standard values for open capacitance, short inductance, load offset length, and through delay provided by the probe and calibration substrate company
         1. the load inductance cannot be directly input into the 8510B, it must be input as an equivalent delay length of high impedance waveguide.
         2. Use the formula: delay = \( \frac{L_{load}}{Z_m} \) (eg: \( L_{load} = +1.5 \text{pH}, \ Z_m = 200 \text{ohms} \rightarrow \text{delay} = 7.5 \text{fs} \); the 8510B will only except a resolution of 1fs, so this must be entered as 8fs)
   b. Perform calibration
      i. Loose or damaged cables, damaged probes, damaged calibration substrates, or improperly seated probes can all severely impact calibration. Use extreme caution to avoid all of these scenarios.
      ii. Perform a full 2-port calibration and do not omit isolation
         1. Picoprobe calibration substrates have a specific calibrated open structures, while Cascade’s do not. Perform the Cascade calibration with the probe at least 250um above the substrate (the open capacitance supplied by Cascade assumes this configuration; calibrating using an open part of the substrate will yield an incorrect open calibration)
      iii. Verify and correct the electrical delays and phase offsets
         1. First verify the correct s-parameter amplitudes by connecting to the calibration standards
         2. Short
            a. Place the probes on the calibrated shorts and change the electrical delay and phase offset of the S11 and
S22 required to yield the desired ±180° phase across the entire frequency span (note the values)

3. Open
   a. re-change the delay and offset as above for the open to yield the desired 0° phase across the entire frequency span (note the values)
      i. In the case of Cascade substrates be sure to press the probe down onto the substrate in order to provide the correct phase during this test.

4. Use the average of the open and short delays and offsets to produce the best fitting

5. Through
   a. verify that the S12 and S21 show that the through standard would require an electrical delay corresponding to the value from the calibration company to produce a negligible phase (return the electrical delay to 0s when finished)

5. RF Measurement
   a. All the structures illustrated in this thesis are reciprocal, so the S11 and S22 should ideally be identical. The S12 and S21 should also be identical.
   b. Be sure the probes are settled properly to yield ideal s-parameter values. Improper probing or calibration will result in non-reciprocal scattering factors.

6. 8510 Labview data extraction
   a. display the desired s-parameter data on the 8510B
   b. put this data into memory
      i. display / data to memory
   c. display the memorized data
      i. display / memory
   d. use HP8510.vi (written by GuoLiang Li) to extract the data
      i. start and stop frequencies, and number of points must match the values in the 8510B
   e. return the 8510B to local operation mode
      i. press ‘local’ button
   f. display data instead of memorized data
      i. display / data
   g. repeat until all s-parameter data has been extracted
Appendix E: Software Source Code

E.1 Universal MOCVD Control Program

This source code appendix section presents the universal MOCVD recipe program used to grow bondable material throughout this dissertation’s investigation. It was written by the dissertation author with help from a fellow group member: Clint Novotny. It is a text based program capable of controlling the MOCVD machine which writes and executes growth recipe files and is written in HPBASIC in order to control the machine.

```
10 ! sections v.7
20 ! * * * This program will grow anything in the reactor
30 ! improvements on v.6 include:
40 ! 1) increased time for Inficon to zero-out from 300 to
500 seconds
50 !
60 ! Materials allowed include: In1 In2 Ga1 Ga2 Ga3 As1 As2 As3 P H
70 Si Zn
80 !
80 PRINTER IS 1 ! this sets the CRT as the location to PRINT to
90 DIM Sv$[70]
100 DIM Homedir$[46]
110 Homedir$="C:\Program Files\HTBwin\programs\new_programs"
120 !
130 ! *****This opens the connection to the IEEE 488/80
controller*****
140 CLEAR 705
150 CLEAR 708
160 CLEAR 709
170 REMOTE 705
180 REMOTE 708
190 REMOTE 709
200 OUTPUT 708;"C5P0I0X" ! Channel:0 all ports selected as HIGH
TRUE logic
210 OUTPUT 709;"C5P0I16X" ! Channel:1 all ports selected as LOW TRUE
logic
220 OUTPUT 708;"S0X" ! Channel:0 configuration is saved
230 OUTPUT 709;"S0X" ! Channel:1 configuration is saved
240 OUTPUT 709;"A8X" ! this flows N2 through the reactor
250 !
260 ! *****This sets up the Softkey Menu******
270 ON KEY 1 LABEL "Shutdown MOCVD" GOTO Theend
280 ON KEY 2 LABEL "Pause" GOSUB Pausing
290 ON KEY 3 LABEL "Next  Step" GOTO Skips
300 ON KEY 4 LABEL "Next Section" GOTO Skipsection
310 ON KEY 5 GOSUB Unusedkey
320 ON KEY 6 GOSUB Unusedkey
```
330  ON KEY 7 GOSUB Unusedkey
340  ON KEY 8 GOSUB Unusedkey
350  !
360  ! ********** Variable Setup **********************
370  DIM Descr$[400]  ! variable for description of growth
380  INTEGER Counter  ! counter for steps in program
390  INTEGER Totaln  ! integer for total number of sections
400  DIM Total(20,13)  ! this creates the matrix for time,
temperature, and materials
410  MAT Total=(0)  ! this sets all values to be 0
420  DIM Maxperiod(20)  ! matrix for maximum number of periods per
sections
430  MAT Maxperiod=(0)
440  DIM Maxlayer(20)  ! matrix for maximum number of layers per
period
450  MAT Maxlayer=(0)
460  DIM Beglayer(20)  ! keeps track of first layer number per
section
470  MAT Beglayer=(0)
480  Counter=0  ! counter for each "step" or stage of the
program
490  INTEGER Totalindex  ! creates index for number of columns in Total
matrix
500  Totalindex=13
510  !
520  ! *****This is the startup menu*****
530  CLEAR SCREEN
540  INPUT "Would you like to use a previously saved structure? (Y/N)",Y$
550  IF UPC$(Y$)="N" THEN GOTO Per
560  Getfile:  !
570  INPUT "What filename do you want?",Sv$
580  Sv$=Homedir$&Sv$&".dat"
590  ASSIGN @Data TO Sv$;FORMAT ON,RETURN E  ! this assigns @Data to
the file in ASCII mode
600  IF E=56 THEN
610  PRINT "This file does not exist. Try again."
620  GOTO Getfile
630  END IF
640  ENTER
650  GOTO Dontsave
660  !
670  Per:  !
680  !
690  INPUT "Please enter a description of the growth.",Descr$
700  INPUT "How many sections do you want?",Totaln
710  Z=0  ! counter for Total Matrix, Current layer
720  !
730  FOR I=0 TO (Totaln-1)  ! cycles through each section
740  PRINT
750  PRINT "Section";I+1:""
760  PRINT
770  INPUT "Is this a previously used section? (y/n)",Z$
780  IF UPC$(Z$)="Y" THEN
INPUT "Which section do you want to repeat here?", Prev
Copys = Prev - 1
Maxperiod(I) = Maxperiod(Copys)
Maxlayer(I) = Maxlayer(Copys)
Newz = Beglayer(Copys)
Beglayer(I) = Z
FOR Cc = 1 TO Maxlayer(I)
  IF Cc > 1 THEN
    Newz = Newz + 1
  END IF
  FOR A = 0 TO Totalindex
    Total(Z, A) = Total(Newz, A)
  NEXT A
  Z = Z + 1
NEXT Cc
GOTO 1130
END IF
IF I = 0 THEN
  ! PRINT "Remember the first layer must be the time and gas you wish to run during the heater warm-up."
  ! PRINT "Typically for a warm-up to 650 C the time should be set to ~400 seconds."
ENDIF
IF I = (Totaln - 1) THEN
  ! PRINT "Remember the last layer must be the time and gas you wish to run during the chamber cool-down."
  ! PRINT "Typically for a cool-down from 650 C the time should be set to ~400 seconds."
ENDIF
INPUT "How many periods would you like?", Maxperiod(I)
INPUT "How many layers would you like?", Maxlayer(I)
!
FOR J = 1 TO Maxlayer(I)  ! cycles through each layer
  IF J = 1 THEN Beglayer(I) = Z
  PRINT "Please enter the time, temperature, and materials for layer"; J; "."
  GOSUB Totalchoose
  Z = Z + 1
NEXT J
NEXT I
CLEAR SCREEN
Savestructure: ! gives you the opportunity to save the structure
INPUT "Would you like to save this structure? (Y/N)", Y$
IF UPCS$(Y$) = "N" THEN GOTO Dontsave
Filename: !
INPUT "What file name would you like to save the structure as?", Sv$
Sv$ = Homedir$ & Sv$ & ".dat"
ASSIGN @Data TO Sv$; FORMAT ON, RETURN E ! this assigns @Data to the file in ASCII mode
SELECT 1
CASE E = 56
CREATE Sv$, 512 ! this creates the DOS readable file
ASSIGN @Data TO Sv$; FORMAT ON
GOSUB Totalchoose
GOTO Savestructure ! gives you the option to resave structure
END IF
!
PRINT "Press any key when you're ready to start the run."
ON KBD GOTO Rdy
Tst: !
GOTO Tst
Rdy: !
OFF KBD
St=TIMEDATE
Startt=TIMEDATE
!
Purgechamber: ! This will evacuate and purge the reactor tube
Counter=0
CLEAR SCREEN
PRINT "Turn off the atm/vac diverter switch, then press any key."
ON KBD GOTO 1980
GOTO 1970
CLEAR SCREEN
OFF KBD
PRINT "How many purges do you want?",Maxn
!
OUTPUT 708;"A2X" ! turns on the vac diverter
PRINT "I'm purging the reactor for 30 seconds."
ON DELAY 30 GOTO 2090
St=TIMEDATE
GOTO Loop
!
FOR V=1 TO Maxn ! cycles through the purges
CLEAR SCREEN
PRINT "Cycle number: ";V;" of ";Maxn
PRINT
!
OUTPUT 708;"B2X" ! turns off the vac diverter
PRINT "I'm building up pressure in the reactor for 15 seconds."
ON DELAY 15 GOTO Purge
St=TIMEDATE
GOTO Loop
!
OUTPUT 708;"A2X" ! turns on the vac diverter
PRINT "I'm purging the reactor for 45 seconds."
ON DELAY 45 GOTO 2270
St=TIMEDATE
GOTO Loop
!
NEXT V
!
INPUT "Turn on the atm/vac diverter switch, then enter: 'start'",F$
2330 IF UPC$(F$) <> "START" THEN GOTO 2320
2340 !
2350 OUTPUT 708; "B2X" ! turns off the vac diverter
2360 PRINT "Vacuum diverter now under manual control."
2370 PRINT
2380 !
2390 H2on: !
2400 ! ******** This turns H2 gass ON ****************
2410 Counter=1
2420 OUTPUT 709; "B8X" ! shuts N2 off
2430 OUTPUT 709; "A10X" ! flows H2 through the reactor
2440 CLEAR SCREEN
2450 PRINT "I'm flowing H2 through the reactor now for 120 seconds."
2460 PRINT "Next Step: Turn on source gasses for 500 seconds."
2470 ON DELAY 120 GOTO Sources
2480 St=TIMEDATE
2490 GOTO Loop
2500 Sources: !
2510 ! ******** This opens the source gasses OUT valves ********
2520 Counter=2
2530 MAT SEARCH Total(*,2),# LOC (1); In1y
2540 MAT SEARCH Total(*,3),# LOC (1); In2y
2550 MAT SEARCH Total(*,4),# LOC (1); Ga1y
2560 MAT SEARCH Total(*,5),# LOC (1); Ga2y
2570 MAT SEARCH Total(*,6),# LOC (1); Ga3y
2580 MAT SEARCH Total(*,7),# LOC (1); As1y
2590 MAT SEARCH Total(*,8),# LOC (1); As2y
2600 MAT SEARCH Total(*,9),# LOC (1); As3y
2610 MAT SEARCH Total(*,10),# LOC (1); Py
2620 MAT SEARCH Total(*,11),# LOC (1); Hy
2630 MAT SEARCH Total(*,12),# LOC (1); Siy
2640 MAT SEARCH Total(*,13),# LOC (1); Zny
2650 !
2660 CLEAR SCREEN
2670 IF In1y<>0 THEN
2680 OUTPUT 709; "A13X" ! turns on TMI-1 OUT
2690 PRINT "TMI-1 Out: ON"
2700 END IF
2710 IF In2y<>0 THEN
2720 OUTPUT 709; "A27X" ! turns on TMI-2 OUT
2730 PRINT "TMI-2 Out: ON"
2740 END IF
2750 IF Ga1y<>0 THEN
2760 OUTPUT 709; "A11X" ! turns on TEG-1 OUT
2770 PRINT "TEG-1 Out: ON"
2780 END IF
2790 IF Ga2y<>0 THEN
2800 OUTPUT 709; "A7X" ! turns on TEG-2 OUT
2810 PRINT "TEG-2 Out: ON"
2820 END IF
2830 IF Ga3y<>0 THEN
2840 OUTPUT 709; "A19X" ! turns on TEG-3 OUT
2850 PRINT "TEG-3 Out: ON"
2860 END IF
2870 IF As1y<>0 THEN
2880 OUTPUT 709;"A1X" ! turns on As-1 OUT
2890 PRINT "As-1 Out: ON"
2900 END IF
2910 IF As2y<>0 THEN
2920 OUTPUT 709;"A15X" ! turns on As-2 OUT
2930 PRINT "As-2 Out: ON"
2940 END IF
2950 IF As3y<>0 THEN
2960 OUTPUT 709;"A26X" ! turns on As-3 OUT
2970 PRINT "As-3 Out: ON"
2980 END IF
2990 IF Py<>0 THEN
3000 OUTPUT 709;"A3X" ! turns on PH3 OUT
3010 PRINT "PH3 Out: ON"
3020 END IF
3030 IF Hy<>0 THEN
3040 OUTPUT 709;"A21X" ! uses H2 via CC14 V/R
3050 PRINT "H Out: ON"
3060 END IF
3070 IF Siy<>0 THEN
3080 OUTPUT 709;"A6X" ! turns on SiH3 OUT
3090 PRINT "SiH4 Out: ON"
3100 END IF
3110 IF Zny<>0 THEN
3120 OUTPUT 709;"A5X" ! turns on DEZn OUT
3130 PRINT "DEZn Out: ON"
3140 END IF
3150 ON DELAY 500 GOTO Bubbler
3160 PRINT "Source gasses have been turned on. Please wait 500
seconds."
3170 PRINT
3180 PRINT "Next step: Turn on bubblers for 900 seconds."
3190 St=TIMEDATE
3200 GOTO Loop
3210!
3220 Bubbler: !
3230 ! ********* This turns the bubblers ON ******************
3240 Counter=3
3250 CLEAR SCREEN
3260 IF (In1y<>0 OR In2y<>0) THEN
3270 OUTPUT 708;"A14X" ! turns on TMI Bubbler
3280 PRINT "TMI Bubbler: ON"
3290 END IF
3300 IF Ga1y<>0 THEN
3310 OUTPUT 708;"A12X" ! turns on TEG-1 Bubbler
3320 PRINT "TEG-1 Bubbler: ON"
3330 END IF
3340 IF (Ga2y<>0 OR Ga3y<>0) THEN
3350 OUTPUT 708;"A8X" ! turns on TEG-2,3 Bubbler
3360 PRINT "TEG-2,3 Bubbler: ON"
3370 END IF
3380 IF (As1y<>0 OR As2y<>0 OR As3y<>0) THEN
3390 OUTPUT 709;"A2X" ! turns on As IN
3400 PRINT "As In: ON"
3410 END IF
3420 IF Py<>0 THEN
3430 OUTPUT 709;"A4X" ! turns on P IN
3440 PRINT "P In: ON"
3450 END IF
3460 IF Siy<>0 THEN
3470 OUTPUT 709;"A25X" ! turns on SiH4
3480 PRINT "SiH4: ON"
3490 END IF
3500 IF Zny<>0 THEN
3510 OUTPUT 708;"A5X"  ! turns on DEZn Bubbler
3520 PRINT "DEZn bubbler: ON"
3530 END IF
3540 !
3550 OUTPUT 709;"A12X" ! turns the N2-vent on
3560 !
3570 ON DELAY 900 GOTO Mainprogram
3580 PRINT
3590 PRINT "Set all bubbler flows and concentration levels."
3600 PRINT "You have 15 minutes."
3610 PRINT
3620 PRINT "Next step: Main program execution."
3630 St=TIMEDATE
3640 GOTO Loop
3650 !
3660 !
3670 Mainprogram: !
3680 ! ******This is the main program FOR loop******
3690 Counter=4
3700 St=TIMEDATE
3710 Currentlayer=0 ! this is the counter for the current layer in Total(*)
3720 OUTPUT 709;"A40X"
3730 !
3740 FOR L=0 TO Totaln ! cycles through each section
3750 !
3760 Sectionskipper: ! see Skipsection
3770 IF L=Totaln THEN ! run gasesreactor after structure is done
to clear RUN lines
3780 GOSUB Gassesreactor
3790 Voltage=50/175+5/7
3800 OUTPUT 705;"C0 P2 A1 V"&VAL$(Voltage)&"X"
3810 END IF
3820 !
3830 FOR M=0 TO Maxperiod(L)-1 ! cycles through each period of the
given section
3840 !
3850 Currentlayer=Beglayer(L) ! helps to recycle back to first
layer of period
3860 !
3870 FOR N=0 TO Maxlayer(L)-1 ! cycles through each layer of the
given period
3880 !
3890 GOSUB Gassesreactor
3900 ON TIME (St+Total(Currentlayer,0)) MOD 86400 GOTO Nxt
3910 Voltage=Total(Currentlayer,1)/175+5/7
3920 OUTPUT 709;"A40X"
3930 OUTPUT 705;"C0 P2 A1 V"&VAL$(Voltage)&"X"
3940 IF Total(Currentlayer,1)=0 THEN
3950 OUTPUT 709;"B40X"
3960 END IF
3970 Display: ! display during run
3980 PRINT
3990 PRINT "Section:";L+1;" of ";Totaln
4000 PRINT " Period:";M+1;" of ";Maxperiod(L)
4010 PRINT " Layer:";N+1;" of ";Maxlayer(L)
4020 !
4030 Loop: !
4040 S=INT(TIMEDATE-St)
4050 DISP S,"Seconds so far"
4060 GOTO Loop
4070 !
4080 Nxt: !
4090 St=TIMEDATE
4100 Currentlayer=Currentlayer+1
4110 NEXT N
4120 NEXT M
4130 NEXT L
4140 CLEAR SCREEN
4150 !
4160 Endgrowth: !
4170 Counter=5
4180 PRINT "Heater is turning off."
4190 PRINT "Bubblers are turning off."
4200 PRINT "Dopant lines are being flushed with H2."
4210 PRINT "H2 is now flowing into the reactor."
4220 !
4230 OUTPUT 709;"B40X" ! turns heater off
4240 OUTPUT 708;"B12X" ! turns TEG-1 bubbler off
4250 OUTPUT 708;"B8X" ! turns TEG-2,3 bubbler off
4260 OUTPUT 708;"B14X" ! turns TMI-1 bubbler off
4270 OUTPUT 709;"B25X" ! flushes SiH4 line with H2
4280 OUTPUT 708;"B5X" ! turns DEZn bubbler off
4290 !
4300 Asoff: ! this flushes out As from the lines (if switch 6(H2 IN)
set to Manual)
4310 Counter=6
4320 ON DELAY 300 GOTO Idone
4330 IF (As1y=0 AND As2y=0 AND As3y=0) THEN
4340 GOTO Loop
4350 END IF
4360 OUTPUT 709;"B2X" ! As:In turned off
4370 PRINT "As:In has been turned off."
4380 GOTO Loop
4390 !
4400 Idone: !
4410 Counter=7
4420 !
4430 PRINT
4440 PRINT "Group V sources are off."
4450 PRINT "Group III out lines are turned off."
PRINT "Dopants are turned off."
OUTPUT 709;"B13X" ! turns TMI-1 out off
OUTPUT 709;"B27X" ! turns TMI-2 out off
OUTPUT 709;"B11X" ! turns TEG-1 out off
OUTPUT 709;"B7X" ! turns TEG-2 out off
OUTPUT 709;"B19X" ! turns TEG-3 out off
OUTPUT 709;"A16X" ! turns As's H2 purge line on
OUTPUT 708;"B1X" ! puts As-1 to vent
OUTPUT 709;"B15X" ! puts As-2 to vent
OUTPUT 709;"B22X" ! puts As-3 to vent
OUTPUT 709;"B4X" ! turns P source off
OUTPUT 708;"B3X" ! puts P to vent
OUTPUT 709;"B6X" ! turns SiH4 out off
OUTPUT 709;"B5X" ! turns DEZn out off
!
ON DELAY 120 GOTO Finished
PRINT "Waiting 120 seconds to purge with H2."
St=TIMEDATE
GOTO Loop
!
Finished:  !
Counter=8
!
CLEAR SCREEN
PRINT "I am done growing the structure."
PRINT "Program finished at: ";TIME$(TIMEDATE)
Totaltime=(TIMEDATE-Startt)
PRINT "Total time for run: ";TIME$(Totaltime)
PRINT
PRINT
GOTO Theend
!
Unusedkey:  ! this is the unused softkey response
BEEP 1220,.2 ! BEEP frequency,duration
RETURN
!
Pausing:  ! this pauses the program, but NOT the ON TIME functions
DISP "Sequence is paused. Please press F2 to resume."
PAUSE
RETURN
!
Skips:  ! skips to next stage of the program
OFF DELAY
OFF TIME
IF Counter=0 THEN GOTO H2on
IF Counter=1 THEN GOTO Sources
IF Counter=2 THEN GOTO Bubbler
IF Counter=3 THEN GOTO Mainprogram
IF Counter=4 THEN GOTO Endgrowth
IF Counter=5 THEN GOTO Asoff
IF Counter=6 THEN GOTO Idone
IF Counter=7 THEN GOTO Finished
IF Counter=8 THEN GOTO Theend
!
Skipsection:  ! skips to next section in Mainprogram (next I)
L=L+1
St=TIMEDATE
GOTO Sectionskipper
!
Totalchoose: ! this is the time, temperature, and material input handler
INPUT "Please enter the time (seconds):",Total(Z,0)
INPUT "Please enter the temperature (Celsius):",Total(Z,1)
PRINT "Choose from: In1 In2 Ga1 Ga2 Ga3 As1 As2 As3 P H Si Zn"
M$=""
INPUT "Please type in material (i.e.: GaAs1)",M$
CLEAR SCREEN
IF POS(UPC$(M$),"IN1")<>0 THEN Total(Z,2)=1
IF POS(UPC$(M$),"IN2")<>0 THEN Total(Z,3)=1
IF POS(UPC$(M$),"GA1")<>0 THEN Total(Z,4)=1
IF POS(UPC$(M$),"GA2")<>0 THEN Total(Z,5)=1
IF POS(UPC$(M$),"GA3")<>0 THEN Total(Z,6)=1
IF POS(UPC$(M$),"AS1")<>0 THEN Total(Z,7)=1
IF POS(UPC$(M$),"AS2")<>0 THEN Total(Z,8)=1
IF POS(UPC$(M$),"AS3")<>0 THEN Total(Z,9)=1
IF POS(UPC$(M$),"P")<>0 THEN Total(Z,10)=1
IF POS(UPC$(M$),"H")<>0 THEN Total(Z,11)=1
IF POS(UPC$(M$),"SI")<>0 THEN Total(Z,12)=1
IF POS(UPC$(M$),"ZN")<>0 THEN Total(Z,13)=1
RETURN
!
Gassesreactor: ! this tells the MOCVD what to flow through the reactor
CLEAR SCREEN
PRINT "Layer data:"
OUTPUT 708;CHR$(66-TOTAL(Currentlayer,2))&"13X" ! runs TMI-1
OUTPUT 709;CHR$(66-TOTAL(Currentlayer,3))&"20X" ! runs TMI-2
(uses TEG-3 V/R line)
OUTPUT 708;CHR$(66-TOTAL(Currentlayer,4))&"11X" ! runs TEG-1
OUTPUT 708;CHR$(66-TOTAL(Currentlayer,5))&"7X" ! runs TEG-2
IF Total(Currentlayer,3)=0 THEN
  OUTPUT 709;CHR$(66-TOTAL(Currentlayer,6))&"20X" ! runs TEG-3
  OUTPUT 708;CHR$(66-TOTAL(Currentlayer,7))&"1X" ! runs As-1
  OUTPUT 708;CHR$(66-TOTAL(Currentlayer,8))&"15X" ! runs As-2
  OUTPUT 709;CHR$(66-TOTAL(Currentlayer,9))&"22X" ! runs As-3
  (via CCl4 line)
OUTPUT 708;CHR$(66-TOTAL(Currentlayer,10))&"6X" ! runs SiH4
OUTPUT 709;CHR$(66-TOTAL(Currentlayer,11))&"22X" ! runs H (via CCl4 line)
OUTPUT 708;CHR$(66-TOTAL(Currentlayer,12))&"6X" ! runs SiH4
OUTPUT 709;CHR$(66-TOTAL(Currentlayer,13))&"4X" ! runs DEZn
RETURN
!
Displaylayer: ! displays the layer data
PRINT " Time Temp Material(s)"
GOSUB Displaylayer
RETURN
!
Displaylayer: ! displays the layer data
5510 PRINT Total(Q,0);"s   ";Total(Q,1);"C    ";
5520 IF Total(Q,2)=1 THEN PRINT "TMI-1 ";
5530 IF Total(Q,3)=1 THEN PRINT "TMI-2 ";
5540 IF Total(Q,4)=1 THEN PRINT "TEG-1 ";
5550 IF Total(Q,5)=1 THEN PRINT "TEG-2 ";
5560 IF Total(Q,6)=1 THEN PRINT "TEG-3 ";
5570 IF Total(Q,7)=1 THEN PRINT "As-1 ";
5580 IF Total(Q,8)=1 THEN PRINT "As-2 ";
5590 IF Total(Q,9)=1 THEN PRINT "As-3 ";
5600 IF Total(Q,10)=1 THEN PRINT "PH3 ";
5610 IF Total(Q,11)=1 THEN PRINT "H2 ";
5620 IF Total(Q,12)=1 THEN PRINT "SiH4 ";
5630 IF Total(Q,13)=1 THEN PRINT "DEZn ";
5640 PRINT
5650 RETURN
5660 !
5670 The end: ! the end of the program
5680 OUTPUT 708;"DOZX" ! turns all bits OFF for channel:0
5690 OUTPUT 709;"DOZX" ! turns all bits OFF for channel:1
5700 OUTPUT 709;"A8X" ! flows N2 through the reactor
5710 PRINT
5720 PRINT "All gases are off.  N2 flowing through reactor."
5730 !
5740 PRINT "Have a Nice Day."
5750 END
This source code appendix section presents the Matlab program that was used to extract transmission line parameters from scattering matrix measurements. It was based on a program written by a former group member: GuoLiang Li. The extraction theory is discussed in the bonded device microwave characterization chapter.

```matlab
clear
format long e

% measurement constants
L2 = 1.0378E-3; % measured length of long transmission line
%(excluding pads: although it doesn't matter)
L1 = 0.5379E-3; % measured length of short transmission line
%(excluding pads: although it doesn't matter)
L = L2 - L1;
c = 2.99792458e8;
Zo = 50; % impedance of measurement system (probes, cables, Network Analyzer)

% load S-parameters data file for shorter device

fid = fopen(char(files(1)),'rt');
shorts11 = fscanf(fid,'%15f',[3,N]);
close(fid);

fid = fopen(char(files(2)),'rt');
shorts12 = fscanf(fid,'%15f',[3,N]);
close(fid);

fid = fopen(char(files(3)),'rt');
shorts21 = fscanf(fid,'%15f',[3,N]);
close(fid);

fid = fopen(char(files(4)),'rt');
shorts22 = fscanf(fid,'%15f',[3,N]);
close(fid);

f = shorts11(1,1:N); % frequency in GHz
```
% repairing any +-180d jumps in the phase angle
% so that they do not create anomalies during averaging

shorts11angle= shorts11(3,:);
shiftedshorts11angle= circshift(shorts11angle',-1)';
blah=find(shiftedshorts11angle-short11angle <-180);
blah=[blah,201];
b=zeros(1,blah(1));
for k=1:length(blah)-1;
    b=[b,360*k*ones(1,blah(k+1)-blah(k))];
end
shorts11angle=shorts11angle+b;
shiftedshorts11angle= circshift(shorts11angle',-1)';
blah=find(shiftedshorts11angle-short11angle >180);
blah=[blah,201];
b=zeros(1,blah(1));
for k=1:length(blah)-1;
    b=[b,-360*k*ones(1,blah(k+1)-blah(k))];
end
shorts11angle=shorts11angle+b;

shorts12angle= shorts12(3,:);
shiftedshorts12angle= circshift(shorts12angle',-1)';
blah=find(shiftedshorts12angle-short12angle <-180);
blah=[blah,201];
b=zeros(1,blah(1));
for k=1:length(blah)-1;
    b=[b,360*k*ones(1,blah(k+1)-blah(k))];
end
shorts12angle=shorts12angle+b;
shiftedshorts12angle= circshift(shorts12angle',-1)';
blah=find(shiftedshorts12angle-short12angle >180);
blah=[blah,201];
b=zeros(1,blah(1));
for k=1:length(blah)-1;
    b=[b,-360*k*ones(1,blah(k+1)-blah(k))];
end
shorts12angle=shorts12angle+b;

shorts21angle= shorts21(3,:);
shiftedshorts21angle= circshift(shorts21angle',-1)';
blah=find(shiftedshorts21angle-short21angle <-180);
blah=[blah,201];
b=zeros(1,blah(1));
for k=1:length(blah)-1;
    b=[b,360*k*ones(1,blah(k+1)-blah(k))];
end
shorts21angle=shorts21angle+b;
shiftedshorts21angle= circshift(shorts21angle',-1)';
blah=find(shiftedshorts21angle-short21angle >180);
blah=[blah,201];
b=zeros(1,blah(1));
for k=1:length(blah)-1;
    b=[b,-360*k*ones(1,blah(k+1)-blah(k))];
end
shorts21angle=shorts21angle+b;
shorts21angle=shorts21angle+b;
shorts22angle= shorts22(3,:);
shiftedshorts22angle= circshift(shorts22angle',-1)';
blah=find(shiftedshorts22angle-shorts22angle < -180);
blah=[blah,201];
b=zeros(1,blah(1));
for k=1:length(blah)-1;
    b=[b,360*k*ones(1,blah(k+1)-blah(k))];
end
shorts22angle=shorts22angle+b;
shiftedshorts22angle= circshift(shorts22angle',-1)';
blah=find(shiftedshorts22angle-shorts22angle >180);
blah=[blah,201];
b=zeros(1,blah(1));
for k=1:length(blah)-1;
    b=[b,-360*k*ones(1,blah(k+1)-blah(k))];
end
shorts22angle=shorts22angle+b;

% averaging to smooth out data a little bit
% (must be done before converting phase or the +-180d correction will
% be for not)
shorts11angle=0.5*(shorts11angle+shorts22angle)*pi/180; %angle in radians
shorts22angle=shorts11angle;
shorts12angle=0.5*(shorts12angle+shorts21angle)*pi/180;
shorts21angle=shorts12angle;

shorts11amp=10.^((shorts11(2,:)/20);
shorts12amp=10.^((shorts12(2,:)/20);
shorts21amp=10.^((shorts21(2,:)/20);
shorts22amp=10.^((shorts22(2,:)/20);

shorts11amp=0.5*(shorts11amp+shorts22amp); %amplitude
shorts22amp=shorts11amp;
shorts12amp=0.5*(shorts12amp+shorts21amp);
shorts21amp=shorts12amp;

% plotting s-parameters
shortS11=shorts11amp.*exp(i*shorts11angle);
shortS12=shorts12amp.*exp(i*shorts12angle);
shortS21=shorts21amp.*exp(i*shorts21angle);
shortS22=shorts22amp.*exp(i*shorts22angle);

figure(11)
smithchart(shortS11);
hold
red1=smithchart(shortS21);
set(red1,'Color',[1 0 0])
% setting a few markers
%%
marker1 = smithchart(shortS11(find(f>0.499,1)));
set(marker1,'Marker','o')
marker2 = smithchart(shortS12(find(f>0.499,1)));
set(marker2,'Marker','o')

marker1 = smithchart(shortS11(find(f>1.962,1)));
set(marker1,'Marker','o')
marker2 = smithchart(shortS12(find(f>1.962,1)));
set(marker2,'Marker','o')

marker1 = smithchart(shortS11(find(f>12.0,1)));
set(marker1,'Marker','o')
marker2 = smithchart(shortS12(find(f>12.0,1)));
set(marker2,'Marker','o')
%

% calculate short abcd transmission matrix
shortA=((1+shortS11).*(1-shortS22)+shortS12.*shortS21)./(2*shortS21);
shortB=((1+shortS11).*(1+shortS22)-
          shortS12.*shortS21)*Zo./(2*shortS21);
shortC=((1-shortS11).*(1-shortS22)-
          shortS12.*shortS21)./(Zo*2*shortS21);
shortD=((1-shortS11).*(1+shortS22)+shortS12.*shortS21)./(2*shortS21);

% load S-parameters data file for longer device

lineNo=1;
files=inputdlg(prompt,title,lineNo,default);
N=str2num(char(files(5)));

fid=fopen(char(files(1)),'rt');
longs11=fscanf(fid,'%15f',[3,N]);
fclose(fid);

fid=fopen(char(files(2)),'rt');
longs12=fscanf(fid,'%15f',[3,N]);
fclose(fid);

fid=fopen(char(files(3)),'rt');
longs21=fscanf(fid,'%15f',[3,N]);
fclose(fid);

fid=fopen(char(files(4)),'rt');
longs22=fscanf(fid,'%15f',[3,N]);
fclose(fid);
% repairing any +-180d jumps in the phase angle
% so that they do not create anomalies during averaging

longs11angle= longs11(3,:);
shiftedlongs11angle= circshift(longs11angle',-1)';
blah=find(shiftedlongs11angle-longs11angle <-180);
blah=[blah,201];
b=zeros(1,blah(1));
for k=1:length(blah)-1;
    b=[b,360*k*ones(1,blah(k+1)-blah(k))];
end
longs11angle=longs11angle+b;
shiftedlongs11angle= circshift(longs11angle',-1)';
blah=find(shiftedlongs11angle-longs11angle >180);
blah=[blah,201];
b=zeros(1,blah(1));
for k=1:length(blah)-1;
    b=[b,-360*k*ones(1,blah(k+1)-blah(k))];
end
longs11angle=longs11angle+b;

longs12angle= longs12(3,:);
shiftedlongs12angle= circshift(longs12angle',-1)';
blah=find(shiftedlongs12angle-longs12angle <-180);
blah=[blah,201];
b=zeros(1,blah(1));
for k=1:length(blah)-1;
    b=[b,360*k*ones(1,blah(k+1)-blah(k))];
end
longs12angle=longs12angle+b;
shiftedlongs12angle= circshift(longs12angle',-1)';
blah=find(shiftedlongs12angle-longs12angle >180);
blah=[blah,201];
b=zeros(1,blah(1));
for k=1:length(blah)-1;
    b=[b,-360*k*ones(1,blah(k+1)-blah(k))];
end
longs12angle=longs12angle+b;

longs21angle= longs21(3,:);
shiftedlongs21angle= circshift(longs21angle',-1)';
blah=find(shiftedlongs21angle-longs21angle <-180);
blah=[blah,201];
b=zeros(1,blah(1));
for k=1:length(blah)-1;
    b=[b,360*k*ones(1,blah(k+1)-blah(k))];
end
longs21angle=longs21angle+b;
shiftedlongs21angle= circshift(longs21angle',-1)';
blah=find(shiftedlongs21angle-longs21angle >180);
blah=[blah,201];
b=zeros(1,blah(1));
for k=1:length(blah)-1;
    b=[b,-360*k*ones(1,blah(k+1)-blah(k))];
end
longs21angle=longs21angle+b;
end
longs21angle=longs21angle+b;

longs22angle= longs22(3,:);
shiftedlongs22angle= circshift(longs22angle',-1)';
blah=find(shiftedlongs22angle-longs22angle <-180);
blah=[blah,201];
b=zeros(1,blah(1));
for k=1:length(blah)-1;
    b=[b,360*k*ones(1,blah(k+1)-blah(k))];
end
longs22angle=longs22angle+b;
shiftedlongs22angle= circshift(longs22angle',-1)';
blah=find(shiftedlongs22angle-longs22angle >180);
blah=[blah,201];
b=zeros(1,blah(1));
for k=1:length(blah)-1;
    b=[b,-360*k*ones(1,blah(k+1)-blah(k))];
end
longs22angle=longs22angle+b;

% averaging
longs11angle=0.5*(longs11angle+longs22angle)*pi/180; %angle in radians
longs22angle=longs11angle;
longs12angle=0.5*(longs12angle+longs21angle)*pi/180;
longs21angle=longs12angle;

longs11amp=10.^((longs11(2,:)/20));
longs12amp=10.^((longs12(2,:)/20));
longs21amp=10.^((longs21(2,:)/20));
longs22amp=10.^((longs22(2,:)/20));

longs11amp=0.5*(longs11amp+longs22amp); %amplitude
longs22amp=longs11amp;
longs12amp=0.5*(longs12amp+longs21amp);
longs21amp=longs12amp;

% plotting s-parameters
longS11=longs11amp.*exp(i*longs11angle);
longS12=longs12amp.*exp(i*longs12angle);
longS21=longs21amp.*exp(i*longs21angle);
longS22=longs22amp.*exp(i*longs22angle);

figure(12)
smithchart(longS11);
hold
red1=smithchart(longS21);
set(red1,'Color',[1 0 0])

% adding a few markers
marker1 = smithchart(longS11(find(f>0.499,1)));  
set(marker1,'Marker','o')

marker2 = smithchart(longS12(find(f>0.499,1)));  
set(marker2,'Marker','o')

marker1 = smithchart(longS11(find(f>1.962,1)));  
set(marker1,'Marker','o')

marker2 = smithchart(longS12(find(f>1.962,1)));  
set(marker2,'Marker','o')

marker1 = smithchart(longS11(find(f>12.0,1)));  
set(marker1,'Marker','o')

marker2 = smithchart(longS12(find(f>12.0,1)));  
set(marker2,'Marker','o')

%%

% calculate long abcd transmission matrix

longA=((1+longS11).*(1-longS22)+longS12.*longS21)./(2*longS21);
longB=((1+longS11).*(1+longS22)-longS12.*longS21)*Zo./(2*longS21);
longC=((1-longS11).*(1-longS22)-longS12.*longS21)./(Zo*2*longS21);
longD=((1-longS11).*(1+longS22)+longS12.*longS21)./(2*longS21);

% calculating propagation constant and impedance

for k=1:N;
    T1=[shortA(k),shortB(k);shortC(k),shortD(k)];
    T2=[longA(k),longB(k);longC(k),longD(k)];
    T2T1=T2*inv(T1);
    T1T2=T1*inv(T2);

    %finding gamma:
    gamma(k)=acosh((T2T1(1,1)+T1T2(1,1))/2)/L;

    %finding Zm:
    Zm(k)=(T2T1(1,2)-T1T2(1,2))/(2*sinh(gamma(k)*L));
end

% plotting attenuation coefficient, velocity index, and impedance

f=f*1e9; %converts the frequency in GHz [as seen in the 8510 '.dat' files]
%to the frequency in Hz [to be sure we're working in SI units]

alpha1=real(gamma)*8.686e-3; %converts alpha1 from Np/m into dB/mm
n1=abs(imag(gamma))*c./(2*pi*f);
figure(1)
clf(1,'reset')
plot(f*1e-9,alpha1,'r');
hold
plot(f*1e-9,n1);
xlabel('Frequency (GHz)')
ylabel('loss (dB/mm) red & nRF blue')

figure(2)
clf(2,'reset')
hold
plot(f*1e-9,real(Zm),'r')
xlabel('Frequency (GHz)')
ylabel('Zm: real red, imag blue')

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% COMSOL simulation results
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

f=[1:15]; % in (GHz)

   9.30-6.93i; 9.05-6.60i; 8.83-6.31i; 8.63-6.06i; 8.46-5.83i];
% note the large imaginary component, therefore loss cannot be ignored

V=[0.161163+0.090169i + -782.203656+129.561282i + -1.465939-5.694175i;
   0.204599+0.145229i + -730.426745+159.212136i + -5.111191-8.641136i;
   0.240195+0.185425i + -688.381575+180.951976i + -8.188207-9.667082i;
   0.269175+0.219804i + -648.054036+190.354206i + -10.372156-9.920258i;
   0.293958+0.25121i + -612.722297+190.283221i + -11.883625-9.466161i;
   0.316182+0.280662i + -583.358821+184.038315i + -12.928039-9.980637i;
   0.336758+0.308525i + -559.639695+175.01092i + -13.69507-10.074342i;
   0.356215+0.335041i + -540.63207+164.756727i + -14.285314-10.481245i;
   0.374875+0.360351i + -525.408496+154.250557i + -14.765492-11.111699i;
   0.39294+0.384558i + -513.182735+144.00331i + -15.176666-10.774326i;
   0.410539+0.407743i + -495.360532+134.258346i + -15.544737-11.483531i;
   0.427757+0.429971i + -479.360532+125.137328i + -15.886475-11.881727i;
   0.444648+0.451295i + -465.360532+116.674085i + -16.212972-12.732195i];
%Vx + Vy + Vz (note that Vy is much greater than Vx or Vz therefore a
%quasi-TEM analysis is justified)

I=[-3.790594+1.621751; -2.684863+2.357457i; -1.760141+2.448643i;
   -1.116667+2.285517i; -0.685523+2.049391i; -0.403108+1.817461i;
   -0.211654+1.607775i; -0.080135+1.425746i; 0.011936+1.269052i;
   0.077242+1.134053i; 0.123857+1.017225i; 0.157077+0.915549i;
   0.180485+0.826552i; 0.19657+0.748232i; 0.207111+0.678978i];
%Iz (Ix and Iy are negligible)
1895.331046;
8.009771 + 11.896412 + 1962.527738; 6.830466 + 12.974159 +
1971.27958;
6.006043 + 13.744282 + 1949.89224; 5.500289 + 14.33805 +
1917.563115;
5.225349 + 14.849939 + 1886.405491; 5.124046 + 15.325459 +
1860.463582;
5.150686 + 15.78961 + 1841.123564; 5.273088 + 16.255062 +
1828.395878;
5.468458 + 16.72798 + 1821.756088; 5.720385 + 17.211048 +
1820.514963;
6.016801 + 17.705032 + 1823.969809; 6.348652 + 18.209664 +
1831.469052;
6.709017 + 18.72412 + 1842.431511];
%Px + Py + Pz (note that Pz is much greater than Px or Py therefore
a
%quasi-TEM analysis is justified)

loss=[5.48; 6.82; 8.02; 9.05; 9.94; 10.73; 11.45; 12.12; 12.74; 13.32;
13.88; 14.42; 14.94; 15.44; 15.93];
%in (dB/mm)

Zmvp=V.^2./(4*P);
Zmvi=V./(2*I); %I cannot be defined accurately enough to yield a
%reasonable Zmvi

figure(1)
plot(f,loss,'rd');
plot(f,real(n),'bd');

%%
figure(2)
plot(f,real(Zmvp),'rd')
plot(f,imag(Zmvp),'bd')
%
%
figure(2)
plot(f,real(Zmvi),'rd')
plot(f,imag(Zmvi),'bd')
%
E.3 TWEAM Simulation Programs

This source code appendix section provides the Matlab code used to implement the two TWEAM equivalent circuit models.

1. The crude TWEAM equivalent circuit model implementation

```matlab
function zonew()
    format long

    muo=4*pi*1e-7;
    epsilono=8.854e-12;
    c=2.998e8;

    width=3.1e-6;
    gap=10e-6;
    playerthickness=1.58e-6;
    ilayerthickness=0.27e-6;
    nstubthickness=0.25e-6;
    metalwidth=2.4e-6;
    metalthickness=0.6e-6;
    rhoc=1.4e-5/10000; \%/10000 converts from ohm-cm^2 to ohm-m^2
    Auconductivity=62e6; \%S/m
    Agconductivity=40e6; \%S/m
    surfaceroughnessconductivity=51.3e6; \%S/m
    ilayerconductivity=0; \%S/m
    epsilonr=12.7;
    epsilon0surrounding=1; \%~8.9 for AlN, 2.5 for BCB, 1.0 for Air

    Zs=50; \%50; \%ohm
    ZL=26; \%50; \%ohm
    nopt=3.3; \%3.3; \%optical group velocity index
    Length=200e-6; \%active length of device

    f=linspace(0.5e9,20e9,70);
    w=2*pi*f; \%I used 'w' in lue of 'omega'

    fff=(2.04*sqrt(Auconductivity/Agconductivity)/(metalthickness*1e6))^2;
    kinkpoint=fff*1e9;

    ff=f/1e9;
    Rmet=7.3*ff.^0.5*1000;
    Rmet(find(ff<fff))=7.3*fff^0.5*1000;

    effectiveMetalthickness=2.04e-6*sqrt(Auconductivity/Agconductivity)./sqrt(ff);
    effectiveMetalthickness(find(ff<fff))=metalthickness;
    effectiveconductivity=1/(1/Auconductivity + 1/surfaceroughnessconductivity);
    Rmetp=1./(effectiveconductivity*metalwidth*effectiveMetalthickness);
```
%metalwidtheff=metalwidth +
((playerthickness+ilayerthickness+nstubthickness)*2/pi)*(1 +
log(2*pi*(metalwidth*0.5/(playerthickness+ilayerthickness+nstubthickness) + 0.92)));%

\[Lp=\mu_o*(playerthickness+ilayerthickness+nstubthickness)/metalwidtheff\]
%is really only meant to find \(L\) for a wider
parallel plate
alpha=\(\pi*0.5*metalwidth/(4*(playerthickness+ilayerthickness+nstubthicknes\])\);
\[Lp=\mu_o/(1.1*4*\pi/log(2*(sqrt(cosh(alpha))+1)/(sqrt(cosh(alpha))-1)));\]
L=0.4e-9*1000;

Rcp=rhoc/metalwidth;
Rc=0.58/1000;

Gp=ilayerconductivity*width/ilayerthickness;
G=0;%(<= this assumes no light, therefore perfect isolation)

widtheff=width + (ilayerthickness*2/pi)*(1 +
log(2*pi*(width*0.5/ilayerthickness + 0.92)));
Cp=\(\varepsilon_{r0}*(\varepsilon_{r}-\varepsilon_{r_{surrounding}})*width/ilayerthickness +\)
epsilon_{r0}*(\varepsilon_{r_{surrounding}}*widtheff/ilayerthickness;
C=1.3e-12*1000;

-------------------- microwave property calculations--------------------
\%Rmetp=Rmet;  %all these were used to test my EO response 'M(f)'
against Guoliang's Thesis
\%Lp=L;
\%Rcp=Rc;
\%Gp=G;
\%Cp=C;

\[Z=Rmet+j*w*L;\]
\[Zp=Rmetp+j*w*Lp;\]
\[Y=1./(Rc + 1./(G+j*w*C));\]
\[Yp=1./(Rcp + 1./(Gp+j*w*Cp));\]
\[Zo=sqrt(Z./Y);\]
\[Zop=sqrt(Zp./Yp);\]
\[gamma=real(gamma);\]
\[alphap=real(gammap);\]
\%(exp(-alphap*Length)-1)/(alphap*Length) \}^2 \%
%trying to understand
the effect of loss on the bandwidth
alphadBmm=alpha*8.686e-3;
alphadBmmp=alphap*8.686e-3;
beta=imag(gamma);
betap=imag(gammap);

\[\lambda=2*\pi/\beta;\]
\[
\text{lambda}_p = \frac{2\pi}{\beta_p};
\]
\[
\text{neff} = \frac{c}{(f \cdot \lambda_p)};
\]
\[
\text{neff}_p = \frac{c}{(f \cdot \lambda_p)};
\]
\[
\text{epsiloneff} = \text{neff}^2;
\]
\[
\text{epsiloneff}_p = \text{neff}_p^2;
\]
\[
\text{transmission}_S = 1 - \text{reflection}_S;
\]
\[
\text{reflection}_L = \left(1 + \text{reflection}_L \cdot \exp(-2 \cdot \gamma_p \cdot \text{Length})\right) \cdot \left(1 - \text{reflection}_L \cdot \exp(-2 \cdot \gamma_p \cdot \text{Length})\right);
\]
\[
\text{T}_1 = 2 \cdot \text{Zin} \cdot (\frac{\text{Zs} + \text{Zin}}{\text{Zs}});
\]
\[
\beta_{\text{opt}} = \frac{w \cdot \text{nopt}}{c};
\]
\[
\text{Mo} = \text{abs}\left(\frac{\text{transmission}_S \cdot (1 - \text{reflection}_S \cdot \exp(-2 \cdot \gamma_p \cdot \text{Length}))}{(j \cdot \beta_{\text{opt}} - \gamma_p) \cdot \text{Length}}\right)^2;
\]
\[
\text{Mo}_2 = \text{abs}\left(\frac{\text{T}_1 \cdot (1 - \text{reflection}_S \cdot \exp(-2 \cdot \gamma_p \cdot \text{Length}))}{(j \cdot \beta_{\text{opt}} + \gamma_p) \cdot \text{Length}}\right)^2;
\]
\[
\text{Z}_{\text{junct}} = \frac{1}{(G_p + j \cdot w \cdot C_p)};
\]
\[
\text{M} = \text{Mo} \cdot \text{abs}\left(\frac{\text{Z}_{\text{junct}} \cdot \text{Y}_p}{1 - \text{reflection}_L \cdot \exp(-2 \cdot \gamma_p \cdot \text{Length})}\right)^2;
\]
\[
\text{M}_{\text{dB}} = 10 \log_{10}(\text{M});
\]
\[
\text{M}_{\text{dB}}^2 = 10 \log_{10}(\text{M}_2);
\]
\[
\text{figure}(1);
\]
\[
\text{plot}(\text{f}, \text{real}(Zo), '\ '+);
\]
\[
\text{hold}
\]
\[
\text{plot}(\text{f}, \text{real}(Zop))
\]
\[
\text{xlabel}(\text{'Frequency (GHz)'})
\]
\[
\text{ylabel}(\text{'Zo (Ohm)'})
\]
2. The improved TWEAM equivalent circuit model implementation

function zomushtransreflect3()
format long e

%%%%%%%%%%%%%%%%%%%%%% universal physical constants
%%%%%%%%%%%%%%%%%%%%%%%
muo= 4*pi*1e-7; %Henrys/meter
epsilon= 8.854187e-12; %Farads/meter
c= 2.99792458e8; %meters/second (definition)
etao= sqrt(muo/epsilon); %ohms

%%%%%%%%%%%%%%%%%%%%%%% device structure constants
%%%%%%%%%%%%%%%%%%%%%%%%
mesawidth= 2e-6; %meters
gap= 10e-6; %meters
topmetalwidth= 10e-6; %meters
bottommetalwidth= 1.5e-6; %meters
playerthickness= 0.7e-6; %meters
ilayerthickness= 0.21e-6;%0.5e-6; %meters
nlayerthickness= 2e-6; %meters
%nstumpthickness= 0;%0.6e-6; %meters %not used at the moment
bcbtopthickness= 0.2e-6; %meters
topmetalthickness= 0.6e-6;0.6e-6; %meters
contactmetalthickness= 0.18e-6; %meters
bottommetalthickness= topmetalthickness + contactmetalthickness; %meters
rhoc= 5e-6 /10000; %/10000 converts from ohm-cm^2 to ohm-m^2
playerconductivity = 100/0.026; \%100/ converts 1/ohm-cm to Siemens/meter
ilayerconductivity = 1e-20; \%Siemens/meter
nlayerconductivity = 100/0.0019; \%100/ converts 1/ohm-cm to Siemens/meter
Auconductivity = 40.9e6; \%Siemens/meter
surfaceroughnessconductivity = 1e20; \%Siemens/meter
effectiveAuconductivity = 1/(1/Auconductivity + 1/surfaceroughnessconductivity); \%Siemens/meter

epsilon_rsc = 12.7;
epsilon_rbc = 2.5;
\%epsilon_r = 12.7 for ilayer, \~8.9 for AlN, 2.5 for BCB, 1.0 for Air

Z_s = 50; \%50; \%ohm
Z_L = 50; \%50; \%ohm
nopt = 3.3; \%optical group velocity index
Length = 2000e-6; \%active length of device (in meters)

f = linspace(0.25e9, 18e9, 50);
w = 2*pi*f; \%I used 'w' in lieu of 'omega'

%%%%%% circuit element calculations

%%%%%% parallel circuit elements %%%%%%%

%it's possible that the 'bottommetalwidth' here (and in L section) should be 'mesawidth' instead, don't know which fits the data better yet
metalskindepth = skindepth(effectiveAuconductivity, w);
\%[ds]=skindepth(conductivity, radianfrequency);
ext_effectivebottommetalthickness = effectivethickness(metalskindepth, bottommetalthickness); \%[teff]=effectivevethickness(ds, totalthickness);
ext_effectivetopmetalthickness = effectivethickness(metalskindepth, topmetalthickness); \%[teff]=effectivevethickness(ds, totalthickness);
topmetalminusbottommetalwidthhalfdifference = 0.5*(topmetalwidth-bottommetalwidth);
ext_effectivetopmetalwidth = bottommetalwidth + 2*effectivethickness(metalskindepth, topmetalminusbottommetalwidthhalfdifference ); \%[teff]=effectivevethickness(ds, totalthickness);
Rmettop = 1./(effectiveAuconductivity*(bottommetalwidth*(effectivebottommetalthickness) + (topmetalwidth-bottommetalwidth).*effectivevethickness));

playerskindepth = skindepth(playerconductivity, w);
\%[ds]=skindepth(conductivity, radianfrequency);
ext_effectiveplayerthickness = effectivethickness(playerskindepth, playerthickness); \%[teff]=effectivevethickness(ds, totalthickness);
Rplayerparallel = 1./(playerconductivity*mesawidth*effectiveplayerthickness);}
nlayerskindepth= skindepth(nlayerconductivity, w);
\[(ds)=\text{skindepth}(\text{conductivity, radianfrequency});
\]
effectivenlayerthickness= effectiveethickness(nlayerskindepth, nlayerthickness); \[\text{[\text{\[ds\]}]}=\text{effectiveethickness}(ds, \text{totalthickness});\]
Rnlayerparallel= 1./( nlayerconductivity*(mesawidth + 2*nlayerskindepth).*effectivenlayerthickness );

gapp= gap + 0.5*(topmetalwidth - mesawidth);
Rmetgnd= 0.6*1./( effectiveAuconductivity*2*(nlayerskindepth- gapp).*metalskindepth );
\%**************
\text{that 1.8 factor makes a big difference in the Rmet value because}\n\% Rnlayerparallel is pretty large in comparison to Rmetgnd
\%**************

bottommetalcenterofmass= centerofmass(metalskindepth, bottommetalthickness); \[\text{xcm}\]=centerofmass(ds, totalthickness);
nlayercenterofmass= centerofmass(nlayerskindepth, nlayerthickness); \[\text{xcm}\]=centerofmass(ds, totalthickness);
\%*************
nlayercenterofmass=nlayercenterofmass*1;
\%*************
effectiveLbottomheight= 1*bottommetalcenterofmass + playerthickness +
ilayerthickness + 1*nlayercenterofmass;
Lbottom= muo*effectiveLbottomheight/bottommetalwidth

simpleLtopwidth= (topmetalwidth - bottommetalwidth);
simpleLtopheight= bcbtopthickness + playerthickness + ilayerthickness + 
1*nlayercenterofmass;
\%thickstriptothinstripLtopwidth=
thickstriptothinstripLtopwidth(simpleLtopwidth, simpleLtopheight, 
effectivetopmetalthickness, 1); \[\text{wp}\]=thickstriptothinstripLtopwidth(w, h, 
t, k);
topmetalcenterofmass= centerofmass(metalskindepth, topmetalthickness);
\[\text{xcm}\]=centerofmass(ds, totalthickness);
effectiveLtopheight= topmetalcenterofmass -
0*0.5*effectivetopmetalthickness + simpleLtopheight;
\%effectiveLtopwidth= effectiveLtopwidth(thickstriptothinstripLtopwidth, 
effectiveLtopheight); \[\text{weff}\]=effectiveLtopwidth(wp, h);
Ltop=muo*effectiveLtopheight./effectiveLtopwidth;
Ltop=muo*effectiveLtopheight./simpleLtopwidth;

%\text{etam}=\sqrt(j*w*muo/Auconductivity);%
%\text{etaxmo}=\text{etam}.*\text{coth}((1+j)*topmetalthickness./skindepth);
%\text{zm}=etaxmo/topmetalwidth;

Rmet= 1./( 1./Rmettop + 1./Rplayerparallel ) + 1./( 1./Rnlayerparallel + 1./Rmetgnd )
L= 1./( 1./Ltop +1./Lbottom ) %this method of including the L of the
\text{topmetal was found to be the most accurate estimation after running my}
\text{poisson solver}

Rmet=Rmet*1.0;%*1.33;
L=L*1.50;
Z = R_{\text{net}} + jwL;

%%%%%% perpendicular circuit elements %%%%%%%

R_{\text{c}} = \rho_{\text{heoc}}/\text{bottommetalwidth}

%playerperpendicular = \text{playerthickness}/(\text{playerconductivity} \times \text{mesawidth}) * 1e-10

[playercenterofmass] = \text{centerofmass}(\text{playerskindepth}, \text{playerthickness});
%[xcm] = \text{centerofmass}(ds, \text{totalthickness});
%effectiveplayerthickness = \text{bottommetalcenterofmass} + \text{playerthickness} - playercenterofmass;
%C_{\text{player}} = \varepsilon_{\text{rsc}} \times \varepsilon_{\text{o}} \times \text{mesawidth} / \text{effectiveplayerthickness};

%(200 is just a random number that should be high enough. The sqrt(200) is to correct the capacitance driven Rwit
withdiel function)

waveimpedanceforR_{\text{ilayerperpendicular}}with\text{dielectric} =
effectivewaveimpedance\text{withdielectric}(\text{mesawidth}, ilayerthickness, 200);
%[Rwithdiel] = effectivewaveimpedance\text{withdielectric}(wp, h, k);
\text{effective}\text{mesawidth} =
etao*ilayerthickness./(waveimpedanceforR_{\text{ilayerperpendicular}}with\text{dielectric} * \sqrt{200});

R_{\text{ilayerperpendicular}} = ilayerthickness/(ilayerconductivity*effective\text{mesawidth})

%simpleCilayerheight = playercenterofmass + ilayerthickness; % + 0* nlayercenterofmass;
simpleCilayerheight = ilayerthickness; % + 0* nlayercenterofmass;
thickstrip\text{tothinstrip}Cilayerwidth\text{withdielectric} =
\text{thickstrip\text{tothinstrip}width}(\text{mesawidth}, simpleCilayerheight, effectiveplayerthickness + bcbtopthickness, \varepsilon_{\text{rsc}} - \varepsilon_{\text{rbcb}});
%[wp] = thickstrip\text{tothinstrip}width(w, h, t, k);
thickstrip\text{tothinstrip}Cilayerwidth\text{withoutdielectric} =
\text{thickstrip\text{tothinstrip}width}(\text{mesawidth}, simpleCilayerheight, effectiveplayerthickness + bcbtopthickness, 1);
%[wp] = thickstrip\text{tothinstrip}width(w, h, t, k);
\text{effectiveCilayerheight} = playercenterofmass - 0.5*effectiveplayerthickness + simpleCilayerheight;
waveimpedance\text{forCilayer}\text{with\text{dielectric}} =
effectivewaveimpedance\text{with\text{dielectric}}(\text{thickstrip\text{tothinstrip}Cilayerwidthw ith\text{dielectric}}, simpleCilayerheight, \varepsilon_{\text{rsc}} - \varepsilon_{\text{rbcb}});
%[Rwithdiel] = effectivewaveimpedance\text{with\text{dielectric}}(wp, h, k);
waveimpedance\text{forCilayer}\text{without\text{dielectric}} =
effectivewaveimpedance\text{with\text{dielectric}}(\text{thickstrip\text{tothinstrip}Cilayerwidthw ithout\text{dielectric}}, simpleCilayerheight, 1);
%[Rwithdiel] = effectivewaveimpedance\text{with\text{dielectric}}(wp, h, k);

C_{\text{ilayer1}} =
\text{waveimpedance\text{forCilayer}without\text{dielectric}} / (\text{waveimpedance\text{forCilayer}with\text{dielectric}}^2 * c);
C_{\text{ilayer2}} = \varepsilon_{\text{rbcb}} / (\text{waveimpedance\text{forCilayer}without\text{dielectric}} * c);
C_{\text{ilayer}} = C_{\text{ilayer1}} + C_{\text{ilayer2}}

simpleCbcbwidth = (\text{topmetalwidth} - \text{mesawidth});
simpleCbcbheight = bcbtopthickness + playerthickness + ilayerthickness + 0*nlayercenterofmass;
topmetalheight = bcbtopthickness + playerthickness;
effectiveepsilonrbcb = 1/(1/(topmetalheight+ilayerthickness))*(topmetalheight/epsilonrbcb + ilayerthickness/epsilonrsc);
thickstripothinstripCbcbwidthwithdielectric = thickstripothinstripwidth(simpleCbcbwidth, simpleCbcbheight, topmetalthickness, effectiveepsilonrbcb);
%[wp]=thickstripothinstripwidth(w, h, t, k);
thickstripothinstripCbcbwidthwithoutdielectric = thickstripothinstripwidth(simpleCbcbwidth, simpleCbcbheight, topmetalheight, 1);
%[wp]=thickstripothinstripwidth(w, h, t, k);
%effectiveCbcbheight = 0*topmetalcenterofmass - 0*0.5*effectivetopmetalthickness + simpleCbcbheight;
waveimpedanceforCbcbwithdielectric = effectivewaveimpedancewithdielectric(thickstripothinstripCbcbwidthwith
dielectric, simpleCbcbheight, effectiveepsilonrbcb);
%[Rwithdiel]=effectivewaveimpedancewithdielectric(wp, h, k);
waveimpedanceforCbcbwithoutdielectric = effectivewaveimpedancewithdielectric(thickstripothinstripCbcbwidthwithout
dielectric, simpleCbcbheight, 1);
%[Rwithdiel]=effectivewaveimpedancewithdielectric(wp, h, k);
Cbcb = waveimpedanceforCbcbwithoutdielectric.(waveimpedanceforCbcbwithdielectric.^2*c)

Rnlayerperpendicular = 0.5*gap/(nlayerconductivity*nlayerthickness)
%this is a very rough approximation, but it should get within 50-100% or so (this is tolerable because it is small in comparison to Rc)

Cilayer=Cilayer;*2.9/1.6;*2.9;
Cbcb=Cbcb;*2.9;

%Y= 1./( Rc + Rnlayerperpendicular + 1./( j*w.*Ccbcb+ 1./
1./((1./Rplayerperpendicular + j*w.*Cplayer) +
1./((1./Rilayerperpendicular + j*w.*Cilayer) ) ) ));
Y= 1./( Rc + Rnlayerperpendicular + 1./(1./Rilayerperpendicular +
 j*w.*Cilayer + j*w.*Cbcb) );

%%%%%%%%%%%%%%%%%%%%% microwave circuit calculations
%%%%%%%%%%%%%%%%%%%%%%

Zo=sqrt(Z./Y);
gamma=sqrt(Z.*Y);

alpha=real(gamma);
alphadBmm=alpha*8.686e-3;
beta=imag(gamma);

lambda=2*pi./beta;
neff=c./(f.*lambda);
epsilononeff=neff.^2;
\[ \text{reflectionS} = \frac{Z_s - Z_0}{Z_s + Z_0}; \]
\[ \text{reflectionL} = \frac{Z_L - Z_0}{Z_L + Z_0}; \]
\[ \text{transmissionS} = 1 - \text{reflectionS}; \]
\[ Z_{\text{in}} = Z_0 \cdot \frac{(1 + \text{reflectionL} \cdot \exp(-2\gamma L))}{(1 - \text{reflectionL} \cdot \exp(-2\gamma L))}; \]
\[ T_1 = 2 \cdot Z_{\text{in}} / (Z_s + Z_{\text{in}}); \]
\[ \beta_{\text{opt}} = w \cdot n_{\text{opt}} / c; \]
\[ M_0 = \left| \frac{\text{transmissionS}}{1 - \text{reflectionL} \cdot \text{reflectionS} \cdot \exp(-2\gamma L)} \right| \cdot \frac{(\exp((j\beta_{\text{opt}} - \gamma) L) - 1)}{(\exp((j\beta_{\text{opt}} + \gamma) L) - 1)}; \]
\[ M_0^2 = \left| \frac{T_1}{1 - \text{reflectionL} \cdot \text{reflectionS} \cdot \exp(-2\gamma L)} \right| \cdot \frac{(\exp((j\beta_{\text{opt}} - \gamma) L) - 1)}{(\exp((j\beta_{\text{opt}} + \gamma) L) - 1)}; \]

\[ C_{\text{total}} = C_{\text{ilayer}} + C_{\text{cb}}; \]
\[ Z_{\text{junct}} = \frac{1}{1/R_{\text{ilayerperpendicular}} + j \omega C_{\text{total}}}; \%
\text{M is not an entirely accurate capacitance to use, but it's better than nothing} \]
\[ M = M_0 \cdot \left| Z_{\text{junct}} \cdot Y \right|^2; \]
\[ M_2 = M_0^2 \cdot \left| Z_{\text{junct}} \cdot Y \right|^2; \]
\[ \text{MDB} = 10 \cdot \log_{10}(M); \]
\[ \text{MDB}^2 = 10 \cdot \log_{10}(M_2); \]
\[ \text{maxMDB} = \text{max(MDB)}; \%
\[ \text{bandwidthfull} = f(\text{find}((\text{maxMDB} - 3) < \text{MDB})); \%
\text{ Ditto} \]
\[ \% \text{bandwidth} = f(\text{find}((\text{MDB}(1) - 3) > \text{MDB}(1))); \]
\[ \% \text{bandwidth} = f(\text{find}(-3 < \text{MDB}, 1, 'last')); \]
\[ \% \text{maxMDB2} = \text{max(MDB2)}; \%
\[ \% \text{bandwidth2} = f(\text{find}((\text{maxMDB2} - 3) < \text{MDB2}, 1, 'last')); \%
\[ \%
\% \text{plotting section} \]
\[ f = f \cdot 10^{-9}; \]
\[ \text{figure(1)} \]
\[ \text{plot}(f, \text{real}(Z_0)) \]
\[ \text{hold} \]
\[ \text{plot}(f, \text{imag}(Z_0)) \]
xlabel('Frequency (GHz)')
ylabel('Zo (Ohm)')

Zohif=Zo(length(Zo))

figure(2)
hold
plot(f,alphadBmm)
xlabel('Frequency (GHz)')
ylabel('waveguide loss (dB/mm)')

figure(3)
hold
plot(f,neff)
xlabel('Frequency (GHz)')
ylabel('waveguide index')

return; %temporarily placed here to reduce clutter (by not plotting any bandwidth stuff)

figure(4)
plot(f,MdB)
%hold
%plot(f,MdB2)
%plot(f,real(transmissionS),'r')
%plot(f,real(T1),'g')
xlabel('Frequency (GHz)')
ylabel('EO response (dB)')

figure(5)
plot(f,MdB*bandwidth)
xlabel('Frequency (GHz)')
ylabel('EO response (dB) * BW')

return;

%%%%%%%%%%%%%%%%%%%%%%%%%% end of main function
%%%%%%%%%%%%%%%%%%%%%%%%%%
%---------------------------------------------------------------
---$
%%%%%%%%%%%%%%%%%%%%%%%%%% subfunction section
%%%%%%%%%%%%%%%%%%%%%%

%[ds]=skindepth(conductivity, radianfrequency);
function [ds] = skindepth(conductivity, radianfrequency)
muo= 4*pi*1e-7; %Henrys/meter (muo has to be repeated here because Matlab does not pass even global variables into subfunctions. Note: each function's variables are local.)
ds= sqrt(2./(radianfrequency*muo*conductivity));
return;

[%xcm]=centerofmass(ds, totalthickness);
function [xcm] = centerofmass(ds, totalthickness)
lds = -totalthickness./ds;
xcm = (exp(lds).*/(lds-1)+1)./(1./ds.*(1-exp(lds)));
return;

%[teff]=effectivethickness(ds, totalthickness);
function [teff] = effectivethickness(ds, totalthickness)
  teff = ds.*(1-exp(-totalthickness./ds));
  return;

%[wp]=thickstriptothinstipwidth(w, h, t, k);
function [wp] = thickstriptothinstipwidth(w, h, t, k) %from MTT-25
  no.8, pp.631-47, (1977).  good for 0 < t/h < 1, 0.1 < w/h < 10
  dw= (t/pi).*log( 4*exp(1)./(w./h).^2 + (1/pi)./(w./t + 1.10) ).^2  );
  wp= w + dw/k;
  return;

%[weff]=effectivewidth(wp, h);
function [weff] = effectivewidth(wp, h) %from MTT-25 no.8, pp.631-47,
  (1977).  good for 0.1 < w/h < 10
  etao=3.767303308559356e+002; %ohms
  hwp=8*h./wp;
  R1= 30*log( 1 + 0.5*hwp.*( sqrt(hwp.^2 + pi^2) ) );
  weff= etao*h./R1;
  return;

%[Rwithdiel]=effectivewaveimpedancewithdielectric(wp, h, k);
function [R] = effectivewaveimpedancewithdielectric(wp, h, k) %from
  MTT-25 no.8, pp.631-47, (1977).  good for 0.1 < w/h < 10, 1 < k < 16 at
  least!  dielectric slab everywhere under conductive strip
  hwp=4*h./wp;
  R= ( 42.4/sqrt(k+1) )*log( 1 + hwp.*( ((14+8/k)/11)*hwp + sqrt(
    ((14+8/k)/11)^2*hwp.^2 + (1+1/k)*0.5*pi^2 )) )
  return;

w=3.3e-4;
h=3.05e-4;
t=0.344e-4
dw= (t/pi).*log( 4*exp(1)./(t./h).^2 + (1/pi)./(t + 1.10) ).^2  );
thickstriptothinstripCilayerwidthkequalto1= w + dw;
thickstriptothinstripCilayerwidthkequalto12minus2point5= w + dw*1/(12-2.5);

wp=thickstriptothinstripCilayerwidthkequalto12minus2point5;
h=3.05e-4;
k=12-2.5;
hwp=4*h./wp;
waveimpedanceforCilayerwithdielectric= ( 42.4/sqrt(k+1) )*log( 1 +
hwp.*( ((14+8/k)/11)*hwp + sqrt( ((14+8/k)/11)^2*hwp.^2 +
(1+1/k)*0.5*pi^2 )) );
wp=thickstripothinstripCilayerwidthkequalto1;
k=1;
waveimpedanceforCilayerwithoutdielectric= ( 42.4/sqrt(k+1) )*log( 1 + hwp.*(((14+8/k)/11)*hwp + sqrt( ((14+8/k)/11)^2*hwp.^2 + (1+1/k)*0.5*pi^2 )) );
Cilayer1= waveimpedanceforCilayerwithoutdielectric./(waveimpedanceforCilayerwithdielectric^2* 3e8);
Cilayer2= 2.5/(waveimpedanceforCilayerwithoutdielectric* 3e8);
Cilayer= Cilayer1+Cilayer2