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S.K. Cheung
(M.S. Thesis)

June 1986

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High Temperature Stability of W/GaAs Schottky Contacts: Structural and Electrical Studies

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M. S. Thesis

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ABSTRACT

Rapid developments in self-aligned-gate GaAs MESFET technology have made the characterization of high-temperature-stable metal/GaAs Schottky contacts an active area of research. Our study attempts to provide an understanding of the thermal stability of the W/GaAs Schottky contact.

W/GaAs Schottky diodes were fabricated and furnace-annealed in the temperature range 100°C-900°C. The diodes were characterized by current-voltage (I-V) and capacitance-voltage (C-V) dependences, Rutherford Backscattering Spectrometry (RBS), Scanning Electron Microscopy (SEM), and Transmission Electron Microscopy (TEM). Deviations from ideal diode behavior were observed at annealing temperatures above 600°C. Interdiffusion of W and GaAs was observed at 650°C by RBS. Our results strongly suggest that the electrical degradation of the diodes is correlated with the formation of a highly resistive layer near the W/GaAs interface. The high resistance of this layer may be attributed to the compensation of substrate dopants by the in-diffused W atoms. Annealing the diodes at temperatures above 850°C resulted in reactions between W and GaAs. The W-GaAs reaction led to the formation of islands of W_2As_3 at the W/GaAs interface resulting in physical breakdown of the W/GaAs diode.
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High Temperature Stability of W/GaAs Schottky Contacts: Structural and Electrical Studies
1. Introduction

Gallium arsenide (GaAs) has become an increasingly important semiconductor material for high performance solid-state electronic devices. Much research activity has been devoted to the development of GaAs devices for high speed analog and digital integrated circuit applications [1-4]. The primary advantages of GaAs include its high electron mobility at low electric field and its ability to exhibit semi-insulating properties when compensated with deep-level impurities. The high resistivity of semi-insulating (SI) GaAs minimizes the parasitic capacitance in an integrated circuit. One of the major active devices in today's GaAs integrated circuits is the Metal-Semiconductor Field Effect Transistor (MESFET). Figure 1.1 shows the cross section of a typical planar GaAs MESFET structure fabricated by localized implantation into semi-insulating (= 10⁸ Ω cm) GaAs [5]. The basic structure consists of a thin (t = 1000 Å) n-type (typically N_d = 2*10¹⁷ cm⁻³) active region (the channel) joining two ohmic contacts (separated typically by a distance of L_ch=3-5 μm) with a narrow (L_g=1 μm) metal Schottky barrier gate separating the source and drain. In essence, a MESFET is a voltage-controlled resistor. The Schottky gate above the channel (Figure 1.1) serves as the control element when reverse bias is applied to it. The conducting n-channel is confined between the gate depletion region and the semi-insulating GaAs substrate which is usually at ground potential. If the drain is biased positively,
current flows from it to the source through the channel. If the source is now grounded and a negative voltage is applied to the gate electrode, the gate depletion region widens and the channel narrows. As the channel narrows, its resistance increases, and less current flows from the drain to the source. Consequently, a voltage signal applied to the gate controls the current flowing through the channel. It is the objective of our study to investigate the electrical and structural characteristics of such a Schottky gate contact on GaAs.

A variety of approaches have been developed for the fabrication of GaAs MESFET [6-10]. Recently, N. Yokoyama et al. [11] have proposed the self-aligned-gate fabrication technology. In this technique, the gate serves as the implantation mask for the formation of highly doped (n\textsuperscript{+}) source and drain regions of the GaAs MESFET. Post-implant annealing activates the implanted dopants in the source and drain regions and removes crystalline damages caused by implantation. A major concern in this self-aligned-gate process is the selection of a refractory material for use as the gate such that the Schottky barrier remains stable at the n\textsuperscript{+} post-implant anneal temperature (typically 850°C).

Various metal-GaAs systems have been studied for their high-temperature electrical and structural stability. Ti/W films on GaAs exhibit stable Schottky diode characteristics above 740°C [12]. Different refractory metal silicides including Ti/W silicides [13], W-silicides [14], and Ta-silicides [15] were also reported as promising candidates for the gate material of self-aligned GaAs.
MESFET. Sputter-deposited W/Al film was found to be a low-resistive and thermally stable gate metal which can form a stable Schottky contact with n-GaAs even after annealing at 900°C [16]. Electron-beam evaporated W film on GaAs [17] was reported to have good thermal stability up to 950°C. WN films deposited on GaAs by reactive sputtering exhibit good Schottky diode characteristics even after annealing at 800°C [18]. There appears to be a close correlation between the chemical stability of a given metal-GaAs system and the stability of the corresponding diode electrical characteristics. For instance, the high-temperature stable Schottky diode characteristics of the various refractory metal silicides on GaAs can be attributed to the relative chemical inertness of the silicides with respect to the underlying GaAs. On the other hand, GaAs Schottky diodes made from the metals Pt [19,20], Pd [21], Au [20], and Al/Ti [22] show degradations in electrical characteristics when the diodes are annealed at temperatures above 500°C. The electrical degradation of these metal-GaAs contacts are believed to be caused by the interfacial chemical interactions between the metals and the GaAs substrate [23]. Recently, S. S. Lau et al. [24] have correlated the thermal stability of Schottky barriers on GaAs with the thermodynamic driving force for chemical reaction between the metallic contacts and the substrate. They have established a minimum requirement for the electrical stability of a metal/GaAs contact after a high-temperature anneal, namely, the enthalpy of reaction, $\Delta H_{298}$, between the metal and the GaAs has to be positive. In essence, they assumed no change
in the entropy of reaction so that a positive enthalpy of reaction implies a thermodynamically unfavorable reaction. Such chemical inertness between the metal and GaAs leads to electrical stability of the metal/GaAs contact.

In this study, we attempt to correlate the electrical characteristics of W/n-GaAs Schottky diodes with the metallurgical interactions between W and GaAs after high-temperature annealing. A. K. Sinha et al. [20] have reported stable electrical characteristics of W/n-GaAs Schottky diodes annealed at temperatures up to 500°C. J. R. Waldrop [25] observed electrical instability of W/n-GaAs diodes annealed at temperatures above 600°C. High-temperature stability of W/GaAs Schottky diode annealed up to 950°C under As overpressure was investigated by K. Matsumoto et al. [26]. They reported stable electrical characteristics for diodes annealed up to 950°C despite their observation of interdiffusion of W and GaAs at the same temperature. A possible explanation of such high-temperature electrical stability of the diodes is the formation of a chemically stable compound at the W/GaAs interface assisted by the As overpressure prevalent during the annealing process. The objective of our study is to investigate the degradation mechanisms of W/GaAs Schottky diodes which have been annealed in a nitrogen atmosphere up to 900°C. An understanding of the failure mechanisms which occur during annealing helps one design a better Schottky diode metallization scheme which is compatible with high-temperature process conditions.
1.1 Motivation of Study

Among the various technologies available for the fabrication of GaAs MESFET, the self-aligned-gate (SAG) approach [11] has proved to be particularly promising. A critical aspect of the self-aligned-gate MESFET process is the selection of a high-temperature stable gate metallization.

As a potential candidate for the gate contact in the SAG MESFET process, W/n-GaAs Schottky diodes are characterized electrically and structurally in this study. We attempt to explore the correlations between electrical degradations of the diodes after high-temperature annealing with metallurgical changes that occur at the metal/GaAs interface. A basic understanding of the possible failure mechanisms of the W/n-GaAs diodes after high-temperature annealing would be fruitful from both the material science and the technology standpoint. Information about the thermal stability of W/n-GaAs Schottky contacts may help one design a better gate metallization scheme for application in the SAG MESFET process.

1.2 Review of Schottky Barrier Junctions

1.2.1 Introduction

Metal-semiconductor interfaces play an important role in semiconductor device technology. Electrical contacts have to be made to the semiconductor to operate it, and this contact almost always involves a metal-semiconductor interface. One type of metal-semiconductor interface is called the ohmic contact in which
the interface offers minimum resistance to current flow in either direction over a wide temperature range. The other type of metal-semiconductor interface offers low resistance to current flow in one direction and very high resistance to the opposite direction of current flow. Such a current rectifying contact is commonly referred to as a Schottky barrier, after W. Schottky [27], who first proposed a model for barrier formation.

A brief review of the basic physics and electrical characteristics of rectifying metal-semiconductor contacts is given in the following sections. In section 1.1.2, various models of Schottky barrier formation are discussed. Section 1.1.3 provides a brief description of the various current transport mechanisms and the resulting current-voltage characteristics. Capacitance-voltage characteristics of Schottky barriers are the subject of section 1.1.4. A number of reviews on the physics of Schottky barriers and their technological applications have been published [28-32].

1.2.2 Models of Schottky Barrier Formation

(A) The Classic Schottky Theory

When a semiconductor is contacted by a metal, charge transfer between the metal and the semiconductor gives rise to a region devoid of mobile carriers (the depletion region) in the semiconductor and a potential barrier at the metal-semiconductor interface. The earliest model put forward to explain the barrier height is that of Schottky [27] and Mott [33]. According to this
model the barrier for mobile charges to go from the semiconductor to the metal results from the difference in the work functions of the two materials. Figure 1.2(a) shows the electron energy band diagram of a metal with work function $\phi_m$ and a n-type semiconductor with work function $\phi_s$ which is smaller than $\phi_m$. The work function of a metal is defined as the amount of energy required to raise an electron from the Fermi level to the vacuum level which is the energy level of an electron outside the metal with zero kinetic energy. The work function $\phi_s$ of the semiconductor is similarly defined and is a variable quantity because the Fermi level in the semiconductor varies with doping. A parameter independent of the doping in the semiconductor is the electron affinity $\chi_s$ which is defined as the energy difference of an electron between the vacuum level and the lower edge of the conduction band. Figure 1.2(b) shows the energy band diagram of the metal-semiconductor system at thermal equilibrium. When the metal is brought into intimate contact with the semiconductor, electrons from the conduction band of the semiconductor, which have higher energy than the metal electrons, flow into the metal until a single Fermi level characterizes both the metal and the semiconductor. The conduction band electrons which cross over into the metal leave behind a region depleted of mobile electrons. This space charge region in the semiconductor adjacent to the metal consists of immobile positively charged ionized donors. The electrons which cross over from the semiconductor accumulate at the metal forming a thin sheet of negative charge at the metal-semiconductor interface. Consequently
an electric field is established from the semiconductor to the metal. This built-in electric field prevents further charge exchange between the metal and the semiconductor once thermal equilibrium is established. For a metal-semiconductor system in thermal equilibrium the important point which determines the barrier height is that the vacuum level must remain continuous from the metal side to the semiconductor side. The resultant band bending is equal to the difference between the two work functions. This difference is given by \( qV_i = (\phi_m - \phi_s) \), where \( V_i \) is expressed in volt and is known as the contact potential or built-in potential of the junction. This built-in potential represents the barrier which an electron moving from the semiconductor into the metal has to overcome. Electrons moving in the opposite direction (from metal to semiconductor) encounter a different potential barrier which is given by

\[
\phi_B = (\phi_m - \chi_S)
\]

where \( \chi_S \) is the electron affinity of the semiconductor and \( \phi_B \) is commonly known as the barrier height of the metal-semiconductor Schottky contact. Equation (1) suggests that the barrier height \( \phi_B \) increases linearly with the metal work function \( \phi_m \). However, most practical metal-semiconductor contacts do not appear to obey this rule. Strong dependence of barrier height on \( \phi_m \) is observed only in predominantly ionic semiconductors (e.g. II-VI semiconductors). For III-V and Group IV semiconductors, the barrier
height is almost independent of $\phi_m$. The insensitivity of barrier height to the metal work function in covalently bonded semiconductors was first explained by Bardeen [34], who proposed that Schottky barrier heights are due to Fermi-level pinning by localized surface states.

(B) Fermi-level pinning

At the surface of a semiconductor the periodicity of the crystal lattice is terminated. In a covalent crystal the surface atoms have neighbors only on the semiconductor side; on the vacuum side there are no neighbors with whom the surface atoms can make covalent bonds. Thus, each of the surface atoms has one broken covalent bond in which only one electron is present and the other is missing. These dangling bonds give rise to localized energy states at the semiconductor surface with energy levels lying in the forbidden gap. These surface states modify the charge in the depletion region and affect the barrier height. Figure 1.3(a) shows the electron energy band diagram for the surface of a n-type semiconductor. The surface states are usually continuously distributed in the band gap in such a way that when there is no band bending in the semiconductor the states are occupied by electrons up to a level $\phi_0$ making the surface electrically neutral. The states below $\phi_0$ are donor-like because they are neutral when occupied and are positive when empty. The surface of the semiconductor comes into equilibrium with the bulk semiconductor when electrons from the bulk occupy states above $\phi_0$ and the Fermi level at the surface aligns with that of the bulk. The surface then becomes negatively
charged and a depletion layer consisting of ionized donors is created in the semiconductor region near the surface. Thus, the presence of surface states leads to the formation of a potential barrier looking from the surface towards the bulk semiconductor even in the absence of a metal contact as shown in Figure 1.3(b). When a metal is now brought into contact with the semiconductor and equilibrium is reached, the Fermi level in the semiconductor must adjust by an amount equal to the contact potential by exchanging charges with the metal. If the density of surface states at the semiconductor surface is very large then the charge exchange can take place mainly between the metal and the surface states, leaving the space charge in the semiconductor practically unaffected. Consequently, the barrier height as shown in Figure 1.3(c) becomes independent of the metal work function and is given by

$$\phi_B = E_g - \phi_0$$

The barrier height is said to be "pinned" by surface states. In other words, the position of the Fermi level relative to the semiconductor bandgap at the interface is "pinned" by surface states and is insensitive to the contact metal. Much investigations have been devoted to the elucidation of the origins of these surface states. S. G. Louie et al. [35] have proposed that the Fermi level is pinned by states intrinsic to the metal-semiconductor interface, often called "metal-induced gap states" (MIGS). More recently, Spicer and co-workers [36] have suggested that the states pinning
the Fermi level are associated with native defects in the semiconductor, perhaps generated by the release of energy as metal is deposited on the semiconductor surface. O. F. Sankey et al. [37] have attributed Fermi-level pinning in III-V semiconductors to bulk-derived deep levels (e.g. the deep donor level for the antisite defect \( \text{As}_{\text{Ga}} \)) and dangling bond deep levels.

1.2.3 Current-Voltage Characteristics

Transport of charge carriers between the metal and the semiconductor of a Schottky barrier diode corresponds to current flow through the diode. There are four mechanisms by which the carrier transport can occur [38]: (i) thermionic emission of electrons and holes over the barrier, (ii) tunneling of electrons and holes through the barrier, (iii) carrier generation (or recombination) in the depletion region, and (iv) carrier recombination in the neutral region of the semiconductor which is equivalent to minority carrier injection. Process (i) is usually the dominant mechanism in Schottky barrier junctions in Si and GaAs and it leads to the ideal diode characteristics. Processes (ii) and (iii) cause deviations from ideal diode behavior. Process (iv) is relatively insignificant and contributes to current transport only when the region of a n-type semiconductor adjacent to the metal has a high concentration of holes; for example, when the barrier height of the n-type semiconductor is substantially higher than half the band gap of the semiconductor. In such case, holes (the minority
carriers) injection from the metal into the neutral region of the n-type semiconductor is possible when the diode is forward biased. The following two sections provide a brief description of the key current transport mechanisms across a typical metal/n-type semiconductor Schottky diode under forward and reverse bias conditions. The case for metal/p-type semiconductor is fully analogous.

1.2.3.1 Forward Characteristics

(i) Thermionic Emission

According to the thermionic emission theory, only those electrons whose kinetic energy exceeds the height of the junction potential barrier will be able to reach the top of the barrier and get across the junction. The current-voltage characteristics of a Schottky diode obeying the thermionic emission model is given by

$$I = I_s \left[ \exp \left( \frac{qV}{nkT} \right) - 1 \right]$$

where $n$ is often called the "ideality factor". For an ideal Schottky barrier where the barrier height is independent of the bias and current flows only due to thermionic emission $n=1$. $I_s$ is given by

$$I_s = A \times A^{**} T^2 \exp \left( -\frac{q\phi_B}{kT} \right)$$

where $A$ is the diode area, $A^{**}$ is the Richardson constant, $T$ is the temperature, $q$ is the electron charge, $\phi_B$ is the barrier
height, and \( k \) is the Boltzmann constant. Factors which make \( n \) larger than unity are the bias dependence of barrier height, electron tunneling through the barrier, and the carrier recombination within the depletion region. In effect, the value of \( n \) provides a measure of the deviation of a Schottky diode from ideal thermionic behavior.

(ii) Tunneling through the barrier

Besides thermionic emission, electrons can also be transported across the barrier by quantum mechanical tunneling. When the n-type semiconductor is so heavily doped that the Fermi level lies inside the conduction band, the depletion region will become very thin and electrons with energy close to the Fermi level can tunnel through the junction barrier from the semiconductor to the metal. This electron transport process in the forward direction occurs only in degenerate semiconductors, and except for very low forward biases, the I-V characteristics in the presence of tunneling can be described by the relation

\[
I = I_0 \exp\left(\frac{qV}{E_0}\right)
\]

where \( E_0 = E_{00}\coth(E_{00}/kT) \)

and \( E_{00} = (qh/4\pi)(N_d/m^*\varepsilon_s)^{1/2} \)

where \( m^* \) is the electron effective mass and \( h \) is Planck's constant. The pre-exponential factor \( I_0 \) is only weakly dependent on voltage and is a complicated function of barrier height, parameters of the semiconductor, and the temperature. When \( E_{00} \gg \)
kT, we have $E_0 = E_{00}$ and the slope of $\ln I$ versus $V$ plot is constant and independent of temperature $T$. At high temperature where $kT \gg E_{00}$, we get $E_0 = kT$ and the slope of the $\ln I$ versus $V$ plot is $q/kT$, which corresponds to thermionic emission.

(iii) Carrier Recombination in the Junction Depletion Region

The depletion region of the Schottky barrier at zero bias is in thermal equilibrium and the rate of electron-hole pair generation in this region is balanced by the rate of recombination. In the presence of an applied voltage the equilibrium electron-hole pair concentration is disturbed and there will be a net generation or a net recombination of carriers depending upon the polarity of the applied bias. If the junction is forward biased then electrons will be injected into the depletion region from the neutral bulk semiconductor and holes will be injected from the metal. These excess electron-hole pairs will recombine in the depletion region to give a forward recombination current. The recombination process is facilitated by recombination centers whose energy levels are near the center of the semiconductor band gap. For recombination through these mid-gap deep traps, the recombination current in the depletion region is given by

$$ I = I_{R0}[\exp(qV/2kT)-1] $$

with

$$ I_{R0} = qA n_i W/2 \zeta_0 $$

where $A$ is the diode area, $n_i$ is the intrinsic carrier
concentration, \( W \) is the depletion width, and \( \tau_0 \) is the minority carrier lifetime. In some cases, this current may be responsible for diodes with \( n > 1 \). Note that the exponential term in the recombination current rises as \((qV/2kT)\) whereas that in the thermionic emission current rises as \((qV/kT)\). This shows that the recombination current will be important only at low values of the forward bias.

1.2.3.2 Reverse Characteristics

(i) Schottky Barrier Lowering

The reverse current of a Schottky barrier junction should theoretically saturate at the value of \( I_s = AA^* T^2 \exp(-q\phi_B/kT) \) in accordance with the thermionic emission model. However, for most practical Schottky diodes the reverse current increases with increasing reverse bias. It can be shown that the reverse current increases as \( \exp(\Delta \phi_B/kT) \), where \( \Delta \phi_B \) is the Schottky barrier lowering at reverse bias. A primary cause of the barrier lowering is the image force on the electron emitted from the metal into the semiconductor. Figure 1.4 shows the electron energy diagram associated with the image force barrier lowering.

When an electron is at a distance \( x \) from the metal there exists an electric field perpendicular to the metal surface. This field may be calculated by assuming a hypothetical positive image charge \( q \) located at a distance \((-x)\) inside the metal. The force of attraction \( F \) between the electron and its image charge is \( q^2/4\pi\varepsilon_s(2x)^2 \) and the electron has a negative potential energy \( Fx = -q^2/16\pi\varepsilon_s x \) relative to that of an electron at infinity, as
shown by the dotted curve in Figure 1.4. This potential energy must be added to the barrier energy $-qE_x$ to obtain the total energy of the electron. As shown in Figure 1.4 the maximum in energy occurs at a distance $x_m$ from the metal surface and it can be shown that the magnitude $\Delta \phi_B$ of the barrier lowering is given by [38]

$$\Delta \phi_B = \left[ q^3 N_d (V_i - V)/(8 \pi^2 e_s^3) \right]^{1/4}$$

where $N_d$ is the donor concentration in the semiconductor, and $V$ is the applied voltage. For a reverse biased junction, $V$ is replaced by $(-V_R)$. Thus, when $\Delta \phi_B$ results from the image force lowering alone the reverse current will increase as $\exp(V_R^{1/4}/kT)$. Hence a plot of log $I_R$ versus $V_R^{1/4}$ should give a straight line.

(ii) Tunneling through the barrier

Besides the barrier lowering, tunneling of electrons from the metal into the semiconductor conduction band through the barrier can also cause the reverse current to increase with bias. The reverse current in the presence of tunneling can be written as [39]

$$I_R = I_0 \exp(qV_R/E')$$

where $E' = E_0 [(E_{00}/kT) - \tanh(E_{00}/kT)]^{-1}$

$I_0$, $E_0$, and $E_{00}$ have been defined previously in section A.2. Electron tunneling becomes particularly important near the edge of the metal contact where the junction curvature enhances the electric field which reduces the barrier height in this region. This edge
leakage is a common cause of the soft I-V characteristics in Schottky barrier diodes. Edge leakage can be eliminated by using a guard ring [40].

(iii) Generation Current in the Depletion Region

A further mechanism that contributes to the reverse current of a Schottky diode is the electron-hole pair generation in the depletion region of the reverse biased diode. As mentioned previously, the electron-hole pair generation process restores the thermal equilibrium concentration of the electron-hole pair which is disturbed by the applied bias. The generation current is directly proportional to the width of the depletion region $W$. Since $W$ varies as $(V_i + V_R)^{1/2}$, the generation current increases as the square root of the reverse bias. Carrier generation in the depletion region is a common cause of the lack of saturation of reverse current in GaAs Schottky diodes especially if the semiconductor has a high concentration of mid-gap deep levels.

1.2.4 Capacitance-Voltage Characteristics

The electric field and potential distribution in the depletion region of a Schottky barrier junction can be obtained from the solution of a one-dimensional Poisson equation. Assuming the semiconductor is n-type and uniformly doped, the Poisson equation at any point in the semiconductor can be written as

$$\frac{d^2 \phi}{dx^2} = \left(\frac{-q}{\varepsilon_S}\right)[N_d + p(x) - n(x)]$$
where $\phi$ is the potential at point $x$, $\varepsilon_s$ is the semiconductor permittivity, $N_d$ is the donor concentration, and $n(x)$ and $p(x)$ are the free electron and hole concentrations at any point $x$ in the semiconductor, respectively. It is assumed that all the donors are ionized. The Poisson equation can be simplified using the depletion approximation. In this approximation, the free carrier concentrations are assumed to fall abruptly from their equilibrium values $n_0$ and $p_0$ in the bulk neutral region to a negligibly small value in the depletion region. Using this approximation, the Poisson equation can be written as

$$\frac{d^2\phi}{dx^2} = \left(-\frac{q}{\varepsilon_s}\right)N_d \quad 0 < x < W$$

where $W$ is the width of the depletion region. After integration with respect to $x$ and using the condition that $d\phi/dx = 0$ at $x=W$, the electric field $E(x)$ in the depletion region can be expressed by

$$E(x) = -\frac{d\phi}{dx} = E_m[1-(x/W)]$$

where $E_m = -qN_dW/\varepsilon_s$

is the maximum electric field which occurs at $x=0$. A second integration with the boundary condition $\phi=0$ at $x=W$ leads to the following relation:

$$\phi(x) = \left(-\frac{qN_dW^2}{2\varepsilon_s}\right)[1-(x/W)]^2$$
Thus the potential varies parabolically with the distance in the
depletion region and has a maximum absolute value at \( x=0 \):

\[
\phi(0) = (\phi_i - V_a) = \frac{qN_d W^2}{2\varepsilon_s}
\]

where \( \phi_i \) is the built-in junction potential and \( V_a \) is the
externally applied voltage. \( V_a \) is taken to be positive for a
forward bias and negative for a reverse bias. The depletion width
can then be expressed as

\[
W = \left[ 2\varepsilon_s (\phi_i - V_a)/qN_d \right]^{1/2}
\]

The depletion width at zero bias, \( W_0 \), is obtained by setting
\( V_a = 0 \). Thus, it can be seen that \( W \) decreases below its value \( W_0 \)
in case of a forward bias and increases above \( W_0 \) in case of a
reverse bias. Figure 1.5 shows the electron energy band diagram at
a metal-semiconductor junction under externally applied bias.

A change in the applied voltage across the Schottky barrier
junction causes a change in the width of the depletion region. Such
a change is accompanied by the movement of charge carriers into or
out of the depletion region. This change in the depletion region
charge in response to a change in the applied voltage can be
modelled with a capacitance.
The space charge in the depletion region can be written as

\[ Q_s = qAN_dW = A[2q\varepsilon_s N_d(\phi_i - V_a)]^{1/2} \]

where \( A \) is the area of the junction contact. Under small-signal ac condition, the reverse biased junction will exhibit a capacitive behavior expressed by

\[ C = \frac{Q_s}{V_a} = A[2q\varepsilon_s N_d/2(\phi_i - V_a)]^{1/2} = A\varepsilon_s/W \]

where \( A\varepsilon_s/W \) represents the general result for small-signal capacitance. The total voltage drop across the junction can then be written as

\[ (\phi_i - V_a) = A^2q\varepsilon_s N_d/2C^2 \]

It can be seen that a plot of \( 1/C^2 \) versus the reverse bias voltage \( V_a \) for constant \( N_d \) would give a straight line. The slope of the straight line can be used to obtain the uniform dopant concentration, \( N_d \), in the semiconductor, and the \( x \)-axis intercept gives the built-in potential \( \phi_i \). In the case where \( N_d \) varies with the distance into the semiconductor the plot of \( 1/C^2 \) versus \( V_a \) is no longer a straight line. Yet, it can be shown that the slope at any point, \( d(1/C^2)/d(V_a) \), is still given by

\[ -2/A^2q\varepsilon_s N_d(W) \]

where \( N_d(W) \) represents the dopant concentration at the edge of the depletion region.
Thus, by measuring the slope at a given depth W from the semiconductor surface, the impurity concentration at that point can be determined. This provides a very convenient method of measuring the impurity distribution in a semiconductor.
Figure 1.1 Cross-sectional view of a planar, ion-implanted GaAs MESFET.
Figure 1.2 Electron energy band diagrams of metal contact to n-type semiconductor with $\phi_m > \phi_s$.
(a) metal semiconductor separated from each other
(b) thermal equilibrium established after contact
Figure 1.3 Electron energy band diagrams of n-type semiconductor with surface states. The diagrams show (a) flat band at the surface, (b) surface in thermal equilibrium with the bulk, and (c) metal in contact with the semiconductor.
Figure 1.4 Electron energy diagram showing image force barrier lowering.
Figure 1.5 Electron energy band diagrams at a metal-semiconductor junction (a) under applied forward bias ($V_a > 0$) and (b) under applied reverse bias ($V_a < 0$).
2. Experimental

Both semi-insulating ($\rho = 10^7 \Omega \cdot \text{cm}$) and Te-doped ($n = 10^{17} \text{cm}^{-3}, \rho = 10^{-2} \Omega \cdot \text{cm}$) $<100>$ GaAs wafers (Wacker Siltronic Corporation) were used as substrate materials for W film deposition. The electrical and structural behavior of the resulting W/GaAs contacts were studied as a function of annealing temperature. Figure 2.1 shows a schematic process flow for the fabrication of W/GaAs contacts for both electrical and structural characterization. The starting GaAs substrate wafers were first degreased in TCA, acetone, and methanol. The wafers were then etched with a solution of 5:1:1 $\text{H}_2\text{SO}_4$:$\text{H}_2\text{O}_2$:$\text{H}_2\text{O}$ for 1 minute at 120°C. The semi-insulating wafers were subsequently etched in a 1:1 $\text{HCl}$:$\text{H}_2\text{O}$ solution for native oxide removal. About 500Å of W film was sputtered onto the semi-insulating wafer in a Perkin-Elmer RF sputtering system using a power of 100W and an Ar pressure of 15 mT. The wafer was then cut into small pieces and the W/GaAs samples were then capped on both sides with 2000Å of sputtered $\text{SiO}_2$ and subjected to furnace annealing in the temperature range of 100-900°C in a flowing $\text{N}_2$ ambient. The oxide cap was then removed and the annealed W/GaAs samples were analyzed by Rutherford Backscattering Spectrometry (RBS) (See Appendix I) and Transmission Electron Microscopy (TEM) (See Appendix II). For electrical characterization and Scanning Electron Microscopy (SEM) (See Appendix III) observation, circular W diodes were fabricated on
the n-GaAs wafer using the standard lift-off technique. The bare n-type wafer was first degreased and then etched in the 5:1:1 \( \text{H}_2\text{SO}_4:\text{H}_2\text{O}_2:\text{H}_2\text{O} \) solution for 1 minute. Circular windows of sizes ranging from 0.2mm to 1mm in diameter were then patterned onto the wafer by photolithography. Prior to W deposition, the patterned wafer was dipped in 10:1 \( \text{H}_2\text{O}:\text{NH}_4\text{OH} \) for 10 seconds to remove carbon contamination and native oxide. W dots of thickness 2000Å were then defined on the n-GaAs substrate using a lift-off technique. The metallized wafer was cut into small pieces and capped on both sides with 2000Å of sputtered SiO\(_2\). The capped W/GaAs Schottky diodes were furnace-annealed in the temperature range of 100-900°C for 20 minutes in a flowing \( \text{N}_2 \) ambient. The oxide cap on the back side was then removed by reactive ion etching (RIE) in a \( \text{CF}_4/\text{O}_2 \) plasma. Ohmic contact was formed on the back side by electron gun evaporation of AuGe and subsequent sintering at 450°C for 2.5 minutes. After removing the top cap in buffered HF, the Schottky diodes were characterized by current-voltage (I-V), capacitance-voltage (C-V) measurements and inspected with a SEM.

RBS measurements of the W/GaAs samples were performed with a 2.0 MeV \( ^4\text{He}^+ \) beam generated by a 2.5 MeV Van de Graaff accelerator. The beam was focused down to 0.75mm in diameter on target. A Si surface barrier detector located at a backscattering angle of 170° provides an energy resolution of 18 keV. The samples were mounted on a goniometer and were tilted at 65° with respect to the normal axis of the sample surface so that a depth resolution of 20Å for W could be achieved. TEM analysis was carried out with the
Siemens 102 system and SEM inspection was done with the Hitachi S310 system.

A HP 4140B current meter with a built-in DC voltage source was used to measure the current-voltage (I-V) characteristics of the W/GaAs Schottky diodes annealed at different temperatures. The diode I-V characteristics were analysed with the thermionic emission model which is represented by the following equation:

\[
I = A^* T^2 \exp(-q\phi_B/kT) \left[ \exp(qV/nkT) - 1 \right]
\]

The capacitance-voltage (C-V) characteristics of the diodes were measured with a HP 4192A impedance analyzer. A plot of \(1/C^2\) versus reverse bias \(V_R\) provides an evaluation of the dopant concentration profile of the GaAs substrate. The dopant concentration \(N_d\) at the edge of the depletion region \(X_d\) under a reverse dc voltage \(V_R\), can be expressed as

\[
N_d(X_d) = -2q\varepsilon_0 A^2 \frac{d(1/C^2)}{dV_R}
\]

where \(\varepsilon\) is the relative dielectric constant of the substrate material.
Figure 2.1 A Schematic process flow for the fabrication of W/GaAs contacts.
3. Results

3.1 Electron Microscopy Measurements

Scanning electron micrographs of the as deposited and annealed W/GaAs diodes are shown in Figure 3.5. A morphologically smooth W film on the GaAs substrate is observed for the diode annealed up to 300°C. After 700°C annealing, small voids start to appear near the edge of the diode indicating a rough W/GaAs interface. 900°C annealing results in larger voids at the interface and holes in the W film. The holes on the W film are likely the result of metallurgical interactions between W and GaAs.

Bright field transmission electron micrographs and the corresponding diffraction patterns for thin (=180Å) W films on GaAs as deposited and annealed at 750°C and 900°C are shown in Figure 3.6. The as deposited film shows fine grain size =70Å. This fine-grain film was identified from the diffraction pattern as the α-W phase with A-15 crystal structure [44]. After annealing at 750°C for 20 minutes, the film transformed into b.c.c. α-W with larger grain size (=900Å). Small amount of W₂As₃ can also be identified from the electron diffraction pattern of this sample. Small voids are also visible at the grain boundaries covering =1/6 of the total surface. Further annealing at 900°C results in physical disintegration of the W film forming spherical grains of =1000Å on
the GaAs substrate. It was estimated that about 60% of the GaAs surface was exposed. This result is consistent with the SEM observations which show the presence of holes on the W film annealed at 900°C. Diffraction pattern of the individual grain revealed that the grain was W_{2}As_{3} with a monoclinic structure. Table I lists the transmission electron diffraction data for the as deposited and annealed (750°C, 900°C) W/GaAs samples. X-Ray diffraction data for the α-W, β-W, and W_{2}As_{3} phases taken from the JCPDS powder diffraction file is also shown in the table.

3.2 Rutherford Backscattering Spectrometry (RBS) measurements

RBS spectra for the as-deposited and annealed W/GaAs samples are shown in Figure 3.1. No apparent changes are observed in the spectra for samples annealed below 650°C. At annealing temperatures between 650°C and 800°C, the shifts in the substrate and W signals in the RBS spectra indicate interdiffusion of W and GaAs. The drastic reduction in the W signal and the out-shift of the GaAs substrate signal in the spectra of the 900°C annealed sample suggest that possible metallurgical reactions between W and GaAs may have occurred at annealing temperatures greater than 850°C. This result agrees with the TEM analysis which shows the formation of W_{2}As_{3} islands at the W/GaAs interface for diodes annealed at 900°C. The inhomogeneous interface also leads to the strong sloping feature of
the GaAs substrate and W signals observed in the RBS spectrum for
the 900°C annealed diode (Figure 3.1(e)).

Using the as-deposited RBS spectrum as a reference, the W
diffusion profiles in GaAs at the various annealing temperatures can
be estimated. Figure 3.2 shows the distribution profiles of W in
GaAs at different temperatures. The profiles seem to follow \( C(x) =
C_0 \exp(-x/\delta) \), where the characteristic diffusion distance \( \delta \)
can be extracted from the diffusion profile at a given annealing
temperature and annealing time. A plot of \( \delta \) versus (annealing
time)\(^{1/2} \) for samples annealed at 700°C is shown in Figure 3.3.
The linear relationship in Figure 3.3 suggests that the diffusion
process is governed by \( \delta = 2(Dt)^{1/2} \) where \( D \), the diffusion
constant of the diffusing species at a given temperature, can be
calculated from the slope of the linear plot. We obtained a \( D \) value
of 2.56x10^{-16} \( \text{cm}^2/\text{sec} \) for W diffusion in GaAs at 700°C. Onuma
et al. [41] reported a diffusion constant of 2x10^{-14} \( \text{cm}^2/\text{sec} \) for
Si diffusion in GaAs at 850°C. P. M. Asbeck et al. [42] reported a
diffusion constant of 8.7x10^{-12} \( \text{cm}^2/\text{sec} \) for Cr redistribution in
semi-insulating GaAs annealed at 850°C. Using values of \( D \) obtained
at different annealing temperatures, a plot of \( \ln(D) \) versus 1/T is
obtained and is shown in Figure 3.4. The linear plot confirms the
temperature dependence of the diffusion constant \( D = \)
\( D_0 \exp(-\Delta E/kT) \). From the slope and intercept of the plot, the
activation energy of W diffusion in GaAs is found to be \( \Delta E = 1.87 \pm
0.65 \text{ eV} \) with the prefactor \( D_0 = 7.3 \text{E-7 cm}^2/\text{sec} \). S. J. Pearton
et al. [43] studied the diffusion of S in GaAs under various capping
conditions over the temperature range of 950-1050°C. They reported a \( D_0 \) value of \( 3.3 \times 10^{-7} \) cm\(^2\)/sec for S diffusion in near-surface implant-damaged GaAs samples. Their results showed that S diffusion is enhanced by lattice damage.

GaAs outdiffusion can also be inferred from the RBS spectra for samples annealed between 650°C and 800°C. However, due to the overlapping of the Ga and As backscattering signals in the spectra, the Ga outdiffusion cannot be easily identified.

3.3 Electrical Measurements

The electrical behavior of the W/GaAs Schottky diode were characterized by both current-voltage (I-V) and capacitance-voltage (C-V) measurements. Figure 3.7 shows the current density (J) versus voltage (V) plots for both the forward bias (a) case and the reverse bias case (b). The family of curves in each plot represents the current-voltage characteristics for diodes annealed at different temperatures. Using the thermionic emission model, the barrier height of the Schottky diode can be calculated from the y-axis intercept of the extrapolated linear region of the \( \ln(J) - V \) curve. The slope of this linear region provides an evaluation of the ideality factor. As shown in Figure 3.7(a), diodes annealed at temperatures below 600°C exhibit a good linear region of \( \ln(J) - V \) curve indicating ideal thermionic emission behavior. The ideality
factor is very close to unity (=1.1) and the barrier height reaches 0.62 eV. Significant deviations from ideal diode behavior are observed for diodes annealed at and above 600°C. The ideality factor increases from 1.1 at 500°C to 1.2 at 600°C while the barrier height decreases from 0.62eV to about 0.58eV. After 700°C annealing, the ideality factor reaches as high as 1.4. The occurrence of such non-ideal diode behaviors coincides with the on-set of interdiffusion of W and GaAs at about 600°C as observed from RBS analysis. For annealing temperatures above 700°C, the Thermionic Emission Model becomes inadequate in describing the current-voltage characteristics of the diodes which undergo macroscopic structural changes as shown by SEM and TEM analysis.

A corresponding behavior is observed for the reverse current-voltage characteristics of the diode annealed at different temperatures (Figure 3.7(b)). Figure 3.8 shows a log-log plot of the diode reverse leakage current versus the diode diameter. It can be deduced from the slope (=2) of the plot that the reverse leakage current of the diode annealed up to 600°C is proportional to the square of the diode diameter. This implies that reverse leakage due to the diode edge effect is insignificant. As seen from Figure 3.7(b), there is an improvement of the diode in terms of an order-of-magnitude decrease in the reverse leakage current when the as-deposited diode is annealed up to 500°C. The reverse current starts to increase again for the diodes annealed at 600°C and for annealing temperatures above 600°C the diodes become very leaky. The enhanced reverse leakage at temperatures above 800°C can be
attributed to the sharp edge effects of the islands formed at the diode interface as a result of metallurgical reaction between W and GaAs. Figure 3.9 shows a plot of the leakage current density versus annealing temperatures for a diode reverse biased at 4V. Figure 3.10 shows the variations of the Schottky barrier height and ideality factor of the diode as a function of annealing temperatures.

The series resistance of the W/GaAs Schottky diode can be modelled with a series combination of a diode and a resistor with resistance $R$ through which the current $I$ flows. An algorithm based on a differentiation approach has been established to extract the series resistance of a Schottky diode from the forward $I-V$ characteristics (See Appendix IV). Table II lists the values of the series resistance of the W/GaAs Schottky diode annealed at different temperatures.

Capacitance-voltage (C-V) measurements of the diodes show that the bulk GaAs substrate dopant concentration for depth greater than about 500Å below the diode interface remains practically constant for different annealing temperatures. Due to the presence of a built-in depletion region of the metal-semiconductor junction, the C-V technique is unable to provide electrical information of the metal/GaAs interface or the substrate layer within 500Å from the interface. Figure 3.11(a) shows the plot of $1/C^2$ versus reverse bias voltage and Figure 3.11(b) shows the dopant profile of the GaAs substrate for diodes annealed at different temperatures. The relatively constant dopant profiles suggest that the electrical degradation of the W/GaAs diode is not due to substrate dopant
redistribution, but rather due to activities occurring within 500Å below the metal/semiconductor interface.
Figure 3.1 RBS spectra for the as-deposited and annealed W/GaAs samples. (This set of spectra was obtained by: Kin-Man Yu)
Figure 3.1(e) RBS spectra for the 900°C annealed W/GaAs sample.
(Spectra obtained by: Kin-Man Yu)
\[ C(x) = C_0 \exp(-x/\delta) \]

Figure 3.2 Distribution profiles of W atoms in GaAs at different annealing temperatures.
(This plot was obtained by: Kin-Man Yu)
\[ \delta = 2(Dt)^{1/2} \]

Figure 3.3 A plot of the characteristic diffusion distance as a function of the square root of the annealing time. (This plot was obtained by: Kin-Man Yu)
\[ D = D_0 \exp[-\Delta E/kT] \]

\[ \Delta E = 1.87 \pm 0.65 \text{ eV} \]
\[ D_0 = 7.34 \times 10^{-7} \text{ cm}^2 \text{ s}^{-1} \]

Figure 3.4 A plot of the diffusion constant of W atom as a function of the reciprocal annealing temperature. (This Plot was obtained by Kin-Man Yu)
Figure 3.5 SEM micrographs of the as-deposited and annealed W/GaAs samples.
Figure 3.6 TEM micrographs and diffraction patterns of the as-deposited and annealed W/GaAs samples. (Micrographs were obtained by Dr. T. Sands)
Figure 3.7 Plots of current density versus voltage for W/GaAs diodes under forward bias (a) and reverse bias (b).

(a) As Deposited
(2) 300°C
(3) 500°C
(4) 600°C
(5) 700°C
(6) 800°C
(7) 900°C

(b) As Deposited
(2) 300°C
(3) 500°C
(4) 600°C
(5) 700°C
(6) 800°C
(7) 900°C
Figure 3.8 A log-log plot of the reverse leakage current versus diode diameter.

\[ \ln(I) = k + n \ln(d) \]

\[ V = 0.5V \]
Figure 3.9 A plot of the reverse leakage current density at 0.4 V as a function of annealing temperatures.
Figure 3.10 A plot of the Schottky barrier height and ideality factor as a function of annealing temperatures.
Figure 3.11(a) A plot of $1/C^2$ versus reverse bias voltage for diodes annealed at different temperatures.
Figure 3.11(b) The dopant concentration profiles for diodes annealed at different temperatures.
TABLE I. Electron diffraction data of W/GaAs samples as-deposited and annealed at 750 and 900 °C for 20 min. X-ray powder diffraction data of α-W, β-W, and W₄As₃ phases taken from the JCPDS diffraction file are also shown for comparison.

<table>
<thead>
<tr>
<th>Transmission electron diffraction data</th>
<th>X-ray powder diffraction data</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>as-deposited</td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td>0.507 (w)</td>
<td>0.58</td>
</tr>
<tr>
<td>0.473</td>
<td>0.467</td>
</tr>
<tr>
<td>0.424</td>
<td>0.366</td>
</tr>
<tr>
<td>0.330</td>
<td></td>
</tr>
<tr>
<td>0.257 (m)</td>
<td>0.264 (w)</td>
</tr>
<tr>
<td>0.229 (s)</td>
<td>0.226</td>
</tr>
<tr>
<td>0.206 (m)</td>
<td>0.206 (110)</td>
</tr>
<tr>
<td>0.175</td>
<td>0.157</td>
</tr>
<tr>
<td>0.158</td>
<td></td>
</tr>
<tr>
<td>0.151</td>
<td>0.151</td>
</tr>
<tr>
<td>0.146 (w)</td>
<td>0.142</td>
</tr>
<tr>
<td>0.140 (m)</td>
<td></td>
</tr>
<tr>
<td>0.135 (w)</td>
<td>0.130 (w)</td>
</tr>
<tr>
<td></td>
<td>0.129</td>
</tr>
</tbody>
</table>

*All plane spacings are in nm. X-ray data are indexed with hkl in parentheses. (w), (m), and (s) denote weak, medium, and strong intensity diffraction rings, respectively.

* X-ray for α-W, β-W, and W₄As₃ are from cards 2-1138, 4-806, and 18-1415 of the JCPDS powder diffraction file.

* These reflections are kinematically forbidden for a perfect A15 structure.

(Courtesy Reference 48)

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Table II. The values of the diode series resistance at different annealing temperatures.

<table>
<thead>
<tr>
<th>Annealing Temperature (°C)</th>
<th>R (ohm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>As deposited</td>
<td>18.8</td>
</tr>
<tr>
<td>100</td>
<td>4.9</td>
</tr>
<tr>
<td>300</td>
<td>3.8</td>
</tr>
<tr>
<td>700</td>
<td>145.6</td>
</tr>
</tbody>
</table>
4. Discussion

The electrical behavior of the W/GaAs diodes annealed at the temperature range of 100°C to 900°C can be correlated with the structural and metallurgical changes of the metal/semiconductor interface. Based upon the correlations, a model can be proposed for the degradation mechanism of the W/GaAs Schottky diode during high temperature annealing. The behavior of the W/GaAs diode can be divided into three temperature regimes: (1) low annealing temperature (T<600°C), (2) intermediate annealing temperature (600°C<T<800°C), (3) high annealing temperature (T>800°C).

4.1 W/GaAs Schottky diode characteristics after low temperature annealing (T<600°C)

RBS analysis of the diodes annealed at temperatures less than 600°C shows no interdiffusion between W and GaAs. The SEM micrographs of the diodes reveal improved adhesion between W and GaAs after annealing at 300°C. This can be attributed to the thermal removal of a thin native oxide (=150Å) at the interface. The resulting sharp metal/semiconductor interface leads to the observed improvements in the diode electrical characteristics in terms of barrier height, ideality factor, diode series resistance, and reverse leakage current when the as-deposited diode is annealed between 300°C and 500°C. Diodes annealed in this temperature range exhibit ideal thermionic emission behavior (n=1.1 and $\phi_B=0.62$eV)
and the reverse leakage current decreases by an order of magnitude compared to the as-deposited diode. The diode series resistance decreases from 18.8Ω for the as-deposited diode to 3.8Ω for the 300°C annealed diode. Previous X-Ray Diffraction analysis of W film sputtered on GaAs indicated that a phase transformation from β-W to α-W occurred at about 300°C. However, the contribution of this phase transformation to the electrical properties of the diode is unclear. Our results seem to be consistent with those of Waldrop [25] who reported that W/GaAs diodes formed by evaporation of W on clean GaAs have ideal rectifying behavior in the temperature range of 350-450°C.

4.2 Electrical degradation due to interdiffusion of W and GaAs (600°C<T<800°C)

RBS results showed that the onset of W diffusion into the GaAs substrate occurred at annealing temperatures greater than 650°C. Outdiffusion of As and Ga atoms into the W film was also observed in this temperature range. About 0.3 at.% of W atoms were observed at a depth of about 500-600Å below the W/GaAs interface after 700°C annealing for 20 minutes. Diodes annealed at 600°C have reverse leakage current an order of magnitude higher than that for diodes annealed at lower temperatures. The ideality factor also increases from 1.1 for as-deposited diodes to 1.2 for 600°C annealed diode. Further deviations from ideal diode behaviors occur at annealing temperature of 700°C. The ideality factor increases to 1.4 and the leakage current increases by a factor of five compared to
the 600°C annealed diodes. These observations suggest that the in-diffused W atoms create recombination centers near the diode interface. These centers lead to high level of recombination current when the diode is reverse biased. For diodes under forward bias, the recombination current component \( J_r \) can be expressed as

\[
J_r = J_{r0} \exp(qV/2kT)
\]

where \( J_{r0} \) is the prefactor which depends on the geometry of the diode and the electronic properties of the substrate material. Hence the ideality factor for the forward I-V characteristics of the diode will approach 2 when the recombination current is large.

Furthermore, the diode series resistance calculation based on the used algorithm (See Appendix IV) indicates that the series resistance of the 700°C annealed diode is about 30 times the resistance of the diode annealed at 300°C annealed diode. Such an increase in the series resistance strongly suggests the presence of a highly resistive layer near the W/GaAs interface. The formation of this resistive layer can again be attributed to the in-diffused W atoms into the GaAs substrate. It has been reported that W atoms act as acceptors in GaAs [45,46]. When present in high concentration, these acceptors are able to electrically compensate the shallow donors in the n-type GaAs substrate resulting in a non-abrupt layer of high resistance at the interface. It has been estimated that this highly resistive layer is between 600Å and 1000Å thick and does not form a sharp interface with the underlying n-GaAs
substrate. In other words, the W/n-GaAs diode becomes a W/GaAs:Te+W/n-GaAs structure after annealing at temperatures above 600°C. Hence, the electrical behavior deviated significantly from the ideal thermionic emission behavior after annealing between 600°C and 800°C. Waldrop [25] reported similar electrical degradation of W/GaAs diodes annealed at temperatures above 550°C. However, no structural information on the interdiffusion of W and GaAs in this temperature range has been reported.

### 4.3 Diode degradation after high temperature annealing (T>800°C)

RBS and TEM analysis indicated that a metallurgical reaction between W and GaAs started at annealing temperature greater than 850°C. The reaction product was identified to be $W_2As_3$ which tended to form spherical islands on the GaAs surface as shown by the TEM micrographs. Dissociation of GaAs during the reaction produced Ga which could diffuse along the voids of the W grain boundaries into the $SiO_2$ cap. As observed from the SEM micrographs, the W film of the 900°C annealed diode became porous and the diode was physically degraded with a very rough and inhomogeneous interface. The Schottky diode parameters (barrier height, ideality factor, depletion width, etc.) obtained from electrical measurements (I-V, C-V) were therefore rendered unreliable for diode annealed at temperatures greater than 800°C. A simplified schematic diagram for the structural evolution of the W/GaAs diode as a function of annealing temperature is shown in Figure 4.1.
Figure 4.1 A simplified schematic diagram showing the structural evolution of the W/GaAs diodes annealed at different temperatures.
5. Conclusions

The thermal stability of W/n-GaAs Schottky diodes was investigated for the annealing temperature range of 100-900°C. Diodes annealed between 300°C and 500°C showed ideal diode behavior \( n=1.1, \Phi_B=0.62\text{eV} \). Deviations from ideal behavior \( n=1.4, \Phi_B=0.58\text{eV} \) were observed for diodes annealed between 600°C and 800°C. Electrical degradations of the diode annealed in this temperature range were attributed to the interdiffusion of W and GaAs. The in-diffused W atoms created acceptor type recombination centers and compensated the shallow donors (Te) in the GaAs substrate resulting in a non-abrupt and highly resistive GaAs layer near the interface. Annealing the diode at temperatures greater than 800°C resulted in the formation of islands of the W\(_2\)As\(_3\) phase at the interface leading to the "physical breakdown" of the diode. Therefore, given our processing conditions for the fabrication of the W/n-GaAs Schottky diode, the diode is only stable up to about 700°C of furnace annealing and hence is not a very suitable candidate for the gate material in the fabrication of self-aligned GaAs MESFET. However, by modifying the processing conditions (e.g. use capless anneal under As overpressure, use rapid thermal anneal instead of furnace anneal, etc.), it is very likely that the high temperature thermal stability of W/n-GaAs Schottky diode can be improved. Alternatively, W/n-GaAs diodes can also find useful applications in situations where temperatures less than those
required by post-implant are encountered. For example, the relatively high metallurgical stability of W with respect to GaAs at temperatures less than 600°C makes it a promising candidate as a diffusion barrier between GaAs substrate and a second layer material. On the other hand, the relatively low resistivity of W film can also be used as a second layer metal on top of a thermally more stable Schottky material on GaAs substrate for self-aligned MESFET application. Other GaAs MESFET technologies where the metal gate material is not subjected to temperatures higher than 700°C, e.g. the dummy gate approach [47], W/GaAs contact can serve well as the Schottky gate.
Appendix I -- Basic operation of RBS

RBS is used to obtain a quantitative analysis of the metallurgical interactions between the tungsten film and the GaAs substrate. RBS is a relatively simple, non-destructive analytical tool which can provide quantitative analysis without reference of standards. A schematic of a typical RBS set-up is shown in Figure AI-1. Basically, the set-up consists of three major components, namely, the beam generation system, the scattering chamber, and the data handling system. The measurement consists of directing a collimated monoenergetic beam of charged particles on a target, detecting only the small fraction of these particles which are backscattered at a particular angle and measuring the resultant energy spectrum of detected particles. Basically, three kinds of information can be obtained from an energy spectrum: (1) identification of elemental constituents, (2) depth information (e.g. film thickness), and (3) compositional ratio of different constituents.

The elemental information is obtained from the kinematic scattering factor $K$ which is the ratio of the energy of the projectile after and before the collision. $K$ is derived from equations expressing the conservation of total energy and total momentum (Figure AI-2) and is different for different pairs of projectile and target atoms. The depth information can be derived from the energy loss ($dE/dX$) characteristics of the projectile in
the target materials. Finally, one can obtain the compositional ratio of the elements from the relative yield of the elements, i.e. from the total number of particles backscattered by a particular element and intercepted by the detector, the probability of collision (the Rutherford scattering cross section\(\sigma\)), and the total number of particles incident on the sample.

Figure AI-3 shows a schematic RBS energy spectrum. The target is a compound of two elements A and B with A heavier than B. By measuring the location of the edges one gets the masses of A and B. The height ratio of the edges in the spectrum is proportional to the composition of the two elements in the compound. An actual RBS spectrum is complicated by two facts, namely, (a) energy loss straggling which arises from the statistical fluctuation of the total energy loss of the projectiles in the target, and (b) detector energy resolution. As a result, the energy spectrum is broadened and the step-like edges in the spectrum is smoothened out.
Figure AI-1. A schematic of a typical RBS set-up.
(Courtesy Reference 49)

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The definition of the kinematic factor $K$ for an elastic collision process between a projectile atom with mass $M_1$ and a target atom with mass $M_2$.

\[
K = \frac{E_1}{E_0}
\]

\[
K = \left[ \frac{(M_2^2 - M_1^2 \sin^2 \theta)^{1/2} + M_1 \cos \theta}{M_2 + M_1} \right]^2
\]

\[
= \left\{ \frac{[1 - (M_1/M_2)^2 \sin^2 \theta]^{1/2} + (M_1/M_2) \cos \theta}{1 + (M_1/M_2)} \right\}^2
\]

\[
K(\theta = 180^\circ) = \left[ \frac{1 - M_1/M_2}{1 + M_1/M_2} \right]^2
\]

Figure A1-2.

The definition of the kinematic factor $K$ for an elastic collision process between a projectile atom with mass $M_1$ and a target atom with mass $M_2$.

(Courtesy Reference 50)
Figure A1-3.
A schematic RBS spectrum for a compound target with elements A and B where A is heavier than B. (Courtesy Reference 50)
Appendix II — Basic operation of a TEM

A TEM is used to examine the microstructure of the W/GaAs interface and to identify different phases that might have formed when the W/GaAs diodes are annealed at different temperatures. Figure AII-1 shows a schematic diagram of a typical transmission electron microscope. Electrons are produced by thermionic emission of electrons from a heated tungsten "hairpin" filament which is held at -100KV with respect to the rest of the microscope. These electrons are then accelerated in the anode and focussed by a set of condenser lenses to produce the desired illumination of the specimen. The specimen to be examined is held in a holder fitted on a stage which is provided with the drives necessary to produce both movement and tilting of the specimen. The objective lens focuses on the specimen. The diffraction pattern is formed initially in the back focal plane of the objective lens and a magnified image in its image plane.

When electrons travel through the specimen, they interact with the effective potential field of the nuclei and are scattered elastically according to the Bragg Law (Figure AII-2). If the scattering centers in the specimen are arrayed in an orderly, regular manner, as in simple crystal, the scattering is coherent and results in spot diffraction patterns. If the sample is a fine-grained polycrystal, circular diffraction patterns are obtained. In either case, the image contrast is a magnified picture
of the diffraction pattern (or, strictly speaking, it is the Fourier Transform of the pattern). The diffraction pattern itself is formed at the back focal plane of the objective lens. By varying the magnification and utilizing projector lenses of variable focal length, the images and their diffraction patterns can be obtained on the fluorescent screen. While phase identification can be derived from an analysis of the diffraction pattern, microstructure and morphology of the specimen can be observed from the image contrasts.
Figure All-1.
A schematic diagram of a typical transmission electron microscope.
Figure AII-2.
A schematic showing the Bragg's law of scattering for fast electrons incident on a closed-packed crystal. (Courtesy Reference 52)

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Appendix III -- Basic operation of a SEM

The basic principle of operation of a SEM is illustrated in Figure AIII-1. Electrons from a tungsten filament are accelerated by a voltage in the range of 1-30 KeV and directed down the center of an electron optical column consisting of two or three magnetic lenses. These lenses cause a fine electron beam to be focused onto the specimen surface. Scanning coils placed before the final lens cause the electron spot to be scanned across the specimen surface in the form of a square raster. The electron beam incident on the specimen surface causes various phenomena (Figure AIII-2) of which the emission of secondary electrons is the most commonly used. A detector that is sensitive to the emitted secondary electrons from the specimen is connected through a video amplifier to the grid of a cathode-ray tube that is scanned in synchronism with the beam on the specimen. Thus, there is a one-to-one correspondence between the brightness at any point on the screen and the strength of the signal from the corresponding point on the specimen. Consequently, an image of the specimen surface is built up on the cathode-ray tube screen point by point.
Figure AIII-1. A simplified schematic showing the basic operation of a typical SEM system.
Figure AIII-2.
Electron-specimen interactions
Appendix IV — Extraction of Schottky diode parameters from I-V measurement

The forward current-voltage (I-V) characteristics of a Schottky diode obeying the thermionic emission model is given by

\[ I = I_S \left( \exp\left(\frac{qV_D}{kT}\right) - 1 \right) \]  

(1)

Most practical Schottky diodes show deviations from ideal thermionic emission behavior. A dimensionless parameter called the ideality factor, \( n \), is usually included in the I-V relationship to take into account of non-ideal diode behaviors:

\[ I = I_S \left( \exp\left(\frac{qV_D}{nkT}\right) - 1 \right) \]  

(2)

where \( q \) is the electronic charge, \( V_D \) the voltage applied across the diode, \( k \) the Boltzmann constant, and \( T \) the absolute temperature. \( I_S \) can be expressed by

\[ I_S = A_{eff} A^{**} T^2 \exp\left(-\frac{q\phi_B}{kT}\right) \]  

(3)

where \( A_{eff} \) is the effective area of the diode, \( A^{**}(=8.6 \ cm^{-2}K^{-2}A) \) is the Richardson constant, and \( \phi_B \) is the Schottky barrier height of the diode.

The effect of the diode series resistance \( R \) is usually modelled with a series combination of a diode and a resistor with resistance \( R \) through which the current \( I \) flows. The voltage, \( V_D \), across the diode can then be expressed in terms of the total voltage
drop, \( V \), across the series combination of the diode and the resistor. Thus, \( V_D = V - IR \), and for \( V_D > 3kT/q \) equation (2) becomes

\[
I = I_S \exp \left[ \frac{q(V-IR)}{nkT} \right]
\]  

(4)

Equation (4) can be rewritten in terms of current density \( J (=I/A_{eff}) \). Thus,

\[
V = R_A^{eff} J + n \phi_B + \frac{n}{\beta} \ln(J/A^{**T^2})
\]  

(5)

where \( \beta = q/kT \)

(6)

Differentiating equation (5) with respect to \( J \) and rearranging terms, we obtain:

\[
\frac{d(V)}{d(\ln J)} = R_A^{eff} J + \frac{n}{\beta}
\]  

(7)

Thus, a plot of \( d(V)/d(\ln J) \) versus \( J \) will give \( R_A^{eff} \) as the slope and \( n/\beta \) as the y-axis intercept. To evaluate \( \phi_B \), we can define a function \( H(J) \):

\[
H(J) = V - (n/\beta) \ln(J/A^{**T^2})
\]  

(8)

From equation (5), we can deduce:
Using the \( n \) value determined from equation (7), a plot of \( H(J) \) vs \( J \) will also give a straight line with y-axis intercept equal to \( n\phi_B \). The slope of this plot also provides a second determination of \( R \) which can be used to check the consistency of this approach. Thus, performing two different plots (equations (7) and (9)) of the J–V data obtained from one measurement can determine all the three key diode parameters: \( n \), \( \phi_B \), and \( R \).

We have applied our proposed procedure to characterize W/GaAs Schottky diodes annealed at temperatures ranging from 100°C to 700°C. The diameter of the tungsten metal dots ranges from 0.02 cm to 0.12 cm. We have observed that the reverse leakage current of the as-deposited and annealed diodes at a given voltage is directly proportional to the geometrical area of the metal dots, indicating that the edge effect of the diodes is insignificant. Hence, we have taken the geometrical area of the diodes to be \( A_{\text{eff}} \). Figure AIV-1(a) shows the plots of \( \frac{d(V)}{d(\ln J)} \) vs \( J \) and \( H(J) \) vs \( J \) for the as-deposited W/GaAs diode. As expected, both plots give straight lines. The values of \( R \) obtained from the two different plots agree with each other within 10%. The values of \( n \) and \( \phi_B \) also agree well with those values obtained from the simple consideration of the linear region of experimental \( \ln J \) vs \( V \) plot. Figure AIV-1(b) shows the calculated and the corresponding experimental \( \ln J \) vs \( V \) plots of the as-deposited W/GaAs diode. Figure AIV-2(a) and (b) show similar

\[
H(J) = RA_{\text{eff}}J^n\phi_B \tag{9}
\]
plots for the 700°C annealed W/GaAs diode. Except for low voltages (< 0.05V), the good agreement between calculated and experimental lnJ vs V plots as seen in Figures AIV-1(b) and 2(b) implies that the Schottky diode indeed can be modelled quite accurately by the series combination of a diode and a resistor. For the low voltage regime, however, other current conduction mechanisms (e.g. recombination current) dominate and a different model has to be invoked to explain the diode behaviors.
Figure AIV-1. As-deposited W/GaAs Schottky diode
(a) plots of $d(V)/d(\ln J)$ vs $J$ and $H(J)$ vs $J$
(b) Experimental and calculated $\ln J$ vs $V$ plots.
Figure AIV-2.
700°C annealed W/GaAs Schottky diode
(a) Plots of $d(V)/d(\ln J)$ vs $J$ and $H(J)$ vs $J$
(b) Experimental and calculated $\ln J$ vs $V$ plots

$n = 1.4$
$R = 145.6 \, \Omega$ from (1)
$R = 161.5 \, \Omega$ from (2)
$\Phi_B = 0.58 \, eV$
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