Title
Highly-linear sampling receivers in silicon and BiCMOS processes for multi-GS/s optically and electrically sampled systems

Permalink
https://escholarship.org/uc/item/5mq3f9h8

Authors
Gathman, Timothy D.
Gathman, Timothy D.

Publication Date
2012

Peer reviewed|Thesis/dissertation
UNIVERSITY OF CALIFORNIA, SAN DIEGO

Highly-linear Sampling Receivers in Silicon and BiCMOS Processes for Multi-GS/s Optically and Electrically Sampled Systems

A dissertation submitted in partial satisfaction of the requirements for the degree Doctor of Philosophy in Electrical Engineering (Electronic Circuits and Systems)

by

Timothy D. Gathman

Committee in charge:

Professor James F. Buckwalter, Chair
Professor Gert Cauwenberghs
Professor Ian Galton
Professor Tom Murphy
Professor Stojan Radic

2012
The dissertation of Timothy D. Gathman is approved, and it is acceptable in quality and form for publication on microfilm and electronically:

Chair

University of California, San Diego

2012
DEDICATION

To my wife Sarah.
# TABLE OF CONTENTS

Signature Page ................................................................. iii
Dedication ........................................................................ iv
Table of Contents ............................................................. v
List of Figures ....................................................................... viii
List of Tables ......................................................................... xv
Acknowledgements ............................................................. xvi
Vita .................................................................................. xviii
Abstract of the Dissertation ................................................ xx

Chapter 1  Introduction: Multi-GS/s Electrical and Photonic Sampling  1
  1.1 Sampling Methods: Optical versus Electrical ................. 1
    1.1.1 Photonic Sampling Gates ................................. 3
    1.1.2 Electrical Sampling Gates ............................. 4
  1.2 Injection-Locking as a Means of Spectrum Analysis ....... 5
  1.3 Dissertation Organization .................................... 6

Chapter 2  Sampling Receivers for Optical Communication .... 9
  2.1 Integrate-and-Dump Receivers ................................. 11
    2.1.1 Signal-to-Noise Ratio ................................. 11
    2.1.2 Clock Jitter .............................................. 13
    2.1.3 Finite Reset Bandwidth ............................ 14
    2.1.4 Nonlinearity ........................................... 15
  2.2 Circuit Design ....................................................... 16
    2.2.1 45nm SOI Device Behavior ........................ 16
    2.2.2 Active Integrator ...................................... 18
    2.2.3 Common-gate Input Buffer ....................... 19
    2.2.4 Operational Transconductance Amplifier ....... 22
    2.2.5 Amplifier Offset and DC Photocurrent .......... 25
    2.2.6 Large-Signal Behavior ............................. 26
  2.3 Measurements ........................................................ 27
  2.4 Conclusions ........................................................... 33
Chapter 3 Silicon Integrated Circuits for High Dynamic Range Photonic Analog-to-Digital Conversion
3.1 2GS/s Photonically-Sampled Integrate-and-Dump Receiver
   3.1.1 Integrate-and-Dump Circuit Design
   3.1.2 Integrate-and-Dump Measurement Results
3.2 Rate-Scalable Multi-GS/s Photonic Analog-to-Digital Conversion
   3.2.1 Performance Limitations for Optical Sampling
   3.2.2 Circuit Design: Integrate-and-Sample Receiver
   3.2.3 Measurement Results: 2GS/s
3.3 Complementary Photonically-Sampled 2 GS/s ADC for Subsampling up to 50GHz
3.4 Conclusions

Chapter 4 High-Speed Sampling Circuits and Interleaved Front-ends in SiGe and InP BiCMOS Technology
4.1 Track-and-hold Amplifier Architecture
4.2 120nm SiGe BiCMOS Circuit Design
   4.2.1 Linearity
   4.2.2 Hold-mode Feed-through
   4.2.3 Bandwidth and Mismatch
   4.2.4 Noise
4.3 2GS/s 120nm SiGe BiCMOS Measurement Results
   4.3.1 Cascaded Master/Slave SHA
   4.3.2 Resampled Master/Slave SHA
   4.3.3 Linearity Comparison
4.4 40GS/s TAH and Interleaved Sampling Circuits in 250nm InP CoSMOS
   4.4.1 40 GS/s InP DHBT Track-and-Hold Amplifier
   4.4.2 Time-interleaved InP and CMOS Hybrid Architecture for 40GS/s Sample-and-hold Circuits
4.5 Conclusions

Chapter 5 Distributed Techniques for Wideband Mm-Wave Communication
5.1 High Pass Distributed Amplifier
   5.1.1 Circuit Design
   5.1.2 Measurement Results
5.2 A 92-GHz Deterministic Quadrature Oscillator and \( N \)-Push Modulator in 120-nm SiGe BiCMOS
   5.2.1 Constructive-Wave Oscillator
   5.2.2 Measurement Results
LIST OF FIGURES

Figure 1.1: Aperture jitter from random fluctuations in the clock period (jitter $t_{j,rms}$) which creates an error in the sampled voltage. 2
Figure 1.2: Electronic ADC performance trends for converter bandwidth versus signal-to-noise and distortion ratio [1]. 3
Figure 1.3: Switched-capacitor sampling circuit using (a) a MOS switch and (b) using a bipolar switched emitter-follower. 5
Figure 2.1: Integrate-and-dump optical QAM receiver. 10
Figure 2.2: Noise model for the IAD receiver. 13
Figure 2.3: Achievable resolution in bits as a function of the product of the reset bandwidth and reset period. 15
Figure 2.4: Transition-frequency $f_T$ and intrinsic gain $g_{mro}$ for a 56-nm floating body and body contacted NFET ($V_{gs} = V_{ds}$). 17
Figure 2.5: Simulated harmonic distortion for a normalized 1V input amplitude. $HD_2$ decreases proportionally as the input amplitude is reduced, and $HD_3$ follows the square of the input amplitude. 18
Figure 2.6: Architecture of the active feedback integrate-and-dump receiver implemented in 45-nm SOI CMOS. 20
Figure 2.7: Simulated input impedance of the OTA integrator. 21
Figure 2.8: Schematic of the operational transconductance amplifier (OTA) implemented with a 56-nm body-contacted FET. 23
Figure 2.9: OTA small-signal gain and phase. 24
Figure 2.10: Schematic of the continuous-time common-mode feedback circuit. 25
Figure 2.11: Simulated SINAD from the frequency domain calculations similar to the inset with $f_{in}=964.84375$ MHz. 27
Figure 2.12: Microphotograph of the 45-nm CMOS SOI integrate-and-dump receiver. 28
Figure 2.13: Measurement setup for the integrate-and-dump receiver. 29
Figure 2.14: FFT plot of a 3.3 GHz input to the DSO 80604b sampling at 20 GS/s with an input bandwidth of 6 GHz. 30
Figure 2.15: Measured FFT of samples from active integrator for an input frequency of 964.84375MHz. 30
Figure 2.16: SINAD, SNR, and ENOB vs. frequency for a sinusoidal input. 31
Figure 2.17: Screenshot from Agilent 80604B real-time oscilloscope. The input frequency to the integrate-and-dump circuit is 19.53125 MHz. 32
Figure 2.18: Screenshot from Agilent 80604B real-time oscilloscope. The input frequency pulse width is 100ps and the integration time is 300ps. 32
Figure 3.16: Schematic of the Gm-C integrator with the common-mode feedback amplifier.

Figure 3.17: Simulation results for the cascaded master/slave double-switched sample-and-hold showing a linearity linearity better than 11 ENOB for a 1V_{pp} input and output swing.(3.17)

Figure 3.18: Schematic of the timing circuits for the integration, reset, and the sampling clocks for the two track-and-hold amplifiers.

Figure 3.19: Differential-mode feedback amplifier for canceling common-mode current offset of the photodetector.

Figure 3.20: Simulated frequency-domain performance for an input frequency sinusoid of 937.5 MHz. The simulated ENOB is 8.35b.

Figure 3.21: Simulated frequency-domain performance for a photonically-sampled pulse train. From this simulation, the ENOB for the integrate-and-sample receiver is approximately 8.1b.

Figure 3.22: Microphotograph and printed circuit board layout of the two-channel integrate-and-sample receiver.

Figure 3.23: Input return loss of the IAS packaged onto the PCB, both measured single-ended for each differential input, and also simulated with a PCB package model with 0.5 nH of bondwire inductance.

Figure 3.24: Output return loss of the IAS and TAH PCB, measured single-ended for each differential output, and simulated with a PCB package model with 0.5nH of bondwire inductance.

Figure 3.25: Measured oscilloscope waveform of the differential output of the IAS (i.e. the output of the second track-and-hold buffered over 50-Ω) with a 605 MHz sinewave input (dotted gray).

Figure 3.26: Frequency-domain measurement for effective-number-of-bits. An ENOB of 8.1b is measured with a 223 MHz input frequency.

Figure 3.27: Frequency-domain measurement for spurious-free dynamic range for an input amplitude envelope equal to that measured for peak ENOB.

Figure 3.28: Effective-number-of-bits versus frequency.

Figure 3.29: SNR and SFDR measured at peak ENOB versus frequency.

Figure 3.30: Frequency-domain measurement for effective-number-of-bits with photonic sampling setup.

Figure 3.31: Photonic subsampling system.

Figure 3.32: Demonstration of the photonic subsampling measurement where all tones alias to the same frequency of approximately 202.1 MHz. The 202.1 MHz signal is then subsequently received in the integrate-and-sample receiver and passed off to a commercial ADC for digitization.

Figure 3.33: Measured photonic subsampling system of the SNR of the subsampled signal versus frequency at a 2 GS/s sampling rate. An SNR better than 36 dB is obtained with an input of 49.8 GHz.
Figure 3.34: Photonic subsampling measurement with an unlinearized modulator. A 49.8 GHz input is sampled on the dual-output Mach-Zhender modulator at a sample rate of 2 GS/s and aliased down to 200 MHz.  

Figure 4.1: Use of a sample-and-hold at the front-end of an ADC to improve the performance and/or reduce the sample rate of the ADC if the SHA is subsampling. The output of the second track-and-hold amplifier holds the sampled value for almost the entire sample period, reducing the settling and dynamic requirements of the ADC.  

Figure 4.2: Effect of pedestal compensation; a pedestal feedback amplifier reduces the asymmetry between the differential voltage steps during the track to hold transition.  

Figure 4.3: Early bipolar track-and-hold architecture.  

Figure 4.4: Conventional bipolar track-and-hold architecture with pedestal compensation and feedthrough attenuation.  

Figure 4.5: Double-switched bipolar track-and-hold architecture with pedestal compensation and improved feedthrough attenuation.  

Figure 4.6: Schematic of the double-switched track-and-hold architecture in 120nm SiGe BiCMOS.  

Figure 4.7: Half circuit schematic of the switched emitter-follower during hold mode.  

Figure 4.8: Small-signal half-circuit schematic for the switched-emitter follower.  

Figure 4.9: Simulated output noise spectral density during both hold and track modes for the layout extraction of a single THA operating at 2GS/s with 5 GHz of bandwidth.  

Figure 4.10: Sample-and-hold architecture test setup. The master/slave and resampler architectures are determined by the clock generation circuits (not shown).  

Figure 4.11: Clock waveforms for the sample-and-hold architectures: (a) represents the waveforms CLK1 for the master and CLK2 for the slave which are 180 degrees out-of-phase. The resampler waveforms (b) have the slave clocked at one half the rate with a duty cycle of 25 %, therefore reducing the sample rate by half.  

Figure 4.12: Microphotograph of the 2 GS/s master/slave sample-and-hold circuit. The master/slave sample-and-hold consumes approximately 500mA from a 5V supply and 30mA from a 2.5V supply.  

Figure 4.13: Time-domain measurement of the master/slave SHA with an input frequency of 2100 MHz subsampled and aliased to 100 MHz measured on the Agilent DSO80604b 20GS/s real-time oscilloscope.
Figure 4.14: Frequency-domain subsampling measurement of the master/slave THA with an input frequency of 2030 MHz aliased to 30 MHz. The third harmonic is at a power of -55dBc related to the fundamental, which is at 1Vpp at the input to the SHA.  

Figure 4.15: Frequency-domain subsampling two-tone intermodulation distortion measurement of the master/slave SHA with input frequencies of 2099.5 and 2100.5 MHz aliased to 99.5 and 100.5 MHz. The 3rd order intermodulation distortion term for the subsampled waveform is -52.8 dBc.  

Figure 4.16: Microphotograph of the 2 GS/s resampled sample-and-hold circuit. The resampled sample-and-hold consumes approximately 420mA from a 5V supply and 100mA from a 2.5V supply.  

Figure 4.17: Time-domain measurement of the resampled SHA with an input frequency of 2100 MHz aliased to 100 MHz measured on the Agilent DSO80604b 20GS/s real-time oscilloscope.  

Figure 4.18: Frequency-domain subsampling measurement of the resampled SHA with an input frequency of 2030 MHz aliased to 30 MHz. The third harmonic is at a power of -51dBc related to the fundamental, which is at 1Vpp at the input to the SHA.  

Figure 4.19: Frequency-domain subsampling two-tone intermodulation distortion measurement of the resampled SHA with input frequencies of 2099.5 and 2100.5 MHz aliased to 99.5 and 100.5 MHz. The 3rd order intermodulation distortion term for the subsampled waveform is -51.65 dBc.  

Figure 4.20: Measured $P_{IIP3}$ versus frequency for the master/slave SHA and resampled SHA configurations. The input envelope is 1Vpp and the input power for each tone is -2dBm (0.5Vpp).  

Figure 4.21: Simulation results for the InP DHBT track-and-hold. The $HD_2$, $HD_3$, and $THD$ are the result of the worst case linearity for 10 Monte Carlo runs.  

Figure 4.22: InP DHBT unity-gain buffer.  

Figure 4.23: InP DHBT 50-Ω output buffer.  

Figure 4.24: Layout for the InP DHBT track-and-hold and 50-Ω output buffer.  

Figure 4.25: Architecture for the InP DHBT front-end track-and-hold followed by 8 CMOS sample-and-hold circuits.  

Figure 4.26: Simulation results for the 40 GS/s InP DHBT track-and-hold and a single channel of the time-interleaved MOS sample-and-hold operating at 5 GS/s.  

Figure 4.27: Layout for the 40GS/s InP HBT track-and-hold followed by 8 time-interleaved MOS sample-and-holds sampling at 5GS/s.
Figure 5.1: Distributed amplifiers operating with (a) conventional low-pass synthetic transmission line topology and (b) the proposed high-pass synthetic transmission line.

Figure 5.2: Simple loss-less model of a lumped-element artificial transmission line with (a) low-pass characteristics and (b) high-pass characteristics.

Figure 5.3: $S_{21}$ of the high-pass artificial transmission line varying the ratio $\frac{C_{par}}{C}$.

Figure 5.4: Circuit schematic for a single stage of the high-pass distributed amplifier.

Figure 5.5: Comparison of simulation results with $R_e = 15\Omega$ (solid) and with $R_e = 0\Omega$ (dashed).

Figure 5.6: CPW structure (a) and cascaded loss $S_{21}$ for multiple stages of the high pass artificial transmission line with shunt inductor CPWs and series MIM capacitors (b).

Figure 5.7: Microphotograph of the high pass distributed amplifier implemented in a 0.12$\mu$m SiGe BiCMOS process.

Figure 5.8: HPDA S-parameters: transmission $S_{21}$ and reverse isolation $S_{12}$ measured (solid) and simulated (dashed).

Figure 5.9: Input and output return loss: measured (solid) and simulated (dashed).

Figure 5.10: Group delay: measured (solid) and simulated (dotted).

Figure 5.11: Measured noise figure (solid) and output 1-dB compression point $P_{1dB}$ (dashed).

Figure 5.12: Architecture of the constructive-wave oscillator.

Figure 5.13: Simulated voltages on the transmission lines at the junctions between the 0, 90, 180, and 270 phase amplifications cells after layout parasitic extraction. The voltage amplitude on the transmission line is approximately 400 $mV_{pp}$.

Figure 5.14: Simulated S-parameters for the a single feedback cell for the constructive-wave oscillator.

Figure 5.15: Microphotograph of the constructive-wave oscillator.

Figure 5.16: Simulated and measured of oscillator output frequency and power versus tuning voltage.

Figure 5.17: Oscillator spectrum measured using a W-band LNA, the Agilent 11970W harmonic mixer, a MiniCircuits amplifier, and the Agilent E4448A spectrum analyzer.

Figure 5.18: Oscillator phase noise ($dBc/Hz$) versus frequency offset for the free-running oscillator oscillating at 92.4GHz. At 1MHz, the measured phase noise is -78.6dBc/Hz.

Figure 5.19: CWO output spectrum with 50 Msymbol/s BPSK modulation.

Figure 6.1: Filter Selectivity.
Figure 6.2: Filter Selectivity. ............................................. 139
Figure 6.3: Reciprocal mixing due to poor selectivity RF filter and poor phase noise VCO. ................................. 140
Figure 6.4: Injection locking sensitivity curve. The oscillator is locked to the injected frequency inside of the gray region. ........................................................................ 140
Figure 6.5: Nonlinear model of van der Pol Oscillator .............. 142
Figure 6.6: Simulation results for impact of harmonic content on the injection-locking range \((A_{osc} = 0.5V, Q = 10, f_n = 5.5 GHz, \text{ and } \frac{g_1}{g_3} = \frac{1}{3})\). ............................................................... 143
Figure 6.7: Injection-locked oscillator array for spectrum analysis (a) and an array of three injection-locked oscillators to detect a single input tone (b). ........................................................................ 145
Figure 6.8: System schematic for a dual oscillator injection-locking circuit (a) and microphotograph of the fabricated circuit (b). ............................................................... 148
Figure 6.9: Output spectrum of Oscillator 1 (a) with a fundamental frequency of 5.76 GHz and Oscillator 2 (b) with a fundamental of 5.11 GHz. ............................................................... 149
Figure 6.10: Measured phase noise (dBc/Hz) versus frequency for both oscillators and the injection reference. ......................... 149
Figure 6.11: Measured phase noise (dBc/Hz) at a 1kHz offset for each oscillator under injection by the reference. The reference phase noise is measured at a 1kHz offset versus \(P_{inj}\) ............................... 150
Figure 6.12: Measured injection sensitivity for a dual-oscillator array fabricated in 120nm SiGe BiCMOS. ................................................. 150
Figure 6.13: Simulated injection-locking, phase-locking, and simultaneous injection- and phase-locking ranges ................................................. 150
Figure 6.14: Balanced injection-locked phase-locked loop array. ............................................................... 151
Figure 6.15: Tuning voltages for amplitude and frequency variation of the injected signal. ............................................................... 154
# LIST OF TABLES

Table 2.1: Performance Summary .................................................. 33
Table 4.1: Simulated output noise contributions in the THA. ................. 93
Table 4.2: Comparison table for high-speed bipolar track-and-hold amplifiers. ................................................................. 110
ACKNOWLEDGEMENTS

I would like to thank my advisor, Professor James Buckwalter, for his encouragement and guidance throughout my graduate studies. I have learned a great deal from him both as my advisor and teacher during my years at UCSD. I have really enjoyed discussing new techniques, architectures, and ideas with Professor Buckwalter.

I would like to thank the other members of my dissertation committee for constructive comments and suggestions: Professor Stojan Radic, Professor Ian Galton, Professor Tom Murphy, and Professor Gert Cauwenberghs.

I would like to thank Don Kimball at UCSD CalIT2 for his measurement advice and assistance. He always took time to listen and give advice on measurement design and improvements; his assistance is much appreciated.

I would also like to thank my former and present labmates: Joohwa Kim, Mehmet Parlak, Arpit Gupta, Wei Wang, Nader Kalantari, Mohammad Mehrjoo, Tissana Kijsanayotin, Jun Li, Po-Yi Wu, Cooper Levy, and Kristian Madsen. In addition, I would like to thank the members of other research groups: Hayg Dabag, and Bassel Hanafi. I will miss all the discussions and jokes.

My thanks also go out to the UCSD Photonic Systems Group, Professor Radic, and Dr. Andreas Wiberg. We have had many interesting and helpful discussions about design, measurement, and testing of the components for photonic analog-to-digital converters. Thanks to Andreas for his help with photonic measurements. Additionally, I would like to thank Dr. Bryan Stossel from Lockheed Martin for his help, suggestions, and project management while assembling the photonic analog-to-digital converter.

Finally, I want to express my gratitude to my lovely wife, Sarah Gathman. Her love and encouragement the last five years have made all the difference in the world.

The material in this dissertation is based on the following papers which are either published or submitted for publication. Chapter 2 is mostly a reprint of the material accepted for publication in IEEE Transactions on Circuits and Systems I: Regular Papers, T. D. Gathman, J. F. Buckwalter. Chapter 3 is reprinted from
a combination of three publications, the first reprinted from the IEEE Topical
Gathman, J. F. Buckwalter, the second from material that has been submitted
to IEEE Transactions on Microwave Theory and Techniques, T. D. Gathman, J.
F. Buckwalter, and the third from material submitted to IEEE Journal of Solid
State Circuits, T. D. Gathman, J. F. Buckwalter, A. O. J. Wiberg. Most of the
material in Chapter 4 has been submitted to the IEEE Journal of Solid State
Circuits, T. D. Gathman, J. F. Buckwalter, A. O. J. Wiberg. Chapter 5 is mostly
a reprint both from the IEEE International Microwave Symposium, 2010, T. D.
Gathman; J. F. Buckwalter, and from material submitted to IEEE Microwave
6 is mostly a reprint from three publications: first, the IEEE Radio Frequency
Buckwalter, and, finally, the International Conference on Nonlinear Dynamics,

The dissertation author was the primary author of these materials, and
co-authors have approved the use of the material for this dissertation.

Timothy D. Gathman
San Diego, CA
July 27th, 2012
VITA

2002-2007 B. S. in Electrical and Computer Engineering, University of Colorado, Boulder

2002-2007 B. M. in Violin Performance, University of Colorado, Boulder

2007-2009 M. S. in Electrical Engineering (Electronic Circuits and Systems), University of California, San Diego

2008-2012 Graduate Research Assistant, University of California, San Diego

2009-2012 Ph. D. in Electrical Engineering (Electronic Circuits and Systems), University of California, San Diego

PUBLICATIONS


ABSTRACT OF THE DISSERTATION

Highly-linear Sampling Receivers in Silicon and BiCMOS Processes for Multi-GS/s Optically and Electrically Sampled Systems

by

Timothy D. Gathman

Doctor of Philosophy in Electrical Engineering (Electronic Circuits and Systems)

University of California, San Diego, 2012

Professor James F. Buckwalter, Chair

In this dissertation, high-linearity sampling circuits are presented for wideband (multi-GS/s) electrical and optical sampling, millimeter-wave circuits are discussed for wideband communication, and injection-locking is presented for nonlinear sampling and spectrum analysis. A 2GS/s sampling receiver with 4.5 measured effective-number-of-bits is presented for spectrally efficient optical communication in a 45nm SOI CMOS process. Next, jitter limitations for broadband sampling circuits are discussed as sampling rates and input bandwidths are increased. An integrate-and-dump optical receiver is introduced for high dynamic range photonic analog-to-digital conversion at a sample rate of 2GS/s. Next, a novel rate-scalable photonic analog-to-digital converter is described that enables very-low-jitter, high
linearity, and low-noise photonic sampling and subsequent analog-to-digital conversion of wideband signals up to 10GHz and beyond. A special emphasis is placed on achieving high system linearity. Integrate-and-sample receivers will be discussed within this context, as they bring both signal-to-noise ratio benefits due their approximation of a matched filter, and because they reduce the subsequent electronic analog-to-digital converter bandwidth, linearity, and jitter requirements. In addition, an alternative complementary photonic sampling architecture is presented for novel pseudo-differential photonic analog-to-digital conversion, and measurement results will be provided for the photonic sub-sampling front-end and the integrate-and-sample receiver with input frequencies up to 50GHz at a 2GS/s rate. The jitter benefits of optical sampling are demonstrated with a measurement of 36.4dB of SNR with a 49.8GHz input at a 2GS/s rate.

Following this discussion of high-linearity receivers for photonic analog-to-digital conversion, electronic sampling circuits in SiGe BiCMOS and InP BiCMOS are described for sampling with high dynamic range. First, the design and measurement results for a track-and-hold 120nm SiGe BiCMOS are provided with 9-bit linearity at 2GS/s with an electrical input of $1V_{pp}$. Next, very high-speed track-and-hold and time-interleaved sampling architectures are described in an InP BiCMOS technology for sampling at 40GS/s and beyond.

In the second part of this dissertation, traveling-wave techniques for millimeter-wave wide-band communication circuits and nonlinear techniques for spectrum analysis are discussed. A Ka-band high-pass distributed amplifier is implemented in a 120nm SiGe BiCMOS process with a gain of 8.5 dB, sharp rejection below the low-frequency cutoff, a bandwidth of 21.5GHz, and a power consumption of 28mW from a 1.7V supply. Following, a constructive-wave deterministic quadrature oscillator and N-push modulator in 120nm SiGe BiCMOS is presented for operation at 92GHz in W-band. Operating at 32mW from a 2V supply, the oscillator contains an integrated quadrature modulator suitable for BPSK and QPSK modulation and a measured phase noise of -78.6dBc/Hz at an offset of 1MHz. Both of these millimeter-wave designs support wideband communication and could be used in receiver designs in conjunction with multi-GS/s analog-to-digital convert-
Injection-locking as a means of spectral sampling is presented for chip-scale, low-power spectrum analysis suitable for cognitive radio and adaptive radio architectures. In comparison to state-of-the-art optical and electrical sampling techniques described in the first part of the dissertation, this all-analog injection-locked “sampling” technique has significant advantages in terms of power dissipation and integration on-chip. Two architectures will be presented for injection-locked spectrum analysis. First, an injection-locked oscillator array with measurement results from two injection-locked oscillators is implemented in 120nm SiGe BiCMOS with oscillation frequencies close to 5.5GHz. Second, an improved architecture is presented with balanced injection-locked phase-locked loops in which detection of the input signal’s frequency and power is orthogonal.
Chapter 1

Introduction: Multi-GS/s Electrical and Photonic Sampling

This dissertation discusses high dynamic range wideband sampling circuits and receivers designed in silicon and BiCMOS processes for photonically and electrically sampled analog-to-digital converter systems, communication circuits enabling wideband communication, and injection-locking techniques for spectrum analysis. Wideband sampling in this dissertation corresponds to Nyquist bandwidths larger than 10 GHz, requiring sampling rates of 20 GS/s and above. High dynamic range data converter design entails maintaining low noise, low jitter, and high linearity, especially difficult with these high sample rates and input bandwidths. With advancements in jitter performance and dynamic range, direct digitization of RF (radio frequency) signals is made possible with high dynamic range sampling. As an alternative to very wideband and power-intensive techniques for sampling and analog-to-digital conversion, an analog spectral-“sampling” method using injection-locking is introduced for radio-frequency (RF) low-power, chip-scale spectrum analysis.

1.1 Sampling Methods: Optical versus Electrical

Sampling interfaces continuous-time signals and systems to discrete-time signal processing systems. In high-speed analog-to-digital converters (ADCs),
Aperture jitter, or sampling jitter, refers to random deviations from the ideal sampling instant caused by fluctuations in the period of the clock signal. As demonstrated in Fig. 1.1, fluctuations, or jitter, in the rising edge of the sampling clock yield uncertainty in the sampled voltage of input signal $V_{in}(t)$, i.e. in a sampled noise voltage determined by the slope of the input waveform. Higher input frequencies require lower jitter (less timing uncertainty) from the sampling clock to accurately resolve the sampled voltage.

Photonic sampling clocks and gates have several advantages over electronic clock sources and sampling circuits. First, photonic sampling gates have significantly larger bandwidths (>100GHz) than their electronic counterparts. Secondly, photonic sampling sources and gates have significantly better measured jitter performance. Electronic ADCs have recently broken the 100fs jitter mark [3]; however, photonic ADCs have boasted a measured jitter less than 8.5fs including the sam-
Figure 1.2: Electronic ADC performance trends for converter bandwidth versus signal-to-noise and distortion ratio [1].

In contrast, it is very difficult to find an electronic source with $rms$ jitter below 10fs, plus additional jitter from clock buffers and the sampling gate. The SINAD (signal-to-noise and distortion ratio) for traditional electronic ADCs is shown in Fig. 1.2. The jitter lines for 1psrms and 0.1psrms are shown in red; optical jitter in photonic sampling is currently one to two orders of magnitude lower than the state-of-the-art electronic ADC measured jitter. In mode-locked lasers, for instance, attosecond-level jitter has been measured over short integration periods [5]. This translates into significantly better SINAD performance for wideband data converters with input signals in the GHz range.

1.1.1 Photonic Sampling Gates

Two methods for photonic sampling described in this dissertation are, at lower rates, using an optical modulator [6], and, at higher-rates for time-interleaved
analog-to-digital converter systems, via nonlinear fiber [2]. In the modulator sampling scheme, sampling for a single channel (i.e. without interleaving) is performed as an optical pulse train is passed through a Mach-Zehnder modulator and is intensity modulated with the electrical input. For very wideband, time-interleaved approaches, an alternative solution is to use a more elaborate sampling scheme with highly nonlinear fiber to provide time-interleaved wavelength-multiplexed optical sampling [6–9]. A more in-depth discussion of these techniques will be presented in chapter 3.

1.1.2 Electrical Sampling Gates

Electronic sampling can be performed using various circuit architectures. High-fidelity closed-loop switched-capacitor sampling circuits are typically used at in the 100s of MS/s and below, trading off sample rate and speed for higher fidelity (accuracy, noise, and distortion) due to closed-loop feedback. Open-loop sampling circuits are typically used at higher speeds but have lower performance. In CMOS processes for high-speed data converters, a MOS transistor and a capacitor are used in an open loop configuration to track and sample the input voltage, as shown in Fig. 1.3(a). Bipolar processes have typically had speed advantages over their MOS counterparts; most conventional high-speed track-and-hold circuits are built using SiGe, Gallium-Arsenide (GaAs), and Indium-Phosphide (InP) and utilize a switched emitter-follower (SEF) architecture demonstrated in Fig. 1.3(b). However, as scaling progresses more favorably for CMOS, the device speed, i.e. $f_T$, is catching up to bipolar and III-V technologies. CMOS has now entered the realm of multi-GHz sampling ADCs by using many time-interleaved samplers and ADCs and with fairly modest resolution [10]. However, bipolar track-and-holds can tolerate larger signal swings and have better high-frequency distortion performance than their interleaved MOS counterparts, which must have significant post-processing to calibrate timing, offset, and gain mismatches such that the spurious tones caused by mismatch between the interleaved channels [11] don’t limit the overall performance and spurious-free dynamic range (SFDR). Timing mismatch at higher frequencies motivates the use of a single high-speed track-
Figure 1.3: Switched-capacitor sampling circuit using (a) a MOS switch and (b) using a bipolar switched emitter-follower.

and-hold to relax the timing requirements [12]. Although there have been some attempts made in CMOS to design a single multi-GHz track-and-hold amplifier [13], SiGe and III-V designs typically have higher sample rates, better distortion performance, larger signal swings, and higher bandwidth [14].

Typically, the open-loop linearization performance of bipolar track-and-holds results in modest distortion performance in the 8–12 bit range, depending on input frequency and sample rate. With an improved architecture such as [15], feedback across the emitter-follower switch performs pedestal compensation, and the linearity can be as high as 10-bits at 500 MHz and 1Vpp signal swings [15]; the linearity performance degrades as the input frequency and sample rates are increased. These bipolar track-and-holds continue to push the forefront of sampling rates beyond 40GS/s and up to 50GS/s [14, 16]. An in-depth discussion of high-speed, high-linearity bipolar track-and-hold architectures in both SiGe and InP BiCMOS will be presented in chapter 4.

1.2 Injection-Locking as a Means of Spectrum Analysis

As an alternative to these power-intensive wideband sampling circuits and analog-to-digital converter systems, injection-locking offers a means of analog “sam-
pling” of RF signals for spectrum analysis. Lowering power consumption while maintaining modest performance is required for chip-scale integration of RF spectrum analyzers.

Typical spectrum analyzers seek to improve image rejection and dynamic range through multiple mixers, local oscillators, and filters. Integration of these components on-chip for chip scale spectrum analysis yields typically poor results in CMOS. Filters using CMOS passives have much lower $Q$ compared with other technologies, resulting in poor rejection, and CMOS oscillators have high phase noise due to the low $Q$ of their resonators, resulting in reciprocal mixing of the oscillator’s phase noise with out-of-band jammers. Additionally, many components require high power consumption, making chip-scale integration difficult due to thermal constraints. Nonlinear techniques offer novel methods to determine an input signal’s power and frequency. For chip scale spectrum analyzer applications where performance requirements are modest and minimal power consumption is a necessity, injection-locking offers an alternative to traditional spectrum analyzer topologies.

1.3 Dissertation Organization

Chapter 2 discusses optical sampling circuits for multi-carrier optical quadrature amplitude modulation (QAM) or pulse amplitude modulation (PAM), enhancing channel capacity across optical fiber by using more spectrally efficient modulation schemes for optical communications. An integrate-and-dump optical receiver is designed and measured at 2GS/s in 45nm CMOS SOI with better than 4.5b of measured effective-number-of-bits (ENOB) sufficient to receive 16-PAM at a bit-rate of 8Gb/s, or, if two integrate-and-dump receivers are used with an optical QAM demodulator, 16Gb/s for spectrally efficient 16-QAM.

Chapter 3 discusses photonic sampling and photonic rate-scalable receivers for wideband analog-to-digital converter systems, including both single-channel photonic sampling systems and also interleaved rate-scalable photonic analog-to-digital converters. First, a 2GS/s integrate-and-dump circuit fabricated in 120nm
SiGe BiCMOS is introduced with a measured ENOB of approximately 7.5b. Following, an improved integrate-and-sample architecture with an integrated sample-and-hold is demonstrated for higher dynamic range and closed-loop offset cancellation. The integrate-and-sample receiver achieves 8.1b at 2GS/s with an electrical input and achieves close to 7.5 bits of ENOB (noise only) with an unlinearized optical modulator. At the end of the chapter, an improved pseudo-differential single channel photonic sampling architecture is demonstrated using the integrate-and-sample receiver for subsampling of signals up to 50 GHz with low jitter and high dynamic range. The low frequency SNR is measured to be 48.5dB, which falls to approximately 36.4dB with a subsampled input of 49.8GHz.

Chapter 4 discusses high-speed SiGe and InP BiCMOS as well as CMOS sampling circuits for high dynamic range sampling 40GS/s and beyond, including hybrid sampling circuits employing both InP and CMOS track-and-holds for high-speed interleaved data-conversion. The double switching bipolar track-and-hold architecture is discussed, with measurement results for two sample-and-hold structures operated at 2GS/s. Both structures have close to 9-bit linearity subsampling 2100 MHz input frequencies and with 1V_{pp} signal swings. They consume close to 500mA from 5V and 2.5V supplies. Simulation results and layout are shown for an InP DHBT double switching track-and-hold operating at 40GS/s with a simulated input bandwidth of 36GHz and a power consumption under 500mW. In a subsequent architecture, this track-and-hold is connected to an interleaved bank of 8 MOS sample-and-holds sampling at 5GS/s. Simulation results for the hybrid InP and MOS time-interleaved sample-and-hold are described.

Chapter 5 discusses millimeter-wave techniques for wideband communication, including traveling-wave amplifiers and oscillators. A high-pass distributed amplifier is demonstrated with d.c. isolation between stages (eliminating bias tees at input/output) as well as low-frequency rejection, attributes not present in the traditional low-pass distributed amplifier. The high-pass amplifier has a gain of 8.3dB, 21.5GHz of bandwidth, and has a relatively high rejection of 25dB 5GHz below the lower cutoff frequency. In addition, a traveling-wave, or constructive-wave oscillator is demonstrated which has $N$-push harmonic selection to obtain the
second and fourth harmonics, as well as an integrated quadrature modulator which can be used for wideband binary phase-shift keying (BPSK) or quadrature phase-shift keying (QPSK). The center frequency of the constructive-wave oscillator is 92GHz, with 1.5GHz of tuning range via varactors loading the transmission lines. Modulation is also demonstrated with a 50MS/s baseband BPSK signal applied to the modulator.

Chapter 6 discusses injection-locking techniques for low-power spectrum analysis. First, nonlinear dynamics for injection-locking are described, with two-tone injection. Second, an injection-locked oscillator array is described for chip-scale spectrum analysis. Measurements of two injection locked oscillators with center frequencies in the 5−6GHz range are described with their locking behavior and phase noise. Subsequently, a more promising architecture with orthogonal frequency and power detection is described with simulation results and an analysis of the nonlinear behavior.

Chapter 7 concludes the dissertation with remarks about the future of wideband sampling.
Chapter 2

Sampling Receivers for Optical Communication

Increasing demands for higher data-rate optical communication continue to push circuit technology limits to attain sufficient bandwidth and transimpedance. Traditionally, a linear increase in data-rate is accompanied by a quadratic increase in the gain-bandwidth requirement of transistors in transimpedance amplifiers [17, 18]; this tradeoff is somewhat relaxed with inductive peaking and multi-stage designs at the expense of higher power consumption [19]. Higher transistor unity gain-bandwidth ($f_T$) requires compound semiconductor (III-V) processes or coping with poor analog performance of short-channel CMOS processes [20].

Alternatively, more bandwidth-efficient modulation schemes such as multi-carrier quadrature-amplitude modulation (QAM) [21] and quadrature phase-shift keying (QPSK) [22] have been proposed for optical communication but demand higher linearity from the electronic receiver. For instance, a 16-level multi-carrier QAM optical signal could be coherently demodulated in the optical domain but requires at least 4 bits of linearity at the photodetector and sampling receiver. The performance of this receiver is best described in terms of the signal-to-noise-and-distortion ratio (SINAD) since both noise and distortion impair the accurate demodulation of multi-carrier QAM.

A QAM optical receiver is illustrated in Fig. 2.1 and consists of an I and Q channel receiver each with a photodetector, transimpedance amplifier, and analog-
to-digital converter (ADC) [23]. This proposed optical demodulator actually requires that the two receive channels effectively handle pulse-amplitude modulation (PAM). Traditionally, transimpedance amplifiers (TIAs) with $Z_{FB} = R_{FB}$ have been used. However, a transimpedance integrator with the ability to reset the charge on the integration capacitor $C_{int}$ is also viable with $Z_{FB} = \frac{1}{sC_{int}}$ and is referred to as an integrate-and-dump (IAD) receiver. IAD receivers are used for RF and sampling IF receivers [24] as well as optical binary-encoded digital communication systems with both RZ and NRZ encoding [20, 25–27]. However, these prior demonstrations [20, 25–27] did not demonstrate the linearity required for higher-order modulation.

![Figure 2.1: Integrate-and-dump optical QAM receiver.](image)

Section 2.1 describes the noise, linearity, and sampling-rate tradeoffs for an electronic IAD receiver. Section 2.2 describes the approach implemented in this receiver to realize a high-linearity IAD receiver in 45-nm SOI CMOS that operates at 2GS/s. Section 2.3 presents measurements of the implemented IAD receiver.
2.1 Integrate-and-Dump Receivers

The integrate-and-dump (IAD) receiver achieves a better signal-to-noise ratio (SNR) than traditional low-pass TIAs since the IAD realizes a matched filter for a pulse-amplitude-modulated (PAM) signal [28]. For an optical PAM signal, 

\[ s(t) = \sum_{k=-\infty}^{\infty} I_{\text{sym}}(kT_{\text{sym}}) \text{rect}\left( \frac{t - \left[ k + \frac{1}{2} \right] T_{\text{sym}}}{T_{\text{sym}}} \right), \]  

(2.1)

where \( \text{rect}(x) = 1 \) for \( 0 < x \leq 1 \), \( I_{\text{sym}} \) is the symbol current amplitude, and \( T_{\text{sym}} \) is the symbol period. The matched filter has an impulse response that is the time reversal of the signal [29] and the \( \text{rect}(\cdot) \) function is itself the impulse response of the matched filter. Windowed integration realizes the impulse response necessary for this matched filter operation.

The SNR performance of the IAD suffers, however, from the time required to reset the receiver. The finite bandwidth of the reset circuitry dictates the reset period \( T_{\text{reset}} \) and inevitably reduces the available integration time \( T_{\text{int}} \). For a PAM signal, the SNR is proportional to the integration time, \( T_{\text{int}} \), as long as \( T_{\text{int}} \leq T_{\text{sym}} \) as shown in Fig. 2.2. The integration time is bounded by \( T_{\text{int}} = T_{\text{sym}} - T_{\text{reset}} \); finite reset bandwidth with \( T_{\text{reset}} > 0 \) degrades the maximum achievable SNR unless at least two integrate-and-dump filters are interleaved [20, 30], increasing both the power and area consumption. If the signal is no longer present and integration persists longer than the symbol period, (i.e. \( T_{\text{int}} > T_{\text{sym}} \)), the IAD is no longer a matched filter, and the SNR degrades with increasing \( T_{\text{int}} \) as shown in Fig. 2.2. In highly-scaled CMOS processes, high \( f_T \) devices offer short reset periods and time-interleaving can avoid the sensitivity degradation from the shortened integration period [30].

The following sections detail the calculation of the SNR for the IAD in the presence of clock jitter, finite reset bandwidth, and harmonic distortion.

2.1.1 Signal-to-Noise Ratio

The windowed integration is expressed as a convolution of the input current (and noise) with the rectangular function:
where \( g_m \) is the transconductance of the ideal voltage amplifier shown in Fig. 2.2, \( C_{int} \) is the integration capacitance, and \( R_S \) is the source resistance. In the frequency domain, the magnitude of the transfer function is

\[
|Z(f)| = \frac{T_{int} g_m R_S}{C_{int}} |\text{sinc}(T_{int} f)|. 
\]  

(2.3)

Based on a simplified noise model in Fig. 2.2, noise from the transconductor, photodetector shot noise, and source resistance thermal noise respectively sum to

\[
\overline{i_{n,t}^2} - \overline{i_{n,t}^2} \Delta f = 4kT \gamma g_m R_S^2 + 2qI_{DC,pd} + 4kT R_S.
\]  

(2.4)

Consequently, these noise sources suggest a white noise current density that is shaped by (2.3) in the IAD receiver. To facilitate a traditional calculation of SNR referenced to the photodetector’s symbol current amplitude \( I_{sym} \), the sampled noise is referred here to the input of the IAD after dividing by the square of the low-frequency integration gain, \( \left( \frac{T_{int} g_m}{C_{int}} \right)^2 \):

\[
\overline{i_{n,in}^2} = \overline{i_{n,t}^2} \int_0^\infty |Z(f)|^2 df + \frac{kT}{C_{int}} \left( \frac{C_{int}}{T_{int} g_m R_S} \right)^2 (C_{int} T_{int} g_m R_S)^2.
\]  

(2.5)

For an approximately constant \( I_{sym} \) during each symbol period, the SNR is

\[
\text{SNR} = \frac{\frac{1}{2} I_{sym}^2}{\overline{i_{n,in}^2} BW_n + \frac{kT C_{int}}{T_{int} g_m R_S}}.
\]  

(2.6)

When \( T_{int} = T_{sym} \), (2.6) indicates that the effective noise bandwidth \( BW_n = \frac{1}{2 T_{int}} \) for the noise current \( \overline{i_{n,t}^2} \) is approximately half of the symbol rate. In comparison, low-pass receivers have noise bandwidths that are approximately \( 1.1 \cdot f_b \) for a single pole frequency at \( 0.7 \cdot f_b \). If \( T_{int} \sim 0.5 T_{reset} \), the IAD receiver noise bandwidth approaches that of a low-pass receiver. Fig. 2.2 displays the relationship between the integration time and symbol period.

In this design, a single 2 GS/s integrate-and-dump receiver is realized. The 500-ps sampling period is divided into a 300-ps integration period \( T_{int} \) and a
200-ps reset period ($T_{\text{reset}}$). Therefore, the SNR is approximately 0.8 dB better than a low-pass receiver.

\[ I_{\text{sym}}(t) \]

![Figure 2.2: Noise model for the IAD receiver.](image)

2.1.2 Clock Jitter

Clock jitter also degrades the noise performance of the IAD receiver. Fig. 2.2 shows the integration window of a single symbol; on average, the integration time is $t_2 - t_1 = T_{\text{int}}$. The random variable $\delta t$ expresses the uncertainty of the start and end of the integration window. This integration window is expressed as

\[
v_{\text{out}} = \frac{g_m R_S}{C_{\text{int}}} \int_{t_1+\delta t(t_1)}^{t_2+\delta t(t_2)} I_{\text{sym}} \, dt. \tag{2.7}
\]

The timing uncertainty $\delta t$ between the start and stop of the integration period is presumed to be partially correlated due to the phase noise of the clock source. For small integration periods $T_{\text{int}}$, there will be some correlation between the edge-edge jitter due to the Lorentzian jitter spectrum [31,32]. The variance of the output voltage $v_{\text{out}}$ is calculated from the random variable $\delta t$ which has a variance of $t_{j,\text{rms}}^2$ and edge-edge correlation $c_{\delta t\delta t}$:

\[
\sigma_{v_{\text{out}}}^2 = 2\frac{g_m^2 (I_{\text{sym}} R_S)^2}{C_{\text{int}}^2} \frac{t_{j,\text{rms}}^2}{t_{j,\text{rms}}^2} (1 - c_{\delta t\delta t}), \tag{2.8}
\]
Correlation between the rising and falling edges is shown to reduce the output noise relative to the total timing jitter in so far as we assume that the input current amplitude is roughly constant during the symbol period. The SNR due to jitter is

$$SNR = 10 \log_{10} \left( \frac{T_{int}^2}{2 T_{j, rms}^2 (1 - c_{\delta t} \delta t)} \right), \quad (2.9)$$

and is independent of symbol amplitude with the preceding assumptions. Faster symbol rates demand lower clock jitter to maintain the same SNR.

### 2.1.3 Finite Reset Bandwidth

Finite reset bandwidth causes a residue from a previous integration to affect the voltage at the end of the current integration period. This history is expressed by the discrete-time difference equation

$$v_{out}[n] = \frac{g_m T_{int} R_S}{C_{int}} I_{sym}[n] + v_{out}[n - 1] \exp(-x), \quad (2.10)$$

where $x = 2\pi BW_{reset} T_{reset}$, and $BW_{reset}$ is the reset bandwidth which results from the closed-loop unity-gain reset bandwidth for the active feedback integrator in section 2.2.4. The transfer function is expressed from the discrete-time Fourier transform as

$$Z(e^{j\omega}) = \frac{g_m T_{int} R_S}{C_{int}} \frac{1 - \exp(-2\pi BW_{reset} T_{reset}) e^{j\omega}}{1 - \exp(-2\pi BW_{reset} T_{reset}) e^{j\omega}}; \quad (2.11)$$

the signal history results from a low-pass response that boosts both signals and noise at low frequencies and provides attenuation at frequencies close to the symbol rate. For optical PAM, the residue builds over sequential periods and leads to a degradation in overall performance and resolution. As a worst case, the maximum symbol will occur for a long period, followed by the minimum symbol. Writing (2.10) as an infinite sum instead of a difference equation leads to

$$v_{out}[n] = \frac{g_m T_{int} R_S}{C_{int}} I_{sym}[n] + \sum_{k=1}^{\infty} v_{out}[n - k] e^{-kx}. \quad (2.12)$$

where the current output voltage at the end of integration is determined by all previous symbols through the residue left over after the reset period. For a given
reset period length $T_{\text{reset}}$, the $N$-bit resolution is calculated when the residue due to a infinitely long sequence of maximum symbols is equal to $\frac{1}{2}$ LSB, i.e.

$$N = \log_2 (e^x - 1) - 1.$$  \hspace{1cm} (2.13)

This relationship is shown graphically in Fig. (2.3). To achieve more than 6 bits of resolution, $x > 4.9$.

![Figure 2.3: Achievable resolution in bits as a function of the product of the reset bandwidth and reset period.](image)

### 2.1.4 Nonlinearity

Distortion dominated by the integrator transconductance nonlinearity is expressed with a Taylor series expansion as

$$i(v) = g_{m,1} I_{\text{sym}} R_S + g_{m,2} (I_{\text{sym}} R_S)^2 + g_{m,3} (I_{\text{sym}} R_S)^3 + \ldots$$  \hspace{1cm} (2.14)

For a balanced differential pair the even order distortion should cancel, leaving only odd order terms in (3.18) [33]. The third-order harmonic distortion for a low
frequency input sinusoid with amplitude $I_{sym}R_S$ is

$$HD_3 = \frac{g_{m,3}(I_{sym}R_S)^2}{4g_{m,1}}$$  \hspace{1cm} (2.15)

Minimizing (2.15) entails either reducing the input amplitude or the ratio of $\frac{g_{m,3}}{g_{m,1}}$. Both options result in increased noise through either smaller signal swings or by reducing the effective transconductance and IAD gain if the transconductor is biased at a higher gate-source voltage with the same bias current. For PAM, both noise and distortion must be minimized. Combining the metrics of noise from (2.5), jitter from (2.9), and odd order distortion from (2.15), the SINAD can be written as:

$$SINAD = 10\log_{10} \left[ \frac{1}{\frac{1}{2}f^2_{sym}T^2_{int} + \frac{kTc_{int}}{2T_{m}^2\sigma_{m}^2 R_S^2} + \frac{1}{2f^2_{sym}T^2_{int}} + \frac{1}{2f^2_{sym}HD_3^2}} \right].$$ \hspace{1cm} (2.16)

### 2.2 Circuit Design

#### 2.2.1 45nm SOI Device Behavior

This integrate-and-dump (IAD) receiver is fabricated in a 45-nm digital CMOS SOI process with 11 metal layers and thin oxide, thick oxide, floating-body, and body-contact devices. The minimum gate length for floating body devices is 40 nm and for body-contacted devices is 56 nm.

A number of device challenges face high-dynamic range circuit design in short-channel silicon-on-insulator (SOI) technology. Gate-oxide breakdown limits the supply voltage and thus reduces the maximum signal swing. The excess channel noise factor $\gamma$ is increasing with gate scaling. Device noise is also increased due to floating-body effects, leakage current, and potentially through the parasitic bipolar in partially depleted SOI [34]. Additionally, short-channel effects such as drain-induced barrier lowering (DIBL) are more pronounced in 45-nm FETs, especially the floating-body devices, and results in significant variations not only in the threshold voltage but also in the drain-to-source resistance $r_{ds}$ with applied drain-to-source voltage $V_{ds}$. 


The $f_T$ and intrinsic gain are plotted for $V_{gs} = V_{ds}$ in Fig. 2.4 for a 56-nm floating-body and body-contacted analog NFET device from schematic simulation. Digital floating-body NFETs (not shown) have a minimum channel length of 40 nm in this process and have significantly poorer analog performance but a peak $f_T$ of around 380 GHz. The 56-nm floating-body NFETs have a peak $f_T$ of around 275 GHz. The 56-nm body-contacted NFETs exhibit an $f_T$ of around 200 GHz.

For analog circuits, increased DIBL resulting in low intrinsic gain, body potential variability resulting in threshold mismatch, and floating-body effects are mitigated with body-contacted rather than floating-body NFETs. The intrinsic gain $g_{mr_{ds}}$ of the body-contacted NFET is approximately double that of the floating-body device over much of the bias range. The intrinsic gain of the body-contacted NFET is only slightly higher than 10 and cascode amplifiers offer limited effectiveness and additional noise contributions. Due to their higher intrinsic gain, the body-contact devices were used exclusively in this design.

![Graph of $f_T$ and intrinsic gain for 56-nm floating and body-contacted NFETs](image)

**Figure 2.4:** Transition-frequency $f_T$ and intrinsic gain $g_{mr_{ds}}$ for a 56-nm floating body and body contacted NFET ($V_{gs} = V_{ds}$).

The power series coefficients of the device transconductance in (3.18) are
plotted in the inset of Fig. 2.5, and the corresponding harmonic distortion for a normalized 1 V input amplitude is shown in Fig. 2.5. The second-order distortion decreases proportionally as the input amplitude is reduced as $HD_2 \propto v_{in}$. The third-order distortion follows the square of the input amplitude from (2.15). A sweet spot for third order suppression [35] is at a gate bias of approximately 0.44 V; however, $HD_3$ continues decreasing as the gate-to-source voltage is increased. Although differential operation significantly mitigates the second order distortion, offsets and mismatch [36] will contribute to $HD_2$. Like $HD_3$, $HD_2$ improves with increasing gate-to-source voltage as seen in Fig. 2.5.

![Figure 2.5: Simulated harmonic distortion for a normalized 1V input amplitude. $HD_2$ decreases proportionally as the input amplitude is reduced, and $HD_3$ follows the square of the input amplitude.](image)

### 2.2.2 Active Integrator

The IAD receiver is based on the active feedback integrator shown in Fig. 2.6. The photodetector current is buffered through a common-gate FET that real-
izes a broadband, 50 Ω impedance match. An active feedback integration stage is realized with an operational transconductance amplifier (OTA). Although negative feedback is applied through $C_{fb}$, the unity-gain-bandwidth (UGB) of the active integrator is limited by the output capacitance of the OTA, $C_{int}$, i.e. $C_{int} \gg C_{fb}$. The input signal is integrated on the capacitor $C_{int}$ and reset through transistors $M_1$ and $M_2$ with unity-gain feedback. A high-linearity broadband driver follows the OTA which employs resistive source degeneration for transconductance linearization. The 56-nm body-contacted devices are implemented in all circuits in the signal path except the broadband 50 Ω buffer which uses thick-oxide, body-contacted NFETs.

The finite output resistance of the OTA results in a lossy windowed integration. The frequency response from $Z(f)$ in (2.3) can be modified with the 3-dB (output) bandwidth of the integrator $BW_{3dB}$ to account for integrator droop [37]:

$$|Z_{droop}(f)| = \left| \frac{g_m T_{int} R_S}{C_{int}} \frac{1 - e^{-(j2\pi f T_{int} + 2\pi BW_{3dB} T_{int})}}{(j2\pi f + 2\pi BW_{3dB} T_{int})} \right|. \quad (2.17)$$

The finite gain of the OTA has only a small effect on the transfer function of (2.3) if $4\pi BW_{3dB} T_{int} \ll 1$ and the depth of the nulls in the response of (2.17) are not significant. In addition, the integration of $Z(f)$ in (2.5) can be approximated as $1/(2T_{int})$ if $4\pi BW_{3dB} T_{int} \ll 1$. It is also desirable to minimize droop to mitigate the impact of the nonlinear output resistance of the 56 nm FETs. To achieve a total droop $<\frac{1}{2}$ LSB of 6-bits during the integration period of 300ps, the bandwidth of the OTA (determined by the output resistance and $C_{int}$) should be $\approx 4$ MHz to minimize any nonlinear effects of the output resistance of the 56-nm devices. With this specification, (2.17) is well approximated by (2.3).

### 2.2.3 Common-gate Input Buffer

Due to the low intrinsic gain in 45-nm CMOS SOI, the input impedance of the common-gate (CG) stage is correlated to the impedance seen at the drain of the common-gate FET. The CG FET reduces the impedance seen looking into the integrator by the intrinsic gain.

$$Z_{in} \approx \frac{1}{g_m} + \frac{Z_{L,CG}(s)}{g_m r_{ds}}, \quad (2.18)$$
where $Z_{L,CG}$ is the load impedance seen at the drain of the common-gate transistor. To maintain a broadband, matched input impedance, the impedance at the drain should satisfy $Z_{L,CG}(s) \ll r_{ds}$. The input impedance looking into the OTA integrator differs depending on whether the input signal is single-ended or differential.

### Differential Inputs

The OTA frequency response is approximated with a finite gain $A_o$, and a transfer function $A(s) = \frac{A_0}{1 + \frac{s}{\omega_p}}$, where $\omega_p$ is the OTA dominant pole. For $A_o \gg 1$, the differential input impedance of the integrator with a parasitic input capacitance $C_{input}$ is

$$Z_{INT,Diff} \approx \frac{1 + \frac{s}{\omega_p}}{A_0 s C_{fb} \left(1 + \frac{s}{A_0 \omega_p}\right)} \left| \frac{1}{s C_{input}} \right|. \quad (2.19)$$

The input impedance appears capacitive; therefore, broadband impedance matching for the differential integrator is not possible. The input impedance for the differentially driven OTA integrator is shown in Fig. 2.7; the high impedance mo-
tivates the addition of a common-gate buffer at the input to the IAD. A 500-Ω resistor is added at the drain of the common-gate transistor to provide the drain bias current and to lower $Z_{L,CG}(s)$ in (2.18). In this configuration the common-gate buffer provides approximately a $50 - \Omega$ input impedance over more than a 2 GHz bandwidth.

![Figure 2.7](image-url): Simulated input impedance of the OTA integrator.

**Single-ended Inputs**

Single-ended inputs to the OTA integrator result in a higher input impedance because the feedback is applied differentially around the OTA and half of the feedback current is returned to the other (undriven) side of the integrator. For single-ended inputs, the load impedance to the common-gate stage is

$$Z_{INT,S.E.} \approx \frac{1}{2s(C_{fb} + C_{\text{input}})} \left( \frac{1 + \frac{2s(C_{fb} + C_{\text{input}})}{A_0\omega_p C_{fb}}}{1 + \frac{s(C_{fb} + C_{\text{input}})}{A_0\omega_p C_{fb}}} \right)$$

(2.20)

The simulated single-ended input impedance is shown in Fig. 2.7 and is very high at low frequencies. Similar reasoning to the preceding section motivates the use of
the common-gate buffer and $R_L=500 \, \Omega$ to have $Z_{in} = 50\,\Omega$ for the common gate input buffer for both single-ended and differential inputs.

### 2.2.4 Operational Transconductance Amplifier

During the integration period, the OTA UGB determines the gain from (2.3) and the response of the integrator as long as $C_{fb}$ is small - in this case $C_{fb} \approx 40 \, fF$ and is realized with a vertical natural capacitor formed within the interconnect stack. The UGB during the integration period is

$$ UGB_{INT} \approx UGB_{OTA} = \frac{g_m}{2\pi C_{int}}. $$  \hspace{1cm} (2.21)

Because of the finite unity-gain-bandwidth of the OTA, the integration is performed in an almost open-loop fashion as dictated by (2.3) and Fig. 2.2 and the UGB determines the frequency response during integration.

To allow the output to settle to $\frac{1}{2}$ LSB of 6-bits within a 200-ps reset period, the reset loop $UGB_{res}$ should be greater than 4 GHz. To add margin for process, temperature, and voltage variations, $UGB = 6.6 \, GHz$ after layout extraction and a phase margin of 68° is designed into the OTA to limit ringing in the settling behavior during the reset period.

Due to the limited drain-source channel resistance of the 56nm body-contact devices, cascoding results in a gain of approximately 30 dB. To increase the gain, a folded cascode OTA with gain boosting amplifiers was used. The main OTA is shown in Fig. 2.8. The devices widths are $25\,\mu m$ for the input differential pair $M_{1-2}$ and the cascode transistors $M_{6-9}$, $50\,\mu m$ for the current source $M_3$, $20\,\mu m$ for $M_{4-5}$, and $37.5\,\mu m$ for $M_{10-11}$ to minimize the parasitic capacitance at the folding nodes.

The gain of the OTA must be greater than 60 dB to minimize droop and with the transconductance and integration capacitance fixed from (2.21). Approximately 64 dB of gain is achieved in simulation by using folded cascode gain-boosting amplifiers to increase the amplifier output impedance as shown in Fig. 2.8 in spite of the poor intrinsic gain of the body-contact 56-nm devices. This is consistent with the droop requirements from section 2.2.2 and minimizes the effect
Figure 2.8: Schematic of the operational transconductance amplifier (OTA) implemented with a 56-nm body-contacted FET.

of the nonlinear output resistance of the 56-nm devices.

The reset loop gain and phase characteristics determine the settling behavior of the IAD during the reset period. The reset bandwidth should be large enough for accurate settling and to minimize any residue that might be carried into the next integration period. The reset loop gain and phase are shown in Fig. 2.9 after layout extraction of the OTA. The load resistors of the CG stage greatly reduce the DC reset loop gain. The $UGB_{res}$ of the reset loop is approximately 5.1 GHz with a phase margin of 80°, which is sufficient to fulfill the settling requirements of $< \frac{1}{2}$ LSB of 6-bits within the 200-ps reset period. This $UGB_{res}$ and phase margin places a lower limit on process technology as a reset UGB much less than 4 GHz would limit resolution according to (2.13). The non-dominant pole, $\omega_{p2-RES}$, of the reset loop is located at the folding node of the folded cascode amplifier; $\omega_{p2-RES}$ is significantly larger than the $UGB_{res}$ through minimization of the parasitic capacitance at the folding node.

Folded-cascode gain-boosting amplifiers, similar to the OTA in Fig. 2.8,
are used to obtain a gain and output resistance much higher than that of a single folded-cascode OTA. The gain-boosting amplifiers are scaled down five-fold in area and current to save power consumption. The amplifiers are compensated with load capacitors such that the $UGB$ of the gain-boosting amplifiers is slightly higher than the $UGB_{res}$ of the OTA during the reset period but less than the second, non-dominant pole $\omega_{p2-RES}$ as given by [38] in:

$$\omega_{UGB-RES} < \omega_{UGB-GB} < \omega_{p2-RES}. \quad (2.22)$$

With these specifications the gain-boosting amplifiers have a minimal effect on the settling behavior of the overall OTA.

A continuous-time common-mode feedback (CMFB) loop was chosen to suppress instantaneous common-mode fluctuations that might result from the use of a single-ended input, a photodetector in this case. The CMFB compares the average value of the differential outputs to a reference voltage [39]. Fig. 2.10 displays the schematic of the CMFB amplifier; $M_1$, $M_2$, and $M_3$ distribute current to three differential pairs. Two differential pairs are used for comparison of the
output voltage to a reference and the third is a gain-boosting amplifier in conjunction with $M_{13}$. All differential pair transistors are identically sized at $30\mu m$ with channel lengths of $56nm$ for maximum UGB. Transistors $M_{11-13}$ are sized at $25\mu m$ with the minimum channel length of $56\mu m$ to push the non-dominant pole at the node marked CMFB past the UGB of the CMFB loop. Compensation of this feedback loop with an additional vertical natural capacitor $C_{int}$ for the OTA to a phase margin of approximately $55^\circ$ limits the differential UGB (from layout extraction) to approximately 6.6 GHz. The CMFB amplifier is shown in Fig. 2.10 and has a UGB of approximately 5 GHz after layout extraction.

![Figure 2.10: Schematic of the continuous-time common-mode feedback circuit.](image)

Increasing the FET overdrive voltage improves the speed and dynamic range. To allow an output voltage swing of 1 $V_{pp}$ differential without forcing any device into triode, a supply of 2.1 V is used for this design. This supply voltage is higher than the recommended 1 V suggested for reliability but the body-contacted for PFET and NFET devices have their source tied to the body and are stacked to ensure that the drain-source voltage does not exceed 1 V during normal operation with 1 $V_{pp}$ signal swings as shown in Fig. 2.8.

### 2.2.5 Amplifier Offset and DC Photocurrent

The OTA gain enhancement due to the gain-boosting amplifiers comes at the expense of additional noise and input-referred offset. The input offset of the CG
stage and the OTA offset is integrated during the integration period. To achieve \( \frac{1}{2} \) LSB of 6-bit precision with a 1 \( V_{pp} \) output swing, the integrated offset voltage at the output of the OTA should be smaller than 7.8 mV. Achieving low offset with high bandwidth requires increasing both device area and power dissipation [40]. The offset of the CG buffer stage also adds to the output-referred offset. In addition, DC offset currents from the photodetector must be compensated. Finally, charge injection mismatch from the reset switches at the end of the reset period also contributes to the offset voltage. To mitigate all sources of offset, an input offset control voltage is introduced in Fig. 2.6, but in principle a closed-loop compensation scheme with an off-chip capacitor could be used as in [41].

### 2.2.6 Large-Signal Behavior

The OTA must provide a sufficient slew rate to meet the linearity goals; namely, the slew rate must exceed 3.3 V/ns so that the integrated output signal can reach a 1 \( V_{pp} \) differential output swing during the 300-ps integration period. The slew rate of the differential folded-cascode single-stage OTA is determined by the minimum current flowing through the tail and folded cascode. For this design, with the tail current \( (2I_2) \) equal to the folded cascode current \( (2I_1) \) of 7mA, and a load capacitance \( C_{int} \) in Fig. 2.8 of approximately 620 fF after layout extraction, the slew rate is

\[
SR = \min \left( \frac{I_1, I_2}{C_{int}} \right). \tag{2.23}
\]

and is estimated to be approximately 5.65 V/ns so no slewing should occur under normal operating conditions.

The overall distortion is dominated by the transconductance nonlinearity of the OTA integrator because it experiences the highest signal swings due to the gain of the CG input stage. From Fig. 2.6 with \( Z_{FB} = \frac{1}{\text{s}C_{fb}} \), ignoring \( C_{input} \), and an OTA gain of \( A(s) \), the loop gain is simplified to

\[
T(s) \approx A(s) \frac{sR_LC_{int}}{1 + sR_LC_{int}}. \tag{2.24}
\]

The low-frequency feedback is very low due to the zero in the numerator of (2.24). Therefore, the linearity is dominated by the transconductance nonlinearity of the
input differential pair of the OTA. For this integrate-and-dump receiver, the intrinsic linearity of the input differential pair, biased close to the optimum point to minimize $g_m$ in Fig. 2.5, is sufficient to achieve a simulated SINAD of better than 39$dBc$ over a 1 GHz input range as shown in Fig. 2.11. The SINAD is calculated from FFT plots of the output of the IAD such as the one inset in Fig. 2.11 with an input frequency of 964.84375 MHz.

![Figure 2.11: Simulated SINAD from the frequency domain calculations similar to the inset with $f_{in}$=964.84375 MHz.](image)

2.3 Measurements

This integrate-and-dump (IAD) receiver is fabricated in a 45-nm digital CMOS SOI process. The chip area is 0.980 $\times$ 0.762 $mm^2$ including the pads and dissipates less than 100 mW from a 2.1 V supply (not including the 50 $\Omega$ output driver which uses a 3.3 V supply). Approximately 10 mW is consumed in the common-gate buffer, 30 mW in the main OTA, 6 mW in each of the gain boosting amplifiers, and 40 mW in the common-mode feedback amplifier. The
chip microphotograph is shown in Fig. 2.12. All measurements are performed via on-wafer probing.

Figure 2.12: Microphotograph of the 45-nm CMOS SOI integrate-and-dump receiver.

To characterize the integrate-and-dump receiver, the ENOB, SINAD, and SNR is measured using the equipment setup shown in Fig. 2.13. An Agilent N5181A signal generator produces a sinusoidal input tone which is passed through a balun to produce a differential input signal, integrated by the IAD receiver, and then digitized by the Agilent 80604b real-time oscilloscope. Two channels of the oscilloscope were used to capture the differential data. This data is then post-processed in MATLAB in the frequency domain to obtain ENOB, SINAD, and SFDR. An Agilent N81142A serial pulse data generator generates the off-duty-cycle clock necessary for a 300ps integration period and a 200ps reset period.

Several measurement limitations should be quantified including jitter, noise, and distortion. The dominant noise contribution due to sampling uncertainty is from random jitter in the oscilloscope samples; this degrades the SNR of the
Figure 2.13: Measurement setup for the integrate-and-dump receiver.

The sampled IAD output. The 80604b oscilloscope sampling jitter is specified to have less than 1 ps of \( \text{rms} \) jitter. Therefore, with a signal with 1 \( V_{pp} \) amplitude achieved in 300ps and a 20 GS/s sampling rate in conjunction with filtering and decimation ratio of 10:1 to obtain a 2 GS/s output suggests that the maximum measurable SNR is 44.6 dBc [42].

To quantify the harmonic distortion and noise of the measurement setup, the sinusoidal source is directly connected to the 80604b oscilloscope. Fig. 2.14 displays the FFT plot for a 1.91 GHz sinusoidal input which is aliased down to 90 MHz. Notably, with 10:1 decimation and no filtering, the SINAD of the sampling scope is 33.8 dBc and predicts that IAD receiver measurement will be limited in part by the oscilloscope performance.

All measurements are performed with a 1 \( V_{pp} \) output amplitude. Fig. 2.14 shows the FFT plot generated from the oscilloscope samples of the IAD operation for an input frequency of 964.84375 MHz. Calculations of SINAD, SNR, and ENOB account for the \( \text{rms} \) thermal noise of the oscilloscope, (\( \sim 2.23 \text{mV} \) for each channel); however, distortion and jitter noise due to the oscilloscope is still present in the FFT plot of the IAD. The third harmonic distortion was dominant for all of the measurements, but second harmonic distortion was present as well as seen in the FFT plot. Offset and mismatch on-chip as well as asymmetries in the cabling and balun account for this second-order distortion. For this 964 MHz sinusoid, the SINAD is greater than 29 dBc.
Figure 2.14: FFT plot of a 3.3 GHz input to the DSO 80604b sampling at 20 GS/s with an input bandwidth of 6 GHz.

Figure 2.15: Measured FFT of samples from active integrator for an input frequency of 964.84375MHz
The measured SINAD is greater than $29dBC$ over nearly a 1 GHz bandwidth as shown in Fig. 2.16. The dominating term in the SINAD is noise; the SNR is plotted in Fig. 2.16 and is above $29dBC$ for the 1 GHz range. The effective-number-of-bits (ENOB), also plotted in Fig. 2.16, shows both noise and linearity performance better than 4.5b over the 1 GHz bandwidth, meaning that the IAD receiver has both sufficient noise and linearity to resolve better than 4 bits of modulation, or 16-QAM if used in the system of Fig. 2.1.

![Figure 2.16: SINAD, SNR, and ENOB vs. frequency for a sinusoidal input.](image)

The differential IAD waveforms of the sampled sinusoid are shown in Fig. 2.17. During the reset period, the IAD does not fully reset due to the sinewave being applied during both the integration periods, the finite bandwidth of the oscilloscope (6 GHz), a reduction in the gain of the OTA during reset due to the resistive load of the common-gate stage, and the gain of the common-gate stage.

A 100ps pulse is applied to the IAD in Fig. 2.18 to allow observation of the integration period, hold period, and the reset period.
Figure 2.17: Screenshot from Agilent 80604B real-time oscilloscope. The input frequency to the integrate-and-dump circuit is 19.53125 MHz.

Figure 2.18: Screenshot from Agilent 80604B real-time oscilloscope. The input frequency pulse width is 100ps and the integration time is 300ps.
Table 2.1: Performance Summary

<table>
<thead>
<tr>
<th>Process</th>
<th>45nm CMOS SOI</th>
</tr>
</thead>
<tbody>
<tr>
<td>Symbol Rate</td>
<td>2 Gb/s</td>
</tr>
<tr>
<td>OTA UGBW (after layout extraction)</td>
<td>6.6 GHz</td>
</tr>
<tr>
<td>Measured Peak SNR</td>
<td>31.6 dBc</td>
</tr>
<tr>
<td>Measured Peak SINAD</td>
<td>29.8 dBc</td>
</tr>
<tr>
<td>Supply Voltage</td>
<td>2.1 V</td>
</tr>
<tr>
<td>Power Consumption</td>
<td>&lt;100 mW</td>
</tr>
</tbody>
</table>

2.4 Conclusions

An integrate-and-dump receiver suitable for high linearity optical communications is designed and measured. Measurements were provided showing low noise and high linearity as well as time-domain waveform verification. The measured peak SINAD is better than 29.8 dBc, and the measured peak SNR is better than 31.6 dBc. This corresponds to an ENOB of >4.5b, which is suitable for at least 16-level digital coding schemes such as an optical I-Q QAM receiver.

Acknowledgments

Chapter 2 is mostly a reprint of the material accepted for publication IEEE Transactions on Circuits and Systems I: Regular Papers, 2012. Timothy D. Gathman; James F. Buckwalter. This dissertation author was the primary author of this material.
Chapter 3

Silicon Integrated Circuits for High Dynamic Range Photonic Analog-to-Digital Conversion

Sampling jitter poses significant limitations for current electrically-sampled analog-to-digital converter (ADC) architectures and electronic clock sources trying to push the resolution limits for multi-GHz input signals [43–45]. Multi-GHz instantaneous bandwidth systems with resolutions higher than 8-bits are desirable for future radar, surveillance, and communication systems, both for wideband high-data-rate systems and software-defined radio [46].

The signal-to-noise ratio (SNR) of electronic RF sampling ADCs is constrained by both noise and aperture jitter performance, but ultimately at higher input frequencies aperture jitter limits the achievable SNR [45]. This is because thermal noise power increases proportionally to the noise bandwidth of the ADC system, but the jitter noise power increases quadratically with input frequency. Recently, <100fs rms jitter has been reported [44]; 8 effective-number-of-bits (ENOB) has not been reached above 5GHz.

In this work, the goal is to digitize a 10GHz instantaneous bandwidth with 8-bit ENOB through a rate-scalable photonic sampling architecture, with an ultimate goal of reaching 10-bit ENOB in the future. Photonic analog-to-digital converters can potentially reach higher sampling rates at higher resolutions than
electronic ADC techniques [47], and also pose better power scaling tradeoffs for high-speed ADC architectures [48]. Current limits for the state-of-the-art are shown in Fig. 3.1 [47]. The 8-bit ENOB performance at 10 GHz requires < 51fs of rms aperture jitter, and is slightly above current limits in electronic ADCs, but is well within the performance of photonic sources and sampling gates. Photonic clock sources such as mode-locked lasers have been characterized to have attosecond-resolution timing jitter [5], and total converter sampling jitter including the source and gate has been measured to be below 16fs [49] and below 8.5fs [4]. In reality, other noise sources (i.e. quantization noise and thermal noise) as well as distortion are included in the calculation of ENOB and an even more stringent jitter specification must be placed on the clock source and ADC sampling circuitry.

In addition to having extremely low jitter clock sources and sampling gates, wavelength interleaving, frequency channelization, and multicasting can be supported in a single fiber [7, 8, 50–52]. Photonic sampling gates have been realized with Mach-Zehnder modulators [4], or highly nonlinear fiber [52]. These photonic sampling gates have no additive jitter. Multicasting replicates the input signal onto multiple wavelengths in a single fiber for interleaved sampling and subsequent

Figure 3.1: Optical versus electrical jitter.
time-interleaved analog-to-digital conversion. Interleaving at multigigasample-per-second sampling rates is important since electronic ADC power consumption and performance do not scale linearly with sample rate [48].

The signal-to-noise and distortion ratio (SINAD) for a general impulse-sampled GS/s Nyquist analog-to-digital converter can be expressed as

$$SINAD = \frac{A_{sig}^2}{2\frac{\pi}{\Delta f}BW + A_{sig}^2(2\pi f_{in}t_{j,rms})^2 + A_{sig}^2HD_2 + A_{sig}^2HD_3 + ...}, \quad (3.1)$$

where $A_{sig}$ is the signal amplitude, $t_{j,rms}$ is the $rms$ aperture jitter, $v_n^2$ is the voltage noise spectral density of all circuit noise sources, $BW$ is the effective noise bandwidth, and $HD_2$ and $HD_3$ are the second and third order harmonic distortion (both are functions of $A_{sig}$). The effective-number-of-bits (ENOB) of an analog-to-digital converter is calculated as

$$ENOB = \frac{SINAD[dB] - 1.76}{6.02}. \quad (3.2)$$

For GS/s ADCs with ever-increasing input frequencies, sampling jitter can be the limiting factor in the SINAD due to the quadratic relation between input frequency and jitter noise power in (3.1). To achieve a jitter-only-limited 10 effective-number-of-bits with a 1GHz input sinewave, $t_{j,rms}$ must be less than 127fs, an aggressive number for silicon integrated circuits, which have just recently broken the 100fs mark [3]. At 10GHz the <12.7fs of required jitter is aggressive even for a low phase noise electronic clock source. Maintaining high broadband linearity, low noise, low jitter, and low power consumption at GS/s rates mandates strict tradeoffs in traditional electronic ADCs.

This discussion of photonic sampling and analog-to-digital conversion is split into two sections. Section 3.1 describes a single-channel 2GS/s integrate-and-dump receiver suitable for 2GS/s high-linearity photonic analog-to-digital conversion. Section 3.2 describes a rate-scalable photonic sampling technique for time-interleaved sampling (i.e. at a rate of $N\cdot2GS/s$), with design and measurement results for one of the sub-rate (2GS/s) time-interleaved integrate-and-sample electronic receivers. The integrate-and-sample receiver exceeds the performance of the
integrate-and-dump receiver in terms of noise and distortion (i.e. SINAD), signal integrity, and closed-loop offset cancellation.

3.1 2GS/s Photonically-Sampled Integrate-and-Dump Receiver

A single-channel of a simple optical sampling system is illustrated in Fig. 3.2. An analog (RF) electrical signal is both sampled and modulated onto an optical pulse train via a Mach-Zehnder modulator, although other methods could be used as in [51]. The sampled optical pulses are then detected through a high-linearity photodetector and a current pulse is fed to the input of the integrate-and-dump (IAD) receiver. The IAD then integrates the pulses and buffers them to an electronic ADC. Integration provides a relatively constant output waveform to be sampled at $s_B$ (instead of $s_A$ at the peak of the optical pulse), thus reducing the jitter requirements of the subsequent ADC. By interleaving the samples on multiple wavelengths, multiple integrate-and-dump channels could be used in an interleaved fashion to achieve sampling rates greater than 20 GS/s.

In this work, the high-linearity electronic front-end is realized with an integrate-and-dump receiver. The IAD precedes an electronic ADC and relaxes
its bandwidth, jitter, and dynamic linearity requirements. The following subsec-
tions discuss the circuit design and measurement of the IAD in a 120nm SiGe
BiCMOS process.

### 3.1.1 Integrate-and-Dump Circuit Design

A high dynamic range, opto-electronic IAD interface must overcome several
 circuit obstacles to simultaneously achieve low harmonic distortion and low noise
to maximize the SINAD from (3.1). First, the IAD must receive a single-ended
signal from the photodetector and convert this to a differential signal with minimal
added distortion and noise. Secondly, the large electrical bandwidth of the current
pulses requires both low input-referred noise spectral density and high broadband
linearity. Next, the output swing should be approximately $1V_{pp}$ in order to take
advantage of the full-scale range of the ADC, requiring a sufficiently high unity-
gain-bandwidth ($UGB$) from the integrator. Secondly, the photodetector can only
supply positive photocurrent and a DC offset must be removed from the waveform
as shown in Fig. 3.2

Although MOS open-loop integrators and buffers can achieve modest lin-
earity up to several hundred MHz, wideband linearity and high signal swings are
difficult to achieve. SiGe BiCMOS offers both high device $f_T/f_{max}$ and larger
signal swings. Open-loop SiGe buffers and integrators can achieve high-linearity,
low-noise, and thus high dynamic range performance and have been employed in
this design.

The proposed integrate-and-dump receiver is shown in Fig. 3.3 and is de-
signed to operate at 2 GS/s for a single channel. A single-ended-to-differential
conversion is performed through an active broadband balun (balanced-unbalanced)
circuit. This converts the single-ended photocurrent to differential voltage pulses,
which are processed by a linearized Gm-C integrator, and then buffered out to
an electronic quantizer/digitizer (not shown for clarity). A replica photodetector
which is not illuminated is used to provide a balanced impedance at the input.

The active balun shown in Fig. 3.4a is a resistively degenerated differential
amplifier with a resistive load; its single-ended-to-differential conversion and
common-mode rejection relax the linearity and common-mode-feedback specifications for the following Gm-C integrator. Because of the combination of single-ended input, DC offset from the positive photocurrent, and DC offsets from device mismatch, contributions from both second-order harmonic distortion and third-order harmonic distortion must be considered in (3.1). For a balanced differential pair with a DC input offset voltage, increasing negative feedback decreases not only $HD_3$ but also $HD_2$; the Taylor series used in [36] can be adapted for harmonic distortion:

$$HD_{2,f} \approx \frac{6HD_3}{A_{\text{sig}}} v_{os}.$$  \hspace{1cm} (3.3)

Local feedback through emitter degeneration is effective for broadband linearization to decrease $HD_3$:

$$HD_{3,f} \approx \frac{HD_{3,\text{no feedback}}}{(1 + f)^3} v_{os},$$  \hspace{1cm} (3.4)

where feedback factor $f = g_m R_e$. Unfortunately, this resistive degeneration also increases the noise spectral density in (3.1) both by reducing each differential pairs effective transconductance and by adding broadband thermal noise from the degeneration resistors. The output voltage noise spectral density for a unity gain ($R_L \approx R_E$) resistively loaded and degenerated amplifier with strong feedback ($f \gg$)
Figure 3.4: The unity-gain active balun (a) which converts the single-ended optical signal to differential and relaxes the common-mode feedback requirements for the following Gm-C integrator (b) which performs the integrate-and-dump operations.

1) such as the active balun can be approximated as

\[ \frac{v_n^2}{\Delta f} \approx \frac{1}{I_{DC}} (16kTfv_T + 4qv_T^2), \]  \hspace{1cm} (3.5)

Increasing the feedback factor f increases the noise spectral density while reducing distortion. Reducing the noise spectral density requires either reducing f (which increases both HD₂ and HD₃) or increasing the power consumption through a larger bias current I_{DC} (the differential pair consumes 2I_{DC}). Similar linearity/noise tradeoffs apply to the Gm-C integrator as well.

Inserting the active balun to perform single-ended to differential conversion relaxes the amount of degeneration required for the Gm-C integrator shown in Fig. 3.4b. Reducing the degeneration allows the unity-gain-bandwidth to be increased as Re is decreased:

\[ UGB = \frac{g_m}{C_{int}(1 + g_mRe)} \approx \frac{1}{C_{int}Re}. \]  \hspace{1cm} (3.6)
In order to achieve a high $UBG$, minimum channel length devices were used for the pFET load to decrease their (nonlinear) contribution to $C_{int}$, and a capacitance of 83fF was added as MIM capacitors to each differential load to linearize the total capacitance. Resistive degeneration lowers the noise contribution and increases the output resistance of the pFET load. This finite output resistance creates a lowpass response instead of an ideal integrator during the integration period as well as voltage droop during the hold period.

For this photonic integrate-and-dump circuit, the unity-gain-bandwidth target was approximately $2\pi \cdot 5$ GHz to achieve an output signal swing of 1V$_{pp}$; this choice balances the available optical power, photodetector linearity, photodetector shot noise, electronic BW, noise, and linearity. Also assumed in this tradeoff is a linearization of the modulator nonlinearity, either electrically or via digital post-processing.

In order to have differential outputs with a zero average value and maximum signal excursions, the positive photocurrent d.c offset must be canceled. This is accomplished via a current pulse of opposite (average) amplitude during the integration period as seen in Fig. 3.3. By instantaneously canceling the d.c. offset during the integration period, this current pulse further reduces the second order distortion. The amplitude of the current can be adjusted externally by adjusting $v_{offset}$.

The timing circuits must generate clocks for the reset and integration/d.c. offset cancellation period that are non-overlapping and are less than 50% duty cycle. This is done by slicing the input clock voltage to adjust its duty cycle. An AND gate and a time delay of approximately 60ps is used to generate the proper time alignment for the reset period as shown in Fig. 3.5. The integrate (INT) signals drive a differential pair that injects a current to cancel the DC offset of the photocurrent during the integration period. The reset signal is applied through AC coupling to the triple well nFET that shorts the differential outputs of the Gm-C integrator together. Out of the total period of 500ps, integration period is less than 200ps, the hold period is approximately 100ps, and the reset period is less than 200ps. Simulations for the entire timing chain indicate that <160fs of
Figure 3.5: Timing circuits to modify the clock duty cycle and generate the integrate and reset signals off of a 2 GHz clock. Current-mode logic is used for the buffers and AND gate.

jitter is added to the integration pulse, and <116fs of jitter is added to the reset pulse.

3.1.2 Integrate-and-Dump Measurement Results

The integrate-and-dump receiver is fabricated in a 120nm SiGe BiCMOS process. The chip microphotograph is shown in Fig. 5. A 5-V analog supply is used for the first two stages and supplies 84mA to the active balun and Gm-C integrator. A 3.5-V supply is used for the output buffer to lower its output common-mode voltage and supplies 67mA of current. The integrate-and-dump timing circuits consume 37mA from a 2.5-V supply. In total the integrate-and-dump receiver consumes less than 750mW.

To verify the waveform behavior an Agilent DSO80604b real-time oscilloscope was used to measure the output of the integrate-and-dump receiver for a sinewave input of 100 MHz. Both differential inputs were applied to separate channels and subtracted on the scope as seen in Fig. 3.7. Because the input sinusoid is
continuously applied, and due to the finite input bandwidth of the oscilloscope (6 GHz), there exists some residual signal during the reset period. The vertical scale is 200mV/div; the approximate differential output voltage is $1V_{pp}$.

In order to validate the performance of the integrate-and-dump receiver with an input sinusoid, the IAD was connected to a National ADC1600RB ADC evaluation board with a measured low-frequency ENOB of approximately 9.4b. This board offers both better linearity and noise performance compared to the real-time oscilloscope, but unfortunately a lower input bandwidth 2.8 GHz @ only 1.6GS/s. Therefore, the frequency-domain measurements in Fig. 3.8 and 3.9 are measured at 1.6GS/s. Fig. 3.8 displays an FFT of the digitized output of the IAD with a 793 MHz input tone and an ENOB of better than 7.5b. The SNR and ENOB measured versus input frequency with the ADC1600RB board are shown in Fig. 3.9. The measured ENOB is close to 7.5b from 222 to 900 MHz and includes the ADC boards noise and distortion.
Figure 3.7: Integrate-and-dump receiver measured with a 100 MHz input sinusoid on an Agilent DSO80604b real-time oscilloscope.

3.2 Rate-Scalable Multi-GS/s Photonic Analog-to-Digital Conversion

The rate-scalable photonic sampling architecture is shown in Fig. 3.10 [7, 8, 50–52]. The RF input is impressed onto an optical carrier via the Mach-Zehnder Modulator (MZM). Four-wave mixing in a single highly-nonlinear fiber replicates the RF input onto multiple optical wavelengths. Subsequently, each wavelength is delayed so that the RF signal is shifted by $\Delta t = 50 \text{ps}$, and a subrate clock (relative to 20 GS/s) samples all interleaved wavelengths simultaneously, again in a single fiber. Sharp sampling pulses are dispersively stretched in single-mode fiber, spreading the optical power temporally so that the instantaneous power does not saturate the photodetectors and electronic receivers. After an arrayed waveguide grating, each wavelength is demultiplexed to a separate photodetector and integrate-and-sample (IAS) receiver. Sample-and-hold outputs are provided to an array of electronic ADCs. The scalability and potential jitter improvements of this Copy-and-Sample-All technique are discussed in [9]; the achieved sample
Figure 3.8: FFT of the IAD output connected to the National ADC1600RB evaluation board with a 793 MHz input tone. The sample rate is reduced to 1.6GS/s due to the ADC evaluation board.

rate for a single channels is significantly higher [7] compared to previous work [5,49] which would require significantly more subrate channels to achieve the same instantaneous bandwidth.
Figure 3.9: SNR and ENOB versus input frequency for a differential sinusoidal input using the National ADC1600RB evaluation board. SNR is measured at the peak ENOB input amplitude. The sample rate is reduced to 1.6GS/s due to the ADC evaluation board.
Figure 3.10: Photonic sampling architecture with electrical receiver and quantizer.
To reach a linearity of $57\,dBc$ requires a photonic link, multicasting, and sampling performance with an SFDR of $\sim 130\,dBH\,z^{3/2}$. This is approximately an order of magnitude higher than state-of-the-art microwave linearized photonic links which have achieved $>120\,dBH\,z^{3/2}$ [53]. The bottleneck for SFDR is the RF to photonic modulation process. Since the MZM represents a well-known nonlinearity, distortion from modulator nonlinearity can be compensated [54,55].

Fig. 3.11 shows the optical pulse train for a single channel sampling a d.c. signal and a 200MHz sinusoid at 2GS/s. Pulses are spaced in time by a period of 500ps. These amplitude-modulated pulse samples will be applied to a photodetector to convert optical power into current, and then subsequently integrated, sampled, and digitized by the electronic receiver.

**Figure 3.11**: Photonic sampling pulses at 2 GS/s sampling a d.c. signal (top) and a 200 MHz sinusoid (bottom) measured on an optical scope. The pulse FWHM duration is approximately 2 ps and is dispersed in SMF to approximately 50 ps for electronic sampling. The data was acquired with an optical equivalent sampling oscilloscope with 800 fs resolution.

The amplitude and bandwidth of the pulse are determined by the full-width half-maximum (FWHM) pulsewidth. For the same pulse energy, the FWHM and amplitude are inversely related as shown in Fig. 3.12. Dispersion limits the achievable SNR for long pulse widths, but short pulses require high bandwidth and high peak current excursions, which cause excessive receiver distortion. The
pulse 3-dB bandwidth is related to the pulsewidth as $BW_{3dB, pulse} = \frac{0.31}{FWHM}$. A 50 ps FWHM pulse in the optical domain will have an electrical bandwidth of approximately 6.2 GHz, which is significantly larger than the Nyquist frequency (1 GHz) for a 2 GS/s ADC.

![Figure 3.12: Gaussian pulsewidths for various FWHM and dispersion, normalized in integrated current (charge). Longer FWHM reduces the peak voltage for the same pulse energy and reduces the subsequent bandwidth and linearity requirements of the photodetector and electronic receiver.](image)

To maximize the SNR, an integrate-and-sample (IAS) electronic receiver is used, which is the combination of the integrate-and-dump receiver from [6] and a sample-and-hold circuit consisting of two cascaded track-and-holds. The photonic pulse is approximated as a Gaussian pulse from an electronic standpoint with a full-width half-maximum (FWHM) in optical power and electric current of 50 ps. Mathematically, this can be expressed for a sample rate $T_S$ as

$$i_{pd}(t, n) = \sum_{n=-\infty}^{\infty} i_{RF}(nT_S) \exp \left(-\frac{(t - nT_S)^2}{FWHM^2} \frac{4 \ln(2)}{FWHM^2} \right). \quad (3.7)$$
The IAS receiver approximates a matched filter for the Gaussian pulse as long as integration persists only when there is considerable optical power. Longer integration periods degrade the SNR since the noise power increases proportionally with the integration time. However, longer integration time mitigates photodetector saturation by continuing integration of the low amplitude tail as the peak pulse is spread over a longer duration in the time domain due to photodetector saturation [56], [57]. Integration also provides the subsequent sampling circuits with a relatively constant waveform after the integration period, relaxing both bandwidth requirements and sampling jitter. Windowed integration is expressed in the time-domain with an impulse response of

\[ z(t) = \frac{g_m R}{C_{int}} \left[ u(t) - u(t - T_{int}) \right], \]  

(3.8)

where \( g_m \) is the transconductance of the integrator, \( C_{int} \) is the integration capacitance, and \( T_{int} \) is the integration period. Taking the Fourier Transform of (3.8), the frequency response of the ideal Gm-C IAS is

\[ |Z(f)| = \frac{T_{int} g_m R}{C_{int}} |\text{sinc}(T_{int} f)|. \]  

(3.9)

The IAS receiver improves the performance of the photonic ADC front-end from [7] via matched filtering, d.c. offset compensation, and distortion mitigation due to windowed integration.

### 3.2.1 Performance Limitations for Optical Sampling

**Noise Sources**

Noise contributions at the input of the IAS are amplitude spontaneous emissions (ASE), relative intensity noise (RIN), shot noise, thermal noise from the 50-Ω interconnects, as well as thermal, shot, and channel noise from the Gm-C integrator and track-and-hold stages. As the signal-to-noise ratio (SNR) and SINAD are established by the electronic receiver response, the SNR is calculated here assuming impulse sampling following the windowed integration. The operating regions for the photonic link noise are shown in Fig. 3.13. At low optical power, the link is thermal-noise limited. At medium optical powers, the shot noise limits the
link as increasing the optical power results in a quadratic increase in electrical power since \( I_{PD} = R_\lambda P_{opt} \) where \( R_\lambda \) is the optical responsivity. At high power, the link is limited by laser amplitude and the relative intensity noise; the optimum optical power and peak SINAD is obtained in this region. Further increases in optical power result in photodetector and receiver saturation, ultimately resulting in distortion-limited performance.

**Figure 3.13**: Various operating regimes for signal-to-noise ratio as a function of optical power.

A model of the front-end noise of the IAS receiver is shown in Fig. 3.14. The noise current spectral density \( \frac{\Delta}{\Delta f} \) contains contributions from photodetector shot noise, thermal noise from the source and input resistance, and transconductor noise.

\[
\frac{\Delta^2}{\Delta f} = 2qI_{PD} + \frac{4kT}{R_s} + \frac{\Delta^2}{g_m^2}. \tag{3.10}
\]

The IAS receiver provides noise shaping due to the windowed integration. The magnitude of the Fourier Transform of the integration window gives a noise transfer function from (3.9). Adding all noise sources, the SNR is expressed at the output.
of the Gm-C integrator as

\[
\text{SNR} \approx \frac{\left\langle \left( \int_{nT_S}^{nT_S+T_{int}} i_{pd}(t, n) \, dt \right)^2 \right\rangle}{\frac{1}{2T_{int}} \left[ \frac{i_{n,T}^2}{\Delta f} \right] + \frac{kTC_{int}}{(g_mT_{int})^2}}.
\] (3.11)

Finite Reset Bandwidth

Finite reset bandwidth causes a residue to persist from previous integration periods as described in subsection 2.1.3. To minimize the effects on both SNR and interleaved SFDR [58], the residue must be minimized.

Figure 3.14: Integrate-and-sample system for analyzing jitter and SNR.

Jitter

In the following subsections, jitter will be described for the optical sampling front-end with optical pulses. Integration relaxes the jitter requirements in the IAS: the integration window is significantly longer than the pulse FWHM, capturing the entire pulse as shown in Fig. 3.14. Therefore, the most important sources of jitter are the d.c. offset compensation and the voltage droop in the Gm-C integrator. To compare between windowed integration and the alternative of impulse sampling, the jitter limitations impulse sampling the Gaussian pulse shown in Fig. 3.14 are described in a following subsection.
Jitter due to d.c. offset compensation

In the photonic sampling architecture, the d.c. imbalance in the photonic sampled pulse creates a jitter issue in the electronic receiver. A sampled discrete-time feedback loop is used in the IAS to instantaneously cancel the d.c. offset, applying a pulse opposite in polarity to the Gaussian photocurrent pulse as depicted in Fig. 3.14. Unfortunately, the duration of this compensation period $T_{off}$ is varied by the clock jitter $\delta t$, both on the rising and falling edges of the pulse. As a result, the SNR due to jitter is

$$\text{SNR}_{DT-jitter} \approx 10 \log_{10} \left( \frac{T_{off}^2}{t_{j,rms}^2 (1 - c_{\delta t\delta t})} \right), \quad (3.12)$$

where $c_{\delta t\delta t}$ is the correlation between the rising and falling edges of the offset current pulse, and $t_{j,rms}$ is the rms timing jitter. Correlation $c_{\delta t\delta t}$ serves to reduce the impact of jitter for an integrated pulse [59].

Jitter due to droop

The output of the integrator will droop due to the finite output resistance of the npn and pFET load. As such, there is an additional opportunity for droop-induced-jitter for the optical modulated pulse train. During the hold period, the output of the Gm-C integrator follows:

$$v_{out,Gm-C}(t) = \frac{g_m R_S T_{int} i_{RF} (kT_S)}{C_{int}} e^{-t/\tau}, \quad (3.13)$$

where $\tau$ is the time constant of the output impedance of the integrator. Taking the Taylor series expansions around $t \approx 0$ and integrating a whole period of $i_{RF} (kT_S)$, the SNR due to leaky integration is

$$\text{SNR}_{droop} \approx 20 \log_{10} \left( \frac{\tau}{t_{j,rms}} \right). \quad (3.14)$$

Because the pole frequency due to the output impedance of the integrator is much less than the signal frequency, the SNR degradation due to droop can be neglected.

Jitter due to impulse sampling of Gaussian pulse

Integration and sampling provides significantly better jitter performance compared to impulse sampling of the original Gaussian pulse waveform which has
a bandwidth higher than 6 GHz. If instead impulse sampling is used to sample the peak of the Gaussian pulse as shown in Fig. 3.14, jitter $t_{j,rms}$ and sampling skew $t_{skew}$ impacts the SNR as

$$\text{SNR}_{\text{impulse}} \approx 20 \log_{10} \left( \frac{\text{FWHM}^2}{t_{j,rms} t_{skew} 8 \ln(2)} \right). \quad (3.15)$$

For instance, for a FWHM=50 ps pulse, $t_{skew} = 10$ ps, and $t_{j,rms} = 100$ fs, the maximum achievable ENOB is 8.5b. In contrast, windowed integration has an insignificant impact on SNR if the integration window is longer than the pulse duration, i.e. $T_{int} > 3 \text{FWHM}$.

**Settling into ADC**

Accuracy between the sampled data at the track-and-hold output and the ADC input requires sufficient settling time. The settling accuracy is degraded by finite input and output bandwidth, packaging, interconnect signal integrity, and differential mismatch. With the cascaded master-slave track-and-hold architecture, the output waveform is held constant for most of the clock period of 500 ps. Assuming that the track-and-hold output is settled for approximately 400 ps, the output track-and-hold bandwidth and input bandwidth of the subsequent ADC should exceed 2.75 GHz for proper settling to 10-bits. Packaging inductance also degrades settling as excessive bondwire inductance causes ringing and instability in the output waveform. Frequency-dependent loss and dispersion in the PCB transmission lines and cables produces low amplitude settling tails with relatively long time constants. Differential mismatch converts common-mode noise, distortion, and interference into differential mode. In order to mitigate 2nd-order distortion from appearing in the presence of interconnect and packaging mismatch, a fully-differential 50-Ω buffer is implemented with symmetric layout routing to avoid differential mismatch.

**Distortion**

The IAS receiver must simultaneously have low noise performance and low distortion. The photonic sampling architecture provides several obstacles that
must be overcome to achieve high dynamic range. First, the single-ended photocurrent from the photodetector must be converted to a differential signal and integrated with minimal distortion. Single-ended signals are especially taxing on the 2\textsuperscript{nd}-order distortion performance of a differential circuit. Additionally, the photodetector swing must be kept to a minimum to avoid distortion while at the same time maximizing the SNR due to shot and thermal noise requires maximizing the output photocurrent; this tradeoff is expressed in terms of optical power in Fig. 3.13.

**SINAD**

As both noise and linearity contribute to the overall performance, the best performance metric for the hybrid electronic photonic ADC is SINAD/ENOB. SINAD is listed here for the integrate-and-sample receiver in terms of the voltage noise spectral density $\frac{v^2}{\Delta f}$, the effective noise bandwidth $BW_n$ which for the IAS is approximately $\frac{1}{2T_{int}}$, the jitter noise power $P_{n,j}$, and the second and third-order harmonic distortion terms.

\[
SINAD = \frac{A_{\text{sig}}^2}{2 \frac{v^2}{\Delta f} BW_n + 2P_{n,j}(A_{\text{sig}}) + A_{\text{sig}}^2 HD_2 + A_{\text{sig}}^2 HD_3 + \ldots}
\]

Integration helps to mitigate distortion due to the nonlinearity of the IAS for pulse inputs, as integration of the photocurrent averages the entire pulse. In contrast, impulse sampling samples the photocurrent peak amplitude which experiences the most nonlinear distortion.

**3.2.2 Circuit Design: Integrate-and-Sample Receiver**

A single channel of the integrate-and-sample receiver is shown in Fig. 3.15. A photodetector receives the dispersed, single-ended Gaussian sampling pulses shown in Fig. 3.10. The Gm-C circuit integrates the photocurrent and is reset after the integration period, ending the integration period and providing windowed integration. A cascaded master/slave track-and-hold provides a stable output waveform for almost an entire period that is 50–Ω buffered to a commercial ADC
Figure 3.15: Integrate-and-sample receiver with integrated track-and-hold for low-jitter, high dynamic-range photonic analog-to-digital conversion.

for quantization and data capture. The held output of the second track-and-hold allows proper settling at the input to the ADC, relaxing bandwidth, dynamic non-linearity, and jitter requirements for the commercial ADC. Finally, a discrete-time offset current is provided during the integration period to cancel the d.c. offset of the photocurrent pulse as well as the inherent offsets of the Gm-C filter and cascaded track-and-holds. Each block will be described in detail in the following subsections.

**Gm-C Integrator**

MOS-input Gm-C integrators have much better noise-linearity tradeoffs due to the intrinsic linearity of the MOS transistor compared to the exponentially nonlinear voltage-to-current relation of bipolar devices that must be heavily degenerated to obtain sufficient linearity [60]. However, a photonic system does not readily provide differential signals (i.e. photodetectors are single-ended) and the single-ended input places stringent requirements on the second-order distortion required in the front-end integrator.
Therefore, highly-degenerated bipolar devices must be used to get low 2nd-order distortion at the cost of higher thermal noise due to a reduction in transconductance and the thermal noise of the degeneration resistors. To simultaneously achieve low noise, high linearity, and high (unity-gain) bandwidth, a resistively-degenerated Gm-C integrator shown in Fig. 3.16 was used both to convert from single-ended to differential and also to integrate the optical pulse samples. Increasing the degeneration of the differential pair decreases their transconductance and reduces the unity-gain-bandwidth of the Gm-C integrator. High bandwidth is required to provide sufficient gain \( g_m T_{int} / C_{int} \) between the voltage generated by the photocurrent at the input of the Gm-C filter and the subsequent track-and-hold which requires \( 1V_{pp} \) to maximize the signal-to-noise ratio. The unity-gain-bandwidth (UGB) of the Gm-C integrator is expressed with strong degeneration \( g_m R_E \gg 1 \) as

\[
UGB = \frac{g_m}{C_{int} (1 + g_m R_E)} \approx \frac{1}{C_{int} R_E}. \tag{3.17}
\]

The main source of nonlinearity is the transconductance of the HBT and is expressed as

\[
i(v_{in}) = g_{m,1} v_{in} + g_{m,2} v_{in}^2 + g_{m,3} v_{in}^3, \tag{3.18}
\]

where \( v_{in} = i_{pd} R_S \) is the input voltage and \( R_S \) is the combination of the photodetector termination and input termination of the Gm-C integrator. Resistive degeneration was required in this block to provide wideband linearization due to the high bandwidth, single-ended optical pulses.

The second order harmonic distortion is the most difficult specification due to the inherent d.c. offset of the photodetector and the single-ended photocurrent. From [6], the distortion analysis in [36] is adapted for second-order harmonic distortion as

\[
HD_2 \approx \frac{6HD_3}{v_{in}} v_{os}, \tag{3.19}
\]

where \( HD_3 \) is the third order harmonic distortion with resistive degeneration feedback [6]:

\[
HD_3 = \frac{HD_{3, no feedback}}{(1 + g_m R_E)^3} . \tag{3.20}
\]

Increasing the resistive degeneration lowers \( HD_2 \) and \( HD_3 \) but at the cost of increased thermal, shot, and channel noise [6]. The noise spectral density of the
Gm-C integrator for $g_m R_E \gg 1$, $g_{m,p} R_S \gg 1$ can be expressed as

$$\frac{i_{n,Gm-C}}{\Delta f} = \frac{8kT}{R_E} + \frac{2q v_T^2}{I_{DC} R_E^2} + \frac{8kT \gamma g_{m,p}}{R_S} + \frac{8kT \gamma g_{m,p}}{(1 + g_{m,p} R_S)^2},$$

(3.21)

where $\gamma$ is a technology-dependent noise parameter, $R_E$ is the emitter degeneration resistor, $R_S$ is the pFET source degeneration resistor, and $v_T$ is the thermal voltage of the HBT. Degeneration of the pFET current sources is necessary to reduce the noise contribution from the last term in (3.21) but also to reduce droop and droop nonlinearity due to the nonlinear $g_{ds}$ of the pFET.

A reduction in Miller effect is also important for the Gm-C integrator, as the base-to-collector capacitance $C_{bc}$ of the input pair is effectively multiplied by the open-loop gain. Partial cancellation of the Miller capacitance is achieved via cross-coupled neutralization capacitances shown in Fig. 3.16 as a tradeoff between Miller effect and a degradation in input return loss due to additional capacitance at the input to the Gm-C integrator.

The common-mode feedback circuit is shown in Fig. 3.16. It is important that the common-mode feedback amplifier have a unity-gain frequency approximately equal to the differential-mode unity-gain frequency of the Gm-C integrator to avoid excessive common-mode variations, especially as a single-ended photocurrent is applied to the Gm-C integrator. In this architecture, the unity-gain frequency of the common-mode feedback loop is close to 5 GHz.

**Track-and-hold Amplifier**

Conventional GS/s track-and-holds with more than 10-bit linearity typically follow the architecture developed in [15] based on a switched emitter follower with a feed-through attenuation buffer. However, this architecture requires on precisely controlled fabrication, gain, and delay mismatch to reduce the hold-mode feedthrough. Hold-mode feed-through is a major issue for the track-and-hold in the IAS as it experiences a sharp, nonlinear reset waveform due to the switch at the output of the Gm-C integrator. Hold-mode feed-through is itself typically nonlinear even for a sinusoidal input [15]; in addition, the feed-through attenuation network in [15] contributes to pedestal error and thus to nonlinear distortion [61].
Figure 3.16: Schematic of the Gm-C integrator with the common-mode feedback amplifier.
Instead of using a conventional track-and-hold architecture, a new double-switching track-and-hold architecture proposed by [62, 63] is fabricated in SiGe BiCMOS for the first time. This architecture, not only provides better hold-mode isolation than conventional architectures but also provides excellent high-speed linearity due to pedestal compensation. This double-switching track-and-hold architecture is described in the following chapter in more detail.

Two track-and-holds are cascaded and clocked 180° out-of-phase to approximate a sample-and-hold, providing the sampling functionality in this integrate-and-sample receiver. Transient simulation results for a single Monte-Carlo run for the cascaded master-slave sample-and-hold are shown in Fig. 3.17. The simulated SFDR is better than 68 dBc, verifying a linearity-only ENOB of better than 11 bits. The simulated ENOB including noise is above 9b.

Figure 3.17: Simulation results for the cascaded master/slave double-switched sample-and-hold showing a linearity linearity better than 11 ENOB for a 1V\textsubscript{pp} input and output swing.(3.17)
Timing Circuits

To provide relative phase relationships across a broad range of input frequencies, a frequency divider is used to divide a 4 GHz sinewave into 2 GHz quadrature outputs to the subsequent clock buffers. The reset pulse is formed through a logical AND operation between the 4 GHz input frequency and differential quadrature output of the divider. The integration pulse is formed via the input signal and the in-phase output. The track-and-hold clocks are derived from the in-phase output of the divider; the master, or first-stage track-and-hold samples the integrated signal on the rising edge of the clock, and the slave, or second-stage TAH, samples the held output of the master on the rising edge of its clock. The integration period $T_{int}=250$ ps, the offset pulse duration $T_{off}=160$ ps, the reset period $T_{res}=250$ ps, and the track-and-hold clocks have 50% duty-cycles with periods $T_S=500$ ps. Simulation results indicate proper phase relationships between a clock rate of 1 to 8 GHz (500MSps - 4 GSps) operation.

**Figure 3.18**: Schematic of the timing circuits for the integration, reset, and the sampling clocks for the two track-and-hold amplifiers.
Discrete-time Differential-mode Feedback Loop for Offset Cancellation

The offsets of the photocurrent, Gm-C integrator, and cascaded track-and-hold stages are canceled by this discrete-time differential-feedback loop. During the integration period, this feedback loop applies a current pulse at the input to the Gm-C integrator; however, it continuously integrates the offset sensed from the output of the second track-and-hold in Fig. 3.15. In addition to canceling the d.c. offset of the photocurrent during this period, it also serves to instantaneously reduce the peak voltage at the input to the Gm-C integrator by creating a bipolar voltage instead of only a unipolar (positive) voltage excursion. The d.c. balance significantly reduces both second and third-order distortion in the IAS. The differential-mode feedback amplifier in Fig. 3.19 is resistively degenerated both to linearize its response and to reduce its unity-gain frequency. A 250 pF MOS capacitor is placed at the output of the amplifier to further limit its bandwidth and noise contribution to the IAS receiver, especially important as the feedback is applied at the input where the signal swings are the lowest and most susceptible to corruption by noise. An extremely low unity-gain-bandwidth is also necessary for closed-loop stability, as the Gm-C integrator has a pole at low frequencies.

Simulation Results

Simulations are run for a worst case input frequency close to Nyquist for both sinusoidal and optically sampled pulse inputs. Fig. 3.20 demonstrates the IAS receiver performance with a 937.5 MHz sinusoidal input; the simulated ENOB is 8.35b. Fig. 3.21 displays the results for a 937.5 MHz sinusoid sampled in the photonic domain and impressed upon a optical pulse train. The simulated ENOB is approximately 8.1b and displays better linearity performance but lower ENOB due to the additive noise of the d.c. offset compensation loop. The simulated differential output swing is 1 Vpp in both cases.
Figure 3.19: Differential-mode feedback amplifier for canceling common-mode current offset of the photodetector.

Figure 3.20: Simulated frequency-domain performance for an input frequency sinusoid of 937.5 MHz. The simulated ENOB is 8.35b.
Figure 3.21: Simulated frequency-domain performance for a photonically-sampled pulse train. From this simulation, the ENOB for the integrate-and-sample receiver is approximately 8.1b.
3.2.3 Measurement Results: 2GS/s

A two-channel integrate-and-sample receiver is fabricated in a 120nm SiGe BiCMOS process with a maximum $f_T$ for the npn HBT of 210 GHz. Each channel consumes 890mA from 5V and 2.5V supplies. The chip area is $1.6 \times 2.0$ mm$^2$ and is shown in the inset of Fig. 3.22 along with the test PCB. The test PCB is a four-layer board from a Rogers 4003 substrate with a dielectric thickness of 8 mils for high-frequency transmission lines and to accommodate the dense interconnections. The die is directly mounted on a copper block to dissipate heat. Bondwire length is minimized to reduce the inductance and possible settling time issues at the input and output.

Electrical Measurements

To validate the circuit packaging, $S$-parameters measurements show the bandwidth for acceptable input and output return loss of the receiver, which is important for packaging with a matched photodetector. To give a worst case scenario for the input matching, single-ended measurements are shown in Fig. 3.23 to simulate the single-ended photodetector and includes the effects of the PCB, package parasitics, and extracted parasitics of the Gm-C integrator. PCB connectors were not included in the simulated results and likely account for some of the degradation in measured input return loss. Additionally, the bondwire inductance to ground and non-ideal decoupling on-chip accounts for additional degradation in the return loss. The return loss is better than 10 dB to 5.8 GHz and remains better than 8 dB to 8.8 GHz.

The measured output return loss for the track-and-hold is given in Fig. 3.24 and determines the ability of the circuit to provide fast settling at the input of the ADC. The return loss is better than 10 dB to 6.5 GHz.

The track-and-hold output waveforms of the IAS are also captured on a real-time DSA71604C Tektronix scope; the gray dotted line represents the sampled 605 MHz sinusoid. The output of the dual-rank track-and-hold is a staircase waveform with held levels equal to the amplitude of the 605 MHz sinewave. Minimal ringing due to packaging inductance and emitter-follower peaking on-chip is
Figure 3.22: Microphotograph and printed circuit board layout of the two-channel integrate-and-sample receiver.
Figure 3.23: Input return loss of the IAS packaged onto the PCB, both measured single-ended for each differential input, and also simulated with a PCB package model with 0.5 nH of bondwire inductance.
Figure 3.24: Output return loss of the IAS and TAH PCB, measured single-ended for each differential output, and simulated with a PCB package model with 0.5nH of bondwire inductance.
observed during the hold period. The measured output waveform is shown close to its full-scale output of $1V_{pp}$ shown in Fig. 3.25.

![Figure 3.25](image)

**Figure 3.25:** Measured oscilloscope waveform of the differential output of the IAS (i.e. the output of the second track-and-hold buffered over 50-Ω) with a 605 MHz sinewave input (dotted gray).

To assess the frequency-domain performance of the IAS, electrical testing is conducted with a sinusoidal input. The output of the IAS is connected to a single channel of the National Semiconductor ADC1800RF ADC clocked at 2 GS/s. Fig. 3.26 displays the measured frequency-domain results for an input sinusoid of approximately 223 MHz. The measured ENOB is above 8.1b and the measured SFDR is approximately 64.6 dBc. The two-tone intermodulation distortion is measured and shown in Fig. 3.27; for an input approximately 203 MHz the IM3 products are approximately 51.5 dBc, and the SFDR is 57.6 dBc relative to the amplitude measured at peak ENOB.

The ENOB performance of the integrate-and-sample receiver is shown in Fig. 3.28. The peak ENOB is 8.1b with a 223 MHz input, shown in Fig. 3.26. The measured ENOB performance for the electronic ADC is also shown in Fig.
Figure 3.26: Frequency-domain measurement for effective-number-of-bits. An ENOB of 8.1b is measured with a 223 MHz input frequency.

Figure 3.27: Frequency-domain measurement for spurious-free dynamic range for an input amplitude envelope equal to that measured for peak ENOB.
3.28 and gives a baseline for the maximum measurable performance.

![Figure 3.28: Effective-number-of-bits versus frequency](image)

The measured SFDR and SNR are shown in Fig. 3.29 for the IAS and ADC and also with the ADC alone to give the measurement limitations. SFDR and SNR are measured at peak ENOB. Due to the sinc response from (3.9), higher frequency inputs are attenuated in the IAS, requiring a higher input amplitude and resulting in more distortion (lower SFDR and thus lower SNR at peak ENOB). This electrical test results in an overestimate of the distortion for a Gaussian pulse input, as the pulse doesn’t experience the sinc distortion.

**Photonic Sampling Test System**

To demonstrate the photonic sampled ADC performance, a pulse train was modulated with a standard Mach-Zehnder modulator (not linearized) which was fed with an electrical sinusoid at approximately 200 MHz. The pulses were generated using the cavity-less principle [7], i.e. no mode-locked cavity, with repetition rate of 2 GHz and a pulse width of 2.7ps. The modulated pulse train is connected to a single ended photodetector and subsequently fed to the IAS. To keep
Figure 3.29: SNR and SFDR measured at peak ENOB versus frequency.

Figure 3.30: Frequency-domain measurement for effective-number-of-bits with photonic sampling setup.
a balanced impedance, the unused differential input of the IAS is connected to a dummy photodetector that was not illuminated but is biased identically to the other photodetector to cancel out common mode, supply, and ambient noise. Modulator distortion from the MZM accounts dominates the distortion found in Fig. 3.30; the measured SNR is 46.6dB, including contributions from optical noise, photodetector shot noise, the IAS receiver, and the electronic ADC. With the implementing of digital linearization, this indicates an obtainable ENOB close to 7.5b limited by noise for a 2 GS/s (scalable with interleaved channels to 20 GS/s) sampling rate. As a comparison, two interleaved 2 GS/s Copy-and-Sample-All photonically sampled channels without the IAS receiver were measured to have 6.8 ENOB with digital modulator linearization [7].

3.3 Complementary Photonically-Sampled 2 GS/s ADC for Subsampling up to 50GHz

The integrate-and-sample receiver is also demonstrated with a novel photonic subsampling system with a sample rate of 2GS/s. Typical architectures have focused on single-ended electro-optic modulators and photodetectors. However, the single-ended detection severely complicates a high dynamic-range high-speed sampling receiver [6] in terms of second-order distortion and d.c. offset compensation. Dual-output modulators with two photodetectors can steer the sampling pulses between two “pseudo-differential” paths as demonstrated in Fig. 3.31. This “pseudo-differential” approach has several advantages. First, it rejects some of the laser RIN and ASE noise, converting half of the noise to common-mode and half to differential. Secondly, the d.c. offset inherent in the square law detection of the optical pulse via the photodetector is pushed into common-mode. Third, second-order distortion is minimized by having balanced paths with opposite signal excursions. Finally, there is an enhancement in photodetector and the electronic receiver front-end linearity as each photodetector has half the signal swing of a single-ended architecture.

Although used previously for single-ended measurements, the electronic
integrate-and-sample receiver is designed to be fully differential that it could be integrated into a pseudo-differential architecture as shown in Fig. 3.31. Following sampling of the analog input on the dual-output photonic modulator, the photodetectors convert from optical to electronic current and sends the current pulse to the IAS receiver over a 50-Ω A custom ADC board using the National ADC1800RB is operated at 2GS/s to capture and sample the data.

**Figure 3.31:** Photonic subsampling system.

Subsampling measurements are made with the architecture of Fig. 3.31, which is kept at a constant sample rate of 2 GS/s as the analog input is increased to almost 50 GHz and subsampled down to approximately 202.1MHz so that the electronic receiver sees the same 200 MHz amplitude-modulated pulse train as demonstrated in Fig. 3.32.

Without the availability of a linearized modulator with more than 50 GHz of bandwidth, measurement of SNR are performed to almost 50 GHz and are shown in Fig. 3.33. The SNR is approximately 48.5 dB (i.e. a noise-only ENOB of 7.8b) with an input frequency of 202.1 MHz, and drops to approximately 36.4 dB at 49.8 GHz. There is a slight dip at 20 GHz due to excess noise from the amplifier driving the modulator and laser instability. The measured SNR over the entire frequency range indicates an aperture jitter of less than 45 fs.

Fig. 3.34 demonstrates the frequency-domain behavior of the entire photonic subsampling architecture with an input of 49.8 GHz with the digital data processed from the National ADC. The third harmonic is dominant as the modulator is not linearized; however, the SNR was calculated in the frequency-domain.
Figure 3.32: Demonstration of the photonic subsampling measurement where all tones alias to the same frequency of approximately 202.1 MHz. The 202.1 MHz signal is then subsequently received in the integrate-and-sample receiver and passed off to a commercial ADC for digitization.

Figure 3.33: Measured photonic subsampling system of the SNR of the subsampled signal versus frequency at a 2 GS/s sampling rate. An SNR better than 36 dB is obtained with an input of 49.8 GHz.
Figure 3.34: Photonic subsampling measurement with an unlinearized modulator. A 49.8 GHz input is sampled on the dual-output Mach-Zhender modulator at a sample rate of 2 GS/s and aliased down to 200 MHz.

using this data. The linearity for an optical link is given to first order by taking the ratio of the third order harmonic and fundamental from [64]:

\[ HD_{3, MZM} \approx \frac{1}{24} \left( \frac{A_{in}}{V_{\pi}} \right)^2, \tag{3.22} \]

where \( V_{\pi} \) is the half-wave voltage and \( A_{in} \) is the input amplitude to the modulator. To maximize SNR, the input to the modulator should be increased to full extinction. However, for these measurements, the input amplitude to the modulator is kept in a weakly nonlinear region \( (A_{in} \ll V_{\pi}) \) such that either digital linearization or a linearized modulator [64] could result in a reduction in (3.22) so that the photonically-sampled ADC would not be limited by its distortion performance. This presents the highest measured SNR for a multi-GHz BiCMOS THA in a Si/SiGe process.
3.4 Conclusions

Analysis and design of an electronic receiver designed to sample optically generate Gaussian pulse samples in a 2 GS/s ADC with better than 8 ENOB is described. The electronic IAS receiver was measured to have a measured ENOB better than 8.1 b and a SFDR better than 64 dBC for a single tone. The two-tone IMD was measured at the same envelope amplitude as that used for peak ENOB and was approximately 57.6 dBC. Subsampling measurements are presented with a pseudo-differential sampling architecture; a SNR of 36.4dB is measured with an input of 49.8GHz at a sample rate of 2GS/s.

Acknowledgments

Chapter 3 is mostly a reprint of the material as it appears in IEEE Proceedings of SiRF, 2012, Timothy D. Gathman; James F. Buckwalter, from material submitted to IEEE Transactions on Microwave Theory and Techniques, 2012, Timothy D. Gathman, James F. Buckwalter, and also from material submitted to IEEE Journal of Solid Stage Circuits, 2012; Timothy D. Gathman; James F. Buckwalter; Andreas O. J. Wiberg. This dissertation author was the primary author of this material.
Chapter 4

High-Speed Sampling Circuits and Interleaved Front-ends in SiGe and InP BiCMOS Technology

Wideband track-and-hold amplifiers (THAs) are required for high-fidelity sampling of wideband signals and for undersampling high-frequency signals in analog-to-digital converters (ADCs). THAs reduce the timing and dynamic requirements of the following quantization circuitry in flash and other high-speed ADCs, resulting in better ADC performance for wideband (GS/s) systems. Subsampling may also be used to avoid downconversion complexity and impairments, or to allow the ADC to perform quantization at a lower rate [65].

To-date, conventional THAs are mostly oversampling. Recently, there has been interest in THAs for subsampling [65,66]. For subsampling applications, the dynamic nonlinearity and jitter are handled by the front-end track-and-hold, and an undersampling ADC with a lower sample rate than Nyquist (for the input signal), lower bandwidth, and lower power dissipation accurately samples the output of the THA. For better signal integrity and settling into an off-chip ADC, two THAs are cascaded and clocked out of phase to create a sample-and-hold am-
plifier (SHA) as shown in Fig. 4.1. At higher input frequencies (subsampled or oversampled alike), aperture jitter is limited to the achievable signal-to-noise ratio (SNR):

$$SNR_{jitter} = 20 \log_{10} \left( 2\pi f_{in} t_{j,rms} \right),$$

(4.1)

where $f_{in}$ is the input frequency and $t_{j,rms}$ is the $rms$ aperture jitter. To date, commercial bipolar THAs have better measured jitter performance (<50fs) [67] compared with the state-of-the-art jitter performance for ADCs which have only recently broken <100fs [3].

A new approach for bipolar track-and-hold amplifiers is presented which achieves wide-band, high-resolution sampling. Compared to conventional THAs, higher linearity and hold-mode feed-through are obtained via hard-switching the input amplifier from the signal path and from an auxiliary feedback amplifier lowering the pedestal error across the switched-emitter-follower.

In section 4.1, THA architectures will be discussed; section 4.2 details the design tradeoffs including bandwidth, linearity, noise, mismatch, and power dissipation. Measurements are reported in section 4.3 for two sample-and-hold amplifier (SHA) architectures fabricated in 120nm SiGe. Section 4.4 demonstrates the design of 40 GS/s InP THA and a hybrid time-interleaved InP BiCMOS SHA employing MOS devices for the lower-speed, time-interleaved circuits.

### 4.1 Track-and-hold Amplifier Architecture

Both distortion and noise must be considered in the THA architecture to maximize the accuracy of the sampled value. Closed-loop feedback approaches to linearization are attractive at lower sample rates and can yield more than 10 bits of linearity; however, at GHz sample rates open-loop linearization approaches are typically used, forcing the designer to make noise and power consumption tradeoffs to achieve the distortion target. Noise is also significant problem for wideband THAs as the noise bandwidth (and input bandwidth) is significantly larger than the Nyquist bandwidth (i.e. several GHz) and wideband noise is aliased on top of
Figure 4.1: Use of a sample-and-hold at the front-end of an ADC to improve the performance and/or reduce the sample rate of the ADC if the SHA is subsampling. The output of the second track-and-hold amplifier holds the sampled value for almost the entire sample period, reducing the settling and dynamic requirements of the ADC.

the signal bandwidth during the sampling process, degrading the SNR.

Classical track-and-hold architectures have a simplistic topology of a single input buffer, current switch, and output buffer as shown in Fig. 4.3 [68]. However, they are only suitable for 10-bit linearity up to inputs and sample rates of \( \sim 100 \) MHz. Modern high-speed track-and-hold architectures such as [15] shown in Fig. 4.4 by necessity use a more complicated topology to improve high-frequency linearity and accuracy. With input frequencies in the several hundred MHz and above, signal feed-through becomes more difficult to mitigate with simple cross-coupled capacitors; in addition, pedestal compensation is necessary to maintain high linearity and reduce pedestal errors. The architecture in [15] seeks to improve hold-mode isolation and reduce pedestal error via two auxiliary buffers, one to provide feed-through attenuation higher than available with cross-coupled capacitors, and the second to provide pedestal compensation to improve linearity and reduce nonlinear distortion in the held value.

The waveforms at the output of the switched emitter-follower are shown in Fig. 4.2, with and without compensation. The pedestal labeled as uncompensated
in Fig. 4.2 creates a single-ended voltage step that increases the distortion of the sampled value. If instead, both differential inputs to the switched emitter-follower experience the same voltage step, i.e. a common-mode step, then the pedestal error is decreased as in the *compensated* diagram. Pedestal compensation is described in more detail in subsection 4.2.1.

The high-speed double-switching [62, 63] track-and-hold architecture uses current-switched emitter-followers as well for the sampling switch similar to [15]. However, significantly higher feed-through attenuation is provided through hard-switching the signal path from the input buffer. Pedestal compensation is achieved through an auxiliary feedback buffer as in [15]. This double-switching architecture uses one less buffer for lower power dissipation and lower noise and theoretically has much lower hold-mode feed-through due to hard switching of the signal path, rather than relying on precise matching of gains and phases of the feed-through attenuation buffer and cross-coupled feed-through capacitor as in [15].

![Diagram of pedestal compensation](image)

**Figure 4.2:** Effect of pedestal compensation; a pedestal feedback amplifier reduces the asymmetry between the differential voltage steps during the track to hold transition.

### 4.2 120nm SiGe BiCMOS Circuit Design

The double-switching THA is designed in a 120nm SiGe BiCMOS process with $f_T$ and $f_{max}$ of approximately 200 GHz. For maximum signal swings,
Figure 4.3: Early bipolar track-and-hold architecture.

Figure 4.4: Conventional bipolar track-and-hold architecture with pedestal compensation and feedthrough attenuation.

Figure 4.5: Double-switched bipolar track-and-hold architecture with pedestal compensation and improved feedthrough attenuation.
linearity, and speed, npn devices are used exclusively in this design. The double-switching THA schematic is shown in Fig. 4.6 and is comprised of two amplifiers, a switching matrix, a switched emitter-follower, and an emitter-follower buffer. The main and pedestal compensation amplifiers are identical resistively degenerated npn amplifiers with current switching above the input devices to switch the main and pedestal compensation amplifiers between the signal load $R_L$ and the dummy load $R_{dummy}$. Sampling is performed by current-switching the emitter-followers which take their input from $R_L$; the held value is stored on the hold capacitor $C_h$. Unfortunately, the base current of $Q_{17}$ and $Q_{18}$ discharges the voltage stored on $C_h$. The performance and tradeoffs for the main and pedestal amplifiers, current switch matrix, switched emitter-follower, and emitter-follower output buffer will be described in the following sections.
Figure 4.6: Schematic of the double-switched track-and-hold architecture in 120nm SiGe BiCMOS.
4.2.1 Linearity

The linearity of the main and pedestal compensation buffers are dictated by the strength of the resistive degeneration. The nonlinearity of the differential pair is expressed from third-order harmonic distortion $HD_3$:

$$HD_{3,R_E} = \frac{A_{\text{sig}}^2}{12v_1^2(1 + g_m R_E)^3}$$

(4.2)

Fully-differential operation of the buffer and pseudo-differential operation of the switched emitter-follower and interstage buffers significantly reduce the second-order distortion. As a result, only third-order distortion will be considered here.

The other main source of nonlinearity is due to nonlinear base-emitter modulation of the switched emitter-follower (SEF) due to the charging current required to charge the hold capacitor ($C_h$ in Fig. 4.6). Tradeoffs between bandwidth, noise, distortion, and droop must be made when choosing the hold capacitor size. A larger hold capacitor will reduce the bandwidth of the emitter-follower, decreasing the noise bandwidth and $rms$ sampled noise voltage, and will have less droop during the hold-mode. Droop during hold-mode is due to the base current discharged by the following emitter-follower stage, i.e. due to the base current of $Q_{18}$ in the half circuit of the SEF in Fig. 4.7. With perfect matching, the discharge currents into each of the differential bases will be identical, and only a common-mode voltage droop will be observed, i.e.

$$v_{\text{droop}} = \frac{1}{C_h} \int_{t_0}^{t_{\text{hold}}} i_b(V_{ce}) \, dt.$$  

(4.3)

It is desirable to keep the ratio $\frac{T_{\text{hold}}}{i_b C_h}$ larger than the voltage required to turn on $Q_8$; otherwise, $Q_8$ will begin to supply the base current to the emitter-follower buffer $Q_{18}$. As $\beta$ is a nonlinear function of $V_{ce}$ nonlinear distortion will occur [69]. An alternative architecture using two emitter-followers is proposed in [68], but unfortunately it requires the additional headroom of one $V_{be}$ which is not available in this design to keep the power supply below 5V; therefore, only a single emitter-follower is used in this architecture.

In addition to different base currents due to differences in $V_{ce}$, fabrication mismatch in the current gain $\beta$ and bias currents converts the common-mode droop
to differential, as the base currents between the differential emitter-follower buffers will be different due to $\beta$ mismatch, with a differential droop proportional to the current mismatch $\Delta i_b$. Unfortunately, in this 120nm SiGe technology, $\beta$ mismatch is larger than other process variation parameters, so care must be taken for careful matching as described in the following section to minimize the differential droop and nonlinearity.

*Figure 4.7*: Half circuit schematic of the switched emitter-follower during hold mode.

The third-order nonlinearity of the switched emitter-follower is expressed as [68]:

$$HD_{3,SEF} = \frac{v_T i_{C_h}^2}{12 I_{SEF} (0.5 A_{in} I_{SEF} + v_T i_{C_h})}, \quad (4.4)$$

where the bias current for the SEF is $I_{SEF}$, the input amplitude is $A_{in}$, and the charging current into the hold capacitor is $i_{C_h} = 2\pi f_{in} A_{in} C_h$ with an input frequency $f_{in}$. The delay due to $C_h$ causes a nonlinear modulation of the base-emitter voltage of the switch, giving rise to nonlinear distortion. Expressing 4.4 instead in terms of the bandwidth $BW = \frac{g_m}{2\pi C_h}$ of the SEF, 4.4 becomes [69]:

$$HD_{3,SEF} = 20 \log \left[ \frac{1}{12} \left( \frac{2 A_{in}}{v_T} \right)^2 \left( \frac{f_{in}}{BW} \right) \right] \quad (4.5)$$
Pedestal errors in the SEF are typically nonlinear, resulting both from input amplitude-dependent timing differences in the current switching transistors $Q_5$ and $Q_7$ in Fig. 4.6, and also from clock feed-through. Modulation of the switching time between the differential SEF switches $\Delta \tau_a$ during the aperture time $\tau_a$ causes nonlinear coupling of the clock to the hold capacitor creates an input-dependent charge on $C_h$ approximated by:

$$q_h = \int_{t_0}^{t_0+\tau_a} \frac{V_{in}(t) V_{be}(t)}{Z_{Qx}(t)} dt + I_{SEF \Delta \tau_a}(V_{in}) + A_{clk} C_{bc,Q_{14}}(V_{in}),$$  \hspace{1cm} \text{(4.6)}$$

where $A_{clk}$ is the clock amplitude, $Z_{Qx}(t)$ is the impedance of $Q_{14}$ which varies during switching, and $C_{bc,Q_{14}}$ is the base-collector capacitance of $Q_{14}$ [70]. All three terms in 4.6 have a nonlinear dependence on the input $V_{in}$ [70]. A faster clock edge will decrease the distortion in the first two terms, and a smaller clock amplitude will decrease the third term. In this design, the differential clock amplitude $A_{clk}$ is chosen to be $300\text{mV}$ as a tradeoff between speed, amplitude, and fully switching the current.

### 4.2.2 Hold-mode Feed-through

Early designs sought to minimize hold-mode feed-through via cross-coupled capacitances, as shown in Fig. 4.3. However, at input frequencies in the several hundred MHz and above, these cross-coupled capacitors are of limited use, especially when fabrication, bias point, nonlinearity, and time delay mismatch are considered between the cross-coupled capacitors $C_{ff}$ and the $C_{be}$ of the emitter follower switch. To first order, feed-through capacitors alone limit the voltage feed-through [71] as:

$$V_{fth} = \frac{C_{be,SEF}}{C_{be,SEF} + C_h} \left( \frac{C_{be,SEF} - C_{ff}}{C_{be,SEF}} \right).$$  \hspace{1cm} \text{(4.7)}$$

More modern designs at GS/s sample rates and above seek to use both cross-coupled capacitors as well as a feed-through attenuation buffer to further increase the hold-mode isolation [15]. Practically, however, the feed-through attenuation buffer has similar issues as the cross-coupled capacitors in terms of fabrication and phase mismatch.
A more robust approach to hold mode isolation is to hard-switch the signal path from the input buffer as described in [62,63] to provide very high hold-mode isolation (on the order of 100dB from simulation). This approach has another benefit, as it leads to less power consumption, noise, and pedestal error because the input feed-through attenuation buffer is not present; its noise and offset are not present during switching and will not degrade the sampled voltage. However, the current switch required to hard-switch the signal path requires more headroom and a higher supply voltage.

Cascading two THAs to create a master/slave or resampler sample-and-hold increases distortion as well. For two unity-gain THAs with the same $HD_3$, their cascade will have 6 dB higher distortion. Fortunately, the second THA is not handling a dynamic signal, and its distortion contribution is typically less than the master.

4.2.3 Bandwidth and Mismatch

THAs with bandwidths significantly larger than Nyquist can subsample, aliasing the desired frequencies into the Nyquist range, and avoiding the complexity of a downconversion before sampling. However, as will be described in the following section, a larger bandwidth increases the bounds of integration for the noise spectral density, resulting in a larger $rms$ sampled noise voltage. The bandwidths of the master/slave and resampler are designed to be 7 and 5 GHz respectively.

Settling in the second (slave) THA determines its required bandwidth. If the slave tracking bandwidth is insufficiently low, proper settling will not occur, resulting in reduced performance. As the slave in each architecture tracks the master THA for half of the period (250 ps), the track-mode bandwidth of the slave stage should be larger than 4 GHz so that it will settle accurately before switching from track to hold-mode. The bandwidths of the slave stages were designed to have identical bandwidths as the master THAs at 7 and 5 GHz as well for the master/slave and resampler architectures, respectively. This gives some additional margin for switching transients, large-signal behavior, etc. as a
trade-off for additional sampled noise.

The switched emitter-follower bandwidth and ringing determines the settling behavior, the linearity from section 4.2.1, and the sampled \( \textit{rms} \) noise voltage as will be described in section 4.2.4. The equivalent schematic to the SEF is shown in Fig. 4.8 [69]. In order to limit ringing, the input resistance \( R_L \) which is the load of the main amplifier and the base resistance \( r_b \) must satisfy the condition [69] for a \( Q \)-factor of 0.707 (no ringing):

\[
\frac{I_{SEF}}{C_h v_T} < 0.5 \frac{1}{(C_{be} - C_{ff})(R_L + r_b)}.
\]  

(4.8)

Good matching between \( C_{be} \) and \( C_{ff} \) can mitigate ringing (in addition to hold-mode feed-through); careful choice of the bias currents and hold capacitor in the SEF is also necessary.

![Figure 4.8: Small-signal half-circuit schematic for the switched-emitter follower.](image)

Voltage offsets, even-order distortion, and to some extent feed-through and pedestal errors are a function of the mismatch between differential npn devices. The \( V_{be}, I_c, \) and \( I_b \) mismatch have a variance that is a function of the emitter area \( A_e, \) i.e. \( \sigma^2 \propto \frac{1}{A_e}. \) As the device \( f_T \) is within 10\% of its maximum value for almost an order-of-magnitude current density range, it is advantageous in terms of offset to run devices in the differential signal paths at collector current densities \( J_c \) below peak \( f_T J_{c,\text{peak}}-f_T. \) Although typically bipolar devices have mismatch that is not a function of current density over normal current bias conditions [40], simulations indicate that \( V_{be} \) mismatch is exacerbated by biasing at higher current densities close to peak \( f_T \) for the 120nm SiGe process.
4.2.4 Noise

Due to the several-GHz of bandwidth of each track-and-hold and the 50-Ω output buffer, it is difficult to achieve low noise performance. A fully differential architecture is used instead of the split current-source architecture [72] both to keep the signal path fully symmetric and to avoid the noise contributions and mismatch from the current sources. The target SNR is approximately 56 dB for the SHA consisting of two THAs so that noise added by the 50-Ω output buffer and a subsequent ADC will yield approximately 8-bit ENOB performance.

For a low-noise wideband THA, the 50-Ω source and input terminations must be considered in the sampled voltage noise. As the THA bandwidth is approximately 5 GHz, the estimated rms sampled voltage noise from the effectively 25-Ω resistance seen on each differential input should be approximately $6.3 \times 10^{-9} V^2$. For example, with a $1V_{pp}$ swing the maximum achievable SNR of each THA is 73 dB, which doesn’t include the noise of the output buffer, which would degrade the ideal SNR to 70 dB.

The noise from the main unity-gain amplifier and the pedestal compensation amplifiers are integrated across their bandwidth when sampling. The noise spectral density for a highly degenerated unity-gain ($R_L \approx R_E$) amplifier can be expressed as [6]:

$$\frac{\overline{v_n^2}}{2f} \approx \frac{1}{I_{DC}} \left(16kTf v_T + 4qv_T^2\right). \quad (4.9)$$

By necessity, the bandwidth must be at least 4 GHz as shown in section 4.2.3. Therefore, another means must be used to achieve the specified noise contribution, i.e., the bias current and devices must be scaled accordingly to provide a low enough noise spectral density. A bias current $I_{DC}$ of approximately 60mA is used for the main and pedestal compensation amplifier to reduce the noise spectral density. In this case, with strong degeneration, the noise sampled voltage noise should be approximately $6.7 \times 10^{-9} V^2$ for $R_L$ and $6.3 \times 10^{-9}$ for $25\Omega R_E$.

Another significant noise contributor is the base resistance of SEF transistor $Q_5/Q_7$. The bandwidth of the SEF is much larger than input bandwidth to minimize distortion from (4.5); however, this allows broadband noise from the base resistance and base shot noise to be sampled relatively unfiltered across 10s of GHz.
of bandwidth. To reduce the base resistance, a larger device is used for SEF transistor $Q_5/Q_7$. To reduce base shot noise, the SEF device is biased in the region where $\beta$ is maximized. However, increasing the size of the $Q_5/Q_7$ to reduce its base resistance reduces the track-mode bandwidth, increases the hold-mode feed-through in (4.7), and complicates the settling behavior in (4.8) as $C_{be}$ increases with the size of $Q_5/Q_7$. This double-switching relaxes the size-feed-through tradeoff, allowing more flexibility in sizing of the $Q_5/Q_7$ due to hard-switching feed-through reduction.

The simulated noise contributions from the top six noise contributors are summarized in Table 4.1. Noise simulations are performed via SpectreRF using pss and pnoise to analyze the noise sources after layout extraction. As the output of the 2GS/s THA is observed continuously in the noise analysis, the noise spectral density contains noise both from the hold and from the track mode. The voltage noise ($V^2$) is obtained by integrating the noise spectral density of the 50-Ω emitter-follower input buffer and single track-and-hold (with a bandwidth of 5 GHz) in Fig. 4.9 with an integration bound of 1 MHz to twice the bandwidth of the THA, i.e. 10 GHz, as the slave THA which also has a 5 GHz bandwidth samples the master. The worst noise contributor is the intrinsic and extrinsic base resistance of the switching core that alternates between the main amplifier in track mode and the pedestal compensation amplifier in hold mode. These devices can be made larger to reduce $rbx$ and $rbi$; however, this would significantly increase the loading on the timing circuits driving the switching core and would make the layout and routing almost double, as the number of devices would have to be doubled (18$\mu$m is the maximum emitter length). The load resistance $R_L$ is the second noise contributor, with the input 50-Ω interface and emitter degeneration resistor $R_E$ third and fourth, respectively. Interesting to note, as large devices are used for the SEF transistor, its intrinsic and extrinsic base resistance is significantly reduced and it does not contribute as significantly to the overall noise in spite of the wide bandwidth of the switched emitter-follower. A time-domain transient simulation from [2] determined that with a 1$V_{pp}$ input, the master/slave sample-and-hold ENOB is higher than 56dB.
Figure 4.9: Simulated output noise spectral density during both hold and track modes for the layout extraction of a single THA operating at 2GS/s with 5 GHz of bandwidth.
Table 4.1: Simulated output noise contributions in the THA.

<table>
<thead>
<tr>
<th>Device</th>
<th>Parameter</th>
<th>Noise (V^2)</th>
<th>% of Total</th>
</tr>
</thead>
<tbody>
<tr>
<td>Switching Core Q_{3-6}</td>
<td>r_{bx} + r_{bi}</td>
<td>1.2 \times 10^{-8}</td>
<td>21.5</td>
</tr>
<tr>
<td>R_L</td>
<td>r_n</td>
<td>6.2 \times 10^{-9}</td>
<td>11.0</td>
</tr>
<tr>
<td>50-Ω Input</td>
<td>r_n</td>
<td>5.4 \times 10^{-9}</td>
<td>9.5</td>
</tr>
<tr>
<td>R_E</td>
<td>r_n</td>
<td>5.0 \times 10^{-9}</td>
<td>8.8</td>
</tr>
<tr>
<td>Switching Core Q_{3-6}</td>
<td>i_{tZF}</td>
<td>3.5 \times 10^{-9}</td>
<td>6.1</td>
</tr>
<tr>
<td>SEF Transistor Q_{5,7}</td>
<td>r_{bx}</td>
<td>3.3 \times 10^{-9}</td>
<td>5.8</td>
</tr>
</tbody>
</table>

4.3 2GS/s 120nm SiGe BiCMOS Measurement Results

To characterize the performance of the double-switching THA with different sample-and-hold topologies, two test structures are designed. Each topology has different timing circuits, but the overall sample-and-hold topology is given in Fig. 4.10. The first architecture in Fig. 4.10 is a master/slave sample-and-hold; both master and slave THA operate at the full sample rate at 2GS/s. The master track-and-hold samples the RF input signal; its jitter and dynamic linearity have the largest contributions to jitter noise and nonlinear distortion. The following slave THA in Fig. 4.10 is clocked approximately 180 degrees out-of-phase from the master; it tracks while the master is holding, and holds while the master is tracking. The output of the slave approximates the ideal staircase waveform of a sample-and-hold, low-pass filtered by the finite bandwidth of the slave THA. The second sample-and-hold architecture shown in Fig. 4.11 consists of two THAs in a resampling configuration. The master in the resampler architecture is clocked at 2GS/s; however, the slave is clocked at 1GS/s with 25% duty cycle as shown in the timing diagram of Fig. 4.11.
**Figure 4.10:** Sample-and-hold architecture test setup. The master/slave and resampler architectures are determined by the clock generation circuits (not shown).

**Figure 4.11:** Clock waveforms for the sample-and-hold architectures: (a) represents the waveforms CLK1 for the master and CLK2 for the slave which are 180 degrees out-of-phase. The resampler waveforms (b) have the slave clocked at one half the rate with a duty cycle of 25 %, therefore reducing the sample rate by half.
4.3.1 Cascaded Master/Slave SHA

The microphotograph for the 2GS/s master/slave SHA fabricated in 120nm SiGe BiCMOS is shown in Fig. 4.12. The chip area is 1320 x 950 $\mu m^2$ including the pads. The entire test structure consumes approximately 420mA from a 5V supply and 30mA from a 2.5V supply.

![Microphotograph of the 2 GS/s master/slave sample-and-hold circuit](image)

**Figure 4.12:** Microphotograph of the 2 GS/s master/slave sample-and-hold circuit. The master/slave sample-and-hold consumes approximately 500mA from a 5V supply and 30mA from a 2.5V supply.

Time domain measurements are conducted on the master/slave SHA to observe the output waveform when subsampling. Fig. 4.13 displays the time-domain measured data on an Agilent DSO80604b real-time 20GS/s oscilloscope for the master/slave SHA with a sample rate of 2GS/s and an input of 2100 MHz, aliased to 100 MHz. Each output, $V_{out-}$ and $V_{out+}$, is measured on a channel of the scope, and then the differential waveform is measured by subtracting the two channels. As the slave THA switched from track to hold, a common-mode drop can be observed in each waveform. No feed-through of the 2100 MHz input
is observable in the output waveform, and the waveform period is seen to be 100 MHz, verifying the subsampling operation.

**Figure 4.13:** Time-domain measurement of the master/slave SHA with an input frequency of 2100 MHz subsampled and aliased to 100 MHz measured on the Agilent DSO80604b 20GS/s real-time oscilloscope.

Frequency domain measurements are conducted to analyze both the harmonic distortion with subsampling as well as the intermodulation distortion with two-tone inputs. The intermodulation distortion of the master/slave architecture is compared with the resampler in section 4.3.3.

To analyze the subsampled harmonic distortion of the master/slave SHA, a 1V_{pp} 2030 MHz input is applied and aliased down to 30 MHz. Throughout all measurements, calibrations account for cable and coupler loss such that 1V_{pp} is applied to the input of the SHAs at all frequencies. Hybrid couplers are used on the input and output to convert from single-ended to differential from the signal generator and differential to single-ended for the spectrum analyzer, respectively. Single-ended measurements of the output showed significantly higher even and odd-order
distortion; therefore, a 30MHz - 3 GHz hybrid coupler is used to approximate an ideal balun. However, asymmetries and mismatch between the differential signal paths led to significantly higher second-order distortion than expected from Monte Carlo simulations. This is likely due to the amplitude and phase mismatch of the couplers. Fig. 4.14 demonstrates the sub-sampling performance of the master/slave SHA; the third harmonic distortion $HD_3$ is approximately -55 dB, or approximately 9 bits.

**Figure 4.14:** Frequency-domain subsampling measurement of the master/slave THA with an input frequency of 2030 MHz aliased to 30 MHz. The third harmonic is at a power of -55dBc related to the fundamental, which is at $1V_{pp}$ at the input to the SHA.

Two-tone subsampled intermodulation distortion measurements were also conducted to measure the narrow-band linearity. As in the harmonic distortion measurements, the input envelope is $1V_{pp}$; therefore an input power of -2dBm is used for each of the two tones which are 1 MHz apart centered at 2100 MHz. The measured distortion of the alias of both tones and their intermodulation products
to a center frequency of 100 MHz is -52.8 dBc.

Figure 4.15: Frequency-domain subsampling two-tone intermodulation distortion measurement of the master/slave SHA with input frequencies of 2099.5 and 2100.5 MHz aliased to 99.5 and 100.5 MHz. The 3rd order intermodulation distortion term for the subsampled waveform is -52.8 dBc.

4.3.2 Resampled Master/Slave SHA

The second sample-and-hold test structure is a resampled master/slave SHA shown in Fig. 4.16. The 2 GS/s rate applies to the first THA, and the second THA is clocked at 1 GS/s through the on-chip timing circuits. The resampled sample-and-hold consumes approximately 420mA from a 5V supply and 100mA from a 2.5V supply. AC coupling in the timing circuits allows only dynamic measurements of the resampler sample-and-hold architecture.

As in the case of the master/slave SHA, time domain subsampling measurements are performed to observe the output waveforms. A 2100 MHz input is
Figure 4.16: Microphotograph of the 2 GS/s resampled sample-and-hold circuit. The resampled sample-and-hold consumes approximately 420mA from a 5V supply and 100mA from a 2.5V supply.
subsampled at 2GS/s by the first TAH to 100 MHz which is then resampled by the slave as shown in Fig. 4.17. Again, a common-mode variation is observed in each differential output $V_{out^+}$ and $V_{out^-}$ during the switch from track-to-hold; there is significantly less variation when both channels are subtracted to show the differential waveform. Due to the resampling operation of this architecture, the output sample rate is at 1 GS/s (i.e. the held value appears to be 1 ns in duration) due to the half-rate clock used for the slave THA with 25% duty cycle. No feed-through of the 2100 MHz input is observable in the differential THA output which is at 100 MHz.

Figure 4.17: Time-domain measurement of the resampled SHA with an input frequency of 2100 MHz aliased to 100 MHz measured on the Agilent DSO80604b 20GS/s real-time oscilloscope.

The subsampling measurement for the resampler SHA is shown in Fig. 4.18 for an input frequency of 2030 MHz with $1V_{pp}$ amplitude is aliased to 30 MHz. Again, second harmonic distortion is present due to mismatch and asymmetries in the differential signal paths, likely due to the amplitude and phase mismatch of
the input and output hybrid couplers. Fig. 4.18 demonstrates the sub-sampling performance of the resampled SHA with the master clocked at 2 GS/s (1 GS/s for the slave); the third harmonic distortion $HD_3$ is approximately -54.5 dB, or approximately 9 bits.

**Figure 4.18**: Frequency-domain subsampling measurement of the resampled SHA with an input frequency of 2030 MHz aliased to 30 MHz. The third harmonic is at a power of -51 dBc related to the fundamental, which is at 1 Vpp at the input to the SHA.

Two-tone subsampled intermodulation distortion measurements were also conducted as in the previous architecture to investigate intermodulation distortion. As in the harmonic distortion measurements, the input envelope is 1 V$_{pp}$ for both of the two tones centered at 2100 MHz. The measured distortion of the alias of both tones and their intermodulation products to a center frequency of 100 MHz is -51.65 dBc.
Figure 4.19: Frequency-domain subsampling two-tone intermodulation distortion measurement of the resampled SHA with input frequencies of 2099.5 and 2100.5 MHz aliased to 99.5 and 100.5 MHz. The 3rd order intermodulation distortion term for the subsampled waveform is -51.65 dBc.
4.3.3 Linearity Comparison

To compare the linearity of the master/slave and resampler architectures, intermodulation distortion (IMD) - rather than HD - measurements are chosen. In intermodulation measurements, the fundamental and $IM_3$ terms are co-located in frequency whereas in harmonic distortion measurements the fundamentals and harmonics are spread over a wide range of frequencies due to the different sampling rates of the slave THA in the master/slave (2GS/s) and resampler (1GS/s) architectures. Therefore, with the sample-and-hold sinc frequency dependence and frequency-dependent variations in the measurement setup and differing output sample rates, intermodulation distortion is used for the linearity comparison.

The $P_{IIP3}$ for each architecture is measured with a $1V_{pp}$ input envelope (i.e. when both input frequencies add constructively); the input power for each tone is -2dBm, corresponding to $500mV_{pp}$. Maximum input swing ($1V_{pp}$) is used for these measurements to fully characterize the large-signal linearity, which could be overestimated if smaller input powers were used to extrapolate $P_{IIP3}$. Both architectures demonstrate a linearity degradation around the half sampling rate, although in the resampled architecture (at 500 MHz) this is much less noticeable than in the master/slave architecture (at 1 GHz) in Fig. 4.20. The linearity degradation happens for two reasons with $\sim f_s/2$ inputs, due to the maximum to minimum signal transitions. First, the SEF tends to slew rate limit during the first part of tracking during maximum voltage excursions ($1V_{pp}$). The nonlinearity contribution from slew-rate limiting is dependent on the signal period: due to the lower sample rates in the resampler SHA, the linearity degradation will be less as a percentage of the overall period. Also, due to the higher sample rate, the peak-to-peak voltage excursions will occur at a faster rate in the master/slave SHA, which is more demanding on the high-frequency linearity of the output buffer. As a result, the resampler has better performance around $f_{in} \approx f_s/2$. 
Figure 4.20: Measured $P_{\text{IIP3}}$ versus frequency for the master/slave SHA and resampled SHA configurations. The input envelope is $1V_{pp}$ and the input power for each tone is $-2\,\text{dBm} \ (0.5V_{pp})$. 
4.4 40GS/s TAH and Interleaved Sampling

Circuits in 250nm InP CoSMOS

CMOS foundries are beginning to have difficulties with traditional constant
electric-field scaling according to Moore’s Law due to a number of issues including
fabrication technologies, device structures, materials, and transport physics [?,73].
Additionally, although the device speed is increasing, the analog performance of
these fine-line CMOS technologies is quite poor, due mainly to short-channel ef-
facts. There are several technology alternatives for continued scaling and increased
performance for high-speed analog and mixed-signal circuits. One possibility is to
use hybrid architectures with bipolar and FET devices, such as in the 120nm SiGe
process used for the design of the THAs in section 4.2. Another possibility is using
a III-V technology hetero-integrated with traditional CMOS. For similar device
geometries, III-V technologies typically achieve much higher device $f_T$ and $f_{max}$
behavior than SiGe bipolar devices due to significantly larger electron mobilities.
In addition, processes with both bipolar and FET devices (i.e. SiGe BiCMOS)
must make tradeoffs to accommodate both bipolar and FET devices; each device
cannot be optimized independently. InP CoSMOS [74] offers the co-integration
of 90nm RF CMOS and 250nm InP DHBTs, which have significantly higher $f_T$
and $f_{max}$ above 350 GHz and higher breakdown voltages compared to their 90nm
CMOS counterparts. Because each process is fabricated separately before wafer-
scale hetero-integration, the InP DHBTs and CMOS devices can be optimized
independently. Designers may take advantage of the strengths of each technology
as well, using InP DHBTs for high-speed analog and mixed-signal, and 90nm RF
CMOS for lower-speed mixed-signal and low-power digital.

Subsection 4.4.1 describes the design of a 40 GS/s track-and-hold amplifier
using only InP DHBTs. Taking advantage of the heterogeneous integration, section
4.4.2 describes the design and simulation of a time-interleaved hybrid InP-CMOS
sample-and-hold circuit.

4.4.1 40 GS/s InP DHBT Track-and-Hold Amplifier

The design of the InP DHBT THA uses the same architecture as the SiGe BiCMOS version in section 4.2 except for one main difference. As the SiGe architecture operated at 2GS/s with an input bandwidth <7 GHz, MOS current sources were used without significant penalty in Monte Carlo simulations. However, in this 40 GS/s THA, nFET current sources add too much parasitic capacitance at the tail of the differential amplifier. In the presence of mismatch, a significant second-order distortion $HD_2$ is observed due to the additional capacitance at the differential node. Cascoding the nFET current sources is partially effective for reducing the second-order distortion. However, during mismatch simulations, second-order distortion is observed to still be much stronger than odd-order distortion, especially as the input frequency is increased. To avoid this parasitic capacitance at the tail of the differential pair, an InP DHBT current source is used with weak degeneration to prevent thermal runaway. Use of the InP current source reduced the second order distortion in Monte Carlo simulations to levels lower than third-order distortion in the low GHz input range as seen in Fig. 4.21.

The input buffer and pedestal compensation buffer is shown in Fig. 4.22. Although 500nm precise analog devices were available, 250nm devices are used here for their superior speed. The input devices with a device width of 250nm, a length of 4µm, and a multiplicity of two are biased at approximately one-half of peak $f_T$ as a tradeoff between mismatch, bandwidth, and thermal heating. Thermal heating is an important consideration in this technology as AC thermal vias are used to conduct heat into the silicon substrate [74]. The switch devices located above the input pair have a length of 3µm and are biased at 1.3x peak $f_T$ when fully switched for fast switching. Their thermal loading is mitigated by the fact that they conduct current only during half of the sampling period.

A 50-Ω output buffer is used to buffer the output of the THA off-chip. To reduce the severity of the gain, DC power dissipation, bandwidth, and linearity tradeoffs, a loss of approximately 3dB is allowed for this buffer. It is designed such that its linearity shouldn’t heavily influence the linearity of the measured THA.
Figure 4.21: Simulation results for the InP DHBT track-and-hold. The $HD_2$, $HD_3$, and $THD$ are the result of the worst case linearity for 10 Monte Carlo runs.

Figure 4.22: InP DHBT unity-gain buffer.
waveforms.

**Figure 4.23**: InP DHBT 50-Ω output buffer.

The layout of the InP DHBT TAH is shown in Fig. 4.24. The clock is provided differentially through the pads at the bottom of the layout, and the clock signals are buffered from bottom to top across high impedance microstrip transmission lines with a characteristic impedance $Z_0$ of approximately 100Ω.
**Figure 4.24**: Layout for the InP DHBT track-and-hold and 50-Ω output buffer.
Table 4.2: Comparison table for high-speed bipolar track-and-hold amplifiers.

<table>
<thead>
<tr>
<th>Ref.</th>
<th>$f_s$ (GS/s)</th>
<th>$f_m$ (GHz)</th>
<th>THD (dB)</th>
<th>Input ($V_{pp}$)</th>
<th>$P_{DC}$ (mW)</th>
<th>Process / $f_T$ (GHz)</th>
</tr>
</thead>
<tbody>
<tr>
<td>This work</td>
<td>40</td>
<td>1</td>
<td>-68</td>
<td>0.6</td>
<td>500</td>
<td>InP / 350</td>
</tr>
<tr>
<td>[75]</td>
<td>12</td>
<td>1</td>
<td>-38</td>
<td>1.0</td>
<td>390</td>
<td>InP / 120</td>
</tr>
<tr>
<td>[76]</td>
<td>18</td>
<td>2</td>
<td>-32</td>
<td>1.0</td>
<td>128</td>
<td>SiGe / 120</td>
</tr>
<tr>
<td>[16]</td>
<td>40</td>
<td>10</td>
<td>-32</td>
<td>1.0</td>
<td>560</td>
<td>SiGe / 200</td>
</tr>
<tr>
<td>[71]</td>
<td>40</td>
<td>1</td>
<td>-33</td>
<td>0.4</td>
<td>540</td>
<td>SiGe / 160</td>
</tr>
<tr>
<td>[77]</td>
<td>20</td>
<td>1</td>
<td>-41</td>
<td>0.5</td>
<td>N.A.</td>
<td>InP / 210</td>
</tr>
<tr>
<td>[61]</td>
<td>20</td>
<td>0.9</td>
<td>-45</td>
<td>0.5</td>
<td>735</td>
<td>InP / 175</td>
</tr>
</tbody>
</table>
4.4.2 Time-interleaved InP and CMOS Hybrid Architecture for 40GS/s Sample-and-hold Circuits

Having a single front-end track-and-hold amplifier reduces the timing, gain, bandwidth, and offset specifications for interleaved sampling. Lower sample-rate THAs can follow the first THA as shown in Fig. 4.25. In this architecture, the front-end InP THA samples at 40 GS/s, and the following 8 time-interleaved MOS SHAs sample at 5 GS/s, or 1/8 the rate of the InP THA. A MOS SHA is used instead of a CMOS THA here to prevent any feed-through from the InP THA to the output so that a sample rate reduction with the associated aliasing can be clearly observed in measurement results. Two clock inputs are provided for the ability to align the phase of the front-end full-rate InP THA and the time-interleaved CMOS SHAs. On-chip current-mode logic is used for dividing a 20 GHz clock input down to a frequency of 5 GHz; subsequently, a CML-to-CMOS converter converts the clock to full swing (0V to a $V_{dd}$ of 1.2~1.5V) suitable for driving the MOS sampling switches.

Complementary MOS switches are used for the first and second MOS THA. AC coupling is used prior to the first MOS THA, relaxing biasing of the nFET switch to increase its $V_{GS}$, lower its on-resistance, and increase its bandwidth. A feedback source-follower similar to [78] but using only active devices is used here to minimize power dissipation while increasing bandwidth and linearity. As the voltage is stepped up by the source-follower preceding the second THA, a pFET switch is used in the second THA to increase its $V_{GS}$ with the CMOS clock. A 50-Ω source-follower buffer then follows for measurements.

The simulation results for a single channel $HD_3$ are provided in Fig. 4.26. Better than 9-bit linearity is demonstrated with a 600$mV_{pp}$ differential input across most of the input frequencies.

The layout for the InP THA and time-interleaved CMOS SHAs is shown in Fig. 4.27. The MOS sampling circuits are arranged in a line with H-tree delay balancing between cells to minimize the phase mismatch and clock delay. Two clocks, a 40 GHz differential clock supplied to the InP THA and a 20 GHz differential clock supplied to the CML dividers are provided via the pads on the
Figure 4.25: Architecture for the InP DHBT front-end track-and-hold followed by 8 CMOS sample-and-hold circuits.
Figure 4.26: Simulation results for the 40 GS/s InP DHBT track-and-hold and a single channel of the time-interleaved MOS sample-and-hold operating at 5 GS/s. 

4.5 Conclusions

Two test structures are designed and measured to analyze a double-switched track-and-hold amplifier topology fabricated for the first time in SiGe BiCMOS. Measurements indicate linearity from the 3rd harmonic and intermodulation products close to 9b for the sample-and-hold test structures.

Design and simulation results are shown for a single track-and-hold amplifier in 250nm InP CoSMOS. Simulations indicate excellent high-frequency linearity compared to state-of-the-art THAs. Also shown is an interleaved sample-and-hold leveraging the heterogeneous integration of 250nm InP with 90nm RF CMOS, demonstrating linearity better than 9 bits.
Figure 4.27: Layout for the 40GS/s InP HBT track-and-hold followed by 8 time-interleaved MOS sample-and-holds sampling at 5GS/s.
Acknowledgments

Chapter 4 is mostly a reprint of the material submitted to IEEE Journal of Solid State Circuits, 2012, Timothy D. Gathman; James F. Buckwalter, and Andreas O. J. Wiberg. The dissertation author was the primary author of this material.
Chapter 5

Distributed Techniques for Wideband Mm-Wave Communication

Millimeter waves are being explored for wideband communication systems with data rates >Gbit/s. Unlicensed bands exist around 24 and 60 GHz that can be used for consumer electronics and communication devices. W-band (75-110GHz) is attractive for applications in RADAR and imaging. In this chapter, distributed techniques will be described for millimeter-wave amplifiers and oscillators. Distributed techniques are attractive due to their large gain bandwidth product and absorption of transistor parasitics into the input and output transmission line structures.

5.1 High Pass Distributed Amplifier

Traditional low-pass DAs are designed to optimize their gain-bandwidth product; however, other transmission line filter types can provide desirable frequency characteristics. Band-pass artificial transmission lines (ATLs) have been investigated to increase the maximum operating frequency; their center frequency can be higher than the cutoff frequency of the low-pass DA [79]. As an alternative to band-pass ATLs, metamaterial CRLH filter structures can provide a directional
frequency response where the amplified signal is directed to one of the output ports depending on the input frequency [80]. High-pass ATLs have been used for the output transmission line in distributed frequency doublers to allow only the second harmonic to pass [81].

In practice, high-pass structures are inherently band-pass due to intrinsic active device and passive parasitics; however, they do not require the extra passives of a band-pass amplifier. High-pass ATLs have two benefits in frequency response compared to a low-pass ATL. First, a high-pass structure has the ability to significantly reject signals below the cutoff frequency. Second, the maximum frequency of operation is higher than a comparable low-pass structure [82]. This work studies the circuit design of a high-pass distributed amplifier, fabricated in a SiGe BiCMOS process for $K_a$-band operation.

A conventional distributed amplifier design is illustrated in Fig. 5.1a and consists of periodic low-pass constant-$k$ or $m$-derived T-filter structures. The device parasitic capacitance is absorbed into the shunt capacitance of the synthetic transmission line and placed between series inductors [83]. Series inductors can be realized with lumped elements or from an appropriate transmission line length. A simple T-model for a low-pass ATL is shown in Fig. 5.2. Assuming lossless transmission lines, the distributed amplifier voltage gain is:

$$G_v = N \frac{g_m Z_o}{2}, \quad (5.1)$$

where $Z_o = \sqrt{\frac{L}{C}}$, $N$ is the number of stages, and $g_m$ is the transconductance of each transistor. The DA bandwidth is limited by the cutoff frequency of the transmission lines, i.e.

$$f_c = \frac{2}{2\pi \sqrt{LC}}, \quad (5.2)$$

which is independent of the number of stages $N$ [84]. The gain-bandwidth (GBW) for the low-pass distributed amplifier can be approximated to first-order from (5.1) and (5.2) as

$$GBW \approx N f_T, \quad (5.3)$$
Figure 5.1: Distributed amplifiers operating with (a) conventional low-pass synthetic transmission line topology and (b) the proposed high-pass synthetic transmission line.
where $f_T = \frac{g_m}{2\pi C}$ is the transit frequency of the active device.

The inverse of the low-pass line is constructed if the inductors and capacitors are exchanged (i.e. series capacitors and shunt inductors). This results in a high-pass distributed amplifier (HPDA) as illustrated in the schematic of Fig. 5.1b. The high-pass ATL, shown in Fig. 5.2b, has been proposed to offer several advantages over the low-pass ATL such as DC isolation between stages, and lower loss per section [82]. The characteristic impedance of the ideal high-pass ATL at high frequencies is the same as the low-pass ATL, i.e. $Z_o = \sqrt{\frac{L}{C}}$, and, consequently, the ideal gain for a lossless HPDA is given by (5.1). The high-pass ATL cutoff frequency is

$$f_c = \frac{1}{4\pi\sqrt{LC}},$$

(5.4)

Whereas the low-pass ATL absorbs the active devices parasitic capacitance, the device capacitance cannot be absorbed by the high-pass ATL. Also, both the shunt inductor and the series capacitor contribute additional parasitic capacitance. The combination of device and passive parasitic capacitance, $C_{par}$, degrades the operation of the HPDA at high frequencies, giving it a band-pass characteristic. $C_{par}$ also decreases the ideal cutoff frequency, and, based on the image parameter method [85], (5.2) becomes

$$f_{c,par} = \frac{1}{4\pi\sqrt{LC + \frac{LC_{par}}{4}}},$$

(5.5)

Careful design must be used to minimize this parasitic capacitance in HPDAs. Fig. 5.3 shows the simulated $S_{21}$ for the high-pass ATL in Fig. 5.2b for several different ratios of $C_{par}/C$. As (5.6) predicts, the cutoff frequency is lowered as the ratio of $C_{par}/C$ increases. More importantly, $S_{21}$ rolls off at higher frequencies decreasing the bandwidth of the amplifier. As long as $C_{par}$ is less than $C$, $S_{21}$ rolls off gradually.

### 5.1.1 Circuit Design

The HPDA design consists of four cascode amplifier stages illustrated in Fig. 5.4. The cascode stage mitigates the Miller capacitance, increases the input impedance of the common-emitter transistor, increases the output impedance of
**Figure 5.2**: Simple loss-less model of a lumped-element artificial transmission line with (a) low-pass characteristics and (b) high-pass characteristics.

the stage, and provides better isolation between input and output transmission lines.

An emitter length of 3\(\mu\)m provides a tradeoff between gain and bandwidth. Larger devices offer additional transconductance at the cost of additional shunt parasitic capacitance, which degrades the frequency response as illustrated in Fig. 5.3. A current of approximately 4mA is required for this device geometry to achieve peak \(f_T\).

**Figure 5.3**: \(S_{21}\) of the high-pass artificial transmission line varying the ratio \(\frac{C_{par}}{C}\).

An emitter degeneration resistor of \(R_e=15\Omega\) is added to increase the device input impedance and decrease the effect of the parasitic shunt capacitor. The
Figure 5.4: Circuit schematic for a single stage of the high-pass distributed amplifier

effective parasitic capacitance seen at the base is reduced by $R_e$ to

$$C_{be,par} = \frac{C_{be}}{1 + g_m R_e}. \tag{5.6}$$

The amount of degeneration is a tradeoff between gain, bandwidth, and input return loss. The simulation results for $S_{11}$ and $S_{21}$ are plotted in Fig. 5.5 with and without $R_e=15\Omega$. A maximum of 12dB of gain is possible without $R_e$; however, the 3dB bandwidth is limited to 41.6GHz and the input return loss $S_{11}<-10$ dB from 20.2 to 32.9GHz. The introduction of $R_e$ reduces the maximum gain to 8.5dB but the frequency response is flat. Additionally, $S_{11}<-10$dB for almost double the bandwidth, extending to 42.1 GHz. For this $Ka$-band design, a cutoff frequency of 17.3GHz is chosen. The circuit distributes gain over four cells as shown in Fig. 5.4; comparing with Fig. 5.2b, $2C = 184fF$, $L = 230pF$, and the characteristic impedance of the line is 50-$\Omega$. To shield the input and output lines ATLs from each other, a ground trench is placed through all metal layers except M1.

CPWs are chosen for the high-pass ATL inductors because of their relatively high $Q$ throughout $Ka$-band, reliable models, and their resistance to crosstalk
and interference. The CPW side shields provide interstage isolation, allowing the placement of neighboring stages in close proximity to minimize chip area. The minimum conductor width of 4µm is used to minimize inductor area and parasitic capacitance, the shield separation is 20µm, and the length is 324µm on the top aluminum interconnect layer. The orientation of the ATL MIM capacitor was found to have a significant effect on the gain and matching characteristics of the amplifier. In particular, the bottom plate of the MIM has the most parasitic capacitance. Although only one capacitor is required to create the interstage capacitance C shown in Fig. 5.1b, each stage was designed with its own MIM capacitor to avoid adding the bottom plate capacitance to $C_{be,par}$ of the HBT. Thus, the bottom plates of the MIMs are oriented away from the amplifier stage and are connected in series as shown in Fig. 5.4. Each stage is biased through the shunt inductor and AC coupling to ground at the end of each inductor is provided through 4.6pF nwell fringe bypass capacitors. The base bias voltage, $V_{bb}$, and cascode bias voltage, $V_{casc}$, are generated on-chip.
Figure 5.6: CPW structure (a) and cascaded loss $S_{21}$ for multiple stages of the high pass artificial transmission line with shunt inductor CPWs and series MIM capacitors (b).

5.1.2 Measurement Results

The prototype high pass distributed amplifier was fabricated in a 0.12µm SiGe BiCMOS process. The chip microphotograph is shown in Fig. 5.7 and the chip area is 0.6 x 1.0$mm^2$ including the pads with an active area of approximately 0.28$mm^2$. Each of the four cells is 80µm wide and 786µm in length and draws nominally 4.1mA from a 1.7V supply. The total power consumption is 28mW. For all measurements $V_{cc}$ is approximately 1.7V, $V_{casc} \approx 1.9V$, and $V_{bb} \approx 1.0V$.

The transmission S-parameters are characterized using an Agilent N5250A Network Analyzer and are shown in Fig. 5.8. The peak gain is 8.3 dB and the 3dB BW is from 21 to 42.5 GHz. The benefit of the high-pass ATL structure illustrates high out of band rejection (>30dB) less than 5 GHz below the lower edge of the 3dB bandwidth. The gain roll-off at high frequencies is caused by interconnect parasitics in the layout which increase the parasitic capacitance, $C_{par}$, verifying the prediction in Fig. 5.5. The reverse isolation, $S_{12}$, is better than 30 dB across all frequencies; unmodeled substrate coupling between the input and output ATLs which are in close proximity account for the 15dB difference between the simulated and measured results.

The input and output return losses are shown in Fig. 5.9 and are under
Figure 5.7: Microphotograph of the high pass distributed amplifier implemented in a 0.12μm SiGe BiCMOS process.

Figure 5.8: HPDA S-parameters: transmission $S_{21}$ and reverse isolation $S_{12}$ measured (solid) and simulated (dashed).
-10dB for most of the 3dB bandwidth. $S_{11}$ is below -10dB from approximately 20.1 to 37.5 GHz, and the output return loss $S_{22}$ is below -10dB from 21.2 to 43.8 GHz. Over the 3dB bandwidth $S_{11}$ is below -6.3 dB and $S_{22}$ is below -9.2 dB. $S_{11}$ tends to be worse than $S_{22}$, particularly at higher frequencies, because of the additional base-emitter capacitance.

Figure 5.9: Input and output return loss: measured (solid) and simulated (dashed).

Group delay is also measured and compared with simulation in Fig. 5.10. The group delay response increases near the cutoff frequency of the high-pass ATL. The group delay variation for the HPDA is approximately 56.6ps from 25 to 40 GHz.

The noise figure of the HPDA, plotted in Fig. 5.11, is measured using a 50GHz noise source and an Agilent E4480A Spectrum Analyzer. Cable and probe losses in the setup are measured at all frequencies with the Agilent N191A Power Meter and the Agilent E8257D Signal Generator. The minimum noise figure is 6.9dB in the middle of the band, which increases as the gain and input matching degrade toward the edges of the 3dB BW.

Finally, the output compression point of the HPDA is plotted in Fig. 5.11. P1dB is measured with the Agilent N191A Power Meter and the Agilent E8257D
Figure 5.10: Group delay: measured (solid) and simulated (dotted).

Signal Generator. From 25-40 GHz, P1dB is greater than 0dBm.

Compared to a conventional DA in a similar SiGe process with $f_T \approx 200GHz$ [86], the HPDA does not provide the same broadband response but offers similar gain. The HPDA, however, is notable for the low frequency rejection which reduces its susceptibility to low frequency interference.

5.2 A 92-GHz Deterministic Quadrature Oscillator and $N$-Push Modulator in 120-nm SiGe BiCMOS

$\nu$-band offers new millimeter-wave applications for automotive and weather RADAR at 77 and 94 GHz [87]. $\nu$-band oscillators are now realizable using SiGe [87] and fineline CMOS [88] to provide signal sources in millimeter-wave bands except in high power FMCW RADAR applications where III-V Gunn diodes are utilized [89],

Heterodyne image rejection receivers require a local oscillator (LO) with an in-phase ($I$) and quadrature ($Q$) LO component. This is traditionally ac-
Figure 5.11: Measured noise figure (solid) and output 1-dB compression point P1dB (dashed).

An oscillator can be constructed using a polyphase filter or hybrid but can alternately be realized as a quadrature oscillator. Traditional LC quadrature oscillators (QOSC) have a trade-off between phase noise and quadrature accuracy and typically have worse phase noise than a standalone LC oscillator [90]. In addition, traditional QOSC circuits exhibit an ambiguous oscillating condition in which the I/Q relationship is ambiguous and corrective architectures limit the operation and tuning range. A recent QOSC creates a deterministic quadrature phase relationship by adding capacitive loading [91]. Rotary-wave oscillators [92] offer an alternative to LC oscillators and have been recently fabricated at millimeter-wave frequencies [93]. However, the phase relationship along the rotary wave transmission line is not deterministic and adjacent nodes arbitrarily lead or lag one another. For heterodyne image rejection architectures, it is crucial to have deterministic LO I/Q relationships for proper operation.

This letter presents a technique for generating deterministic phases in a single constructive-wave oscillator (CWO). The quadrature phase outputs can also be combined for N-push harmonic operation or dynamically combined for quadrature
modulation.

5.2.1 Constructive-Wave Oscillator

The block diagram for the CWO is shown in Fig. 5.12. It consists of four traveling-wave stages with delay and amplification based on the constructive-wave amplifier (CWA) developed in [94]. The phase delay through each of the four stages is approximately 90 degrees so that the total delay around the traveling-wave loop is $360^\circ$. As described in [94], forward traveling waves are amplified, and backward traveling waves are attenuated. Therefore, when constructed in a ring as in Fig. 5.12, the forward traveling wave will propagate only in a clockwise direction while the backward traveling wave (counter-clockwise) is attenuated and will not satisfy the oscillation condition. For this design, the quadrature phases are selected and multiplexed through an $N$-to-1 modulator; by proper selection of the quadrature outputs, the 92 GHz frequency of the oscillator can be modulated with either BPSK or QPSK modulation. Alternatively, an $N$-push frequency generation can be realized to generate the 2nd and 4th harmonics by combining multiple phases of the fundamental [95].

The CWA delay and amplification cell is shown in Fig. 5.12. As described in [94], the forward and reverse gain in $S$-parameters for a single stage are determined as follows:

$$S_{21} = \frac{1}{1 + \alpha l + A_v e^{-j(\omega T_d + \theta)}}$$

and

$$S_{12} = \frac{e^{-j\theta} - A_v e^{-j\omega T_d} (1 + \alpha l - (1 - \alpha l) e^{-j2\theta})}{1 + \alpha l + A_v e^{-j(\omega T_d + \theta)}}$$

where the voltage gain through the feedback amplifier is $A_v = g_m Z_0/2$, the phase through the transmission line is $\theta$, and the delay through the feedback path is $T_d$, and $\alpha$ is the transmission-line attenuation coefficient. Waves traveling in the forward direction, i.e. clockwise, add constructively given by (5.7), whereas backward traveling waves (counter-clockwise) add destructively from (5.8). Maximum gain occurs when the phase through the transmission line and the delay through
Figure 5.12: Architecture of the constructive-wave oscillator.
the inverting amplifier are matched at 90°, for 360° of total phase shift. As given by (5.7), the maximum gain \( (1 - A_v)^{-1} \) through the entire CCWA stage can be greater than one even though the gain through the feedback amplifier is less than one. Therefore, the overall loop gain in one direction is 6 dB higher than the gain of a single stage \((1 - A_v)^{-1}\). Simulations of the four-stage ring in Fig. 5.12 indicate that the voltage swing on the transmission line during oscillation is approximately 400 \( mV_{pp} \) as shown in Fig. 5.13.

**Figure 5.13:** Simulated voltages on the transmission lines at the junctions between the 0, 90, 180, and 270 phase amplifications cells after layout parasitic extraction. The voltage amplitude on the transmission line is approximately 400 \( mV_{pp} \).

A grounded CPW is used for the transmission line delay with electrical length \( l \). This GCPW is implemented on the top metal layer with a thickness of 4 \( \mu m \), a width of 8 \( \mu m \), 8 \( \mu m \) shield spacing, and approximately 8 \( \mu m \) spacing to the ground layer beneath. The characteristic impedance of this transmission line is approximately 45 \( \Omega \) which alleviates some of the capacitive loading by the hyperabrupt varactor and the active bipolar devices. A hyperabrupt varactor with an effective capacitance of 5.7 \( fF \) is used to vary the delay through the
transmission line, effectively changing its electrical length \( l \). The simulated tuning range is approximately 1.35 GHz.

To demonstrate the performance of a CWA cell, \( S_{21}, \angle S_{21}, \) and \( S_{12} \) are shown in Fig. 5.14 for three different values of the tuning voltage \( V_{\text{tune}} \). At the oscillator’s center frequency the maximum gain (\( S_{21} \)) is approximately 3 \( dB \) and the isolation (\( S_{12} \)) is less than -2 \( dB \). Increasing the tuning voltage slightly shifts the maximum gain lower in frequency and changes the delay from \( \angle S_{21} \), but the loading and finite \( Q \) of the varactor at higher tuning voltages negatively impacts the gain. Fig. 5.14 shows suppression of the backward traveling wave in (5.8) and amplification of the forward traveling wave from (5.7), demonstrating the deterministic traveling wave propagation.

![Figure 5.14: Simulated S-parameters for the a single feedback cell for the constructive-wave oscillator.](image)

Quadrature outputs are tapped from the center node of each cell and routed to the 50-\( \Omega \) output multiplexer with NFET switches to turn the quadrature outputs on and off. In Fig. 5.12, the node connected to the output buffer is marked as \( \text{tap} \). By combining the proper phases, the fundamental is canceled and harmonics can be selected, similar to the linear superposition technique in [95]. For instance, \( 0^\circ \) and \( 180^\circ \) are combined together to cancel the 92GHz fundamental and select the
184GHz second harmonic. Likewise, if all four phases are selected, the fundamental and second harmonic are canceled, leaving only the fourth harmonic at 368GHz at the output. A 50Ω load resistor is chosen to create a broadband output driver, although a significant power loss \(\approx 23\,dB\) between the output power and the power on the transmission line resonator is incurred due to the degeneration of the HBT by the NFET device. In simulation, the 400\(mV_{pp}\) oscillation in the CWO resonator produces approximately -26.8dBm output power into a 50-Ω load after full layout extraction. The simulated phase noise is approximately -78\(dBc\) at a 1 MHz offset.

### 5.2.2 Measurement Results

The constructive-wave oscillator is fabricated in a 120-nm SiGe BiCMOS process and consumes 32\(mW\) from a 2\(V\) supply. The microphotograph is shown in Fig. 5.15 and the chip area including the pads is 0.65 \(\times\) 0.67 \(mm^2\). The CWO was measured via on-wafer probing with a 110-GHz Cascade waveguide probe, a W-band LNA to improve sensitivity, and an Agilent 11970W waveguide harmonic mixer to convert the fundamental frequency of 92GHz down to the Agilent E4448A spectrum analyzer’s IF. Calibration of the mixer loss and probe loss is performed using the tables provided by the manufacturers.

The measurements results of oscillator output power and tuning voltage versus frequency are shown in Fig. 5.16. The tuning range is approximately 1.3GHz and the maximum output power of -24.5dBm is measured at 92.6GHz, which closely matches the simulated tuning range but with a 1GHz drop in center frequency. The simulated output power is to -26.8dBm across most of the tuning range, and closely matches the measured results. The oscillator output spectrum is demonstrated in Fig. 5.17, with the measured phase noise shown in Fig. 5.18. High frequency testing limitations prevented \(2\)-push (184GHz) and \(4\)-push (368GHz) measurements. The figure-of-merit [93] for this work is 163dBc/Hz, lower than the \(LC\) oscillators from [87] (~180dBc/Hz) which lack (deterministic) quadrature outputs or an integrated \(N\)-push modulator.

To demonstrate modulation of the oscillator, a 50Msymbol/s differential pseudo-random bit-stream is generated from a pulse pattern generator. This ran-
Figure 5.15: Microphotograph of the constructive-wave oscillator.

Figure 5.16: Simulated and measured of oscillator output frequency and power versus tuning voltage.
dom data stream is used to turn off and on the oscillator’s 0 and 180 degree outputs to achieve BPSK modulation. Fig. 5.19 demonstrates the output spectrum with BPSK modulation.

![Figure 5.17: Oscillator spectrum measured using a W-band LNA, the Agilent 11970W harmonic mixer, a MiniCircuits amplifier, and the Agilent E4448A spectrum analyzer.](image)

5.3 Conclusions

Two novel distributed circuits are designed for mm-Wave frequencies, a high-pass distributed amplifier and a constructive-wave oscillator.

The high pass distributed amplifier is demonstrated in a 120nm SiGe BiCMOS process. A peak gain of 8.3dB is reported with a 3dB bandwidth greater than 21GHz which covers the entire $\text{K}_\alpha$-band. The minimum noise figure is 6.9dB and the output $\text{P}_{1\text{dB}}$ is greater than 0dBm.

Traveling-wave techniques can be applied to oscillators as well. A deterministic quadrature oscillator is realized at 92GHz based on traveling-wave amplification; it is fabricated in a 120-nm SiGe BiCMOS process with an area of 0.65 x 0.67$mm^2$. The measured tuning range is 1.3GHz, the measured phase noise is
Figure 5.18: Oscillator phase noise \((dBc/Hz)\) versus frequency offset for the free-running oscillator oscillating at 92.4GHz. At 1MHz, the measured phase noise is -78.6dBc/Hz.

Figure 5.19: CWO output spectrum with 50 Msymbol/s BPSK modulation.
-78.6dBc/Hz at a 1MHz offset, and the power dissipation is 32mW from a 2V supply. A multiplexer output driver allows BPSK and QPSK modulation.

Acknowledgments

Chapter 5 is mostly a reprint of the material as it appears in IEEE Proceedings of the International Microwave Symposium, 2010, Timothy D. Gathman; James F. Buckwalter, and of the material submitted to IEEE Microwave and Wireless Component Letters, 2012, Timothy D. Gathman; James F. Buckwalter. This dissertation author was the primary author of these materials.
Chapter 6

Injection-Locking Techniques for Spectrum Analysis

Commercial and defense UHF and SHF communications systems are beginning to have the ability to be adaptive to their environment as they adopt software-defined radio architectures [46]. Even cellphones are soon expected to become reconfigurable and wideband through the incorporation of software control [96]. With the capability of a software-defined radio, wideband systems can dynamically adapt to their current spectral surroundings. Such adaptive techniques have been referred to as cognitive radios and require spectral estimation to evaluate unused portions of the available spectrum and to estimate channel capacity [97]. To provide this spectral estimation, a spectrum analyzer is one alternative that must be selective and sensitive to the RF environment and consume low power. A target specification for chip-scale spectrum analysis might have a sensitivity of more than -70dBm, a 1% resolution bandwidth with respect to the center frequency, low latency, and power consumption under 100mW.

Spectrum analysis is the quantization of frequency and power information over a given bandwidth. A spectrum analyzer must have high sensitivity to allow detection of very low-power signals, and have a selective frequency response that measures power at a single frequency and rejects power from all other frequencies. However, a spectrum analyzer does not need to retain meaningful phase information and a linear receiver is not necessary. In a linear resonator, frequency
selectivity is related to the transfer function of the filter, $|H(\omega)|$, as a function of frequency. As demonstrated in Fig. 6.1, a finite quality factor $Q$ of the filter results in increased insertion loss in the passband and a rounding off of the filter shape outside of the passband [98]. Increased insertion loss degrades the sensitivity through a decrease in the signal-to-noise ratio. A rounding of the filter shape degrades the selectivity, and thus the filter’s ability to attenuate outside of the passband. Therefore, both the detection of very low-power signals and the ability to reject out-of-band interference are related to the filter $Q$. Achieving high-$Q$ resonators in a low-cost silicon integrated circuit process is difficult without the incorporation of external components such as SAW or cavity filters. The conventional swept super-heterodyne spectrum analyzer architecture shown in Fig. 6.2 typically offers much higher sensitivity and resolution than chip-scale implementations through the use of high-performance, non-integratable components that are not competitive with CMOS in terms of cost, level of integration, and yield. In addition, swept super-heterodyne systems calculate only one frequency point at a time which may fail to capture frequency-hopping or finite-time transmissions [99].

Previous work, outside of heterodyne architectures, has attempted to approach real-time spectrum analysis with a variety of linear techniques. One approach is to channelize the spectrum in the frequency domain. This can be accomplished by splitting the spectrum of interest into $N$ channels that have $N$ bandpass filters to essentially perform a hardware Fourier transform of the signal. Each of the channels would be sensitive to frequencies close the center frequency of the bandpass filter. This type of system is difficult to implement at microwave
frequencies [48]. Most recently, CMOS cross-correlation spectrum analyzers are being explored for cognitive radio applications [100], but these require decade tuning range CMOS voltage-controlled oscillators (VCOs).

CMOS implementations of spectrum analyzers are typically limited by the poor quality factor of passive components. The use of low-$Q$ passives in filters implies that filter performance in terms of out-of-band interference rejection is limited from Fig. 6.1; low-$Q$ passive resonators used in $LC$ VCOs imply poor phase noise characteristics. Reciprocal mixing due to oscillator phase noise is demonstrated in Fig. 6.3, which is enabled by a low-$Q$ RF filter that fails to sufficiently reject an out-of-band interferer. To make matters worse, CMOS VCOs also have limited frequency tuning ranges, and phase noise is typically traded off with the tuning range. Nonlinear dynamics, specifically injection locking into CMOS oscillators, provides a way to mitigate the shortcomings of CMOS passives while taking advantage of low power chip-scale integration. The high level of integration achievable in CMOS enables the fabrication of arrays of injection-locked oscillators that can be used to perform spectrum analysis over a wide bandwidth in quasi-real time.

6.1 Injection-Locking Dynamics

A nonlinear $LC$ oscillator incorporates the (linear) second-order passband response into a feedback system with a nonlinear active device. The active device
**Figure 6.3:** Reciprocal mixing due to poor selectivity RF filter and poor phase noise VCO.

**Figure 6.4:** Injection locking sensitivity curve. The oscillator is locked to the injected frequency inside of the gray region.
provides the negative resistance necessary to overcome the losses of the LC tank and allows oscillation at $\omega_n$. The sensitivity to injection locking, shown graphically in Fig. 6.4, can be described by the injection-locking range in terms of the injected power and frequency; the sensitivity is maximum at the resonant frequency, $\omega_n$, when the minimum $P_{inj}$ is required for locking. The selectivity of an injection-locked oscillator can also generally be described by the locking range. This injection-locking range was first derived by Adler in [101] and can be written as (6.1) for the single-sided locking range under the low injection assumption: $P_{inj} \ll P_{osc}$.

$$\Delta \omega_L = \frac{\omega_n}{Q} \sqrt{\frac{P_{inj}}{P_{osc}}}.$$  (6.1)

Lower-Q CMOS oscillators tend to have larger injection-locking ranges and can analyze wider bandwidths, but the identification of individual signal attributes becomes more difficult. In addition, direct detection of the locking range is difficult; however, phase detection is more easily performed in CMOS. An injection-locked oscillator is synchronized in frequency and has a constant phase offset determined by the characteristics of the injected signal;

$$\Delta \varphi = \arcsin \left( \frac{\omega_{inj} - \omega_n}{\Delta \omega_L} \right).$$  (6.2)

Knowledge of the relative phase shift depends on the injected power and frequency, and at least two non-identical injection-locking systems are required in order to estimate both the frequency and power of an injected signal.

**6.1.1 Injection-Locked Oscillator: Two-tone Injection**

The performance of a spectrum analysis method is determined from the response to multiple tones. For instance, how does a strong out-of-band interferer desensitize the spectrum analyzer? As a basis to analyze two-tone injection into an oscillator, a van der Pol LC oscillator model is constructed as shown in Fig. 6.5. The behavior of this oscillator is expressed from

$$I_{inj1} + I_{inj2} + \ldots + I_{injM} = C \frac{dV}{dt} + \frac{1}{L} \int_0^t V dt + (G_L - G_d(V)) V,$$  (6.3)
where $G_L$ is the tank conductance and $G_d(V)$ is the nonlinear device transconductance. Following van der Pol’s oscillator model [102], the nonlinear transconductance is modeled as a third-order nonlinearity which captures both the amplitude limiting and injection-locking characteristics of nonlinear oscillators: $G_d(V) = g_1 - g_3 V^2$. The analysis in [103] is repeated for the general case of $M$ injected currents from (6.3), where $I_{osc} = A_{osc} G_L$ expresses the oscillator amplitude as a current and low injection is assumed ($I_{inj} \ll I_{osc}$).

$$\frac{d\theta}{dt} = \omega_n + \frac{\omega_n}{2Q_{osc}} \sum_{k=1}^{M} I_{inj,k} \sin (\theta_{inj,k} - \theta)$$  \hspace{1cm} (6.4)

For the case of two injected tones ($M = 2$), the steady state solution for the oscillator phase indicates that the oscillator will lock to the strongest of the two tones that falls within the injection-locking range but the time-dependence of the phase has an additional periodic component from the weaker of the two tones. When the amplitude of the second tone approaches zero, (6.4) simplifies to Adler’s differential equation [101].

The injection-locking behavior is simulated using (6.3) to analyze the desensitization with two-tone injection. We assume an injected signal at $f_{inj1}$, equal to the resonant frequency of the oscillator as seen in the inset of Fig. 6.6(a), and an out-of-band (OOB) interfering signal which is located at an offset $f_{offset}$ away from the oscillator’s resonant frequency; e.g. $f_{inj2} = f_n + f_{offset}$. Ideally, the oscillator locks to $f_{inj1}$ and there is no offset observed from the OOB signal. However, the injection-locked oscillator eventually succumbs to the higher power of the OOB signal. The average frequency deviation $\Delta f = f_{osc} - f_{inj1}$ of the oscillator is plotted against the ratio of interfering currents, $I_{inj2}/I_{inj1}$, for three different values of $f_{offset}$. As one would expect from the sensitivity curve in Fig. 6.4, a larger ratio of $I_{inj2}/I_{inj1}$ is required to force the oscillator to lock to $f_{inj2}$ as $f_{offset}$ is increased.
(a) Simulated perturbation of the average oscillation frequency due to an out-of-band interferer.

(b) Simulated locking range perturbation versus relative phase of the 3rd harmonic.

**Figure 6.6**: Simulation results for impact of harmonic content on the injection-locking range ($A_{osc} = 0.5V$, $Q = 10$, $f_n = 5.5$ GHz, and $g_1/g_3 = 1/3$).
6.1.2 Third Harmonic Injection into an Injection-Locked Oscillator

A similar issue is the desensitization of the nonlinear spectrum analyzer in response to harmonics of the injected signal. The model from (6.3) is adapted to include harmonics of an injected signal and simulated to investigate the effects of the phase of the 3rd harmonic on the locking range. Even under strong harmonic conditions when the magnitude of the first and third are equal, i.e. $I_{3\omega_{\text{inj}}} = I_{\omega_{\text{inj}}}$, Fig. 6.6(b) shows that the locking range is relatively independent of the 3rd harmonic content with a locking range deviation of approximately $\pm 3\%$.

6.2 Injection-Locked Oscillator Arrays

An injection-locked oscillator array (ILOA) was proposed and demonstrated by the authors to use multiple low-\(Q\) CMOS oscillators to perform spectrum analysis over a wide RF bandwidth in quasi-real-time [104]. Arrays of injection-locked, coupled oscillators have been used in the past for phase synchronization and beam steering in phased arrays [105], and more recently integrated into CMOS [106]. The ILOA scheme differs from this previous coupled oscillator array work because each oscillator in the ILOA has a different resonant frequency as shown in Fig. 6.7(a), and there is ideally minimal coupling between these oscillators. Like the previous work in linear spectrum analyzer arrays, the ILOA also performs a function similar to a Fourier Transform in that each oscillator responds to, or channelizes, a signal that lies within its injection locking bandwidth.

Fig. 6.7(a) illustrates the ILOA system. A low noise amplifier (LNA) amplifies the RF signal and injects it into a bank of oscillators each with a different natural frequency. The bank of oscillators effectively samples the injected signal(s) through locking at least two oscillators according to (6.1). Each locked oscillator provides a phase offset as a function of its natural frequency as well as its locking range according to (6.2). The phase output of each oscillator can be compared to a neighboring oscillator through a phase detector (PD) to calculate the relative phase. The relative phase of the oscillators is digitized by an ADC and digital signal
Figure 6.7: Injection-locked oscillator array for spectrum analysis (a) and an array of three injection-locked oscillators to detect a single input tone (b).

processing subsequently estimates the amplitude and frequency of the injected signal from the outputs of two neighboring PDs. Such an ILOA can analyze wide bandwidths with the realization of a large number of low-power oscillators. Also, the spacing between oscillators can be reduced for better frequency resolution.

6.2.1 Single Tone Injection into an Array of Three Injection-Locked Oscillators

Three locked oscillators provide, through the comparison of their phases,
two sets of equations to estimate the injected power and frequency. Each of the
three oscillators has a different natural frequency and, therefore, a different phase
offset with respect to the injected frequency as given by (6.2). This three-oscillator
array is illustrated in Fig. 6.7(b). If the PD is a mixer, then the output of each
phase detector, $V_i$, contains a term with frequency $2\omega_{inj}$ that is filtered out and a
DC term given by (6.5) that depends on the relative phases of the oscillators with
respect to the injected frequency from (6.2).

$$V_i \propto \cos \left( \arcsin \left( Q \frac{\Delta \omega_{n,i}}{\omega_{n,i}} \sqrt{\frac{P_{osc}}{P_{inj}}} \right) - \arcsin \left( Q \frac{\Delta \omega_{n,i+1}}{\omega_{n,i+1}} \sqrt{\frac{P_{osc}}{P_{inj}}} \right) \right),$$

where $\Delta \omega_{n,i} = \omega_{inj} - \omega_{n,i}$. Since the natural frequencies of each oscillator are
known, the outputs of two PDs produce two equations that can be numerically
solved to estimate both $P_{inj}$ and $\omega_{inj}$.

### 6.2.2 Monolithic Integration of Two Injection-Locked Oscillators

The prototype ILOA is fabricated in a 120nm SiGe BiCMOS process to
observe simultaneous injection-locking behavior of the ILOA [104]. While the
desirable locking behavior includes sensitivity to the input RF signal, undesirable
locking occurs when neighboring oscillators mutually lock through coupling or
leakage mechanisms. Reducing leakage between neighboring oscillators allows each
oscillator to act as an independent sampler where the phase responds only to the
injected signal.

A circuit schematic of the injection-locked oscillator array is shown in Fig.
6.8(a) and consists of a 50Ω matching network that divides the injected signal
equally between each oscillator, a current injecting NMOS differential pair, an os-
cillator core, neutralization capacitors to reduce the coupling between oscillators,
and an output driver circuit (not shown). The amplitude of the injected current
controls the bandwidth in which the oscillators will lock from (6.1) as well as the
phase difference between the injected signal and the oscillator from (6.2). Increas-
ing the injection bias current will increase the transconductance, expanding the
locking range.
The injection pair provides an undesirable signal path due to the inherent device parasitic capacitance between gate and drain, $C_{gd}$ in Fig. 6.8(a). Since the drain sees the full oscillator swing, energy leaks into the matching network and into the neighboring injection pair. To neutralize the $C_{gd}$ leakage, neutralization capacitances, $C_c$ are included and cancel out the differential leakage current. This is the primary method to introduce isolation between the two oscillators; other methods to mitigate substrate leakage using guard rings have been explored in [107]. Because of the close proximity of the two oscillators in frequency as well as location, there will be three frequency ranges: one in which neither of the oscillators is locked, one in which only one oscillator is locked, and one in which both oscillators are simultaneously locked. The output of each oscillator is followed by a 50-Ω driver for stabilization of the output impedance seen by the oscillator.

The circuit consumes less than 20mW (excluding the output drivers) as shown in Fig. 6.8(b). The natural frequencies of the oscillators are approximately 5.1 GHz and 5.7 GHz. The spectrum of each oscillator (absent any injection) is shown in Fig. 6.9, with a 4mA injection bias. These spectra illustrate the undesirable coupling due to the neighboring oscillator and illustrate the effectiveness of the neutralization capacitance. The output spectrum contains not only the fundamental tone, denoted by the first marker, but also the fundamental tone of the neighboring oscillator, denoted by the second marker, and intermodulation products, denoted with the third marker for 3rd order intermodulation (IM3) and the fourth marker for the 5th order intermodulation (IM5). The isolation is deduced by comparing the power of the oscillator with the leakage power present from the neighboring oscillator. Therefore, the isolation of Oscillator 1 is 24.7 dB, and the isolation of Oscillator 2 is 14.3 dB. The IM3 and IM5 contributions for both oscillators are less than the neighboring tone. The impact of the coupling is to reduce the sensitivity of the ILOA to weak, distant injected signals. Although the leakage is acceptable for close-in injected signals, better isolation through the substrate and power supply could be achieved.

The phase noise measurement verifies the sensitivity of the locking range. The phase noise of both oscillators is plotted in Fig. 6.10 and shows that the
phase noise at an offset of 1MHz is less than -110dBc/Hz. The phase noise of the oscillators decreases in the presence of a relatively clean injected signal [108]. For higher injected power levels, the oscillators phase noise approaches the injection sources phase noise. In Fig. 6.11 the oscillators phase noise at a 1kHz offset approaches the sources phase noise at power levels greater than -50dBm indicating the onset of injection locking.

The performance measurement for the ILOA is the locking sensitivity, graphed as a function of the locking bandwidth with respect to input power, as depicted previously in Fig. 6.4. The sensitivity curves for both oscillators are shown in Fig. 6.12, both the absence and presence of the neighboring oscillator. The dashed line corresponds to the case when only one oscillator is biased and the alternate is off; the solid line corresponds to the case when both oscillators are functioning. The locking range increases as predicted from (6.1) and intersects for an injected power
Figure 6.9: Output spectrum of Oscillator 1 (a) with a fundamental frequency of 5.76 GHz and Oscillator 2 (b) with a fundamental of 5.11 GHz.

Figure 6.10: Measured phase noise (dBc/Hz) versus frequency for both oscillators and the injection reference.
Figure 6.11: Measured phase noise (dBc/Hz) at a 1kHz offset for each oscillator under injection by the reference. The reference phase noise is measured at a 1kHz offset versus $P_{inj}$.

Figure 6.12: Measured injection sensitivity for a dual-oscillator array fabricated in 120nm SiGe BiCMOS.

Figure 6.13: Simulated injection-locking, phase-locking, and simultaneous injection- and phase-locking ranges.
of about -15 dBm; the intersection is shown in hatched lines.

**6.3 Balanced Injection-Locked Phase-Locked Loops**

The ILOA suffers from sensitivity (power) and selectivity (frequency) characteristics that are not independent; the power of an injected signal impacts the frequency offset from (6.1) at which the signal can be detected, and both injected power and frequency are incorporated into the phase relationship (6.2). Phase-locked loops (PLLs) typically offer a larger locking bandwidth than ILOs [109], and the combination of both injection- and phase-locking increases the locking range as seen in Fig. 6.13. A balanced injection-locked phase-locked loop (ILPLL) array, shown in Fig. 6.14, was proposed in [104] for high-sensitivity spectrum analysis and orthogonalizes the detection of the injected power and frequency. The balanced ILPLL array uses two separate PLLs with positive and negative loop gain polarity. The injected signal is split between the oscillator and PLL; it provides the PLL reference frequency and is also injected into the oscillator.

**6.3.1 Balanced ILPLL Theory**

In the absence of an injection-locking path, the PLL locks each VCO into quadrature with respect to the injected signal. The opposite polarity of the two PLL loops ensures that the oscillators are 180° out-of-phase with respect to one
another. The addition of injection-locking changes the steady-state phase dynamics; injection into the oscillators forces the oscillators to a mutual phase, and, in response, the PLL detunes the oscillators to return to the quadrature phase relationship. Therefore, the oscillator’s natural frequency shifts to the edge of the injection-locking range. The locking range is proportional to the amplitude injected into the oscillator, and the PLL detunes the natural frequencies more dramatically for increasing injected amplitudes. Since the opposite polarity of the PLL loops causes balanced changes in the natural frequencies, the common-mode and differential tuning voltages of the two oscillators estimate the power and frequency of the injected signal.

Adler’s differential phase equation in (6.4) can include the combination of both injection and phase locking dynamics [109], [110]:

\[
\frac{d\theta_i}{dt} = \omega_{n,i} + \Delta \omega_{L,i} \sin (\theta_{inj} - \theta_i + \Psi_i')
\]

(6.6)

where

\[
\Psi_i' = \tan^{-1}\left(\frac{(-1)^{i-1}G_{A_{inj}} \cos(\Psi_{inj})}{\Delta \omega_{L,i}^2 - (-1)^{i-1}G_{A_{inj}} \sin(\Psi_{inj})}\right)
\]

(6.7a)

\[
\Delta \omega_{L,i}' = \sqrt{\Delta \omega_{L,i}^2 + G^2 A_{inj}^2 - (-1)^{i-1}2G_{A_{inj}} \Delta \omega_{L,i} \sin(\Psi_{inj})}
\]

(6.7b)

In (6.6), \(\Delta \omega_{L,i}'\) is the locking range that results from the phase-locked loop and injection-locking dynamics. Each PLL has loop gain \(G = (-1)^{i-1}K_v K_{mix} A_i\), where \(K_{mix}\) is the mixer gain and \(K_v\) is the VCO tuning sensitivity; \(G_{A_{inj}}\) is assumed to be much larger than \(\Delta \Omega_{L,i}\), given by (6.1). The loop filter dynamics are ignored for small variations in the phase deviation \(\theta_{inj} - \theta_i\) near equilibrium. Finally, \(\Psi_{inj}\) is the phase shift between the PLL and the injection-locking path; the impact of the excess phase, \(\Psi_{inj}\), degrades the locking bandwidth and impacts the balanced ILPLL’s stability. In equilibrium, the frequency and amplitude of the injected signal are estimated from the differential and common-mode tuning voltages between the oscillators. The tuning voltages at equilibrium are found by rewriting (6.6) as

\[
0 = \omega_{n,i} + \Delta \omega_{L,i} \sin (\theta_{inj} - \theta_i + \Psi_{inj}) - (-1)^{i-1}K_v v_{c,i}(t).\]

(6.8)
If neighboring oscillators have the same natural frequency, locking range, and amplitude, the differential tuning voltage is approximately

\[ v_{c,2}(t) - v_{c,1}(t) \approx \frac{\omega_0}{K_v Q A_{osc}} A_{inj}. \]  

(6.9)

Note that the differential tuning voltage is directly proportional to the injected amplitude but not the injected frequency. Next, the common-mode voltage between the two PLLs is

\[ \frac{v_{c,2}(t) + v_{c,1}(t)}{2} \approx \frac{\omega_{inj} - \omega_{osc}}{K_v}. \]  

(6.10)

Now the common-mode voltage determines the injected frequency independent of injected power. Narrow resolution bandwidths are achieved with an accurate measurement of the common-mode voltage. Likewise, maximum sensitivity is achieved with an accurate measurement of the differential-mode voltage. Therefore, the differential and common-mode tuning voltages form a unique basis for estimating the injected frequency and power.

### 6.3.2 Balanced ILPLL Simulation

To verify balanced ILPLL operation, noiseless van der Pol oscillators with free-running frequencies of approximately 1GHz, \( A_{osc} = 2V \), \( Q = 10 \), \( K_v = 2\pi \cdot 100\text{MHz} \), ideal mixers, a (Type-I) low pass loop filter with a pole at 2MHz, and loop gain \( G = 2\pi \cdot 10\text{GHz} \) are studied in Simulink. The locking range as a function of the injected power is shown in Fig. 6.13. The balanced ILPLL enhances the locking bandwidth and increases the sensitivity with respect to injection-locking by almost two orders of magnitude; at \( P_{inj} = -27\text{dBm} \), the ILO locking range is 0.7MHz and the locking range of the balanced ILPLL is 42MHz.

The balanced ILPLL system is simulated against injected amplitude and frequency variations. The common-mode and differential-mode tuning voltages should be orthogonal, so changes in the injected amplitude should produce only differential variations, and changes in the injected frequency should produce only common-mode variations. In Fig. 6.15(a), the BILPLL is injected with a frequency of 1.01 GHz with various injected powers; phase locking occurs from \( t = 0\text{s} \) with a small locking transient. The injection-locking path is enabled at 1 \( \mu\text{s} \) and causes
Figure 6.15: Tuning voltages for amplitude and frequency variation of the injected signal.
realignment of the VCOs. Fig. 6.15(b) displays the variation in differential-mode and common-mode tuning voltage with respect to the injected amplitude. As anticipated, only the differential-mode tuning voltage is sensitive to changes in injected amplitude and is linearly related to the injected amplitude from (6.9).

Likewise, to illustrate the effects of an injected signal on the common-mode voltage, a tone with \( P_{\text{inj}} = -25 \text{dBm} \) is injected into the BILPLL for various injected frequencies as shown in Fig. 6.15(c). In this case only the frequency is varied, which results in only a common-mode variation. The relationship between frequency and voltage is plotted in Fig. 6.15(d) and demonstrates the linear relationship from (6.10).

### 6.4 Conclusions

Spectrum analysis circuit techniques have been proposed based on nonlinear oscillator dynamics to detect an unknown signal’s power and frequency. A van der Pol nonlinear oscillator model was used to investigate interference rejection in injection-locked oscillators. Subsequently, injection-locked oscillator arrays were described with measurement results for single and simultaneous injection of two LC oscillators. As an alternative to ILOAs, the dynamics of a balanced ILPLLs is shown to provide independent estimates of the power and frequency of an injected signal.

### Acknowledgments

Chapter 6 is mostly a reprint of three publications. First, material is reprinted from IEEE Proceedings of the Radio Frequency Integrated Circuits Symposium, 2009, Timothy D. Gathman; James F. Buckwalter. Second, chapter 6 is reprinted from material as it appears in IEEE Proceedings of the Antennas and Propogation Society, 2009, Timothy D. Gathman; James F. Buckwalter. Additionally, chapter 6 is mostly a reprint of material as it appears in the American Institute of Physics publication of the International Conference on Nonlinear Dynamics,
2010, Timothy D. Gathman; James F. Buckwalter. The dissertation author was the primary author of these materials.
Chapter 7

Conclusions

This dissertation presented photonic and electrical techniques for time-interleaved analog-to-digital conversion with sampling rates at 20GS/s and beyond. First, a 2GS/s optical sampling receiver in 45nm CMOS SOI was presented with a measured effective-number-of-bits higher than 4.5, suitable to resolve 16-PAM or optical 16-QAM. This linear transimpedance integrator pushes spectral capacity limits of optical communication beyond typical RZ or NRZ encoding. Next, a 2GS/s integrate-and-dump receiver was demonstrated in 120nm SiGe BiCMOS for high-linearity, low-jitter photonic analog-to-digital conversion. The measured effective-number-of-bits for this receiver is 7.5b. This integrate-and-dump receiver performs single-ended to differential conversion and open-loop offset compensation of the photonic pulses. Extending on this work, an integrate-and-sample receiver was presented for rate-scalable time-interleaved photonic sampling and analog-to-digital conversion. The integrate-and-sample receiver operating at 2GS/s has more than 8 effective-number-of-bits measured electronically and approximately 7.5 measured with the photonic sampling front-end (ignoring the photonic modulator distortion). The integrate-and-sample receiver performs both single-ended to differential conversion and also has closed loop offset compensation for highest signal fidelity. The output of the integrate-and-sample-receiver approximates a staircase waveform of integrated/sampled values from the optical pulses and reduces the linearity and bandwidth requirements for a subsequent analog-to-digital converter. A “pseudo-differential” variation of the photonic sampling architecture
was introduced for sub-sampling with high dynamic range up to 50GHz with a SNR of 36.4dB. A 2GS/s double-switching BiCMOS track-and-hold amplifier was presented that had a linearity of approximately 9bits with a 1V_{pp} differential input swing. This topology has been fabricated in 120nm SiGe BiCMOS for the first time. Subsequently, this double-switching track-and-hold architecture is designed at a 40GS/s rate into a wafer-scale heterogeneously integrated 250nm InP and 90nm RF CMOS process.

As scaling steadily pushes CMOS, SiGe, and III-V device $f_T$ and $f_{max}$ higher and higher, analog-to-digital converters continue to advance at a rate of 1.5 bits every 6-8 years [45]. Designs in CMOS have spread into heavily time-interleaved sampling architectures using low-power lower-speed ADCs to decrease power consumption. Due to the need for digital calibration of gain, offset phase, and mismatch CMOS is the best technology choice for these time-interleaved architectures, and will likely continue to see speed improvements with scaling and heavy interleaving. SiGe and III-V technologies, on the other hand, continue to push speed barriers both in full-Nyquist versions and also with limited interleaving to sample rates beyond 50GS/s. Photonics currently has both bandwidth and jitter advantages over electronic sampling architectures and may become one of the forefront technologies for direct-RF sampling or as input frequencies increase into the several-GHz range.

In the second part of this dissertation, millimeter-wave techniques were explored for distributed amplification, oscillation, and spectrum analysis. Distributed amplifiers have typically embraced low-pass topologies governed by the device parasitics which are absorbed into the input and output transmission lines. For the first time, a high-pass distributed amplifier topology is demonstrated with the added benefits of low-frequency rejection and d.c. isolation between stages. Building on these traveling-wave techniques, a deterministic constructive-wave oscillator was built utilizing four traveling-wave, or constructive-wave cells, demonstrating an alternative architecture for W-band oscillator design. Finally, injection-locking was proposed as a means of low-power, chip-scale spectrum analysis. Injection locking demonstrates an alternative architecture to traditional spectrum-analyzer
designs which have limit performance in CMOS due to the low-\(Q\) of passives and the high phase noise of CMOS voltage-controlled oscillators.

Chapter 2 described the design and implementation of an optical sampling receiver in 45nm CMOS SOI with a power consumption under 100mW for the integrate-and-reset active feedback amplifier. At a 2GS/s rate, the measured performance was better than 4.5 ENOB, suitable for optical 16-PAM, or if two receivers are used, for 16-QAM. More spectral efficient schemes for optical communication are being investigated as demands for data capacity continue to develop, motivating the design and analysis of optical sampling receivers with linearity sufficient for multi-level optical PAM and QAM. A jitter and noise analysis is performed in this chapter for such receivers.

Chapter 3 introduced architectures for photonic analog-to-digital conversion. First, a single full-Nyquist photonic sampling architecture was introduced with the design and analysis of a 120nm SiGe BiCMOS integrate-and-dump receiver. The 2GS/s receiver had an active balun performing single-ended to differential conversion, and an open-loop offset compensation to remove the d.c. component of the optical pulse train. Measurements indicated a performance better than 7.5 ENOB for the integrate-and-dump. Extending the sampling rate from 2 to 20GS/s, a rate-scalable architecture suitable for 20 GS/s photonic analog-to-digital conversion was introduced, with the design and analysis of a 120nm SiGe BiCMOS integrate-and-sample receiver. The integrate-and-sample receiver was designed for a dual-channel IC, mounted on a copper heatsink, and packaged onto a PCB for measurements with the optical system. Electrical measurements confirmed an ENOB better than 8.1b for the 2GS/s integrate-and-sample receiver. Optical measurements demonstrated a performance (ignoring the modulator distortion) of approximately 7.5 ENOB. Following, a “pseudo-differential” photonic sampling system was demonstrated with the integrate-and-sample receiver. Subsampling measurements with a sample rate of 2GS/s were conducted up to a 50 GHz input with a measured SNR better than 36.4dB.

Chapter 4 discussed the design of a bipolar double-switching track-and-hold amplifier. Two sample-and-hold test circuits were fabricated and tested in
120nm SiGe BiCMOS, with power consumption less than 520mA from 5V and 2.5V supplies. The measured linearity was approximately 9-bits with a 1V_{pp} input. Sub-sampling was also demonstrated with inputs in the third Nyquist zone at 2100MHz, and intermodulation distortion was measured and compared against the two sample-and-hold architectures. Following, the design of a 40GS/s track-and-hold was described in InP CoSMOS, with simulation results for the double-switching architecture. An interleaved sample-and-hold was also described and simulated, integrating InP full-Nyquist sampling at the front-end, preceding 8x interleaved MOS sample-and-hold circuits.

Chapter 5 described the application of millimeter-wave techniques to construct novel circuits for amplification, oscillation, and spectrum analysis. A high pass distributed amplifier with 21.5GHz of bandwidth was described for wide-band amplification in 120nm SiGe BiCMOS. A deterministic constructive-wave oscillator and quadrature modulator was presented for architectures which require a deterministic quadrature phase relationship, such as image rejection receivers. The constructive-wave oscillator consumed 32mW from a 2V supply, and had a measured phase noise of -78.6dBc/Hz at a 1MHz offset. This oscillator offers a deterministic alternative to traditional quadrature oscillators and rotary-wave oscillators and, additionally, contains an integrated quadrature modulator. BPSK modulation was measured at a symbol rate of 50MS/s at a center frequency of 92 GHz in W-band.

Chapter 6 described the application of injection locking, traditionally used for synchronization, frequency division and multiplication, among other things, to low-power chip-scale spectrum analysis. An injection-locked oscillator array was presented to allow the oscillators to "sample" the injected signal and then power and frequency could be detected by comparing the phases of the oscillators. Following, an alternative architecture employing balanced injection-locked phase-locked loops was presented. This architecture simplifies estimation of an input signal’s power and frequency as the tuning voltages in the two balanced loops provide an orthogonal basis for power and frequency estimation. Simulation results are provided for this architecture showing orthogonality in the common-mode and
differential-mode tuning voltages.
Bibliography


