Title
High Performance RF MEMS Metal-Contact Switches and Capacitive Switches

Permalink
https://escholarship.org/uc/item/5v50m20g

Author
Niu, Chenhui

Publication Date
2016

Peer reviewed|Thesis/dissertation
UNIVERSITY OF CALIFORNIA, SAN DIEGO

High Performance RF MEMS Metal-Contact Switches and Capacitive Switches

A dissertation submitted in partial satisfaction of the requirements for the degree Doctor of Philosophy in Electrical Engineering (Electronic Circuits and Systems)

by

Chenhui Niu

Committee in charge:
Professor Gabriel Rebeiz, Chair
Professor James Buckwalter
Professor William Hodgkiss
Professor Brian Keating
Professor Daniel Sievenpiper

2016
The dissertation of Chenhui Niu is approved, and it is acceptable in quality and form for publication on microfilm and electronically:

____________________________________

____________________________________

____________________________________

____________________________________

____________________________________

Chair

University of California, San Diego

2016
DEDICATION

To my wife and my parents.
EPIGRAPH

Everything is in a state of flux.
—Heraclitus of Ephesus
TABLE OF CONTENTS

Signature Page ............................................................... iii
Dedication ................................................................. iv
Epigraph ................................................................. iv
Table of Contents ......................................................... vi
List of Figures ........................................................... ix
List of Tables ............................................................ xii
Acknowledgements ....................................................... xiii
Vita ................................................................. xv
Abstract of the Dissertation ........................................... xvi

Chapter 1  Introduction .................................................. 1
  1.1 MEMS and RF MEMS in Summary ............................... 1
  1.2 RF MEMS Metal-Contact Switch ................................. 2
    1.2.1 RF MEMS Metal-Contact Switch Applications ............ 2
    1.2.2 Design Considerations ........................................ 3
  1.3 RF MEMS Capacitive Switch ...................................... 6
    1.3.1 Capacitive Switch Application ............................ 6
    1.3.2 Design Considerations ........................................ 8
  1.4 Scope of Dissertation ........................................... 9

Chapter 2 A Miniature RF MEMS Metal-Contact Switch with High Biaxial and Stress Gradient Tolerance ............................. 10
  2.1 Introduction ..................................................... 10
  2.2 Switch Design .................................................... 11
  2.3 Fabrication Process ............................................. 14
  2.4 Measurements .................................................... 14
    2.4.1 Stress Gradient Analysis .................................. 14
    2.4.2 RF Measurements ............................................. 15
  2.5 Conclusion ..................................................... 16

Chapter 3 A Multi-Contact mN-Force RF MEMS Metal-Contact Switch ... 18
  3.1 Introduction ..................................................... 18
  3.2 Design and Analysis ............................................. 19
    3.2.1 Device Topology and Operation ........................... 19
<table>
<thead>
<tr>
<th>Appendix</th>
<th>The UCSD Thick Metal Process in Detail</th>
<th>76</th>
</tr>
</thead>
<tbody>
<tr>
<td>A.1</td>
<td>Wafer Cleaning</td>
<td>76</td>
</tr>
<tr>
<td>A.2</td>
<td>SiCrNx Bias Lines</td>
<td>76</td>
</tr>
<tr>
<td>A.3</td>
<td>Bottom Metal</td>
<td>77</td>
</tr>
<tr>
<td>A.4</td>
<td>SiNx Dielectric Layer</td>
<td>78</td>
</tr>
<tr>
<td>A.5</td>
<td>Bottom Ru Contact</td>
<td>80</td>
</tr>
<tr>
<td>A.6</td>
<td>Spin Coat SAC Layer Stack</td>
<td>80</td>
</tr>
<tr>
<td>A.7</td>
<td>Develop Dimple</td>
<td>81</td>
</tr>
<tr>
<td>A.8</td>
<td>SAC Layer RIE Etch</td>
<td>82</td>
</tr>
<tr>
<td>A.9</td>
<td>Seed Layer Deposition</td>
<td>83</td>
</tr>
<tr>
<td>A.10</td>
<td>Seed Layer Release Hole Etch</td>
<td>84</td>
</tr>
<tr>
<td>A.11</td>
<td>First Au Electroplating</td>
<td>84</td>
</tr>
<tr>
<td>A.12</td>
<td>Second Au Electroplating</td>
<td>85</td>
</tr>
<tr>
<td>A.13</td>
<td>Seed Layer Etch</td>
<td>86</td>
</tr>
<tr>
<td>A.14</td>
<td>Release</td>
<td>87</td>
</tr>
</tbody>
</table>

Bibliography 88
# LIST OF FIGURES

| Figure 1.1: | A SEM image of DMD by Texas Instrument. | 2 |
| Figure 1.2: | RFMD RF1102 SOI SP9T switch used in iPhone 5. | 4 |
| Figure 1.3: | Teledyne SP2T electro-magnetic relay. | 4 |
| Figure 1.4: | Omron SP2T RF MEMS metal-contact switch. | 5 |
| Figure 1.5: | Wispy MEMS tunable digital capacitor (TDC) and a tuner model. | 6 |
| Figure 1.6: | Cavendish Kinetics 5 bits digital variable capacitor (DVC) and an antenna tuning model. | 7 |

| Figure 2.1: | Top view and cross section view of the miniature switch. | 12 |
| Figure 2.2: | (a) Simulated tip deflections of the miniature tethered RF MEMS switch and a 60 μm standard cantilever. (b) Simulated pull-down voltage versus stress gradient of the miniature tethered RF MEMS switch. | 13 |
| Figure 2.3: | Fabrication process of the miniature RF MEMS metal-contact switch. | 14 |
| Figure 2.4: | Measured and simulated surface profile of a test 200 μm free cantilever built using the 1 μm sputtered gold layer. | 15 |
| Figure 2.5: | Microphotograph of the miniature RF MEMS switch. | 15 |
| Figure 2.6: | Measured and simulated S-parameters of the miniature RF MEMS switch in the (a) up-state and (b) down-state position with \( V_{act} = 30 \) V. | 16 |

| Figure 3.1: | Top view and cross section view of the multi-contact switch. | 19 |
| Figure 3.2: | Fixed-fixed beam with two contacts. | 23 |
| Figure 3.3: | Effect of contact heights’ deviation from the nominal height on the fixed-fixed beam. | 24 |
| Figure 3.4: | Contact force difference of the fixed-fixed beam versus \( a/L \). | 24 |
| Figure 3.5: | Simply supported beam with two contacts. | 25 |
| Figure 3.6: | Effect of contact heights’ deviation from the nominal height on the simply supported beam. | 25 |
| Figure 3.7: | Contact force difference of the simply supported beam versus \( a/L \). | 26 |
| Figure 3.8: | Pull-down voltage and collapse voltage versus contact dimple distance \( D \). | 27 |
| Figure 3.9: | Contact force with \( V_{op} = 60 \) V and release force versus contact dimple distance \( D \). | 27 |
| Figure 3.10: | Contact force difference with \( V_{op} = 60 \) V and \( \Delta d = 50 \) nm versus contact dimple distance \( D \). | 28 |
| Figure 3.11: | Simulated contact force versus \( V_{op} \). | 29 |
| Figure 3.12: | Pull-down voltage versus biaxial residual stress. | 29 |
| Figure 3.13: | Contact force with \( V_{op} = 50 \) V, \( V_{op} = 60 \) V and release force versus residual stress. | 30 |
| Figure 3.14: | Simulated Ru coated contact total series resistance versus operation voltage. | 33 |
Figure 3.15: Simulated Ru coated highest contact temperature with 10W THR power versus operation voltage. ........................................ 34
Figure 3.16: Fabrication process of the multi-contact switch. ............. 35
Figure 3.17: Microphotograph of the multi-contact switch. .................. 36
Figure 3.18: Typical switching time and release time. ....................... 37
Figure 3.19: Measured switch mechanical frequency response. .......... 37
Figure 3.20: Measured Vp and Vr versus Temperature. ..................... 38
Figure 3.21: Measured and simulated S-parameters of the switch in the up-state and down-state with Vop=65 V. .............................. 39
Figure 3.22: Measured series resistance Rs versus Vop. ...................... 39
Figure 3.23: Measured 2nd and 3rd order harmonic of the down-state switch and the 1mm CPW line. ........................................ 40
Figure 3.24: Measured IIP2 (top) and IIP3 (bottom) of the down-state switch. ................................................................. 40
Figure 3.25: Shorted switch Rs versus Current. ................................ 41
Figure 3.26: Switch Rs versus Current with Vop=60V. ....................... 42
Figure 3.27: Series resistance versus cycle count. ............................ 42
Figure 4.1: Top view and cross section view of the high capacitance ratio switch. .............................................................. 45
Figure 4.2: Simulated C-Vh curve from 0V to 40V. ............................ 47
Figure 4.3: Simulated C-Vh curve from 30V to 40V. ........................... 48
Figure 4.4: A single shunt nonlinear capacitor circuit. ...................... 49
Figure 4.5: OIP3 versus \( \beta \) of a 1pF shunt capacitor with \( \alpha = 0.01 \) by Volterra series calculation and ADS HB simulation at 16GHz. ........................................ 51
Figure 4.6: A single series nonlinear capacitor circuit. ...................... 52
Figure 4.7: OIP3 versus \( \beta \) of a 1pF series capacitor with \( \alpha = 0.01 \) by Volterra series calculation and ADS HB simulation at 16GHz. ........................................ 54
Figure 4.8: A series back-to-back capacitor circuit. .......................... 55
Figure 4.9: OIP3 versus \( \beta \) of a series back-to-back capacitor with \( C0 = 1 \) pF and \( \alpha = 0.01 \) by Volterra series calculation and ADS HB simulation at 16GHz. ........................................ 57
Figure 4.10: A shunt back-to-back capacitor circuit. .......................... 58
Figure 4.11: OIP3 versus \( \beta \) of a shunt back-to-back capacitor with \( C0 = 1 \) pF and \( \alpha = 0.01 \) by Volterra series calculation and ADS HB simulation at 16GHz. ........................................ 59
Figure 4.12: Cross section view of a back-to-back switch. .................. 62
Figure 4.13: \( \alpha \) differences of switches versus OIP2 improvement. ...... 63
Figure 4.14: Fabrication process of the RF MEMS capacitive switch. .... 64
Figure 4.15: Microphotograph of the high capacitance ratio switch. ...... 65
Figure 4.16: Microphotograph of the back-to-back switch with linearity improvement. ......................................................... 65
Figure 4.17: Surface profile of a test 400 \( \mu \)m X-axis free cantilever. .... 66
Figure 4.18: Surface profile of a test 400 \( \mu \)m Y-axis free cantilever. ...... 67
Figure 4.19: Switch mechanical response from 1kHz to 100 kHz. ........ 67
<table>
<thead>
<tr>
<th>Figure</th>
<th>Description</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>4.20</td>
<td>Measured series device C-Vh curve.</td>
<td>68</td>
</tr>
<tr>
<td>4.21</td>
<td>Measured series back-to-back device C-Vh curve.</td>
<td>69</td>
</tr>
<tr>
<td>4.22</td>
<td>Two-tone IP2 and IP3 measurement setup.</td>
<td>69</td>
</tr>
<tr>
<td>4.23</td>
<td>Measured single series device IP2.</td>
<td>70</td>
</tr>
<tr>
<td>4.24</td>
<td>Measured single series device IP3.</td>
<td>70</td>
</tr>
<tr>
<td>4.25</td>
<td>Measured series back-to-back device IP2.</td>
<td>71</td>
</tr>
<tr>
<td>4.26</td>
<td>Measured series back-to-back device IP3.</td>
<td>72</td>
</tr>
</tbody>
</table>
## LIST OF TABLES

<table>
<thead>
<tr>
<th>Table</th>
<th>Description</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.1</td>
<td>RF Switching Technology Overview [1]</td>
<td>3</td>
</tr>
<tr>
<td>2.1</td>
<td>Simulated parameters of the switch</td>
<td>11</td>
</tr>
<tr>
<td>3.1</td>
<td>Simulated parameters of the switch without and with the release hole</td>
<td>20</td>
</tr>
<tr>
<td>3.2</td>
<td>Switch performance versus stress gradient</td>
<td>30</td>
</tr>
<tr>
<td>4.1</td>
<td>Simulated switch parameters</td>
<td>46</td>
</tr>
<tr>
<td>4.2</td>
<td>Simulated down-state capacitance values versus stress gradient</td>
<td>47</td>
</tr>
<tr>
<td>4.3</td>
<td>Simulated linear tuning range</td>
<td>48</td>
</tr>
<tr>
<td>4.4</td>
<td>Fitted $\alpha$ and $\beta$</td>
<td>48</td>
</tr>
<tr>
<td>4.5</td>
<td>Simulated single series switch linearity $V_s=30V$ and $V_h=35V$</td>
<td>61</td>
</tr>
<tr>
<td>4.6</td>
<td>Simulated back-to-back series switch linearity $V_s=30V$ and $V_h=35V$</td>
<td>62</td>
</tr>
<tr>
<td>4.7</td>
<td>Series device OIP2 and OIP3 simulation</td>
<td>66</td>
</tr>
<tr>
<td>4.8</td>
<td>Series back-to-back device OIP2 and OIP3 simulation without the canceling effect</td>
<td>68</td>
</tr>
</tbody>
</table>
ACKNOWLEDGEMENTS

I would like to express my deep appreciation and gratitude to many people, as this dissertation would not have been possible without their generous help and support. First of all, I would like to thank my advisor, Prof. Gabriel Rebeiz, for his mentorship, his guidance on this research, and his extreme patience in the face of many obstacles. It has been a great honor working with Prof. Rebeiz, and his dedication to my work is very much appreciated.

Next, I would like to thank my dissertation committee members, Professor James Buckwalter, Professor William Hodgkiss, Professor Brian Keating and Professor Daniel Sievenpiper, for taking time to be at my preliminary exams, qualifying exam, and defense exam.

I also would like to thank the staff of UCSD Nano3 cleanroom facility for all their help, including, Bernd Fruhberger, Larry Grissom, Ryan Anderson, Sean Parks, Xuekun Lu, Ivan Harris and Maribel Montero.

Next, I would like to thank all of my colleagues in the TICS group, including Chirag Patel, Isak Reines, Alex Grichener, Hojr Sedaghat-Pisheh, Berke Cetinoneri, Yusuf Atesal, Mehmet Uzunkol, Ozgur Inac, Fatih Golcuk, Jennifer Edwards, Kevin Ho, Yu-Chin Ou, Yi-Chyun Chiou, Chih-Chieh Cheng, Sangyoung Kim, Woorim Shin, Donghyup Shin, Hosein Zareie, Bon-Hyun Ku, and Yang Yang.

Finally, I would like to thank my wife and my parents. My wife kept on cheering me up and did the proof read of my dissertation. My parents could only visit me once during my study in U.S. This dissertation is not possible without their sacrifice.

Chapter 2 is largely a reprint of material published in *IEEE MTT-S International Microwave Symposium Digest*, 2012; Chenhui Niu and G. M. Rebeiz. The dissertation author is the primary author of the source material.

Chapter 3 is largely a reprint of material in preparation for submission to *IEEE Transactions on Microwave Theory and Techniques*, Chenhui Niu and G. M. Rebeiz. The dissertation author is the primary author of the source material.

Chapter 4 is largely a reprint of material in preparation for submission to *IEEE Transactions on Microwave Theory and Techniques*, Chenhui Niu and G. M. Rebeiz. The dissertation author is the primary author of the source material.
This work was supported by the Defense Advanced Research Projects Agency (DARPA) N/MEMS S&T Fundamentals program.

Chenhui Niu
La Jolla, California
2016
VITA

2001-2005  B. E. in Electronic Engineering, Tsinghua University, Beijing, China

2005-2008  M. S. in Electronic Engineering, Tsinghua University, Beijing, China

2008-2010  Graduate student in Electrical Engineering, Arizona State University, Tempe, AZ

2010-2016  Ph. D. in Electrical Engineering, University of California, San Diego, CA

PUBLICATIONS

ABSTRACT OF THE DISSERTATION

High Performance RF MEMS Metal-Contact Switches and Capacitive Switches

by

Chenhui Niu

Doctor of Philosophy in Electrical Engineering (Electronic Circuits and Systems)

University of California, San Diego, 2016

Professor Gabriel Rebeiz, Chair

This dissertation presents designs, fabrication processes and measurements of a series of high performance RF MEMS switches.

Chapter 2 presents a miniature RF MEMS metal contact switch based on a tethered-cantilever structure. The miniature size and the use of tethers result in an excellent biaxial residual stress and stress gradient tolerance. The switch is built using thin metal process with a large biaxial stress and a high stress gradient (50 MPa and -105 MPa/µm), and works well under these conditions. In the up-state, the switch capacitance is 9.4 fF and results in an isolation of 20 dB at 20 GHz. In the down-state, the switch resistance is 3.6 Ω for a gold-gold contact under 30 V actuation voltage.
The switch is compatible with CMOS back-end processing. With its miniature size, the switch could be placed in arrays to achieve lower contact resistance and higher power handling.

Chapter 3 presents a multi-contact mN-force RF MEMS metal-contact switch with a pull-down voltage (Vp) of 45 V-50 V and an operation voltage of 60V-65V. The switch gets a contact force of \( \sim 2.0 \) mN under 65 V actuation voltage and a release force of \( \sim 1.2 \) mN (simulated). The switch gets an on-state resistance of \( \sim 1.8 \) \( \Omega \) with Ru-Au contact and an off-state capacitance of 13.5 fF, which results in a figure of merit of 24 fs. In the temperature stability measurement, the switch shows a change of 4V in pull-down voltage and a change of 2V in release voltage from 25 C to 125 C. In the high power handling measurement, the switch demonstrates a reliability of \( > 10 \) million cold switching cycles with 5 W RF power.

Chapter 4 first presents a high capacitance ratio (Cr) capacitive switch with continuous tuning capability after pull-down. The measured up-state capacitance is 74 fF. The pull-down voltage of the switch is 30V -32V and there is an 8.4\% linear tuning range from 33V to 40V actuation voltage. The measured down-state capacitance is 1296 fF under 40V actuation voltage, resulting in a Cr of 17.5. Next, a back-to-back switch using the high Cr switch is designed to improve IP2 without extra power supply. The back-to-back switch shows an up-state capacitance of 31fF, a Cr of 19.7 and a 6.8\% continuous tuning range from 34V to 40V. The back-to-back switch shows a 14 dB higher OIP2 than the single switch does.
Chapter 1

Introduction

1.1 MEMS and RF MEMS in Summary

Micro-Electro-Mechanical Systems (MEMS) are miniature systems composed of integrated electrical and mechanical parts to sense and/or control things on a \(\mu \text{m}\) scale. The concept of MEMS is attributed to Richard Feynman’s famous talk on December 29th, 1959 [2, 3]. Dr. Feynman foresaw many aspects of future MEMS development with his insight in microphysics. In particular, material properties in the \(\mu \text{m}\) scale are different from bulk properties and the scaling down of integrated circuits (IC) fabrication technology has been a major driving force of MEMS development.

Typical MEMS applications include accelerometers, gyroscopes, pressure sensors, microphones, optical displays, and radio frequency (RF) MEMS. The first four devices have already been used in the latest smartphones. While MEMS optical display technologies like Mirasol [4] are still working their way into the mobile field, the digital light processing (DLP) for desktop applications is considered one of the most successful MEMS products. Fig. 1.1 shows the SEM image of a digital micro mirror device (DMD) in the DLP.

Radio frequency (RF) MEMS make use of micrometer-sized mechanical parts to control or react to RF signals. In this field there are RF micro-mechanical resonators and filters, thin film bulk acoustic resonators (FBAR) and RF MEMS switches.

RF MEMS switches are the focus of this dissertation. Their low-loss, high-isolation and low power consumption make RF MEMS switches the future of tunable
The recent development of carrier aggregation (CA) in LTE puts the new demand in the tunable agile RF front end. For the first time, RF MEMS switches are competitive in the consumer mobile market. RF MEMS switches are categorized into two groups, namely metal-contact switches and capacitive switches. They are discussed in the following sections.

1.2 RF MEMS Metal-Contact Switch

1.2.1 RF MEMS Metal-Contact Switch Applications

The major application fields of RF MEMS metal-contact switch are

1. Antenna switch in the mobile handset: Hundreds of millions of SOI switches are being used in smartphones now. LTE CA puts new linearity challenges and RF MEMS is a promising candidate.

2. High performance relays in automatic testing equipment (ATE): defense and satellite systems. Instrument companies like Agilent and NI have been looking for a high performance RF MEMS switch for decades.

Table 1.1 shows the comparison among major switch technologies [1]. RF MEMS provides the best Ron*Coff figure of merit with the lowest power consumption. Its switching speed could be a limitation. But the major limitation is still the high cost.
Table 1.1: RF Switching Technology Overview [1]

<table>
<thead>
<tr>
<th>Switch Technology</th>
<th>PIN diode</th>
<th>GaAs</th>
<th>SOI/SOS</th>
<th>GaN</th>
<th>RF MEMS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Insertion Loss (dB)</td>
<td>0.3-1.5</td>
<td>0.3-2.5</td>
<td>0.3-2.5</td>
<td>0.1-1.5</td>
<td>0.1-5</td>
</tr>
<tr>
<td>Isolation (dB)</td>
<td>≥30</td>
<td>≥25</td>
<td>≥30</td>
<td>≥30</td>
<td>≥30</td>
</tr>
<tr>
<td>Ron*Coff (fs)</td>
<td>100-200</td>
<td>220</td>
<td>250</td>
<td>400</td>
<td>20-50</td>
</tr>
<tr>
<td>Power Handling (W)</td>
<td>≤50</td>
<td>≤10</td>
<td>≤50</td>
<td>≤100</td>
<td>≤10</td>
</tr>
<tr>
<td>Power Consumption</td>
<td>High</td>
<td>Low</td>
<td>Low</td>
<td>Low</td>
<td>Low</td>
</tr>
<tr>
<td>Switching Speed</td>
<td>ns to μsec</td>
<td>ns to μsec</td>
<td>μsec</td>
<td>ns</td>
<td>μsec</td>
</tr>
<tr>
<td>Operation Voltage (V)</td>
<td>3-5</td>
<td>3-5</td>
<td>2.5-5</td>
<td>10-40</td>
<td>20-100</td>
</tr>
<tr>
<td>Cost</td>
<td>High</td>
<td>Low</td>
<td>Low</td>
<td>High</td>
<td>High</td>
</tr>
</tbody>
</table>

Fig. 1.2 shows the SOI SP9T switch used in iPhone 5. There is no commercially available RF MEMS product to compete with it right now. Some research projects [6, 7] present various ideas and achieve better performance.

Fig. 1.3 shows an electro-magnetic SP2T relay [8]. It needs a 30V DC voltage to operate and consumes around 3W of power.

Fig. 1.4 [9] shows an Omron RF MEMS SP2T metal-contact switch consuming < 10 μW. It provides low loss (Ron<1Ω), high isolation (>30 dB isolation @ 10GHz), excellent power handling (>10W) and higher linearity (>70 dBm). But the product priced at around $50 was discontinued during 2014 due to weak market demand.

1.2.2 Design Considerations

- Mechanical
  - Size: Die size is a major cost factor of a commercial device. The typical dimension of a single RF MEMS metal-contact switch is 100-200 μm. Omron’s higher contact force switches [10, 11] have a dimensions of ~0.5mm to achieve the high contact force.
  - Residual stress and stress gradient tolerance: Movable parts of RF MEMS switches deflect and show stiffness deviation with residual stress and stress
Figure 1.2: RFMD RF1102 SOI SP9T switch used in iPhone 5.

Figure 1.3: Teledyne SP2T electro-magnetic relay.
A residual stress and stress gradient tolerant mechanical structure could reduce the impacts of process variation and improve the yield.

- **Pull-down voltage** ($V_p$): RF MEMS switches operate with voltages higher than $V_p$ and usually require a much higher supply voltage (30-50 V) than IC power rails do. A charge pump is used to supply the internal actuation voltage. A higher voltage gain results in larger silicon area. The power consumption of the charge pump is the dominant factor of the switch power consumption and is also proportional to $V_p$.

- **Collapse voltage** ($V_c$): Movable parts of the switch collapse onto the actuation electrode when the actuation voltage is too high. The threshold voltage $V_c$ is the absolute maximum actuation voltage. $V_p$ and $V_c$ determine the operation range of MEMS switches.

- **Contact material and contact force**: Contact material and contact force and are the key determinants of contact resistance [12].

- **RF**
  - **Isolation**: Off-state capacitance ($C_{off}$) is the key determinant of the switch off-state isolation. A 10 fF $C_{off}$ results in 40 dB isolation at 2GHz.
  - **Insertion loss**: On-state resistance ($R_{on}$) is the key determinant of the switch insertion loss. An 1 Ω $R_{on}$ results in 0.1 dB loss at 2 GHz.
1.3 RF MEMS Capacitive Switch

1.3.1 Capacitive Switch Application

The major application of RF MEMS capacitive switches is the tunable RF front end in the mobile handset. The two major technologies are the impedance tuner and the antenna aperture tuning.

The impedance tuner is placed between a power amplifier (PA) and an antenna to tune the antenna impedance to the optimum point. It increases PA bandwidth, linearity and efficiency (PAE). The extended PA bandwidth also means less PA in the handset, saving both space and cost. Fig. 1.5 presents a tuner model and a Wispry tunable digital capacitor (TDC) component [13].

The antenna aperture tuning technology places the switch into the antenna and tune the resonance frequency of the antenna, as shown in Fig. 1.6. It does not require the space like the tuner circuit and could improve the antenna efficiency by up to 3 dB [14].
Figure 1.6: Cavendish Kinetics 5 bits digital variable capacitor (DVC) and an antenna tuning model.
1.3.2 Design Considerations

- **Mechanical**
  
  - Size: The silicon area consideration is the same as the metal-contact switch case. After the dielectric material and thickness are chosen for the specific application, the capacitive area is proportional to the maximum capacitance ($C_{\text{max}}$).
  
  - Residual stress and stress gradient tolerance: The benefits of a residual stress and stress gradient tolerant mechanical structure also apply to the capacitive switch.
  
  - Pull-down voltage ($V_p$): The power consumption consideration also applies to the capacitive switch. The linearity of the capacitive switch is also affected by the actuation voltage.

- **RF**
  
  - Minimum capacitance ($C_{\text{min}}$)/Capacitance Ratio ($C_r$): For the antenna tuner and the tunable filter applications, $C_r$ determines the tuning range. $C_{\text{min}}$ usually determines the highest or lowest frequency of the tunable circuit.
  
  - Quality factor ($Q$): In the capacitive switch case, higher $Q$ of the switch means lower insertion loss. For varactors in tunable antennas, $Q$ of the varactor determines the efficiency of the antenna. In the antenna tuner, as $Q$ of inductors is low (20-30), $Q$ of varactors does not impact the system much.
  
  - Linearity: RF signal also generates electro-static actuation force on the switch beam. The variation of capacitance value versus RF signal results in non-linear behavior of the capacitive switch. It is usually measured by second/third order intercept points (IP2/IP3) and second/third order harmonics (H2/H3).
1.4 Scope of Dissertation

This dissertation is devoted to the designs, analysis, fabrication processes and measurements of a series of high performance RF MEMS switches.

Chapter 2 presents a miniature RF MEMS Metal-Contact switch that is tolerant to high biaxial stresses and high stress gradients. The switch is designed with a tethered-cantilever structure and is built using a thin metal process. The miniature switch functions well under a wide range of stress conditions and is compatible with CMOS back-end processing.

Chapter 3 presents a multi-contact switch achieving mN-level contact force and restoring force. The inverted crab-leg structure makes sure that the switch is thermal stable from 25°C-125°C. Multiple contact dimples are used to reduce the on-state resistance. The effects of contact dimple placement and contact dimple height deviation on the switch performance are analyzed in details. The switch demonstrates high reliability and high power handling.

Chapter 4 first presents a high capacitance ratio capacitive switch based on a free cantilever structure. A pair of dimples is used to achieve continuous tuning capability after pull-down. A nonlinear capacitive switch model based on Volterra series is used to develop and analyze a back-to-back topology. A back-to-back switch with improved IP2 performance is demonstrated.

Chapter 5 summarizes the whole work and proposes future works, which include new packaging processes and further analysis of the varactor mechanical response.
Chapter 2

A Miniature RF MEMS Metal-Contact Switch with High Biaxial and Stress Gradient Tolerance

2.1 Introduction

In the past few years, there has been a concerted effort in the development of miniature capacitive and metal-contact RF MEMS switches as an alternative solution to the standard designs [15–20]. Miniature designs are less sensitive to stress effects and most important, are compatible with CMOS back-end processing. The effort started at UCSD with arrays of miniature switched capacitors [15], and several other designs were recently demonstrated in different labs and companies [16, 17]. Miniature metal-contact switches (single-element and arrays) were also demonstrated and with good reliability when packaged [18, 19]. One key issue which is applicable to all miniature switch designs is their transfer to a CMOS back-end process. The CMOS process uses Ti/Ta/Al layer for the mechanical portions of the switch with a large biaxial stress (50-100 MPa) and a very high stress gradient (50-100 MPa/um). For example, the metal-contact switches designed in [18, 19] are based on standard cantilevers (or drum) and suffered strongly from stress gradient effects (curvature of the beam, lower contact force), and are not transferable to CMOS designs.
Table 2.1: Simulated parameters of the switch

<table>
<thead>
<tr>
<th></th>
<th>No biaxial stress</th>
<th>50 MPa residual stress</th>
</tr>
</thead>
<tbody>
<tr>
<td>$k_{act}$ (N/m)</td>
<td>165</td>
<td>183</td>
</tr>
<tr>
<td>$k_{release}$ (N/m)</td>
<td>40</td>
<td>44</td>
</tr>
<tr>
<td>Release force (µN)</td>
<td>12</td>
<td>13</td>
</tr>
<tr>
<td>Pull-down voltage $V_p$ (V)</td>
<td>30</td>
<td>32</td>
</tr>
<tr>
<td>Contact force at 45 V(µN )</td>
<td>29</td>
<td>27</td>
</tr>
</tbody>
</table>

This chapter presents a miniature RF MEMS (Micro-Electro-Mechanical System) switch design optimized for the high residual stress and stress gradient available in a thin metal layer process. The switch is built using thin metal layers (1 µm thick gold) and show good planarity and actuation voltage over a wide range of stress conditions. The switch demonstrates a stress gradient tolerance of +/-100 MPa/µm, with <40% pull-down voltage change. The up-state capacitance is 9.4 fF and results in 20 dB isolation at 20 GHz. The contact resistance is 3.6 Ω for a Au-Au contact under 30 V actuation voltage.

2.2 Switch Design

The design is based on a 48x60 µm² Au cantilever structure which is 1 µm thick (Fig. 2.1). A pair of 20 µm-wide supporting tethers are utilized at the cantilever free end to increase the tolerance to biaxial stress [20]. The anchor at the tether is cut at a 45 angle to reduce the stress concentration at the anchors. A 0.3 µm thick dimple is used to form the Au-Au contact, and a 0.3 µm thick stopper is placed at the maximum deflection point to eliminate the beam collapse on the pull-down electrode, and therefore increase the actuation voltage. Table 2.1 presents electrical and mechanical switch simulations for a biaxial stress of 50 MPa. It is seen that the switch is merely affected by residual stress.

The effect of stress gradient on the pull-down voltage is studied by sweeping the stress gradient from -100 MPa/µm to +100 MPa/µm with a 50 MPa residual stress (Fig. 2.2). The maximum change in the pull-down voltage is 7.5 V (20%) for a stress gradient
Figure 2.1: Top view and cross section view of the miniature switch.
Figure 2.2: (a) Simulated tip deflections of the miniature tethered RF MEMS switch and a 60 \( \mu \)m standard cantilever. (b) Simulated pull-down voltage versus stress gradient of the miniature tethered RF MEMS switch.

of +100MPa. The negative stress gradient has a larger effect on \( V_p \) since the switch gap is 0.6 \( \mu \)m. The pull-down voltage decreases by 13\% at -50 MPa/\( \mu \)m and 40\% at -100 MPa/\( \mu \)m. As a comparison, a 60 \( \mu \)m long standard un-supported cantilever is pulled down completely (touches the substrate) at -30 MPa/\( \mu \)m stress gradient. It is clear that the tethered miniature switch has much higher tolerance to stress gradients than a free cantilever (or a fixed-fixed beam).
2.3 Fabrication Process

The switch is fabricated on a 500-μm-thick high-resistivity Si wafer with 250 nm thermal silicon-dioxide on top (Fig. 2.3). The first layer is a 10 nm/100 nm Ti/Au layer sputtered and etched to form the CPW feed-line and bottom electrode. Secondly a 100 nm SiCr layer is sputtered for the bias line. A 10 kΩ/sq resistivity results in a 150 kΩ resistor ($R_{bias}$). A 150 nm SiNx is deposited by PECVD to protect bias lines. A 300 nm PMMA is spun as the bottom sacrificial layer. A 300 nm PMGI is then spun and patterned on top of the PMMA to define the dimple. Next, the PMMA and PMGI sacrificial layers are patterned through an O2 RIE etching. A 1 μm thick Au layer is sputtered and pattern to define the switch (beam) and a 2 μm Au layer is electroplated to thicken the CPW lines. The device is then immersed in Microposit remover 1165, and finally released by a CPD (Critical Point Dryer). Note that the 1 μm sputtered Au layer has a lot of stress and stress gradient and no attempt was done to reduce it (annealing, sputter chamber pressure control, etc.) so as to mimic the stresses present in a CMOS back-end process.

2.4 Measurements

2.4.1 Stress Gradient Analysis

The surface profile is done by a Wyko interferometry system on a test cantilever. The stress gradient of the 1 μm sputtered gold layer is -105 MPa/μm obtained by fitting
Figure 2.4: Measured and simulated surface profile of a test 200 \( \mu \text{m} \) free cantilever built using the 1 \( \mu \text{m} \) sputtered gold layer.

Figure 2.5: Microphotograph of the miniature RF MEMS switch.

the profile of a test 200 \( \mu \text{m} \) -long free cantilever (Fig. 2.4). The cantilever buckles up as its free end touch the bottom wafer surface.

2.4.2 RF Measurements

All RF measurements are done in a Nitrogen filled chamber. The measurement is calibrated at planes A and A’ in Fig. 2.5 using a standard probe-tip SOLT method. A Wyko scan of the tethered RF MEMS switch shows that the tip is bent by 220 nm which agrees well with simulations. The pull-down Vp is \(~17 \text{ V}\) (measured on several samples), and also agrees with the simulated value based on a stress gradient \(~-105 \text{ MPa/\mu m}\).

Fig. 2.6 presents the measured S-parameters. The switch results in an isolation of 29 dB at 6 GHz and 20 dB at 20 GHz in the up-state position. The fitted up-state capacitance is 9.4 fF and agrees very well with Sonnet EM simulations. In down-state position, the fitted contact resistance is \(R_s = 3.6 \Omega\) for a 30 V actuation voltage (Au-to-
Figure 2.6: Measured and simulated S-parameters of the miniature RF MEMS switch in the (a) up-state and (b) down-state position with $V_{act}=30$ V.

Au contact used).

The 3-4 $\Omega$ contact resistance is expected due to the low contact force of a single switch (10-20 $\mu$N) and the presence of contaminants in the test chamber. In the future, arrays of these switches will be fabricated together to result in $< 1$ $\Omega$ contact resistance [18].

### 2.5 Conclusion

This chapter presents a new design for the miniature RF MEMS metal-contact switch which operates well under very high stress conditions (50 MPa and -105 MPa/µm$^2$). The design can be placed in arrays to reduce the contact resistance and increase the power handling in the switch. It is compatible with a CMOS back-end under a range of stress conditions.

This chapter is largely a reprint of material published at the IEEE MTT-S In-
ternational Microwave Symposium Digest, 2012; Chenhui Niu and G. M. Rebeiz. The dissertation author is the primary author of the source material.
Chapter 3

A Multi-Contact mN-Force RF MEMS Metal-Contact Switch

3.1 Introduction

Recent research has shown that metal-contact RF MEMS switches have the potential to replace semiconductor switches and the electromagnetic relay [21–23]. Nonetheless, conventional electromagnetic relays still have the edge in power handling over RF MEMS switches. The factors limiting the power handling of RF MEMS metal-contact switches are the contact material and the contact force. The low softening temperature of gold makes it impractical to use gold-gold contact in the high power application. Refractory metals with high softening temperatures could be used to improve the power handling. Ruthenium(Ru)-gold contact is a common choice, as RuO is also conductive [24, 25]. The use of Ru results in a large contact resistance with μN contact force. Contact force in the mN range results in the contact resistance of 1-2 Ω. In [20, 26], switches reach mN contact force with pull-down voltages of 60-70V and operation voltages higher than 90V. For integrated MEMS devices using internal charge pump to supply the actuation voltage, such a high actuation voltage means a large silicon area and high power consumption.

In this chapter, a low operation voltage metal-contact switch is demonstrated with mN contact force. The multi-contact mN force metal-contact switch gets a contact
force of 2.0 mN and a Ron of 1.8 Ω with 65V operation voltage. A double contact topology is designed to reduce contact resistance. The effect of dimple height deviation is analyzed. The switch reaches more than 10 million cycles with 5W RF power cold switching.

3.2 Design and Analysis

3.2.1 Device Topology and Operation

The switch is based on an invert crab-leg structure, as shown in Fig. 3.1. This structure is demonstrated in section 3.2.4 to be tolerant to residual stress and stress gradient.

The whole switch is \( \sim 500 \, \mu m \times 500 \, \mu m \). The actuation electrode has an active area of \( 0.127 \, mm^2 \). The center plate is \( \sim 300 \, \mu m \times 260 \, \mu m \). Due to the plate size, the step g) in 3.16 shows solvent penetration issue and has failed to totally remove the sacrificial layer. A \( 50 \, \mu m \times 50 \, \mu m \) release hole is introduced at the plate center to solve the problem. Finite element method (FEM) simulation results are compared in Table

![Figure 3.1: Top view and cross section view of the multi-contact switch.](image)
Table 3.1: Simulated parameters of the switch without and with the release hole

<table>
<thead>
<tr>
<th></th>
<th>No Release Hole</th>
<th>50x50 um Release Hole</th>
</tr>
</thead>
<tbody>
<tr>
<td>Length</td>
<td>488 µm</td>
<td>488 µm</td>
</tr>
<tr>
<td>Width</td>
<td>490 µm</td>
<td>490 µm</td>
</tr>
<tr>
<td>Actuation Area (mm²)</td>
<td>0.131</td>
<td>0.127</td>
</tr>
<tr>
<td>Vp</td>
<td>36 V</td>
<td>35 V</td>
</tr>
<tr>
<td>Vc</td>
<td>90 V</td>
<td>88 V</td>
</tr>
<tr>
<td>$k_{act}$</td>
<td>6075 N/m</td>
<td>5986 N/m</td>
</tr>
<tr>
<td>$k_r$</td>
<td>2212 N/m</td>
<td>2160 N/m</td>
</tr>
<tr>
<td>$F_c(50\text{ V})$</td>
<td>1.07 mN × 2</td>
<td>1.03 mN × 2</td>
</tr>
<tr>
<td>$F_c(60\text{ V})$</td>
<td>1.60 mN × 2</td>
<td>1.55 mN × 2</td>
</tr>
<tr>
<td>$F_c(65\text{ V})$</td>
<td>2.00 mN × 2</td>
<td>1.98 mN × 2</td>
</tr>
<tr>
<td>$F_r$</td>
<td>1.22 mN × 2</td>
<td>1.19 mN × 2</td>
</tr>
</tbody>
</table>

3.1. As the release hole takes only 2% of the total actuation area, its impact on the mechanical property of the switch is trivial.

Double contact dimples are employed on each side of the switch to improve both collapse voltage and contact force. The distance between the contact dimple pair D is analyzed in section 3.2.3.

The top movable plate is made of 15 µm electroplated gold. FEM simulation shows the actuation spring constant $k_{act}= 5986$ N/m and the release spring constant $k_r=2160$ N/m. The switch has a simulated pull-down voltage (Vp) of 35 V. It works with operation voltage (Vop) of 60-65 V and achieves a contact force ($F_c$) of 1.5-2.0 mN on each contact dimple.
To avoid the dielectric charging, no dielectric layer is used on top of the actuation electrode. So one of the catastrophic failure scenarios is that the top movable plate is pulled by too much voltage and collapses on the actuation electrode. The movable plate is then shorted to DC operation voltage and the device is permanently damaged. The operation voltage threshold to cause this scenario is defined as collapse voltage \((V_c)\). Multiple stoppers that land on isolated pads are used to increase \(V_c\). In section 3.2.3, \(V_c\) is also an optimization goal in the placement of double contact dimples.

For the contact metallurgy, Ruthenium is chosen for its hardness, high melting point and conductive Ruthenium oxide, which improves power handling and reduces the contact wear at mN contact forces.

### 3.2.2 Pull-Down Dynamics

The MEMS switch satisfied the conditions of the classic small deflection thin plate model, as its thickness \(t \ll l\). The governing equation is

\[
D \nabla^2 \nabla^2 w(x, y, t) = p_z(x, y, t) - \frac{m}{\ddot{w}(x, y, t)}
\]

where \(D = \frac{Eh^3}{12(1-\nu^2)}\) is the flexural rigidity of the plate, \(m = \rho h\), and

\[
p_z(x, y, t) = \varepsilon_0 \frac{V_{act}^2}{2(g_0 - w(x, y, t))^2}
\]

There is no analytical solution to this non linear partial derivative equation, and it is bifurcation. But at the initial stage, we could estimate the displacement.

In the initial state, the actuation voltage \(V_{act}\) is applied.

\[
\begin{align*}
& w(x, y, 0) = 0 \\
& \left. \frac{\partial w(x, y, t)}{\partial t} \right|_{t=0} = 0
\end{align*}
\]

So the initial acceleration of the plate

\[
\frac{m}{\ddot{w}(x, y, t)} = p_z(x, y, t) = \varepsilon_0 \frac{V_{act}^2}{2g_0^2}
\]
For the initial small deflection, the elastic energy could be simplified to the case of a uniform loaded plate. The initial load is a simple uniform load \( p_0 = \varepsilon_0 \frac{V^2}{2a_0^2} \). Every point above the actuation electrode would get the same initial acceleration.

During the plate movement, the strain energy in the plate is

\[
dU = \frac{1}{2} D \left[ \left( \frac{\partial^2 w}{\partial x^2} \right)^2 + \left( \frac{\partial^2 w}{\partial y^2} \right)^2 + 2\nu \left( \frac{\partial^2 w}{\partial x \partial y} \right)^2 \right] dx \, dy + D (1 - \nu) \left( \frac{\partial^2 w}{\partial x \partial y} \right)^2 dx \, dy \tag{3.4}
\]

The plate kinetic energy is

\[
\frac{1}{2} m \left( \frac{\partial w}{\partial t} \right)^2 dx \, dy \tag{3.5}
\]

The energy conservation relationship is

\[
dT + dU = dW \tag{3.6}
\]

As the signal dimples are not placed along the center line, stoppers can land on pads earlier than signal dimples during the pull-down. If stoppers land on pads first, the switch stiffness increases and the signal dimples get less contact force. From (3.6), we could see that the constant displacement contour is also the constant velocity contour in the initial state. To make sure that signal dimples moves faster than all stoppers, the condition is

\[
k_{signal} \leq k_{stopper} \tag{3.7}
\]

### 3.2.3 Double Contact Dimple Design

According to FEM simulation, with a single contact at the plate center, \((D=0)\) in Fig. 3.1, the switch has a pull-down voltage of \( \sim 35 \) V. The single center contact dimple gets a contact force of 2.96 mN with \( V_{op}=60 \) V and 3.76 mN with \( V_{op}=65 \) V. The \( k_r \) is 1980 N/m and the release force is 1.09 mN. Its collapse voltage is \( \sim 69 \) V. There is not enough margin for an operation voltage of 60-65V. This topology has a \( F_c/F_r > 2.5 \),
which may result in stiction problems from our experience. The collapse voltage has a margin less than 10V for $V_{op}=60V$.

A pair of separate contact dimples is utilized to improve the contact force and release force. The following analysis shows that the contact dimple pair also improves the collapse voltage. An analysis of dimple height deviation shows the process tolerance of the design.

### 2-Dimension Case

The 2-dimension uniformly loaded beam is considered first to provide the intuition. As shown in Fig. 3.2, a uniform beam of Young’s modulus $E$ and moment of inertia $I$ is fixed-fixed supported and uniformly loaded with $q$. Two contacts are symmetrically placed at $(x = a, y = 0)$ and $(x = 2L - a, y = 0)$.

The contact force on each contact can be solved by the method of superposition as in (3.9). The contact force increases with the distance between the two contacts.

\[
M = \frac{1}{12} q (8L^3 - 18aL^2 + 12La^2 - 3a^3)/(4L - 3a) \quad (3.8)
\]

\[
F_c = \frac{qL}{2} \frac{4L^2 - 4La + a^2}{a(4L - 3a)} \quad (3.9)
\]

In the ideal case, the double contacts are the same height. In reality, contacts inevitably deviate from the nominal value due to the metal roughness and the sacrificial layer thickness variation. The effect of contacts height deviation could also be derived by the method of superposition as shown in Fig. 3.3.
Figure 3.3: Effect of contact heights’ deviation from the nominal height on the fixed-fixed beam.

Figure 3.4: Contact force difference of the fixed-fixed beam versus a/L.

Assuming the two contacts have a height deviation $\pm \Delta d$ from the nominal height, the contacts are now at $(x = a, y = -\Delta d)$ and $(x = 2L - a, y = \Delta d)$. This case could be further simplified to the superposition of $-\Delta F_c$ at $x = a$ and $\Delta F_c$ at $x = 2L - a$. A pair of differential forces, $\Delta F_c$ and $-\Delta F_c$, is solved.

\[
\frac{\Delta F_c}{\Delta d} = \frac{96EI L^3}{a^3(4L^3 - 9L^2a + 6La^2 - a^3)}
\]  

(3.10)

With a given $\Delta d$, $\Delta F_c$ reaches the minimum at $a/L = (2 - \sqrt{2})$. The force difference curve normalized with $\Delta F_c^{\text{min}}$ is shown in Fig. 3.4. The normalized force difference is $<2$ while $a/L$ is in the range of 0.3-0.8.

The beam reaches the maximum stiffness when $a = \frac{2}{3}L$. The maximum spring constant is $k_{max} = 1296 \frac{EI}{L^4}$. It is $\frac{77}{8}$ times of the center single dimple case where $k_0 = 384 \frac{EI}{L^4}$.

For the simply supported beam in Fig. 3.5 and Fig. 3.6, the same analysis can
Figure 3.5: Simply supported beam with two contacts.

Figure 3.6: Effect of contact heights’ deviation from the nominal height on the simply supported beam.

be done.

The results are shown below.

\[
M = \frac{1}{8} q \frac{(4L^3 - 8aL^2 + 4La^2 - a^2)}{3L - 2a} \tag{3.11}
\]

\[
F_c = \frac{qL}{2} \frac{(8L^3 - 4La^2 + a^3)}{a(3L - 2a)} \tag{3.12}
\]

The contact force increases with a wider span between the two contact dimples.

\[
\frac{\Delta F_c}{\Delta d} = \frac{24L}{a^2(L^2 - 2La + a^2)} \tag{3.13}
\]

With a given \(\Delta d\), \(\Delta F_c\) reaches the minimum at \(a/L = 0.5\). The force difference curve normalized with \(\Delta F_c^{\text{min}}\) is shown in Fig. 3.7.

For other combined support boundary conditions, the optimal \(a\) value is between \(0.5L\) and \((2 - \sqrt{2})L\).
**MEMS Switch Design**

FEM simulation is used to analyze the placement of the double contact dimples. As in Fig. 3.1, the distance $D$ between the double dimples is analyzed for the collapse voltage, the contact force, the release force and the dimple height deviation tolerance.

Fig. 3.9 shows that as the contact dimple distance $D$ increases from 60 $\mu$m to 140 $\mu$m, the pull-down voltage merely increases from 35 V to 38V. The collapse voltage changes more significantly, from the high ~90V with D=80-100 $\mu$m to 67V with D=140 $\mu$m.

The contact force with $V_{op}=60V$ and the release force on each contact dimple are shown in Fig. 3.9. Both the contact force and the release force increase ~50-60 $\mu$N for every 20 $\mu$m increase in D. The contact force has a sudden jump of at D=140 $\mu$m, because $V_{op}=60V$ is close to $V_c=67V$ and the top plate goes too close to the actuation electrode.

Fig. 3.10 shows the contact force difference curve. The contact dimple pair has a height deviation $\Delta d = 50nm$. The longer dimple gets a larger contact force $F_{c0}$. The shorter dimple #1 gets a smaller contact force $F_{c1}$. The contact force difference $\Delta Fc = F_{c0} - F_{c1}$ decreases from 2.4 mN with D=60 $\mu$m to 0.83 mN with D= 120 $\mu$m. For D<60 $\mu$m cases, only the longer dimple contacts with $V_{op}=60V$.

There is a trade-off between the collapse voltage and the dimple deviation toler-
Figure 3.8: Pull-down voltage and collapse voltage versus contact dimple distance D.

Figure 3.9: Contact force with Vop=60V and release force versus contact dimple distance D.
Figure 3.10: Contact force difference with Vop=60V and Δd = 50nm versus contact dimple distance D.

D = 100µm is chosen to balance the two factors. The high collapse voltage (88V) provides a good margin for 60-65V operation voltage. The contact force difference of 1.20 mN is ±40% contact force deviation. The contact force of 1.55 mN × 2 and the release force of 1.19 mN × 2 with Vop=60V. \( \frac{F_c}{F_r} = 1.3 \) reduces the possibility of the switch being stuck down.

The effect of dimple deviation on contact force is further studied for Δd = 25nm and Δd = 50nm at different operation voltages, as shown in Fig. 3.11.

### 3.2.4 Residual Stress and Stress Gradient Tolerance

Fig. 3.12 shows the effect of residual stress on the pull-down voltage. As residual stress increases from -100 MPa to 100 MPa, the pull-down voltage increases from 34V to 38V. The variation from the nominal value with 0 MPa residual stress is ±9%.

Fig. 3.13 shows the effect of residual stress on the contact force and the release force. With Vop=60V, contact force decreases by ~0.1 mN for every 50MPa increase in residual stress. The variation from the nominal value is ±13%. With Vop=50, contact
Figure 3.11: Simulated contact force versus Vop.

Figure 3.12: Pull-down voltage versus biaxial residual stress.
force is also affected by the change of pull-down voltage and gets a variation of ±16%. The release force increases by ~0.08 mN for every 50 MPa increase in residual stress.

As shown in Table 3.2, the switch design is resilient to stress gradient. The pull-down voltage varies from 34 V to 40 V and the collapse voltage varies from 83 V to 90 V with the stress gradient from -1 MPa/µm to +1 MPa/µm. The positive stress gradient bends the plate edge up for +280 nm, while the dimples moves only -25 nm. So the pull-down voltage is barely affected. The negative stress gradient bends the plate edge down and makes stoppers on the edge contact before the signal dimples contact. Therefore the -1 MPa/µm case has the highest pull-down voltage and the lowest Vc/Vp (2.08).
3.2.5 Contact Resistance and Contact Temperature

Clean Metal Contact

All metal surfaces are rough under the microscope. The electric contact forms at a separate asperity point. The contact resistance could be written in the following format as in [27]

\[ R_c = \frac{\rho}{2a} \]  

(3.14)

\[ a = \sqrt{\frac{F_c}{\pi H}} \]  

(3.15)

where \( \rho \) is the resistivity of the contact metal, \( H \) is the Meyer hardness of the contact metal (10.1 GPa for Ru, 1.6 GPa for Au [25]), and \( a \) is the radius of the contact spot due to the contact force \( F_c \).

The contact series resistance on one side is

\[ R_s = \frac{R_{c0}R_{c1}}{R_{c0} + R_{c1}} = \frac{\rho \sqrt{\pi H}}{2 \sqrt{F_{c0} + F_{c1}}} \]  

(3.16)

As \( \frac{1}{\sqrt{F_{c0} + F_{c1}}} = \frac{1}{\sqrt{F_{c0} + 2\sqrt{F_{c0}F_{c1} + F_{c1}}}} < \frac{1}{\sqrt{F_{c0} + F_{c1}}} \) is valid for \( F_{c0} > 0 \) and \( F_{c1} > 0 \), the double contact resistance is always lower than the simple center contact case.

The current through the contact resistance generates Joule heat and raises the temperature of the contact. When the temperature of the contact is higher than the softening temperatures of both contact metals, the stiction of contact metals happen [12]. The softening temperature of Au is \( \sim 373K \) and Ru is \( \sim 700K \) as in [28]. The temperature of the contact is

\[ T_m = \sqrt{\frac{V_c^2}{4L} + T_0^2} = \sqrt{\frac{I_c^2 R_c^2}{4L} + T_0^2} \]  

(3.17)

where \( V_c \) is the voltage across the contact resistance, \( I_c \) is the current through the contact resistance, \( T_0 \) is the ambient temperature and \( L \) is Lorenz number \( (2.44 \times 10^{-8}V^2/K^2) \).

For \( R_c \ll Z_0 \), we can get
\[ I_c = \sqrt{\frac{P_{in}}{Z_0}} \]  

(3.18)

\( I_c \) is split between 2 shunt signal dimples. Ignoring high frequency effect, we get

\[
\begin{align*}
I_{c0} &= \sqrt{\frac{P_{in}}{Z_0}} \frac{R_{c1}}{R_{c0} + R_{c1}} \\
I_{c1} &= \sqrt{\frac{P_{in}}{Z_0}} \frac{R_{c0}}{R_{c0} + R_{c1}}
\end{align*}
\]  

(3.19)

The temperature of each contact dimple is

\[
\begin{align*}
T_{m0} &= \sqrt{\left(\frac{R_{c1}}{R_{c0} + R_{c1}}\right)^2 \frac{P_{in}}{Z_0} \frac{R_{c1}^2}{4L} + T_0^2} \\
&= \sqrt{\left(\frac{R_{c0}R_{c1}}{R_{c0} + R_{c1}}\right)^2 \frac{P_{in}}{Z_0} \frac{R_{c0}^2}{4L} + T_0^2} = \sqrt{\frac{R_{c1}^2}{R_{c0} + R_{c1}} \frac{P_{in}}{Z_0} + T_0^2} \\
T_{m1} &= \sqrt{\left(\frac{R_{c0}}{R_{c0} + R_{c1}}\right)^2 \frac{P_{in}}{Z_0} \frac{R_{c0}^2}{4L} + T_0^2} \\
&= \sqrt{\frac{R_{c0}^2}{R_{c0} + R_{c1}} \frac{P_{in}}{Z_0} + T_0^2} = T_{m0}
\end{align*}
\]  

(3.20)

As shown in (3.20), the contact temperature is determined only by the total contact series resistance.

**Ru coated contact**

To combine the softness of Au and the high melting temperature of Ru, Ru is coated on top of Au.

\[ R_c = \frac{\rho_{Au}}{2a} + \frac{\rho_{Ru}d}{\pi a^2} = \sqrt{\frac{\rho_{Au}^2 \pi H}{4F_c}} + \frac{\rho_{Ru}dH}{F_c} \]  

(3.21)

where \( d \) is the thickness of the Ru layer. Resistivity of thin Ar plasma sputtered Ru film is studied in [24], \( \rho \approx 1 \mu\Omega \cdot m \) depending on the process. It is much larger than the resistivity of Au. So the contact resistance is dominated by the Ru layer.

\[ R_c \approx \frac{\rho_{Ru}dH}{F_c} \]  

(3.22)

The contact series resistance on one side is
The contact series resistance is determined by the total contact force on the side. So the resistance improvement of the double contact comes from its higher total contact force. Fig. 3.14 shows the effect of the dimple height deviation on the contact series resistance. As the pull-down voltage goes higher than 60V, the contact series resistance changes no more than $\pm 0.05\Omega$ due to 50 nm of dimple height deviation.

The heat generated by the contact is modeled as a cylinder heat source $q$. The contact temperature is shown in [29].

$$T_m = q_c a \frac{a}{2K} + T_0$$

(3.24)

$$q_c = \frac{I^2 R_c}{\pi a^2}$$

(3.25)

The current of each contact dimple is

$$\left\{ \begin{array}{l}
I_{c0} = \sqrt{\frac{P_{in}}{Z_0}} \frac{R_{c0}}{R_{c0} + R_{c1}} = \sqrt{\frac{P_{in}}{Z_0}} \frac{F_{c0}}{F_{c0} + F_{c1}} \\
I_{c1} = \sqrt{\frac{P_{in}}{Z_0}} \frac{R_{c1}}{R_{c0} + R_{c1}} = \sqrt{\frac{P_{in}}{Z_0}} \frac{F_{c1}}{F_{c0} + F_{c1}} 
\end{array} \right.$$ 

(3.26)

The contact temperature of each contact dimple is
From (3.27), the contact temperature is proportional to the square root of the contact force. The longer dimple gets a higher contact temperature. As shown in Fig. 3.11, the total contact force $F_{c0} + F_{c1}$ does not vary much with the dimple height deviation. When $F_{c0} = F_{c1}$, the switch get the lowest contact temperature. The dimple height deviation is a negative impact on the switch power handling. Fig. 3.14 shows the effect of the dimple height deviation on the highest contact temperature. As the operation voltage goes higher than 60V, the highest contact temperature increases no more than 15K due to 50 nm of dimple height deviation.

### 3.3 Fabrication Process

The switch is fabricated on a 500 µm thick high-resistivity Si wafer with 250 nm thermal silicon-dioxide on top. Firstly, 100 nm SiCr is sputtered as the bias line. A 15 kΩ/ resistivity results in a ≈1 MΩ bias resistor (Rbias). Secondly, a 10 nm/500 nm Ti/Au layer is patterned to form the CPW feed-line and bottom electrode. 150 nm SiNx is deposited by PECVD to protect the bias line. 100nm Ru is then patterned by lift off,
as the bottom contact metal. 550 nm PMMA is spun as the bottom sacrificial layer. A 300 nm PMGI is then spun and patterned on top of the PMMA to define the dimple. Next, the PMMA and PMGI sacrificial layers are patterned through an O2 RIE etching. The 300nm Au seed layer is sputtered. The 50 µm release holes are patterned on the electroplating seed layer first. 15 µm thick Au is done by a 2-step electroplating. In the first step plating, a 10 µm layer SPR-220-7 is patterned as the electroplating mold and 7.5 µm Au is electroplated. The 1st mold is then removed by flood exposure and develop. The 2nd 15 µm layer of SPR-220-7 is patterned as the 2nd electroplating mold and the 2nd 7.5 µm Au is electroplated. After electroplating, the seed layer is removed by etchant and the switch is released in critical point dryer (CPD).

The fabricated device is shown in Fig. 3.17.

### 3.4 Measurements

All measurements are done on a probe station in a standard N2 filled chamber. Due to the sacrificial layer thickness variation and thick electroplated Au roughness, the pull-down voltage $V_p$ varies from 45 V to 50 V and release voltage $V_r$ varies from 40 V.
The collapse voltage varies from 70 to 75 V. It is ~10 V lower than the simulation result. A possible explanation is that the Au electroplating is not uniform.

### 3.4.1 Mechanics Measurements

The top metal profile is measured by a Veeco NT110 optical profiler. The gold thickness of most devices measured is 16 µm. The surface roughness of the electroplated gold is ±1 µm.

Free cantilever beam test structures are built on wafer with devices. The stress gradient is measured by fitting the curve of cantilever beam. A stress gradient of 0.7 MPa/µm in X axis and 0.55 MPa/µm in Y axis is measured on wafer. The actuation electrode has an up-state capacitance of 1.44 pF. The bias resistance is ~1 MΩ. So the time constant of the actuation circuit in the up-state is 1.44 µs.

The pull-down time and the release time are shown in Fig. 3.18. The switching time is 70 µs for Vop=60 V. After the actuation voltage is applied, the beam does not move in the first 40 µs. The release time is measured to be 20 µs.

The measured mechanical resonant frequency is 129 kHz. The fitted mechanical Q is 1.8.

### 3.4.2 Temperature Measurements

The measured pull-down and release voltages versus temperature are presented in Fig. 3.20. From 25 °C to 125 °C, the measurement shows that the pull-down voltage increases from 48–52 V, while the release voltage increases from 44–46 V.
Figure 3.18: Typical switching time and release time.

Figure 3.19: Measured switch mechanical frequency response.
3.4.3 RF Measurements

Fig. 3.21 shows the measured S-parameters and the simulation prediction by the simplified circuit models. The measurement is done from 0.1 to 18GHz, limited by the bias-T. The measurement and simulation are in good agreement. The fitted up-state capacitance $C_{up}$ is 13.5 fF, resulting in an isolation of 16 dB at 18 GHz in the up-state position. In the down-state, the return loss of the switch is better than 20 dB up to 18 GHz.

Fig. 3.22 shows the fitted series resistance versus the operation voltage. The best case is 0.9 $\Omega$ series resistance with $V_{op}=65V$.

The linearity of the switch is characterized by both single-tone harmonic generation and two-tone inter-modulation measurement. The measurement center frequency is 1.96 GHz, which is the center frequency of the notch filter.

The single tone harmonic measurement is taken from input power level 10 dBm to 30 dBm. Fig. 3.23 shows that the harmonic generation of the switch is less than the 1 mm long CPW line, because the switch transmission length is 800 $\mu$m.

For the two-tone inter-modulation measurement, the input power levels of the measurement are 15 dBm to 25 dBm by a 2 dB step. The two tones are 50 MHz spaced from the center frequency of 1.96 GHz. The switch shows an IIP2 $\geq$ 88 dBm and IIP3 $\geq$ 66 dBm, as in Fig. 3.24. The results are limited by the measurement setup, due to the passive inter-modulation from the probe tip contact.
Figure 3.21: Measured and simulated S-parameters of the switch in the up-state and down-state with V_{op}=65 V.

Figure 3.22: Measured series resistance R_s versus V_{op}.
Figure 3.23: Measured 2nd and 3rd order harmonic of the down-state switch and the 1mm CPW line.

Figure 3.24: Measured IIP2 (top) and IIP3 (bottom) of the down-state switch.
3.4.4 DC Measurements

The switch DC resistance versus DC current is measured through a 4-wire method. Shorted switches are built and measured to characterize the switch line loss. The shorted switch shows a series resistance of \(~0.6\ \Omega\), while the simulation by Ansoft Q3D shows a series resistance of \(0.1\ \Omega\). So there is an additional \(0.5\ \Omega\) of series resistance due to the contamination at the contact metallurgy. Assuming both contact dimples share the same condition, the contamination resistance \(R_{\text{con}}\) is \(1\ \Omega\). It is about 3 times the value of the resistance of Ru film, which is in the range of \(0.3\ \Omega\). So the contact resistance is dominated by the contamination.

The typical curve is shown in Fig. 3.26. The switches are operated with \(V_{\text{op}}=60V\). The DC current handling of the device is \(0.7\ A\). The DC resistance decreases with larger DC current, as the temperature rise at the contact asperity softens the contact metal and increases contact area. The series resistance goes as low as \(0.85\ \Omega\), which is consistent with the RF measurement. According to (3.27), the contact temperature is \(700K-740K\) with \(0.7A\) current, which is close to the Ru softening point. A permanent stuck-down happens after applying \(0.8A\) DC current, which agrees with the simulation.
Figure 3.26: Switch Rs versus Current with Vop=60V.

Figure 3.27: Series resistance versus cycle count.

### 3.4.5 Reliability and Power Handling

The switch is cold-switched at 2.5kHz and Vop=60V with RF input power of 5W at 500MHz. The series resistance is measured at 10k, 100k, 1M, 10M cycles. The switch has failed around 11M cycles. The failure mechanism is that the pull-down voltage increases to 60V at ~11M cycles. The switch then fails after ~5k cycles with Vop=65V.
3.5 Conclusion

In this chapter, a multi-contact mN force RF MEMS metal-contact switch working in 0-18GHz with a pull-down voltage (Vp) of 45V~50V is demonstrated. In the down-state, the switch gets a contact force of \( \sim 2.0 \text{ mN} \) and a Ron of \( \sim 1.8 \Omega \) with 65V operation voltage and a release force of \( \sim 1.2 \text{ mN} \). In the up-state, its off-state capacitance of 13.5 fF, which results in a figure of merit of 24 fs. In the temperature stability measurement from 25°C to 125°C, the switch shows 4V change of pull-down voltage and 2V change of release voltage. In the high power handling measurement, the switch reaches \( > 10 \) million cold switching cycles with 5W RF power.

This chapter is largely a reprint of material in preparation for submission to *IEEE Transactions on Microwave Theory and Techniques*; Chenhui Niu and G. M. Rebeiz. The dissertation author is the primary author of the source material.
Chapter 4

RF MEMS Capacitive Switches with High Capacitance Ratio, Analog Tuning Capability and Linearity Improvement

4.1 Introduction

Various types of varactors have long been used for flexibility, in VCO, PA matching, phase shifter tuning, antenna tuning, etc [30–33]. With the recent development of the smartphone industry, flexibility in RF front end is in heavy demand. Continuously tunable RF MEMS capacitive switches used as varactors for resonators and filters have demonstrated high Q and broad tuning range [34–37]. RF MEMS capacitive switches have also demonstrated low loss, high linearity and very low power consumption compared with BST and GaAs varactor diodes [32, 38, 39].

Second order intermodulation has become an important problem in the modern wireless communication system. For example, the second order harmonic and the second order intermodulation of GSM 900 could interfere with DSC 1800. In [40, 41], an anti-biased topology is presented to improve the linearity, using an extra negative voltage supply.
4.2 Design and Analysis of MEMS Switch

4.2.1 Topology and Principle of Operation

The topology of the switch is shown in Fig. 4.1. The switch is based on a free cantilever made of 4 µm thick electroplated gold. The actuation electrode is divided into 2 parts. The electrode closer to the anchor is used to hold the switch in the down state.
Table 4.1: Simulated switch parameters

<p>| | |</p>
<table>
<thead>
<tr>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Length</td>
<td>178 µm</td>
</tr>
<tr>
<td>Width</td>
<td>160 µm</td>
</tr>
<tr>
<td>Capacitive Area</td>
<td>9600 µm²</td>
</tr>
<tr>
<td>$K_{actuation}$</td>
<td>13.5 N/m</td>
</tr>
<tr>
<td>Cup</td>
<td>63 fF</td>
</tr>
<tr>
<td>Cd</td>
<td>1390 fF</td>
</tr>
<tr>
<td>Cr</td>
<td>22</td>
</tr>
<tr>
<td>Deflection @2MPa/µm</td>
<td>0.55 µm</td>
</tr>
</tbody>
</table>

The voltage on it is $V_h$.

A symmetric trapezoid beam is used as the capacitive area. $V_h$ is applied on the capacitive electrode to tune the capacitance. It is 98 um away from the anchor to increase the capacitance ratio and reduce the pull-down voltage. The ratio of the long base edge and the short base edge is tuned to linearize the C-Vh curve.

The air gap is 1.5 µm. A pair of 0.5 µm thick dimples is used to compose a compound spring structure. The dimples separate the actuation area and the capacitive area of the switch. As the pulling voltage $V_h$ increases, the pull down happens at the beam tip first, then at the dimples. After the dimples contact, the stiffness of the capacitive area increases, and the switch reaches linear tuning range. The switch C-Vh curve shows a linearized slope.

Table 4.1 shows the basic parameters of the switch. 150nm SiNx layer has a roughness comparable to its thickness. Its effective permittivity is estimated to be 3.5, about 50% of Si3N4 bulk value of 7.5. The switch has a pull-down voltage (Vp) of 16V. Without the effect of the metal residual stress and stress gradient, the switch has a up-state capacitance of 63fF and a down-state capacitance of 1390 fF with Vact=40V. The capacitance ratio (Cr) is 22.
Figure 4.2: Simulated C-Vh curve from 0V to 40V.

Table 4.2: Simulated down-state capacitance values versus stress gradient

<table>
<thead>
<tr>
<th>Stress Gradient</th>
<th>Cd (fF) @Vh=20V</th>
<th>Cd (fF) @Vh=30V</th>
<th>Cd (fF) @Vh=40V</th>
</tr>
</thead>
<tbody>
<tr>
<td>0 MPa/µm</td>
<td>1060</td>
<td>1266</td>
<td>1385</td>
</tr>
<tr>
<td>+2 MPa/µm</td>
<td>1064</td>
<td>1262</td>
<td>1379</td>
</tr>
<tr>
<td>-2 MPa/µm</td>
<td>1055</td>
<td>1272</td>
<td>1393</td>
</tr>
</tbody>
</table>

4.2.2 Effect of Stress Gradient on C-Vh Curve

The effect of residual stress on the free cantilever structure is insignificant. The effect of stress gradient is of the most interest and studied by simulating the switch with the stress gradient of -2 MPa/µm and +2 MPa/µm [42]. The switch tip deflects up by 0.55 µm with +2 MPa/µm stress gradient and vice versa. It is about 1/3 of the air gap. A 30V holding voltage V_s is applied on the holding electrode. This voltage can not pull the beam down, but it reduce the effect of the beam deflection.

As shown in Fig. 4.2, with V_s=30V, the pull-down voltage of V_h increases by 2V with both positive and negative stress gradient.

After V_h>20V, the down state capacitance varies less than 15fF with +/-2 MPa/µm stress gradient. The switch is stress gradient resilient.
Table 4.3: Simulated linear tuning range

<table>
<thead>
<tr>
<th>Stress Gradient</th>
<th>C0 @ 35V (fF)</th>
<th>Tuning Range</th>
</tr>
</thead>
<tbody>
<tr>
<td>0 MPa/µm</td>
<td>1340</td>
<td>9.1%</td>
</tr>
<tr>
<td>+2 MPa/µm</td>
<td>1333</td>
<td>9.0%</td>
</tr>
<tr>
<td>-2 MPa/µm</td>
<td>1346</td>
<td>9.1%</td>
</tr>
</tbody>
</table>

Figure 4.3: Simulated C-Vh curve from 30V to 40V.

4.2.3 Linear Tuning C-Vh Curves

After pull down, the switch down-state capacitance is tuned by Vh. The switch could be used as an analog varactor. The Taylor expansion coefficients $\alpha$ and $\beta$ of DC C-Vh curve are fitted with Matlab [43] in the range of 30 to 40V. Table 4.4 presents the fitted $\alpha$ and $\beta$.

Table 4.4: Fitted $\alpha$ and $\beta$

<table>
<thead>
<tr>
<th>Stress Gradient</th>
<th>$\alpha$ ($1/V$)</th>
<th>$\beta$ ($1/V^2$)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0 MPa/µm</td>
<td>8.56e-3</td>
<td>-4.02e-4</td>
</tr>
<tr>
<td>+2 MPa/µm</td>
<td>8.96e-3</td>
<td>-3.81e-4</td>
</tr>
<tr>
<td>-2 MPa/µm</td>
<td>8.72e-3</td>
<td>-4.50e-4</td>
</tr>
</tbody>
</table>
4.3 Nonlinear Capacitor Model

Volterra series analysis is applied to series and shunt cases of single and back-to-back devices in this section. The solving procedure is from [44, 45].

4.3.1 Single Shunt Nonlinear Capacitor

The C-V relationship of the capacitor is given by a Taylor expansion.

\[
C(V) = C_0 + 2C_1V + 3C_2V^2 = C_0(1 + \alpha V + \beta V^2)
\]  

(4.1)

The non-linear current-voltage relationship of the capacitor is given by

\[
I_C = C_0 \frac{dV_c}{dt} + C_1 \frac{dV_c^2}{d^2t} + C_2 \frac{dV_c^3}{d^3t}
\]  

(4.2)

The governing equation of the relationship between the input current input \( I_{in} \) and the output voltage \( V_{out} \) is

\[
V_{out} = H1(\omega) \ast I_{in} + H2(\omega_1, \omega_2) \ast I_{in} \ast I_{in} + H3(\omega_1, \omega_2, \omega_3) \ast I_{in} \ast I_{in} \ast I_{in}
\]  

(4.3)

The circuit Kirchhoff’s Current Law (KCL) calculation of \( V_{out} \) is

\[
I_{in} - Y_a(\omega)V_{out} - I_C = I_{in} - Y_a(\omega)V_{out} - (C_0 \frac{dV_{out}}{dt} + C_1 \frac{dV_{out}^2}{d^2t} + C_2 \frac{dV_{out}^3}{d^3t}) = 0
\]  

(4.4)

Where
\[ Y_a(\omega) = Y(\omega) + \frac{1}{Z_s} + \frac{1}{Z_L} \]  

(4.5)

Solving (4.4) gives the output transfer functions.

\[ H1(\omega) = \frac{1}{j\omega C_0 + Y_a(\omega)} \]  

(4.6)

\[ H2(\omega_1, \omega_2) = -C_1 \frac{j(\omega_1 + \omega_2)H1(\omega_1)H1(\omega_2)}{j(\omega_1 + \omega_2)C_0 + Y_a(\omega_1 + \omega_2)} \]  

(4.7)

For the third order transfer function, define \( \Sigma\omega = \omega_1 + \omega_2 + \omega_3 \).

\[ H3(\omega_1, \omega_2, \omega_3) = -\frac{j\Sigma\omega[2C_1H1(\omega_1)H2(\omega_2, \omega_3) + C_2H1(\omega_1)H1(\omega_2)H1(\omega_3)]}{j\Sigma\omega C_0 + Y_a(\Sigma\omega)} \]  

(4.8)

\[ H1(\omega_1)H2(\omega_2, \omega_3) = \frac{1}{3}[H1(\omega_1)H2(\omega_2, \omega_3)+H1(\omega_2)H2(\omega_3, \omega_1)+H1(\omega_3)H2(\omega_1, \omega_2)] \]  

(4.9)

In the two tone intermodulation case, two RF signals \( I_1(\omega_1) \) and \( I_2(\omega_2) \) are applied on the device.

The output signals are \( 2 \cdot \frac{1}{2} I_1(\omega_1) \cdot H1(\omega_1) \) and \( 2 \cdot \frac{1}{2} I_2(\omega_2) \cdot H1(\omega_2) \).

The 2rd inter-modulations are \( 4 \cdot \frac{1}{2} I_1(\omega_1) \cdot \frac{1}{2} I_2(\omega_2) \cdot H2(\omega_1, \omega_2) \) and \( 4 \cdot \frac{1}{2} I_1(\omega_1) \cdot \frac{1}{2} I_2(\omega_2) \cdot H2(\omega_1, -\omega_2) \).

The 3rd inter-modulations are \( 6 \cdot \frac{1}{2} I_1(\omega_1) \cdot \frac{1}{2} I_1(\omega_1) \cdot \frac{1}{2} I_2(\omega_2) \cdot H3(\omega_1, \omega_1, -\omega_2) \) and \( 6 \cdot \frac{1}{2} I_1(\omega_1) \cdot \frac{1}{2} I_2(\omega_2) \cdot \frac{1}{2} I_2(\omega_2) \cdot H3(-\omega_1, \omega_2, \omega_2) \).

In a linearity measurement setup, 2-tone input signals are equal amplitude and closely spaced.

With \( |\omega_1 - \omega_2| \ll |\omega_1|, |\omega_1_1 - \omega_2| \ll \omega_2 \), we can take the approximation that \( H1(\omega_1) \approx H1(\omega_2) \), \( H3(\omega_1, \omega_1, -\omega_2) \approx H3(-\omega_1, \omega_2, \omega_2) \).

With \( |I_1(\omega_1)| = |I_2(\omega_2)| = I_0 \), the third order inter-modulation (IM3) could be written as \( IM3 = \frac{4}{3} I_0^3 \frac{|H3(\omega_1, \omega_1, -\omega_2)|}{|H1(\omega_1)|} \).

So the output power of each tone are the same power level.

The output 3rd order intercept point (OIP3) \( IM3 = 1 \).

\[ I_0 = \sqrt[3]{\frac{4}{3} |H1(\omega_1)| / |H3(\omega_1, \omega_1, -\omega_2)|} \]
Note the formulas of $H1$ and $H2$, $|H3(\omega_1, \omega_1, -\omega_2)| \sim |H1(\omega_1)|^3$, as $|H1(\omega_1)| \approx |H1(\omega_2)|$. So $I_0 \sim |H1(\omega_1)|$

In (4.8), the terms in the parentheses could completely cancel each other when $2C_1 H1(\omega_1)H2(\omega_2, \omega_3) + C_2 H1(\omega_1)H1(\omega_2)H1(\omega_3) = 0$.

For the simplest case $Y_a(\omega) = \frac{1}{Z_s} + \frac{1}{Z_L} = \frac{2}{Z_0}$ and $\omega C_0 Z_0 \gg 2$, $H1(\omega_1) \approx H1(\omega_2) = \frac{1}{j\omega C_0}$

\[
\frac{C_2}{C_1} \approx -\frac{2}{3} \frac{H1(\omega_1)H1(\omega_1)H1(\omega_2)}{H1(\omega_1)H1(\omega_1)H1(\omega_2)} \approx \frac{2C_1}{3C_0} 
\]

(4.10) could be also written as

\[
\beta = \frac{\alpha^2}{2} 
\]

This result could be verified by harmonic balance (HB) simulation in ADS [46]. Fig. 4.5 shows the OIP3@16GHz versus $\beta$ of a 1pF capacitor with $\alpha = 0.01$. Results calculated by Volterra series model is the same ADS harmonic balance simulation results. OIP3 is the highest when $\beta = 5e - 5$.

A high Q band pass circuit measured at its resonant frequency in [47] gets minimum IM3 when $\beta = \frac{\alpha^2}{2}$.
4.3.2 Single Series Nonlinear Capacitor

The Taylor expansion is the same as the shunt case. The series capacitor case has one more voltage node comparing to the shunt series case, and therefore the transfer functions solving is more complicated. $V_c$ is the voltage across the capacitor. The KCL equations of the circuit is

$$
Vin - I_{out} \ast (Z_S + Z_L) - V_c = 0
$$

$$
I_{out} = C_0 \frac{dV_c}{dt} + C_1 \frac{dV_c^2}{dt^2} + C_2 \frac{dV_c^3}{dt^3}
$$

The output transfer functions are

$$
H_1(\omega) = \frac{j\omega C_0}{1 + j\omega C_0 Z_a(\omega)}
$$

Where

$$
Z_a(\omega) = Z(\omega) + Z_s + Z_L
$$

$$
H_2(\omega_1, \omega_2) = j(\omega_1 + \omega_2)C_1 \left[ \frac{1 - 2H_1(\omega_1)Z_a(\omega_1) + H_1(\omega_1)Z_a(\omega_1)H_1(\omega_2)Z_a(\omega_2)}{1 + j(\omega_1 + \omega_2)C_0 Z_a(\omega_1 + \omega_2)} \right]
$$

Where
To simplify the analysis, the transfer functions of \( V_c \) are

\[
P_1(\omega) = \frac{1}{1 + j\omega C_0 Z_a(\omega)}
\]

\[
P_2(\omega_1, \omega_2) = -j(\omega_1 + \omega_2)C_1 \frac{P_1(\omega_1) \ast P_1(\omega_2) \ast Z_a(\omega_1 + \omega_2)}{1 + j(\omega_1 + \omega_2)C_0 Z_a(\omega_1 + \omega_2)}
\]
Figure 4.7: OIP3 versus $\beta$ of a 1pF series capacitor with $\alpha = 0.01$ by Volterra series calculation and ADS HB simulation at 16GHz.

$$H_2(\omega_1, \omega_2) = j(\omega_1 + \omega_2)C_1 \frac{P_1(\omega_1) * P_1(\omega_2)}{1 + j(\omega_1 + \omega_2)C_0Z_0(\omega_1 + \omega_2)}$$ (4.24)

$$P1P2 = \frac{1}{3}[P1(\omega_1) * P2(\omega_2, \omega_3) + P1(\omega_2) * P2(\omega_1, \omega_3) + P1(\omega_3) * P2(\omega_1, \omega_2)]$$ (4.25)

$$H_3(\omega_1, \omega_2, \omega_3) = \frac{j(\omega_1 + \omega_2 + \omega_3)}{1 + j(\omega_1 + \omega_2 + \omega_3)C_0Z_0(\omega_1 + \omega_2 + \omega_3)}$$* (4.26)

$$[2C_1P1P2 + C_2P1(\omega_1) * P1(\omega_2) * P1(\omega_3)]$$

Similar to the shunt case, the highest OIP3 condition is

$$\beta = \frac{\alpha^2}{2}$$ (4.27)

Fig. 4.7 presents OIP3@16GHz versus $\beta$ of a 1pF capacitor with $\alpha = 0.01$. OIP3 is the highest when $\beta = 5\epsilon - 5$. Maximum OIP3 calculated by Volterra series is higher than the ADS harmonic balance simulation results when OIP3 is higher than 90 dBm, as harmonic balance simulation takes higher orders into calculation.
4.3.3 Series Back-to-Back Nonlinear Capacitor

The topology of a series back-to-back capacitor is shown in Fig. 4.8. The two capacitors are identical and the linear capacitance variation is 180 degree out of phase.

\[
C_1 = L_0 + 2L_1V + 3L_2V^2 = C_0(1 + \alpha_1V + \beta_1V^2) \tag{4.28}
\]

\[
C_2 = M_0 + 2M_1V + 3M_2V^2 = C_0(1 + \alpha_2V + \beta_2V^2) \tag{4.29}
\]

\[
L_0 = M_0, L_1 = -M_1, L_2 = M_2 \tag{4.30}
\]

Transfer function of back-to-back case is more complicated. The voltage at the middle point is defined as \(V_m\). Its transfer functions, \(P1\) and \(P2\), are also calculated.

\[
I_{out} = H1(\omega_1) \ast V(\omega_1) + H2(\omega_1, \omega_2) \ast V(\omega_1) \ast V(\omega_2) + H3(\omega_1, \omega_2, \omega_3) \ast V(\omega_1) \ast V(\omega_2) \ast V(\omega_3) \tag{4.31}
\]

\[
V_m = P1(\omega_1) \ast V(\omega_1) + P2(\omega_1, \omega_2) \ast V(\omega_1) \ast V(\omega_2) + P3(\omega_1, \omega_2, \omega_3) \ast V(\omega_1) \ast V(\omega_2) \ast V(\omega_3) \tag{4.32}
\]

The effect of bias circuit is also taken into account.

\[
k(\omega) = 1 + Gb(\omega)Z_s \tag{4.33}
\]

The output transfer functions are
\[ H_1(\omega) = \frac{j\omega L_0}{1 + j\omega L_0 Z_s + [G_b(\omega) + k(\omega)j\omega L_0](Z_L + \frac{1}{j\omega M_0})} \]  
(4.34)

\[ P_1(\omega) = (Z_L + \frac{1}{j\omega M_0})H_1(\omega) \]  
(4.35)

For the second order transfer function, \( \Sigma \omega = \omega_1 + \omega_2 \).

\[ H_2(\omega_1, \omega_2) = \frac{1}{1 + j\Sigma \omega L_0 Z_s + [G_b(\Sigma \omega) + k(\Sigma \omega)j\Sigma \omega L_0][Z_L + \frac{1}{j\Sigma \omega M_0}]} \]  
(4.36)

\[ \{[G_b(\Sigma \omega) + k(\Sigma \omega)j\Sigma \omega L_0] \frac{M_1}{M_0} [P_1(\omega_1) - H_1(\omega_1)Z_L][P_1(\omega_2) - H_1(\omega_2)Z_L] \]  
\[ + j\Sigma \omega L_1[1 - k(\omega_1)P_1(\omega_1) - H_1(\omega_1)Z_s][1 - k(\omega_2)P_1(\omega_2) - H_1(\omega_2)Z_s] \} \]

\[ P_2(\omega_1, \omega_2) = (Z_L + \frac{1}{j\Sigma \omega M_0})H_2(\omega_1, \omega_2) \]  
(4.37)

\[ \frac{-M_1}{M_0} [P_1(\omega_1) - H_1(\omega_1)Z_L][P_1(\omega_2) - H_1(\omega_2)Z_L] \]

For the third order transfer function, \( \Sigma \omega = \omega_1 + \omega_2 + \omega_3 \).

\[ H_3(\omega_1, \omega_2, \omega_3) = \frac{[G_b(\Sigma \omega) + k(\Sigma \omega)j\Sigma \omega L_0][\frac{M_1}{M_0} 2P_1 + \frac{M_2}{M_0} P_2 + j \Sigma \omega L_1 + 2P_3 + j \Sigma \omega L_2 + P_4]}{1 + j\Sigma \omega L_0 Z_s + [G_b(\Sigma \omega) + k(\Sigma \omega)j\Sigma \omega L_0][Z_L + \frac{1}{j\Sigma \omega M_0}]} \]  
(4.38)

\[ PH_1(\omega_1, \omega_2, \omega_3) = \frac{1}{3} \{[P_1(\omega_1) - H_1(\omega_1)Z_L] * [P_2(\omega_2, \omega_3) - H_2(\omega_2, \omega_3)Z_L] \]  
\[ + [P_1(\omega_2) - H_1(\omega_2)Z_L] * [P_2(\omega_1, \omega_3) - H_2(\omega_1, \omega_3)Z_L] \]  
\[ + [P_1(\omega_3) - H_1(\omega_3)Z_L] * [P_2(\omega_1, \omega_2) - H_2(\omega_1, \omega_2)Z_L] \} \]  
(4.39)

\[ PH_2(\omega_1, \omega_2, \omega_3) = [P_1(\omega_1) - H_1(\omega_1)Z_L][P_1(\omega_2) - H_1(\omega_2)Z_L][P_1(\omega_3) - H_1(\omega_3)Z_L] \]  
(4.40)

\[ PH_3(\omega_1, \omega_2, \omega_3) = \]  
\[ -\frac{1}{3} \{[1 - k(\omega_1)P_1(\omega_1) - H_1(\omega_1)Z_s] * [k(\omega_2 + \omega_3)P_2(\omega_2, \omega_3) - H_2(\omega_2, \omega_3)Z_L] \]  
\[ + [1 - k(\omega_2)P_1(\omega_2) - H_1(\omega_2)Z_s] * [k(\omega_1 + \omega_3)P_2(\omega_1, \omega_3) - H_2(\omega_1, \omega_3)Z_L] \]  
\[ + [1 - k(\omega_3)P_1(\omega_3) - H_1(\omega_3)Z_s] * [k(\omega_1 + \omega_2)P_2(\omega_1, \omega_2) - H_2(\omega_1, \omega_2)Z_L] \} \]  
(4.41)
The highest OIP3 condition is

$$\beta = \frac{3\alpha^2}{2}$$ (4.43)

Fig. 4.9 presents OIP3@16GHz versus $\beta$ of $C_0 = 1$ pF and $\alpha = 0.01$. OIP3 is the highest when $\beta = 1.5e^{-4}$.

### 4.3.4 Shunt Back-to-back Nonlinear Capacitor

With the same principle, we define the RF voltage at the bias point as $V_m$. Its transfer functions $P_1$ and $P_2$ are also calculated.

$$H_1(\omega) = \frac{j\omega(L_0 + M_{01}(\omega))}{Y_a(\omega)j\omega[L_0 + M_{01}(\omega)] + j\omega L_0 * j\omega M_{01}(\omega)}$$ (4.44)

$$P_1(\omega) = \frac{j\omega L_0}{j\omega[L_0 + M_{01}(\omega)]} H_1(\omega)$$ (4.45)

For the second order transfer function, $\Sigma \omega = \omega_1 + \omega_2$. 

---

**Figure 4.9**: OIP3 versus $\beta$ of a series back-to-back capacitor with $C_0 = 1$ pF and $\alpha = 0.01$ by Volterra series calculation and ADS HB simulation at 16GHz.
\[ H_2(\omega_1, \omega_2) = \frac{P_1(\omega_1)P_1(\omega_2)j\Sigma\omega[M_{01}(\omega_1)M_{01}(\omega_2)L_1M_{01}(\Sigma\omega) + M_1L_0^3]}{L_1M_{01}(\Sigma\omega) + j\Sigma\omega Y_a(\Sigma\omega)[L_0 + M_{01}(\omega)]} \]  \hfill (4.46)

\[ P_2(\omega_1, \omega_2) = \frac{P_1(\omega_1)P_1(\omega_2)j\Sigma\omega[M_{01}(\omega_1)M_{01}(\omega_2)L_1M_{01}(\Sigma\omega) + M_1L_0^3]}{L_1M_{01}(\Sigma\omega) + j\Sigma\omega Y_a(\Sigma\omega)[L_0 + M_{01}(\omega)]} \]  \hfill (4.47)

For the third order transfer function, \( \Sigma\omega = \omega_1 + \omega_2 + \omega_3 \).

\[ H_3(\omega_1, \omega_2, \omega_3) = j\Sigma\omega M_{01}(\Sigma\omega)[L_12(H_1 - P_1)(H_2 - P_2) + L_2(H_1 - P_1)^2 + L_0[M_12P_1P_2 + M_2P_1^3]Y_a(\Sigma\omega)[L_0 + M_{01}(\Sigma\omega)] + j\Sigma\omega L_0M_{01}(\Sigma\omega) \]  \hfill (4.48)

\[ \frac{(H_1 - P_1)(H_2 - P_2)}{2} = \frac{1}{3} \left\{ [H_1(\omega_1) - P_1(\omega_1)][H_2(\omega_2, \omega_3) - P_2(\omega_2, \omega_3)] + [H_1(\omega_2) - P_1(\omega_2)][H_2(\omega_1, \omega_3) - P_2(\omega_1, \omega_3)] + [H_1(\omega_3) - P_1(\omega_3)][H_2(\omega_1, \omega_3) - P_2(\omega_1, \omega_3)] \right\} \]  \hfill (4.49)

\[ P_1P_2 = \frac{1}{3} \left\{ P_1(\omega_1)P_2(\omega_2, \omega_3) + P_1(\omega_2)P_2(\omega_1, \omega_3) + P_1(\omega_3)P_2(\omega_1, \omega_2) \right\} \]  \hfill (4.50)

The highest OIP3 condition is

\[ \beta = \frac{3\alpha^2}{2} \]  \hfill (4.51)

Fig. 4.11 presents OIP3@16GHz versus \( \beta \) of \( C_0 = 1 \) pF and \( \alpha = 0.01 \). OIP3 is the highest when \( \beta = 1.5e - 4 \).
4.3.5 Volterra Series Based Mechanical Model of RF MEMS Switches

In [48], an analytic Volterra series based mechanical model for MEMS switches is proposed using a spring-mass-damper model. The model of harmonics modeling is developed here using the same process.

The Volterra series transfer functions of V(Q) relation are

\[ H_1(\omega_1) = \frac{d_0}{\epsilon A} - \frac{Q_0^2}{2k\epsilon^2 A^2}[E(0) + 2E(\omega_1)] \]  \hspace{1cm} (4.52)

\[ H_2(\omega_1,\omega_2) = -\frac{Q_0}{2k\epsilon^2 A^2}[E(\omega_1) + E(\omega_2) + E(\omega_1 + \omega_2)] \]  \hspace{1cm} (4.53)

\[ H_3(\omega_1,\omega_2,\omega_3) = -\frac{1}{2k\epsilon^2 A^2 3}[E(\omega_1 + \omega_2) + E(\omega_2 + \omega_3) + E(\omega_1 + \omega_3)] \]  \hspace{1cm} (4.54)

\[ E(\omega) \] is the normalized mechanical transfer function. For the spring-mass-damper model,

\[ E(\omega) = \frac{1}{1 + j \frac{\omega}{\omega_{\text{res}}} \frac{1}{Q_{\text{mech}}} - \left(\frac{\omega}{\omega_{\text{res}}}\right)^2} \]  \hspace{1cm} (4.55)

From its formula, we have \( E(0) = 1 \) and \( E(\omega) \sim -(\frac{\omega}{\omega_{\text{res}}})^2 = -(\frac{f_{\text{res}}}{f})^2 \) when \( f \gg f_{\text{res}} \).
The Q(V) relations are described with Volterra series transfer functions as

\[ K1(\omega_1) = \frac{1}{H1(\omega_1)} \] (4.56)

\[ K2(\omega_1, \omega_2) = -\frac{H2(\omega_1, \omega_2)}{H1(\omega_1)H1(\omega_2)H1(\omega_1 + \omega_2)} \] (4.57)

\[ K3(\omega_1, \omega_2, \omega_3) = \frac{1}{H1(\omega_1)H1(\omega_2)H1(\omega_1 + \omega_2 + \omega_3)} \]
\[ \{ -H3(\omega_1, \omega_2, \omega_3) + \frac{2}{3} \left[ \frac{H2(\omega_1, \omega_2 + \omega_3)H2(\omega_2, \omega_3)}{H1(\omega_2 + \omega_3)} + \frac{H2(\omega_3, \omega_1 + \omega_2)H2(\omega_1, \omega_2)}{H1(\omega_1 + \omega_2)} \right] \} \] (4.58)

Here K1, K2, K3 are the frequency response kernels of the non-linear behavior.

If the switch is an all-pass system (\(E(\omega) = -1\)), these kernels can be simplified as

\[ K1 = K1(0) = C0 \]
\[ K2 = K2(0, 0) = 2C1 \]
\[ K3 = K3(0, 0, 0) = 3C2 \] (4.59)

For the 2-tone \(\omega_1, \omega_2\) IP2 and IP3 simulation, we are interested in \(K1(\omega_1), K2(\omega_1, \omega_2), K2(\omega_1, -\omega_2)\) and \(K3(\omega_1, \omega_1, -\omega_2)\).

For capacitive switches case, \(\frac{d0}{\gamma A} \gg \frac{Q^2}{2k}\), we have

\[ \frac{K1(\omega_1)}{K1(0)} = \frac{K1(\omega_1)}{C0} \approx 1 \] (4.60)

So the switch capacitance does not change much with frequency.

For the second order Volterra series transfer function,

\[ \frac{K2(\omega_1, \omega_2)}{K2(0, 0)} \approx \frac{H2(\omega_1, \omega_2)}{H2(0, 0)} = \frac{E(\omega_1) + E(\omega_2) + E(\omega_1 + \omega_2)}{3} \] (4.61)

For the third order Volterra series transfer function, note that \(|H3(\omega_1, \omega_2, \omega_3)| \gg \)

\[ \frac{K3(\omega_1, \omega_1, -\omega_2)}{K3(0, 0, 0)} \approx \frac{H3(\omega_1, \omega_1, -\omega_2)}{H3(0, 0, 0)} = \frac{E(\omega_1 + \omega_1) + 2E(\omega_1 - \omega_2)}{3} \] (4.62)
Table 4.5: Simulated single series switch linearity Vs= 30V and Vh=35V

<table>
<thead>
<tr>
<th>Stress Gradient</th>
<th>OIP2 (dBm)</th>
<th>OIP3 (dBm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0 MPa/µm</td>
<td>91.7</td>
<td>53.0</td>
</tr>
<tr>
<td>+2 MPa/µm</td>
<td>91.2</td>
<td>53.2</td>
</tr>
<tr>
<td>-2 MPa/µm</td>
<td>91.6</td>
<td>52.6</td>
</tr>
</tbody>
</table>

4.3.6 Series Varactor Linearity

OIP2 and OIP3 simulation is done by Volterra series transfer functions centered at 1.96 GHz with \( f_1=1983\text{MHz} \) and \( f_2=1937 \text{MHz} \), which is the same as the measurement system.

In the case of the free cantilever design, [49] gives frequency response examples of constrained beam. A simple model could be used as

\[
E(\omega) = \begin{cases} 
1 & f \leq f_{res} \\
-\frac{f_{res}}{f} & f > f_{res}
\end{cases} 
\] (4.63)

\( f_{res} \) is the first pole of the mechanical system, for the down-state of the switch, \( f_{res}=65 \text{ MHz} \) is calculated using the characteristic of electroplated gold from [50]. So the coefficients of capacitance variation are

\[
K^2(\omega_1, \omega_2) = -0.0276 \times K^2(0, 0) \\
K^2(\omega_1, -\omega_2) = 0.3331 \times K^2(0, 0) \\
K^3(\omega_1, \omega_1, -\omega_2) = 0.6611 \times K^3(0, 0, 0)
\]

Table 4.5 presents the simulated OIP2 and OIP3 of the switch.

4.4 Back-to-Back Switch Linearity

The back-to-back series topology of the switch is shown in Fig. 4.12. For the switch 1 at the RF in port, the force applied on the capacitive area of the beam is

\[
F_1 = \frac{1}{2} \varepsilon_0 A \left[ V_h - \frac{V_{RF}}{2} \sin(\omega_1 t + \varphi_1) - \frac{V_{RF}}{2} \sin(\omega_1 t + \varphi_1) \right]^2 \\
= \frac{1}{2} \varepsilon_0 A \left[ V_h^2 + \frac{V_{RF}^2}{2} - V_h V_{RF} [\sin(\omega_1 t + \varphi_1) + \sin(\omega_1 t + \varphi_1)] + ... \right] 
\] (4.64)
Figure 4.12: Cross section view of a back-to-back switch.

Table 4.6: Simulated back-to-back series switch linearity $V_s = 30V$ and $V_h = 35V$

<table>
<thead>
<tr>
<th>Stress Gradient</th>
<th>OIP2 (dBm)</th>
<th>OIP3 (dBm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0 MPa/µm</td>
<td>146.4</td>
<td>50.9</td>
</tr>
<tr>
<td>+2 MPa/µm</td>
<td>145.9</td>
<td>51.0</td>
</tr>
<tr>
<td>-2 MPa/µm</td>
<td>146.3</td>
<td>50.5</td>
</tr>
</tbody>
</table>

While $V_h \gg V_{RF}$, the forces on the other switch is

$$F_2 = \frac{1}{2} \frac{\epsilon A}{g} [V_h + \frac{V_{RF}}{2} \sin(\omega_1 t + \varphi_1) + \frac{V_{RF}}{2} \sin(\omega_1 t + \varphi_1)]^2$$

$$= \frac{1}{2} \frac{\epsilon A}{g} \left\{V_h^2 + \frac{V_{RF}^2}{2} + V_h V_{RF} \left[\sin(\omega_1 t + \varphi_1) + \sin(\omega_1 t + \varphi_1)\right] + \ldots\right\}$$

(4.65)

For RF signal, the two switches have opposite signs for their linear variation coefficients $\alpha$. This results in a canceling effect on IM2. Table 4.6 presents the simulated OIP2 and OIP3 of two perfectly identical switches in the back-to-back topology. OIP3 is $\sim 3$dB lower than the single switch, while OIP2 gets $\sim 55$ dB improvement over the single switch.

4.4.1 Switch Matching

In reality, two MEMS switches are not identical even if they are the same layout and next to each other on the wafer. The perfect canceling of IM2 between two MEMS switches are therefore impossible. For comparison, OIP2 of two switches in series but not back-to-back is calculated by assigning $L_1 = M_1$ in the simulation. For the zero stress gradient case, we get that the OIP2 of not back-to-back series switches is 86.7
The effect of switch $\alpha$ difference is studied by simulating the OIP2 improvement with a number of $\alpha$ difference between 2 back-to-back MEMS switches.

$$L1' = (1 - \Delta)L1$$
$$M1' = (1 + \Delta)M1$$ (4.66)

Fig. 4.13 shows the results. The improvement between the regular series switch and the back-to-back switch $\Delta OIP2$ is

$$\Delta OIP2 = -\log_{10}(2\Delta) \times 20$$ (4.67)

### 4.5 Fabrication Process

The switch is fabricated on a 500 $\mu$m thick high-resistivity Si wafer with 250 nm thermal silicon-dioxide on top. 100 nm SiCr is sputtered for the bias line. A 15 k$\Omega$/ resistivity results in a k$\Omega$ bias resistor (Rbias). Secondly, a 10 nm/500 nm Ti/Au layer is patterned to form the CPW feed-line and bottom electrode. 150 nm SiNx is deposited by PECVD as the dielectric layer of the switch. 550 nm PMMA is spun as the bottom sacrificial layer. A 550 nm PMGI is then spun and patterned on top of the PMMA to
define the dimple. Next, the PMMA and PMGI sacrificial layers are patterned through an O2 RIE etching. 4 μm thick Au is deposited by a 2-step electroplating.

Fig. 4.15 presents the photo of a released series device. Fig. 4.16 presents the photo of a series back-to-back device.

### 4.6 Measurements

#### 4.6.1 Mechanical Measurements

The top metal profile is measured by a Veeco NT110 optical profiler. The measured gold thickness is 4.4.2 μm. The dimple length is measured by Dectak surface profiler during the fabrication and is 550 nm long.

A set of free cantilever test structures are placed on the wafer to measure the residual stress gradient in the top metal. After releasing in the critical point dryer, the deflection of these free cantilevers are measured by Veeco. The according stress gradient is fitted by comparing the deflection with simulation.

In X axis, -300 nm deflection is measured at the tip of a 300 μm long free cantilever structure. It is fitted to be a -0.15 MPa/μm stress gradient.
Figure 4.15: Microphotograph of the high capacitance ratio switch.

Figure 4.16: Microphotograph of the back-to-back switch with linearity improvement.
In Y axis, ~ -320 nm deflection is measured at the tip of a 400 µm long free cantilever structure. It is fitted to be a -0.16 MPa/µm stress gradient.

At the up state, the mechanical resonant frequency of the device is 28 kHz, with a mechanical Q=1.2, as shown in Fig. 4.19.

### 4.6.2 Measured Single Switch C-Vh Curve

The C-Vh curve of a typical device is shown in Fig. 4.20. The pull-down voltage is 30-32 Vh with Vs=30V. The up-state capacitance Cup is 74 fF and the down-state capacitance Cd with an operation Vh of 40V is 1296 fF. A capacitance ratio of 17.5 is achieved.

Dimples contact bottom pads after Vh=33V. There is a 8.4% linear tuning from Vh=33V to 40V. The Taylor expansion coefficients α and β of DC C-Vh curve are fitted with Matlab in the range of 33 to 40V. Table 4.7 presents the fitted α, β and the simulated OIP2 and OIP3.
Figure 4.18: Surface profile of a test 400 μm Y-axis free cantilever.

Figure 4.19: Switch mechanical response from 1kHz to 100 kHz.
4.6.3 Measured Back-to-Back Switch C-Vh Curve

The C-Vh curve of a typical device is shown in Fig. 4.20. The pull-down voltage is 30-32 Vh with Vs=30V. The up-state capacitance Cup is 31 fF and the down-state capacitance Cd with an operation Vh of 40V is 610 fF. A capacitance ratio of 19.7 is achieved.

Dimples contact bottom pads after Vh=34V. There is a 6.8% linear tuning from Vh=34 V to 40 V. The Taylor expansion coefficients $\alpha$ and $\beta$ of DC C-Vh curve are fitted with Matlab in the range of 34 to 40V. OIP2 and OIP3 of the back-to-back switch without the canceling effect is simulated to compare with the measured results, as shown in Table 4.8.

<table>
<thead>
<tr>
<th>C0 @35V</th>
<th>$\alpha$ (1/V)</th>
<th>$\beta$ (1/V^2)</th>
<th>Simulated OIP2</th>
<th>Simulated OIP3</th>
</tr>
</thead>
<tbody>
<tr>
<td>587 fF</td>
<td>11.52e-3</td>
<td>-2.29e-4</td>
<td>82.2</td>
<td>52.3</td>
</tr>
</tbody>
</table>

4.6.4 Linearity Measurements

Fig. 4.22 presents the setup for a two-tone IP2 and IP3 measurement. The two tones are 23 MHz offset the center frequency 1.96 GHz. The input power is coupled through the 20dB coupler and measured by the power meter. Transmission loss from
the output probe tip to the spectrum analyzer is measured by a network analyzer, so that the output power of each tone could be measured by the spectrum analyzer. Therefore IIP2, OIP2, IIP3 and OIP3 are all measured by this setup.

Fig. 4.23 and Fig. 4.24 present the measured IP2 and IP3 of the single device. The IIP2 of the series device is 83.7 dBm and the OIP2 is 80.0 dBm. The IIP3 of the series device is 56.6 dBm and the OIP3 is 53.8 dBm. This complies with the 1.85 dB insertion loss of the series device. The measured OIP2 is 6 dB lower than the simulation result. The measured OIP3 is 2.6 dB higher than the simulation result. A possible explanation is that the mechanical attenuation of the RF signal is higher than the assumption.

Fig. 4.25 and Fig. 4.26 present the measured IP2 and IP3 of the series back-to-back device. The IIP2 of the series back-to-back device is 103.4 dBm and the OIP2 is 94.1 dBm. The IIP3 of the series device is 62.5 dBm and the OIP3 is 55.4 dBm. This complies with the 4.65 dB insertion loss of the series back-to-back device. The
Figure 4.23: Measured single series device IP2.

Figure 4.24: Measured single series device IP3.
back-to-back switch shows a 14 dB higher OIP2 than the single switch.

The OIP2 improvement due to the canceling effect is 17 dB. This implies a 7% variation in the fabricated back-to-back switch pair.

4.7 Conclusion

This chapter first presents a high capacitance ratio (Cr) capacitive switch which shows Cr=17.5 and a 8.4% continuous tuning range after pull-down. The measured up-state capacitance is 74 fF and the measured down-state capacitance is 1296 fF. A Volterra series based model is developed to simulate the switch RF nonlinear properties, specifically IP2 and IP3. Next, a back-to-back switch using the high Cr switch is designed to improve IP2 without any extra power supply. The back-to-back switch shows Cr=19.7 and a 6.8% continuous tuning range after pull-down. The measured up-state capacitance is 31 fF and the measured down-state capacitance is 610 fF. In two-tone IP2 and IP3 measurement, the back-to-back switch shows a 14 dB higher OIP2 than the single switch does, which implies a 7% variation in the back-to-back switch pair.

This chapter is largely a reprint of material in preparation for submission to *IEEE Transactions on Microwave Theory and Techniques*; Chenhui Niu and G. M. Rebeiz. The dissertation author is the primary author of the source material.
Figure 4.26: Measured series back-to-back device IP3.
Chapter 5

Conclusion and Future Work

5.1 Summary

Chapter 2 presents a miniature RF MEMS metal-contact switch based on tethered cantilever structure. The up-state capacitance is 9.4 fF, which results in an isolation of 29 dB at 6 GHz and 20 dB at 20 GHz. The contact resistance is 3.6 Ω for a gold-gold contact under 30 V actuation voltage, which results in a figure of merit of 34 fs. The use of tethers results in low sensitivity to biaxial residual stress and stress gradient. The switch is transferable to a CMOS back-end process under a wide range of stress conditions.

Chapter 3 presents a multi-contact mN force metal-contact switch based on an inverted crab structure. The switch achieves a contact force of 1.55-1.98 mN under 60-65 V actuation voltage, and a release force of 1.19 mN. The measured on-state resistance is 1.8 Ω with Ru-Au contact under 65 V actuation voltage. The measured off-state capacitance is 13.5 fF, which results in a figure of merit of 24 fs. The switch shows excellent temperature stability, a change of 4 V in pull-down voltage and a change of 2V release voltage. Measured results also show high linearity (IIP3>66 dBm, IIP2>88 dBm), and high reliability and power handling (>10 million cold switching cycles at 5 W).

Chapter 4 first presents a high capacitance ratio (Cr) capacitive switch with Cr=17.5 and a 8.4% continuous tuning range from 33 V to 40 V. The measured up-state capacitance is 74 fF and the measured down-state capacitance is 1296 fF under
40V actuation voltage. A nonlinear capacitive switch model is developed, using the switch’s DC voltage response and mechanical response. Next, a back-to-back topology is designed to improve IP2 without any extra power supply. A back-to-back switch composed of two high Cr switches is demonstrated with Cr=19.7 and a 6.8% continuous tuning range from 34 V to 40 V. The measured up-state capacitance is 31 fF and the measured down-state capacitance is 610 fF under 40 V actuation voltage. The back-to-back switch shows a 14 dB OIP2 improvement over the single switch.

All switches presented in this dissertation are fabricated in the UCSD Nano3 cleanroom. All measurements are done on unpackaged devices in a N2 filled chamber on a Cascade Summit probe station.

5.2 Future Work

The new XeF2 dry etching facility in the UCSD Nano3 cleanroom provides a new dry release process. With CVD sacrificial layer and dry release process, zero level packaging of RF MEMS devices could be implemented to improve RF performance and life time of MEMS switches. BCB spin-on encapsulation on top of silicon nitride cap is a promising candidate [51].

The non-linearity model in chapter 4 provides an insight into the switch RF linearity performance before higher power 2-tone RF measurement. As a simple mechanical model of the down-state switch is used, there is room for improvement in the agreement between the theory and the measurement. More detailed FEM simulation and modal analysis would give a more accurate mechanical response of the down-state switch, which would improve the accuracy of the switch non-linearity model.

5.3 Summary of Appendix

Appendix A describes the detailed fabrication process for the UCSD RF MEMS thick metal DC contact switch. This fabrication process is a superset of all other switch fabrications. The process was developed by the dissertation author at the UCSD Nano3 clean room starting from the UCSD standard metal-contact switch process with input
from Chirag Patel, Alex Grichener, and Hojr Sedaghat-Pisheh.
Appendix A

The UCSD Thick Metal Process in Detail

Thick gold electroplating process is explained in detail here.

A.1 Wafer Cleaning

1. Soak wafer in acetone, then put in to ultrasonic cleaner for 5 minutes.

2. Soak wafer in 1165 solvent at 85C for 30min.

3. Rinse wafer in Acetone, Methanol, IPA followed by a DI water rinse and N2 dry.

4. Put wafer in Technics PEIIB Planar Etcher (Asher) at 200W/200mT for 2min.

5. Clean fluoware with Acetone, Methanol, IPA, and N2 dry thoroughly.

A.2 SiCrNx Bias Lines

1. Pattern NR9-1500

   (a) Spin=4000rpm, acc=35, time=40s

   (b) Bake 150C/2 min

   (c) Dose 12s
(d) Postbake 100C/1 min

(e) Develop RD6 15-16s. 20s dev in RD6 introduces small holes on PR. Or RD6 3:1 DI 60s. Lower RD6 rate cannot develop PR well.

(f) Asher 200 W/200 mT for 1 min.

2. Denton Sputter

   (a) 100W 30s RF bias RIE

   (b) Ar=42scm N2=4 sccm. 4.6mT 300W 13 min (3k Ohm). Use dummy glass slides to verify recipe.

3. Lift Off in Acetone

   (a) SiCr is harder to peel off because of the RIE. Wait for a while and take the large peel off part out of beaker.

   (b) Ultrasonic for 5 min in a new acetone beaker.

   (c) Acetone, DI water washing. N2 gun dry.

**A.3 Bottom Metal**

1. Clean Wafer in RD2 110C for 30 min

   (a) Dry 120C 2 min

   (b) Asher 200 W/200 mT for 2 min

2. Denton Sputter 500 nm Au

   (a) 100W 30s RF bias RIE

   (b) Ti Ar=42 sccm 3.8mT 300W 30s

   (c) Au Ar=42scm 3.8 mT 200W 10 min20s (Au Ar=43 sccm 3.8mT 300W 380s)

   (d) Ti Ar=42 sccm 3.8mT 300W 30s
3. Pattern S1818

(a) Spin=4000 rpm, acc=35, time=40s
(b) Postbake 90s/105C
(c) 10S dose
(d) Develop in MIF 319 35S
(e) Asher 200 W/200 mT for 1min

4. Gold Etching

(a) HF 10:1 DI 5s. Rinse with DI water \(\approx\)1min. N2 gun dry.
(b) Gold Etchant for \(\approx\)50S. (This depends a lot on how you stir the wafer holder. Use test samples for a starting guess, but trust your eyes if gold is all gone.)

5. Remove S1818

(a) Acetone, Methanol, IPA washing
(b) 1165 85C for 10min
(c) Dry 120C 2 min
(d) Asher 200 W/200 mT for 2min

6. Remove Ti adhesion layer

(a) 5s in HF 10:1 DI
(b) Rinse with DI water \(\approx\)1min. N2 gun dry.

A.4 SiNx Dielectric Layer

1. Filmetric measure SiO2 on Si thickness.

(a) Measure at least 5 points across the wafer.
(b) Record the initial thickness of the thermal SiO2 layer coming with the high-resistivity Si wafer.

2. PECVD 150nm SiNx

(a) 350 C 100W

(b) SiH4=20 sccm NH3=22sccm N2=380sccm

(c) HF=20W/13s, LF=20W/7s, Time=17 min (Test with dummy Si wafer)

3. Filmetric measure SiNx on SiO2 on Si thickness to verify SiNx thickness.

4. Pattern S1818

(a) Spin=4000 rpm, acc=35, time=40s

(b) Postbake 90s/105C

(c) 10S dose

(d) Develop in MIF 319 35S

(e) Asher 200 W/200 mT for 1min

5. RIE etch

(a) CF4=35 sccm, O2=3 sccm

(b) Power=100 W, Pressure=75 mT

(c) Time=75 S remove 150 nm SiNx and ~15 nm SiO2

(d) Time=83 S remove 165 nm SiNx and ~25 nm SiO2

6. Filmetric measure SiO2 on Si thickness.

(a) Measure around the same sample points.

(b) The after RIE SiO2 thickness should be 5-15nm lower than the initial thickness. This verifies the total removal of SiNx layer.
A.5 Bottom Ru Contact

1. NR9-1500
   
   (a) Spin=4000rpm, acc=35, time=40s
   (b) Bake 150C/2 min
   (c) Dose 12s
   (d) Postbake 100C1 min
   (e) Develop RD6 3:1 DI 15-16s
   (f) Asher 200 W/200 mT for 1 min (Important!)

2. Denton Sputter 100nm Ru
   
   (a) 100W 30s RF bias RIE
   (b) Ar=46sccm 4.4mT
   (c) Test sampe 100W 20 min to calibrate
   (d) 100W 10 min for 100°110 nm

3. Lift Off in Acetone
   
   (a) Wait for a while and take the large peel off part out of beaker.
   (b) Ultrasonic for 5 min in a new acetone beaker.
   (c) Acetone, DI water washing. N2 gun dry.

A.6 Spin Coat SAC Layer Stack

1. Spin 550 nm PMMA 950k C4
   
   (a) 2 step spin recipe
      i. Spin=500 rpm, acc=4, time=5s
      ii. Spin=2100 rpm, acc=8, time=45s
(b) Due to the change of PMMA film thickness, the color of film will change during the spin process. The film thickness is stable after the film color stays stable. The spin time should allow the film to stay stable 5s.

(c) Bake 135C 10 min
(d) Bake 180C 2 min
(e) Filmetric measure PMMA thickness

2. Spin 300 nm PMGI SF6

(a) 2 step spin recipe
   i. Spin=500 rpm, acc=4, time=5s
   ii. Spin=3000 rpm, acc=8, time=45s

(b) Similar color change happens to PMGI film. The spin time should allow the film to stay stable 5s.

(c) Bake 135C 10 min
(d) Bake 180C 2 min
(e) Filmetric measure PMGI on PMMA thickness

A.7 Develop Dimple

1. Pattern S1813

(a) Spin=3000 rpm, acc=35, time=45s
(b) 120s/105C baking,
(c) 8S dose

2. Develop dimple

(a) Develop in MIF319 35-45s. Develop time depends on the actual thickness of PMGI. Verify with the dummy wafer in step 6.
3. Remove S1813

   (a) 50s Flood exposure
   (b) 30s in Microdev:DI 1:1

4. Dry Wafer

   (a) Rinse in DI water and N2 dry
   (b) Bake at 105C/120s

5. Measure developed PMGI thickness with Dektak

A.8 SAC Layer RIE Etch

1. Ti hard mask with evaporator

   (a) Evaporate ~700°A of Ti at 8-10°A/S (use crystal for thickness)
   (b) Watch out for the temperature. The meter read out should not exceed 80C. The internal temperature is 35-40C higher than the read out.
   (c) Real thickness would be 35-40 nm

2. Pattern S1813

   (a) Spin=3000 rpm,acc=35, time=45s
   (b) 120s/105C bake
   (c) 8S dose
   (d) Develop in Microdev:DI 1:1 30s

3. Etch Ti hard mask

   (a) 5s in HF:DI water 1:10

4. Remove S1813
(a) Flood expose for 50s
(b) Develop in Microdev:DI 1:1 for 30s

5. Dry etch sacrificial layer (Oxford P80)

(a) O2 clean recipe
(b) Chiller 35, power=50W, pressure=50mTorr, flow=50sccm
(c) Etch rate of PMMA ~2.0nm/s
(d) Etch rate of PMGI 1.6-1.7 nm/s
(e) 10 Min in total
(f) 150W for 90s

6. Measure with Dektak and Veeco. Dektak data is more trustworthy.

7. Remove Ti hard mask

(a) 5s in HF 10:1 DI
(b) Rinse with DI water for 1min. N2 gun dry.

A.9 Seed Layer Deposition

1. Dry Wafer

(a) N2 clean
(b) Bake at 105C 5min

2. Denton sputter 200 nm Au

(a) Ti Ar=42 sccm 3.8mT 150W 150s
(b) Au Ar=42 sccm 3.8 mT 150W 400s
(c) Ti Ar=42 sccm 3.8mT 150W 150s
A.10 Seed Layer Release Hole Etch

1. Pattern S1813
   
   (a) Spin=3000 rpm, acc=35, time=45s  
   (b) Bake, expose, develop in Microdev:DI 1:1 as usual

2. Seed layer etch
   
   (a) 9s in HF 15:1 DI (HF 10:1 DI could make SAC layer peel off.)  
   (b) Gold Etchant for ~20-25s  
   (c) 9s HF 15:1 DI

3. Remove S1813
   
   (a) 50s flood exposure  
   (b) 30s in Microdev:DI 1:1

A.11 First Au Electroplating

1. Pattern 12 um SPR-220-7 mold
   
   (a) 2 step recipe  
       
       i. Spin=500 RPM, acc=500 rpm/s, time=10s  
       ii. Spin=1700 RPM, acc=1000 rpm/s, time=40s
   
   (b) 60 C/30s on hot plate then ramp up to 105 C and stay for 5 min in total  
   (c) Leave overnight  
   (d) Use edge bead mask to expose for 120s, develop in Microdev:DI 1:1 for 90s  
   (e) Align and expose for 25s  
   (f) Leave overnight  
   (g) Develop in Microdev:DI 1:1 for 120s
(h) Measure thickness with Dektak

2. Electroplating 7.5 um Au

(a) Asher 100 W/200 mT for 1 min
(b) 9s in HF 15:1 DI
(c) Stabilize solution @ 55C for 1 hr, stir @ 200 rpm
(d) Use test slide to measure plating rate. Should be ~2um/30 min
(e) Do 4 steps of plating, rotate to 4 edges, check thickness every time.

3. Remove mold

(a) Flood Expose 200s, develop in Microdev:DI 1:1 for 120s

4. Inspect and Dektak

A.12 Second Au Electroplating

1. Pattern 12 um SPR-220-7 mold

(a) 500 RPM for 10s, ACCL=500 rpm/s
(b) 1000 RPM for 40s, ACCL=1000 rpm/s
(c) 5min @ 90 C on hot plate then 55 min @ 90C in the Brewer oven
(d) Leave overnight
(e) Use edge bead mask to expose for 200s, develop in Microdev:DI 1:1 for 180s
(f) Align and expose for 25s
(g) Leave overnight
(h) Develop in Microdev:DI 1:1 for 130s
(i) PR edge goes up with the first plated gold. Take a long scan to measure PR far away from plated gold.
2. Electroplating 7.5 um Au
   (a) Asher 100 W/200 mT for 1 min
   (b) Stabilize solution @ 55C for 1 hr, stir @ 200 rpm
   (c) Use test slide to measure plating rate. Should be ~2um/30 min
   (d) Do 4 steps of plating, rotate to 4 edges,
   (e) Check thickness every time. Gold roughness goes up to 1um in the second plating. Measure a long structure to take average.

3. Remove mold
   (a) Flood Expose 200s, develop in Microdev:DI 1:1 for 140s

4. Inspect and Dektak

A.13 Seed Layer Etch

1. Pattern S1813
   (a) Bake, expose, develop in Microdev:DI 1:1 as usual

2. Over Develop S1813
   (a) Spin=3000 rpm, acc=35, time=45s
   (b) 105C/120s bake
   (c) 15s over dose
   (d) Develop in Microdev:DI 1:1 45s

3. Over etch seed layer
   (a) Asher 200 W/200 mT for 2 min
   (b) 9s in HF 15:1 DI
   (c) Gold Etchant for ~50S over etch
(d) 9s in HF 15:1 DI

4. Remove S1813
   
   (a) 50s Flood exposure
   
   (b) 30s in Microdev:DI 1:1

5. Rinse and N2 gun dry

6. Save Veeco measurement as the pre-released profiles

A.14 Release

1. Release in 1165 remover
   
   (a) Soak wafer in 1165 @ 85C stir @100 rpm for 30 min, pick out debris released from wafer edge
   
   (b) Move to new 1165 remover, leave over night
   
   (c) Transfer the wafer into the holder in clean DI water, keeping meniscus. Use the holder to transfer wafer between fresh DI water 2 more times.

2. Etch Ti
   
   (a) Use the holder to transfer the wafer into HF 10:1 DI 7s
   
   (b) Transfer wafer into fresh DI water
   
   (c) Transfer wafer between fresh DI water 2 more times.

3. CPD
   
   (a) Use methanol, purge time 15 min
   
   (b) If CPD is down, move wafer back to methanol. Never leave the wafer in DI water for long time. HF residual will etch Ti adhesion layer and destroy everything.
Bibliography


