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Design of Millimeter-Wave Power Amplifiers in Silicon

A dissertation submitted in partial satisfaction of the requirements for the degree Doctor of Philosophy in Electrical Engineering (Electronic Circuits and Systems) by Nader Kalantari

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2013
The dissertation of Nader Kalantari is approved, and it
is acceptable in quality and form for publication on mi-
crofilm and electronically:

Chair

University of California, San Diego

2013
DEDICATION

To my wife,
Donna
"I shall be telling this with a sigh
Somewhere ages and ages hence:
Two roads diverged in a wood, and I
I took the one less traveled by,
And that has made all the difference."

—Robert Frost
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PUBLICATIONS


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ABSTRACT OF THE DISSERTATION

Design of Millimeter-Wave Power Amplifiers in Silicon

by

Nader Kalantari

Doctor of Philosophy in Electrical Engineering (Electronic Circuits and Systems)

University of California, San Diego, 2013

Professor James F. Buckwalter, Chair

The first part of this dissertation focuses on the millimeter-wave power amplifiers in silicon where both switching and linear power amplifiers were investigated. In Chapter 2, a Q-band, Class-E power amplifier has been designed and fabricated in a 120 nm SiGe BiCMOS technology. The amplifier was designed for high output power using on-chip power combining networks. It operates respectively from a 1.2 V supply for peak efficiency and a 2.4 V supply for maximum power and occupies an area of 0.801 $mm^2$. A peak PAE of 18% is measured for an output power of 11.3 dBm at 45 GHz and a maximum of 19.4 dBm is measured at 42 GHz with a PAE of 14.4%. The power amplifier operates from 42 to 50 GHz. Chapter 3, presents a W-band, tapered constructive wave power amplifier
(TCWPA) that has been designed and fabricated in a 120 nm SiGe BiCMOS technology. The amplifier has a 3 dB bandwidth of 19 GHz from 91-110 GHz and a maximum gain of 12.5 dB at 101 GHz. At 98 GHz, OP1dB is 4.9 dBm. At 97 GHz, saturated output power is 5.9 dBm and the PAE is 7.2%. The amplifier operates from a 2.4 V supply and occupies an area of 0.22 $mm^2$. A novel circuit topology for power amplifier was introduced in Chapter 4 where only one network is used to provide both input and output matching. This new topology incorporates a feedback network around the transistor to satisfy matching requirements. Circuit parameters can be tuned for small- and large-signal circuit operation. The power amplifier is fabricated in a 120 nm SiGe BiCMOS process and performs from 36 to 41 GHz. The PA achieves a saturated output power of 23 dBm and a peak power added efficiency of 20% at 38 GHz.

The second part of this dissertation focuses on the performance analysis of phase-interpolated dual loop clock and data recovery. It presents a four channel receiver for high-speed signal conditioning. Each channel consists of a continuous time linear equalizer (CTLE) and a dual loop CDR with phase-interpolator. All channels share a single PLL that generates and distributes quadrature clock phases to each CDR for data recovery. Clock amplitude, phase integral non-linearity (INL) and phase differential non-linearity (DNL) are derived for IQ phase error and predict phase-dependent jitter contributions to the recovered clock. The multilane receiver was designed in 130 nm CMOS technology. The die occupies an area of 1930 $\mu m$ by 1250 $\mu m$ and consumes 67.9 mW per channel. It achieves a maximum data rate of 7 Gbps per channel for 0 and $\pm 200$ ppm clock frequency deviation. Quadrature clocks are used in locking mechanism of phase-interpolated CDRs. Due to circuit non-idealities, any mismatch in the quadrature phase causes jitter increase and ultimately increase of bit error rate. The material is presented in Chapter 5.
Chapter 1

Introduction

1.1 Millimeter-Wave Power Amplifier

Today, we all are swimming in an ocean of electromagnetic waves. Wireless LANs, cellular phones, cordless phones, satellies and many more wireless systems are transmitting electromagnetic signals from tens of meters to hundreds of miles. For each of the above cases, there is one block in the transmitter that defines the range of signal travel. That is the Power Amplifier. Figure 1.1 shows a few wireless applications. The required output power of the PA varies from tens of milli-Watts to hundreds of Watts.

While the history of power amplifiers shows they were mainly built based on III-V materials such as Gallium Arsenide (GaAs), Indium Phosphide (InPh) or Gallium Nitride (GaN), the advancement in Silicon/Silicon Germanium (SiGe) processes has encouraged design engineers to implement millimeter wave radio frequency integrated circuits (RFICs) in silicon. The high speed of SiGe process, $f_t$ and $f_{max}$ of 220 and 250 GHz along with the integration capability with digital baseband has made it quite popular in the last decade [1–4].

Two design challenges have arisen for silicon-based mm-wave power amplifiers (PAs). First, the measured efficiency of mm-wave PAs in Si/SiGe processes has remained relatively low (~ 20%). While amplifier classes exist that demonstrate extremely high efficiency at low-frequency, monolithic amplifiers above X-band (7-12 GHz) have not delivered performance at the theoretical efficiency limits.
Figure 1.1: The range of output power of a PA can vary from tens of milli-Watts to hundreds of Watts depending on the application.

Switching amplifiers, particularly class-E output networks, have been investigated using a 120-nm SiGe heterojunction bipolar transistor (HBT) [5] [6]. While [5] presents the highest power added efficiency (PAE) of 20.9%, saturated output power ($P_{sat}$) is limited to 11.5 dBm (14.1 mW). It has been suggested that the nonlinear device modeling is limited at high frequency and circuit performance is severely impacted by passive losses and parasitic elements, e.g. emitter or source inductance [7]. Work in CMOS has shown PAE above 20% but typically at lower output power [8] [9] [10].

Secondly, Si/SiGe mm-wave PAs offer limited output power. The 120-nm SiGe HBT has a collector-emitter breakdown voltage ($BV_{CEO}$) of 1.7 V. This breakdown voltage is much lower than Indium Phosphide or Gallium Nitride, but the output power can be increased through the use of on-chip or off-chip power


combining. High power SiGe results have shown a saturated output power of 20 dBm (100 mW), but the PAE is limited to 12.7% [11]. To circumvent the power handling limitations, on-chip combining networks, such as the distributed active transformer (DAT), have been proposed to reach a maximum $P_{sat}$ of 23 dBm (200 mW) but at a PAE of 6.4% [12]. These results have indicated trade-offs between power handling and power added efficiency. Power combining approaches suffer from passive losses at high-frequency. Recently, output power and efficiency reaching 20 dBm (100 mW) and 20% have been demonstrated through the use of slow-wave transmission lines, which reduce the combiner losses [13]. The next section goes over some fundamentals of power amplifiers.

1.1.1 Power Amplifier Overview

Figure 1.2 shows a block diagram of a standard monolithic wireless system. On the receiver (RX) side, the signal is received and delivered to the Low Noise Amplifier (LNA) through the antenna. Then a mixer demodulates the signal to Intermediate Frequency (IF) by multiplying it with a Local Oscillator (LO) generated from a Phase Locked Loop (PLL). The output is then filtered and and sent to an Analog-Digital Converter (ADC) to be sampled. The digital data is then provided to the digital baseband for processing. On the transmitter (TX) side, the opposite procedure is done by converting a digital baseband signal to analog through a Digital-Analog Converter (DAC). Then the signal is filtered. Modulation to RF frequency is done by multiplying it with the LO signal. The RF signal is then powered by a pre PA and finally a PA to be transmitted through the antenna.

![Block diagram of a wireless system](image)

**Figure 1.2:** Block diagram of a wireless system. The power amplifier gets a great deal of attention from the power consumption point of view.
Among all the sub-blocks in a wireless transceiver, the power amplifier receives a great deal of attention since PAs are the major power consumer block in any wireless transceivers.

**Power Amplifier Figures of Merit**

In the world of power amplifiers there are a few major Figures of Merit (FoM). The power amplifier block in Figure 1.2 can be presented as a lossless PA plus input, output, DC and loss power associated with it. The power elements are used to define the following FoM:

- **Efficiency**: \( \eta = \frac{P_{out}}{P_{dc}} \)
- **Gain**: \( G = \frac{P_{out}}{P_{in}} \)
- **Power Added Efficiency**: \( PAE = \frac{P_{out} - P_{in}}{P_{dc}} \)
- **Saturated output power**: \( P_{sat} \)
- **1dB compression power**: \( P_{1dB} \)

The saturated output power is the maximum power a power amplifier can deliver. The 1dB compression power is the power when PA gain is dropped by 1dB. The rest of the FoMs are self descriptive.

Sources of loss in power amplifiers are mainly the active device power dissipation and the loss in the passives elements. Based on energy conservation, \( P_{in} + P_{dc} = P_{out} + P_{loss} \). Thus, a lossless PA converts all the energy to the desirable output power. Ideally, if \( P_{loss} \to 0 \) then the \( \eta \to 100\% \) and as \( G \to \infty \), \( PAE \to \eta \). Therefore, minimizing the sources of loss and maximizing the gain of a power amplifier is the main agenda for a PA designer.

Efficiency of a power amplifier is by far the most important FoM of a PA for two reasons. First off, for portable applications such as cellular phones, wireless tablets and PDAs the battery life is directly affected by the efficiency of the PA. Second, a low efficiency PA burns more power in the form of generated heat in the
active device. The high temperature needs to be cooled down. This requires mechanical consideration for better heat transfer and comes with extra cost. On the other hand, the performance of a wireless unit is reduced at high temperature. Low mobility, higher resistance and higher noise power are the penalties that come at the presence of high temperature. For application in which battery life is no of concern (e.g. Cellular tower PA), the lack of efficiency mainly tackles the performance of the system by the generated heat.

**Power Amplifier Classes**

Power amplifiers are categorized into two main classes, linear and switching. Class A, B, AB and C are among the linear PAs whereas class D, E and F belong to the switching one. As it can be predicted, the linear PAs are supposed to amplify the input signal and keep its shape with minimum distortion. They are used in M-ary constellations where both amplitude and phase are used to define a symbol such as 16-quadrature amplitude modulation (QAM), 64-QAM, etc. The linearity is quite important for application such as OFDM where the peak-to-average ratio of the input signal is quite high. That means the PA should handle a relatively high input signal and still does not go to compression although the majority of the time the input signal has much less magnitude.

The switching PAs on the other hand are suitable for constant envelope modulations such as frequency shift keying (FSK), phase shift keying (PSK), quadrature phase shift keying (QPSK) and on-off keying (OOK). The main advantage of switching PAs are their high efficiency. They theoretically can reach to 100% efficiency. However, unlike the linear PAs, they are not capable of transmitting M-ary signals. That means their throughput is less than the linear PAs. Some techniques such as out-phasing has been introduced to linearize switching PAs [14]. Table 1.1 shows the theoretical efficiency of some of the linear and switching PAs.

**Conjugate Match versus Load-Line Match**

To deliver the maximum power to a load from a source, the load and source impedance must be complex-conjugates of each other. This is a well-known theo-
Table 1.1: Type and maximum efficiency of some popular power amplifier (PA) classes.

<table>
<thead>
<tr>
<th>Class</th>
<th>A</th>
<th>B</th>
<th>AB</th>
<th>D</th>
<th>E</th>
<th>F</th>
</tr>
</thead>
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<tr>
<td></td>
<td>Linearity</td>
<td>Linear</td>
<td>Linear</td>
<td>Switching</td>
<td>Switching</td>
<td>Switching</td>
</tr>
<tr>
<td>Efficiency</td>
<td>50</td>
<td>78</td>
<td>50 ≤ η ≤ 78</td>
<td>100</td>
<td>100</td>
<td>100</td>
</tr>
</tbody>
</table>

rem in the circuit theory. However, the above quote does not consider any physical limitation on the source [15]. For example, consider the current generator in Figure 1.3. Assume it has an $I_{\text{max}} = 1 \, \text{A}$ and an impedance of 50 Ω. To deliver the maximum power based on the conjugate match, the load impedance must be 50 Ω too. This means the overall voltage at the generator is 25 V. This voltage of course exceeds the breakdown voltage of most of the RF power devices.

The loadline approach, on the other hand, takes into account the maximum allowable voltage and current from a generator. The minimum and maximum voltage and current range then defines the power triangle shown in Figure 1.3. This is indeed the maximum power that can be achieved from a generator. The optimum load is defined in equation 1.1. The matching techniques are then used to match the $R_{\text{opt}}$ to a 50 Ω impedance.

![Power Triangle](image)

Figure 1.3: Conjugate match versus loadline match. The maximum allowable voltage and current of a generator and the power triangle.
Figure 1.4: Class-E power amplifier circuit. The smart choice of slightly inductive resonant circuit makes the switch node voltage zero at the switching time. This results in zero switch power loss.

\[ R_{opt} = \frac{V_{max} - V_{min}}{I_{max} - I_{min}} = \frac{V_{max} - V_{knee}}{I_{max}} \]  

(1.1)

1.1.2 Wilkinson Power Combined Class-E

Among the switching power amplifiers, class-E got quite of attention in early 1970s [16]. Figure 1.4(a) shows the circuit of a class-E PA. The smart choice of \( C_s \) and slightly inductive tuned LC tank make the voltage at the switch node equal to zero at the switching time. To ensure %100 efficiency, the slope of the switch node voltage needs to be zero at the switching time too. Therefore, there will be no discharge of \( C_s \) at the switching time and as such no power dissipation from the switch. Consequently all the DC energy is converted to the RF fundamental frequency and 100% efficiency is achievable.

While Class-E operation offers high efficiency, theoretically up to 100%, harmonic control is limited at millimeter-wave frequencies and the ideal zero-voltage switching waveforms are only approximated in the tuning of the class-E amplifier [16]. This is demonstrated in Figure 1.4(b) where the actual current and voltage of the switch show some overlap and as such power loss.
Recent work has demonstrated Class-E operation at V-band with Silicon Germanium (SiGe) Heterojunction Bipolar Transistors (HBT) [5]. Other recent work demonstrates high output power using SiGe HBT power amplifiers [11] [7] [2]. Efforts in CMOS process have realized similar efficiency but suffer from lower saturated output power [8].

Emitter scaling of heterojunction bipolar transistor (HBT) devices offers higher $f_T$ at the expense of lower breakdown voltage. At RF frequencies, a single stage Class-E PA operating at 5 GHz has achieved an output power of 19.7 dBm (93.4 mW) and peak PAE of 43.6% [17]. However, efficiency exceeding 25% PAE is a barrier at mm-wave bands because of low quality factor of passive elements and the available gain at harmonics of the RF frequency.

A Wilkinson power splitter/combiner is a passive circuit that splits its input power into two equal power outputs with the same phase. Similarly, it combines two equal phase input signals and provides twice of power in its output. A detail explanation of the functionality of Wilkinson power combiner/splitter is provided by Pozar [18]. Chapter 2 of this dissertation presents a Wilkinson power combined class-E PA in SiGe process. The PA achieves a $P_{sat}$ of 19.4 dBm (87 mW) at 42 GHz with a PAE of 14.4%. That was the highest reported output power at Q-band for a Class-E PA in SiGe when published.

1.1.3 Traveling Wave Power Amplifier

Linear power amplifiers (PAs) at millimeter-wave (mm-wave) frequencies exhibit lower output power and efficiency in silicon technologies. Recent work in SiGe has demonstrated the capability of high-speed HBT devices to generate significant millimeter wave power for automotive radar and communications applications [2,19-21]. W-band applications for imaging and point-to-point communication could offer new platforms for SiGe transceivers where the fully integrated solutions offer advantages over III-V technologies [21].

Conventional W-band amplifiers are mainly either cascaded narrowband [22] or distributed wideband [23]. The former approach can achieve low noise figure and high gain while the latter one provides a much wider bandwidth. Similar
to small signal amplifiers, power amplifiers are shown in cascaded form [2] [21] or distributed format [24] at W-band. Buckwalter and Kim presented the first travelling wave amplification in SiGe in 2009 [25]. The architecture of their work is based on constructive forward wave and destruction of reflected power. This makes the signal amplified as it travels through the chain of amplifier stages. Chapter 3 of this dissertation is focused on a modified version of the traveling wave amplifier presented in [25]. By applying a tapered resistive feedback in the amplifier chain, higher linearity and saturation power were achieved. Figure 1.5 shows the architecture of a tapered constructive wave power amplifier.

Figure 1.5: A tapered constructive wave power amplifier architecture.

1.1.4 Nested Reactance Feedback Power Amplifier

The most important contribution of this dissertation is presented in Chapter 4 where a new class of power amplifier is invented. It provides a different approach for matching and delivering power to a load. As shown in Figure 1.6 the conventional power amplifiers use input and output matching network while this newly invented PA only uses one matching network for both input and output.

Figure 1.7 shows a parallel LC tank and the idea of newly designed PA. The novelty comes by inserting an active device in a parallel $LC$ tank. While
**Figure 1.6:** (a) Conventional PA matching (b) A nested reactance feedback matching

**Figure 1.7:** (a) Parallel LC tank shows open at $\omega_o = \frac{1}{\sqrt{LC_{eff}}}$ (b) The NeRF PA provides a matched network at $\omega_o$. The return loss and isolation are minimized while the forward gain is maximized.

the parallel $LC$ is open at the tuning frequency of $\omega_o = \frac{1}{\sqrt{LC_{eff}}}$, ironically, the presence of the transconductance cell in the loop minimizes its return loss and isolation while maximizing its gain at the tuned frequency of $\omega_o$. This behaviour is indeeded shaped by the feedback capacitance across the transconducatnce cell and the $LC$ tank. Thus, the power amplifier is named *Nested Reactance Feedback Power Amplifier*. The PA, also, takes advantage of the device input capacitance (e.g. $C_\pi$) by creating a dynamic feedback through $C_i$ and $C_\pi$. This prevents the device of going to early compression and providing its maximum PAE near to its maximum saturated output power. A comprehensive analysis along with the simulated and measured results are provided in Chapter 4.
1.2 Multi-Channel Gigabit Clock and Data Recovery

The last part of this dissertation focuses on the high speed multi-channel serial links. The increase demand for applications such video streaming, internet, cloud storage or cloud computing comes with a thirst of higher data rate at the data centers. While at the end user data rates falls into tens or hundreds of megabits per second, at the server side it goes as high as hundreded of gigabits per second. Thus transferring and recovering the data at the enterprise side requires much faster speed. Figure 1.8 shows a block diagram of a data center with gigabit serial links.

![Figure 1.8: Simplified model of gigabit Ethernet data switching at data centers. Picture courtesy of Cisco.](image)

Low energy demands of high-speed serial links place severe constraints on circuit architectures. Input/output (I/O) pin limits compel higher per-pin data rates and clock and data recovery (CDR) is required for each link. However, higher rates require equalization and hence power consumption to overcome channel losses [26,27]. Conventional CDR circuits are based on a phase-locked loop (PLL) which includes a phase detector, a charge pump, a low pass filter and a voltage controlled oscillator (VCO) [28]. The CDR VCO generates a clock at the data rate from the
recovered data sequence [29]. Higher data rates suggest higher VCO frequency and faster phase detectors are necessary unless half-rate or quarter-rate phase detectors are used [30,31].

A dual-loop phase interpolator (PI)-based CDR has been suggested to avoid the need for PLLs at each pin [32,33]. A single PLL generates a clock with quadrature phases that are distributed to each channel. The quadrature phases are introduced to a local phase interpolator that creates the optimal sampling phase for data recovery. A single VCO prevents coupling between separate CDR circuits and reduces the overall power consumption [34,35]. Figure 1.9 shows the block diagram of a multilane channel receiver based on dual-loop CDR.

The dual-loop PI-based CDR faces the design challenge of creating quadrature phases. One approach is to generate a clock at twice the data rate and divide the VCO by two to generate quadrature clock phases known as IQ phases. However, multi-gigabit-per-second data rates require a VCO at twice of data rate frequency. Alternatively, multi-stage ring oscillators produce multiple phases but suffer from poor phase noise [29,36]. Finally, injection locking of two LC VCOs both operating at the data rate creates I and Q phases at the expense of higher area [37]. Due to circuit non-ideality, a phase mismatch exists between the multiple clock phases that degrades data recovery. To avoid the IQ phase mismatch, the phase interpolator can be inserted inside the PLL loop [36]. However, this does not allow sharing the PLL among multiple CDR blocks. A phase mismatch detection and compensation circuit has been presented [38]. Another approach to minimizing the phase mismatch includes Vernier phase shifter circuits implemented with an N-phase PLL and M-step phase interpolator to increase the overall resolution to NxM at the expense of higher power consumption [39].

While solutions have been proposed for clock IQ mismatch and duty cycle distortion (DCD), prior work has not discussed the precise IQ phase mismatch and phase interpolator linearity required to achieve an acceptable bit error rate (BER). The last major contribution of this dissertation is presented in Chapter 5. It presents a jitter analysis in the presence of both these impairments and verifies experimentally the phase-dependent jitter generation and BER degradation.
1.3 Dissertation Organization

The background material for mm-wave power amplifier and gigabit serial link is presented in Chapter 1.

In Chapter 2, a Q-band Wilkinson power combined class-E power amplifier has been designed and fabricated in a 120 nm SiGe BiCMOS technology. The amplifier was designed for high output power using on-chip power combining networks. The design approach is based on distributed matching using the short and open stub transmission lines. The PA operates respectively from a 1.2V supply for peak efficiency and a 2.4 V supply for maximum power and occupies an area of 0.801 \( mm^2 \). A peak PAE of 18\% is measured for an output power of 11.3 dBm (14.1 mW) at 45 GHz and a maximum \( P_{sat} \) of 19.4 dBm (87 mW) is measured at 42 GHz with a PAE of 14.4\%. The power amplifier operates from 42 to 50 GHz. The material of Chapter 2 was originally published in [6].

Chapter 3 goes over the design and analysis of a W-band, tapered constructive wave power amplifier (TCWPA). The PA was designed and fabricated in a
120 nm SiGe BiCMOS technology. The amplifier has a 3 dB bandwidth of 19 GHz from 91-110 GHz and a maximum gain of 12.5 dB at 101 GHz. At 98 GHz, $OP_{1dB}$ is 4.9 dBm (3.1 mW). At 97 GHz, $P_{sat}$ is 5.9 dBm (3.9 mW) and the PAE is 7.2%. The amplifier operates from a 2.4 V supply and occupies an area of 0.22 mm$^2$.

The material of Chapter 3 was originally published in [40].

A newly invented class of power amplifier is presented in Chapter 4. It incorporates a feedback network around the transistor to satisfy matching requirements. Circuit parameters can be tuned for small- and large-signal circuit operation. The PA is fabricated in a 120 nm SiGe BiCMOS process and performs from 36 to 41 GHz. The PA achieves a saturated output power of 23 dBm (200 mW) and a peak power-added efficiency of 20% at 38 GHz. This is the highest reported output power from a single PA at $Q$-band in silicon. The material of Chapter 4 was originally published in [41].

Chapter 5 presents a jitter analysis of clock non-idealities and phase interpolator linearity in dual-loop CDRs. Clock amplitude, phase integral non-linearity (INL) and phase differential non-linearity (DNL) are derived for $IQ$ phase error and indicate phase-dependent random and deterministic jitter contributions to the recovered clock. Therefore, the BER will also demonstrate phase-dependence in dual-loop CDRs. A phase interpolator-based CDR was designed and implemented in 130 nm CMOS technology. Four receive equalizers and four CDRs are implemented that share a common PLL. The die measures 1930 $\mu$m by 1250 $\mu$m and consumes 122 and 86.5 mW per channel with and without equalizers. It achieves a maximum data rate of 7 Gbps per channel for 0 and $\pm$200 ppm clock frequency deviation.

Chapter 6 concludes this dissertation with suggestions for the future work on the mm-wave power amplifier design and giga bit serial links.
Chapter 2

A Wilkinson Power-Combined Q-Band Class-E Power Amplifier

2.1 Circuit Design

Fig. 2.1 illustrates the proposed Class-E power amplifier consisting of two parallel stages with Wilkinson power splitters and combiners at the input and output of the amplifier. One drawback of Class-E operation is the peak collector voltage swing, which ideally exceeds four times the supply voltage and impacts the long-term device reliability. This letter examines increasing the total output power while subjecting the collector of each HBT to a lower voltage swing. Since the power gain along each arm is in-phase, the Wilkinson power combiner offers low insertion loss. Nonetheless, the insertion loss of the on-chip power combining networks degrades the overall PAE. In this design, the simulated Wilkinson power combiner has an insertion loss of 0.6 dB.

The on-chip power combiners and matching networks are implemented using shielded microstrip transmission lines to isolate high-frequency electric fields from the substrate and prevent potential instability. The design of the input matching network at 45 GHz is shown in the Smith chart of Fig. 2.1. The transistor base (1) is matched through a 230 $\mu$m short stub (2), a 155 $\mu$m transmission line (3), and a 150 $\mu$m open stub (4) to a 50 $\Omega$ input source. The output matching network
consists of a transmission line inductor for collector biasing, a 1 pF series Metal-Insulator-Metal (MIM) capacitor at the collector of the transistor, and a 250 $\mu m$ transmission line to resonate with the series capacitor. Biasing transmission lines are bypassed with 30 pF MIM capacitors optimized for high self resonant frequency. The proposed output matching network differs from previous work where the series capacitor is not present [5].

To deliver a peak power of 20 dBm at 45 GHz into a 50 $\Omega$ load from a supply voltage of 1.2 V, the collector DC current must reach 42 mA. We chose a total emitter length of 42 $\mu m$ (3x14 $\mu m$ devices) to achieve the maximum device $f_T$ at a collector current of 40 mA. The $f_T$ is anticipated to be at least 176 GHz for collector currents between 17 mA and 70 mA.

For Class-E operation, bounds exist on the collector parasitics for peak collector efficiency. An optimal collector-substrate capacitance, $C_{cs}$, is a function
of frequency of operation, output power, and the supply voltage, $V_{CC}$.

$$C_{cs} = \frac{P_{out}}{\left(\pi \omega V_{CC}^2\right)}$$

(2.1)

Under the design goals, the required $C_{cs}$ is 39 fF and is slightly lower than the collector parasitics of an HBT with emitter length of 42 $\mu$m. Larger $C_{cs}$ increases the switching time and degrades the PAE but has the advantage of also lowering the peak collector voltage. However, increasing the supply voltage permits higher output power for a given $C_{cs}$. For instance, the output power is quadrupled when the supply is doubled. For this reason, the PA was tested for high efficiency at a supply voltage of 1.2 V and high power for a supply voltage of 2.4 V.

The disadvantage of applying a higher collector voltage is the potential for device breakdown. The 0.12 $\mu$m SiGe HBT breakdown voltage is $\sim 1.7$ V with an open base and $\sim 5$ V with a shorted base. If the base of the HBT is biased from a relatively low impedance voltage source, the swing at the collector at a 2.4 V supply can be withstood. At Q-band, the impedance seen looking from the base into input matching network is 10 $\Omega$. This relatively small impedance implies that the actual breakdown voltage is closer to 5 V and, consequently allows for higher collector bias voltage.

Fig. 2.2 shows the simulated collector voltage and current at 45 GHz for peak efficiency. The peak collector voltage is 1.8 V for a supply voltage of 1.2 V. The peak collector voltage coincides with zero collector current and the peak collector current coincides with minimum collector voltage. The simulated peak power added efficiency of the dual Class-E amplifier is 19.6% at an output power of 14.2 dBm when biased with a 1.2 V supply.

## 2.2 Measurement Results

The PA has been fabricated in a 0.12 $\mu$m SiGe BiCMOS technology. The micrograph is shown in Fig. 2.3 and measures 1.08 mm x 0.740 mm, including pads.

The original layout of the active device was done by a straight stack of metal layers on top of each other. This, however, caused increase of parasitic capacitance
Figure 2.2: Simulated collector voltage and current of the Q-band Class-E PA.

between the base-emitter and base-collector nodes. To tackle this issue, a stairway-style layout was approached where the parasitic capacitances were almost cut in half. Figure 2.4 shows the original and modified active device layout respectively. The post layout extracted capacitances for \( C_{be} \) and \( C_{bc} \) were measured about 60 fF for the original layout shown in Figure 2.4(a). This value dropped to 32 and 29 fF for \( C_{be} \) and \( C_{bc} \) respectively in the modified layout shown in Figure 2.4(b).

Small and large signal characteristics of the PA were measured at room temperature. \( S \)-parameters were measured with an Agilent E8361A Network Analyzer (PNA). The base bias voltage was introduced through the input RF pad using the PNA bias tee. The measured \( S \)-parameters are plotted in Fig. 2.5 and demonstrate a peak single stage gain of 6 dB at 42 GHz from a collector bias voltage of 1.2 V. Both input and output return loss are better than 10 dB between 42 to 50 GHz. The measured isolation is better than 20 dB. The measured and simulated \( S \)-parameters illustrate reasonable agreement for the gain of S21.

Large signal characterization of the PA was measured with an Agilent E8257D Signal Generator (PSG) delivering a maximum 14 dBm at frequencies higher than 30 GHz. However, semi-rigid cables between the PSG and RF probes introduced 7 dB of loss. An additional 4 dB insertion loss was introduced by the bias tee and the RF probe. Finally, the on-chip Wilkinson power splitter reduces
the power available at each amplifier by 3.6 dB. Therefore, roughly 0 dBm of RF power is available at the input of each Class-E PA and is not sufficient to completely switch the HBT device. An external Q-band PA increases the available RF power to compensate for the test cable losses [42]. To calibrate the power measurement, the overall loss was measured between 40 and 50 GHz and the total loss before and after the DUT is calibrated for all power measurements. An Agilent E4448A Spectrum Analyzer (PSA) measures the DUT output power.

Two conditions for collector voltage were studied: 1.2 V for maximum PAE and 2.4 V for a maximum output power. Fig. 2.6 plots the PAE and saturated output power for these two conditions from 40 to 50 GHz. At Vcc = 1.2 V, the PAE is at least 14% from 42 to 50 GHz with a maximum PAE at 45 GHz. At Vcc = 2.4 V, the output power is higher than 18 dBm from 41 to 45 GHz.

Fig. 2.7 plots the gain, output power and PAE with the collector biased at 2.4 V. The maximum saturated output power is 19.4 dBm at 42 GHz. At an output power of 18 dBm, the PAE peaks at 14.4%. The 1 dB gain compression occurs at 16.4 dBm.

Figure 2.3: Micrograph of the PA. The size is 0.801 mm² including pad area.
Figure 2.4: (a) Original active device layout comes with big capacitances between the metal layers. The extracted $C_{be}$ and $C_{bc}$ were measured 60 fF. (b) The modified layout with a stairway-style reduced the parasitic capacitances by almost a factor of 2, measuring a $C_{be}$ and $C_{bc}$ of 32 and 29 fF respectively.

Fig. 2.8 plots the gain, output power and PAE with the collector biased at 1.2 V. The maximum PAE is 18% at an output power of 11.3 dBm at 45 GHz. As anticipated, higher efficiency is achieved from the lower bias.

If the insertion loss of the power combiner and splitter are taken into account, the PAE of each on-chip Class-E amplifier can be determined. The 0.6 dB loss for each combiner and splitter suggests that the PAE of each Class-E PA was 19.8% at 42 GHz and 22% at 45 GHz. These results are compared in Table 2.1 against published Q- and V-band Silicon/Silicon Germanium Power Amplifiers. While [5, 8] demonstrate the highest PAE at around 20%, they also do not offer output power higher than 11.5 dBm [5]. We found the extracted PAE for each on-chip PA to match this prior work. [2, 11] have reported power exceeding 18 dBm but the PAE of these designs is limited to 12.8% [2] and the output power in [11] was recorded from a 4 V supply. While [2] has 4 stages operating at 77 GHz, this work has a single stage operating from 42 - 50 GHz.

2.3 Chapter Summary

A Q-band Class-E PA in 0.12 $\mu$m SiGe HBT process has been demonstrated with a maximum PAE of 18% at 45 GHz at a 1.2 V supply voltage and a maximum saturated output power of 19.4 dBm at 42 GHz with 2.4 V supply voltage. The
Figure 2.5: Simulated (dashed lines) and measured (solid lines) S-parameters of the PA. The collector bias voltage is 1.2 V.

The extracted PAE for each class-E PA is between 19.8% and 22%.

Acknowledgments

Chapter 2 is mostly a reprint of the material as it appears in IEEE Microwave and Wireless Components Letters, Vol. 20, pp 283-285, May 2010, N. Kalantari; J. F. Buckwalter. This dissertation author was the primary author of these materials and co-author has approved the use of the material for this dissertation.
Figure 2.6: Measured saturated output power and power added efficiency for Vcc of 1.2 V and 2.4 V, respectively.

Figure 2.7: Measured large-signal characteristics of the PA at 42 GHz. Vcc is set to 2.4 V to maximize Pout.
Figure 2.8: Measured large-signal characteristics of the PA at 45 GHz. Vcc is set to 1.2 V to maximize PAE.

Table 2.1: Performance comparison of this work with some recently reported mm-wave power amplifiers.

<table>
<thead>
<tr>
<th>Reference</th>
<th>Frequency</th>
<th>Gain</th>
<th>Psat</th>
<th>PAE</th>
<th>Technology</th>
</tr>
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<tbody>
<tr>
<td>This Work</td>
<td>42-GHz</td>
<td>6-dB</td>
<td>19.4-dBm</td>
<td>14.4%</td>
<td>SiGe 120nm</td>
</tr>
<tr>
<td>This Work</td>
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<td>6-dB</td>
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<td>18%</td>
<td>SiGe 120nm</td>
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<tr>
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<td>11.5-dBm</td>
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<td>SiGe 120nm</td>
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<tr>
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Chapter 3

A 91 to 110-GHz Tapered Constructive Wave Power Amplifier

3.1 Traveling Wave Power Amplifier

The proposed linear-mode, traveling wave power amplifier is shown in Fig. 3.1 and consists of gain stages that are tailored to improve linearity as a signal travels along the transmission line [25]. A tapered approach increases each stages linearity to achieve a higher $OP_{1dB}$. In this section, an analysis of the gain and linearity for each stage motivates the tapered amplifier approach.

3.1.1 Gain Analysis

The proposed traveling wave power amplifier consists of shunt-shunt feedback across a transmission line segment as illustrated in Fig. 3.2 [25]. The feedback at each stage consists of an active circuit which provides a small amount of gain to the forward traveling wave. The feedback stage is constructed with emitter follower and common emitter amplifiers and using HBT devices provides high isolation at high-frequency. A simple model of this feedback circuit incorporates the role of the emitter follower and common emitter as a single transconductance, $g_m$. 

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Figure 3.1: Circuit illustration of a wideband, tapered constructive wave power amplifier.

and transconductance delay, $T_d$, through the active feedback circuit. The feedback voltage gain, $A_v$, is the product of $g_m$ and the transmission line impedance seen at the input of the stage, i.e. $A_v = g_m Z_o/2$.

The frequency response of each stage depends on the phase through the transmission line, $\theta$, and active feedback, $\omega_o T_d$. Constructive interference of the forward traveling wave and destructive interference of the backward traveling wave occur when $\theta + \omega T_d = \pi$ and $\theta - \omega T_d = 0$ and defines the center frequency of the response, $f_o = 1/(4T_d)$ [25]. In the absence of feedback, a forward traveling wave, $V_i^+ \sin(\omega t)$, at the input of each stage appears at the output as $V_o^- \approx \alpha V_i^+ \cos(\omega t)$ where $\alpha$ is the transmission line attenuation. The feedback amplifies the output signal by $A_v$ and adds an additional $90^o$ phase shift before returning this signal to the input traveling wave path, i.e. $V_i^+ \sin(\omega t) + \alpha V_i^+ A_v \sin(\omega t)$. Positive regeneration of the traveling wave suggests that the gain of each amplifier stage is

$$G_{ss} = |S_{21}| = \frac{\alpha}{1 - \alpha A_v}.$$  \hspace{1cm} (3.1)

Positive feedback in each amplifier stage suggests that the feedback gain can be less than one-half. Consequently, the low feedback gain allows for more linearization of the feedback amplifier and locally the feedback voltage gain might be
defined by a linearity constraint.

Figure 3.2: Circuit schematic for a single stage TCWPA decomposed into a small signal and large signal circuit.

3.1.2 Feedback Linearity

While positive feedback adds gain to the traveling wave, local negative feedback is introduced in the active feedback circuit to improve the stage’s linearity and increase the power handling. Since the feedback amplifier shunts the transmission line, the linearity of the proposed amplifier could be higher than the linearity of the feedback circuit. Fig. 3.2 shows the large signal circuit for the proposed TCWPA. For simplicity, the transmission line and feedback are assumed to introduce 90° phase shift in section 3.1.1.

The output current of the feedback circuit is

\[ i_o = g_{m1}v_{be} + g_{m2}v_{be}^2 + g_{m3}v_{be}^3, \]

where \( g_{m1}, g_{m2} \) and \( g_{m3} \) are the first-, second-, and third-order transconductance of the feedback circuit. The 1-dB voltage compression in the linearity of the feedback current response is generally found from

\[ V_{1\mathrm{dB}} = \sqrt{\frac{0.44}{3} g_{m1}^2 g_{m3}}, \]

where the second-order transconductance is ignored (i.e. \( g_{m2} = 0 \)). Introducing emitter degeneration resistance, \( R_F \), increases the negative feedback in the circuit and increases the
linearity of the common emitter transistor at the expense of the transconductance. The effective transconductance in the presence of feedback resistor at the emitter is 
\[ G_{m1} = \frac{g_{m1}}{1 + g_{m1}R_F} \text{ and } G_{m3} = \frac{g_{m3}(1 + g_{m1}R_F) - 2g_{m2}R_F}{(1 + g_{m1}R_F)^3}. \] Neglecting the second-order term, the 1-dB compression point for the feedback improves significantly with the feedback resistance, i.e. \( V_{1dB,f} = V_{1dB}(1 + g_{m1}R_F)^{3/2}. \)

The emitter follower is assumed to have higher linearity than the common emitter stage. Since the emitter follower has an effective feedback resistance of 
\[ R_o = g_m r_{o2} R_E = \frac{V_A}{V_T} R_E \] where \( g_m = \frac{I_C}{V_T} \) and \( r_{o2} = \frac{V_A}{I_C} \), the feedback resistance of the emitter follower should be much larger than the negative feedback introduced in the common emitter stage. If the feedback voltage gain is represented by a Taylor series, \( A_v = A_1 + A_2 v_{be} + A_3 v_{be}^2 \), where \( A_x = \frac{1}{2} G_{mx} Z_o \), the 1-dB compression point of the feedback stage is

\[ V_{1dB,FB} = \sqrt{\frac{0.44 A_1}{3 A_3}}. \]  
(3.2)

As with the discussion of the transconductance, the linearity of the feedback circuit improves as negative feedback is introduced to the transconductance. However, since the feedback circuit is connected as a shunt network across the traveling wave transmission line, the feedback 1-dB compression point does not represent the 1-dB compression point of the amplifier stage.

### 3.1.3 Traveling Wave Amplifier Linearity

The linearity analysis in the previous section applies only to the feedback circuit and not to the traveling wave amplifier stage. Since the distortion is introduced in a shunt interconnection network, distortion (and intermodulation products) generated by the active feedback circuit are added to the input traveling wave and the 1-dB compression point described in (3.2) is not directly applicable.

In Fig. 3.2, the output traveling wave is \( \alpha(V_i^+ - A_1V_o - A_3V_o^3) \) where the second-order nonlinearity is ignored for simplicity. Applying a series reversion to the nonlinear series, the single stage 1-dB compression point is
Consequently, the 1-dB compression point of a single stage can be larger than the 1-dB compression point of the feedback amplifier. In the limit that \( A_1 \to 0 \) (feedback contributes no gain), the 1-dB compression point approaches infinity when \( \alpha = 1 \). The amplifier degenerates to a transmission line which is modeled as perfectly linear.

Fig. 3.3 plots the 1-dB compression point of the feedback amplifier and a single stage of the proposed TCWPA against feedback resistance based on the analysis in (3.3). While the linearity of the proposed traveling wave amplifier can be much higher than the linearity of the active feedback circuit, the improvement in the linearity comes at the expense of the gain. As the gain approaches unity, the benefit of adding amplifier stages is diminished. By tapering the gain and linearity through the feedback resistor, \( R_F \), high gain and low linearity is present in the earlier stages while the low gain and high linearity are provided at final stages of the amplifier.

**Figure 3.3:** Simulations of \( V_{1dB} \) from (3.3) for the feedback circuit and a single stage of the TCWPA \((\alpha = 1, A_2 = 0)\).
3.2 Circuit Design

Fig. 3.1 illustrates the schematic of the proposed constructive wave power amplifier. Eight cascaded stages are used with tapered emitter degeneration resistors. The transistors in the feedback path are not tapered and each has a width of 2.5 $\mu m$. In order to amplify the traveling wave over the quarter-wave transmission line the delay in the feedback path should be equal to quarter of the signal period. However, the additional feedback introduced by the emitter resistor tends to change the feedback delay. In particular, more feedback due to this emitter resistor pushes time constants associated with the base-emitter capacitance of the transistor to high frequencies and reduces this delay slightly. Therefore, while we anticipate that a nominal delay of 2.3 ps is provided when the 2.5 $\mu m$ devices are biased at the peak $f_T$ collector current of 2 mA, the actual feedback delay becomes slightly shorter at each stage along the transmission line.

![Figure 3.4](image.png)

**Figure 3.4:** Spectre simulations of $OP_{1dB}$ and gain for a single traveling wave stage with different $R_F$.

Fig. 3.4 plots the simulated $OP_{1dB}$ and single stage gain, $G_{ss}$, from Spectre based on the VBIC models with respect to the feedback resistor, $R_F$. To achieve the highest linearity for the proposed feedback mechanism, linear tapering is applied to the emitter resistor; the first stage implements an emitter resistor of 50 $\Omega$ and each consecutive stage increases the emitter resistance by 50 $\Omega$. The gain is shown
to decrease exponentially; the gain starts at 2.6 dB at the first stage and concludes at 0.55 dB at the final stage. The cumulative gain of each stage determines the overall amplifier gain. On the other hand, the $OP_{1dB}$ increases from 0 to 8 dBm at the final stage. Additional linearization ($R_F > 400\Omega$) does not suggest substantial improvement to the linearity.

3.3 Measurement Results

The PA is fabricated in a 0.12 $\mu$m SiGe BiCMOS process. The micrograph is shown in Fig. 3.5. The circuit measures 330 $\mu$m by 730 $\mu$m including pads. The nominal bias conditions for the power amplifier include emitter follower biasing for all eight stages with a 2-mA collector current from a 2.4-V supply as well as a 2.4-V supply for the common emitter supply. The total collector current consumption is 20.5 mA.

![Figure 3.5: Micrograph of the TCWPA. The circuit measures 330 $\mu$m by 730 $\mu$m including pads.](image)

Small and large signal characteristics of the PA were measured at room temperature. The measurements were performed with Cascade ACP110-LW GSG probes and the Agilent E8361A two-port network analyzer with N5260A mm-wave controller. The simulated and measured $S$-parameters are plotted in Fig. 3.6 and 3.7. The measured $S21$ demonstrates a peak gain of 12.5 dB at 101 GHz. The 3-dB bandwidth of the amplifier extends from 91 to 110 GHz and demonstrates
a relatively wideband response. The measured isolation is better than 14 dB at 100 GHz. The measured gain and isolation match circuit simulations over the entire W-band. Both measured input and output return loss are better than 10 dB between 75 to 105 GHz. The simulated input and output return loss were found to be pessimistic when compared with the circuit measurement.

![Figure 3.6](image.png)

**Figure 3.6**: Simulated (solid) and measured (dashed) S21 and S12 of proposed W-band TCWPA.

Large signal characterization of the PA was measured with the N5260A mm-wave controller and measured with an Agilent E4419B power meter and a W8486 power sensor. First, the power meter was calibrated while connected to the power sensor. Then, the power sensor was connected to the output of Agilent N5260A millimeter waveguide head. The input power was increased through attenuator control of the waveguide head and the power was recorded for each attenuation level to determine the power delivered to the chip through the 100 GHz probe. Next, the output of the waveguide head was connected to the input of the chip. The procedure was repeated and for each attenuation level the gain was calculated.
from the network analyzer. With the input power and associated gain at each attenuator level, the output power, 1 dB compression point and saturated output power were measured. Fig. 3.8 shows the output power vs the input power at 97GHz. The maximum output power is measured at 5.9 dBm but is limited by the input power from the N5260A mm-wave head.

Fig. 3.9 shows the $OP_{1dB}$ and PAE from 90-110 GHz. The maximum $OP_{1dB}$ is 4.9 dBm at 98 GHz. A maximum PAE of 7.2% and $P_{sat}$ of 5.9 dBm occur at 97 GHz. Notably, the $OP_{1dB}$ is greater than 2.2 dBm from 90-110 GHz. Additionally, the PAE is better than 4% over the entire frequency range.

These results are compared in Table 3.1 against recently published W-band silicon/silicon-germanium power amplifiers. While [21] demonstrate the highest $P_{sat}$ at W-band at 17.6 dBm, this design occupies an area of $2.4mm^2$. The proposed amplifier suggests comparable efficiency at a lower output power and a much smaller circuit area. [44] present higher gain but lower PAE in a 90-nm CMOS sil-
[21] and [2] offer higher output power since each uses larger emitter lengths compared to this work. While [21] & [2] use a total area of 80 µm and 72 µm transistor size, respectively, the emitter width is only 2.5µm. Meanwhile, [2] operates at 77GHz where the MAG is higher than 98GHz.

### 3.4 Chapter Summary

A W-band tapered constructive wave power amplifier is demonstrated in a 0.12-µm SiGe HBT process. The amplifier has a 3-dB BW of 19 GHz at 100 GHz and maximum gain of 12.5 dB at 101 GHz. The PA reaches a $OP_{1dB}$ of 4.9 dBm at 98 GHz. $P_{sat}$ is 5.9 dBm at 97 GHz with a PAE of 7.2%. The compact chip occupies an active area including pads of 0.22 $mm^2$. 

![Figure 3.8](image-url): Measured output power vs input power of the TCWPA at 97GHz. The PA reaches a saturated output power of 6 dBm.
Figure 3.9: Measured power added efficiency (PAE) and $OP_{1dB}$ of the presented W-band TCWPA.

Acknowledgments

Chapter 3 is mostly a reprint of the material as it appears in IEEE BiCMOS Circuits and Technology Meeting, pp 125 - 128, Oct 2010, N. Kalantari; J. F. Buckwalter. This dissertation author was the primary author of these materials and co-author has approved the use of the material for this dissertation.
Table 3.1: Performance comparison of this work with some recently published W-band power amplifiers.

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Chapter 4

A Nested Reactive Feedback Power Amplifier for Q-band Applications

4.1 motivation

This section presents insight into the operation of the nested-reactance feedback amplifier based on a parallel $LC$ tank. Figure 4.1 shows the schematic of a parallel $LC$ tank loaded with a source and load impedance. In this case, the network is only matched at low and high frequency when a short is provided through $L$ and $C$. The parallel $LC$ network is, however, an open at the resonant frequency, $\omega_o = \frac{1}{\sqrt{LC_{eff}}}$. The current through the inductor and capacitor are expressed as $i_L(s) = \frac{V_s}{2Z_o} \cdot \frac{\omega_o^2}{s^2 + 2\zeta\omega_o s + \omega_o^2}$ and $i_C(s) = \frac{V_s}{2Z_o} \cdot \frac{s^2}{s^2 + 2\zeta\omega_o s + \omega_o^2}$, where $\zeta = \frac{1}{4Z_o} \sqrt{\frac{L}{C_{eff}}}$ is the damping factor. At $\omega_o$, both $i_L$ and $i_C$ are simplified to $-j\frac{V_s}{\sqrt{L/C_{eff}}} = -jQ \frac{V_s}{2Z_o}$, where $Q$ is the quality factor of $LC$ tank in parallel with $2Z_o$. Since $i_L(\omega_o) = i_C(\omega_o)$ the input current must be zero. This intuitively makes sense since the LC is open at $\omega_o$ makes $Z_{in} \to \infty$.

The topology of a nested-reactance feedback amplifier is presented in Figure
4.1 and differs because of the transconductance inserted in a series capacitive network formed from a input capacitive divider, $C_i$, a feedback capacitor $C_\mu$, and an output capacitive divider $C_o$. If a minimum transconductance of $g_{m,\text{crit}}$ is applied to the circuit, the following behavior is observed at the resonant frequency, $\omega_o$, where $C_{c_{\text{ef}}} = C_i || C_o || C_\mu$ and $A_v = \frac{C_i}{C_\mu}$ is the feedback gain of the transconductance amplifier.

1. Matching: $Z_{in}(\omega_o) = Z_o$. Instead of seeing open, the input is matched to the output and the input current is $|i_i(\omega_o)| = \frac{V_s}{2Z_o}$.

2. Output Current: The feedback around the transconductance forces the output current of the amplifier to be amplified according to the voltage feedback factor, $|i_o(\omega_o)| = A_v |i_i(\omega_o)|$.

3. Loop Current: The current stored in the $LC$ tank is $|i_L(\omega_o)| = |i_{C_i}(\omega_o)| = |i_{C_\mu}(\omega_o)| = QA_v |i_i(\omega_o)|$, where $Q = \frac{Z_o}{\omega_o L} = \frac{Z_o}{\sqrt{c_{c_{\text{ef}}}}}$. 

To understand the role of the transconductor, the current phasors are presented in Figure 4.2 for each node of the amplifier. At node $V_i$, the transconductor reduces the input impedance as the parallel tank tries to force the current through the inductor and the capacitor to be equal. Consequently, the input current compels a phase shift between $i_L$ and $i_{C_i}$. At resonance, the circuit reactances cancel and the sum of $|i_i(\omega_o)|$ and $|i_o(\omega_o)|$ should be equal to the current added by the transistor, $|i_c(\omega_o)|$. Therefore, the current generated by the transconductor $g_m$ adds to the current generated through the loop and is $(A_v + 1)|i_i(\omega_o)|$. Finally the current in $C_o$, $|i_{C_o}(\omega_o)|$ is sum of $|i_L(\omega_o)|$ and $|i_o(\omega_o)|$ and equal to $\sqrt{1 + Q^2} \cdot A_v \cdot |i_i(\omega_o)|$.

At resonance, the direction of the currents shown in Figure 4.2 indicates that the currents out of the source, into the load, and through the transconductor are in phase while the currents through the reactances $i_L$ and $i_{C_i}$ are $\pm 90^\circ$. Therefore, the phase of $i_{C_o}$ is defined as $\tan^{-1}(-Q)$ since it is sum of a real and an imaginary vector. Two interesting observations are made about this amplifier topology that differs from traditional linear amplifiers. First, the gain is defined by the feedback
capacitance. Secondly, the matching is insensitive to the $Q$ of the $LC$ tank. These observation are detailed analytically in the following section.

![Circuit Diagram](image)

**Figure 4.1**: Comparison of conventional parallel $LC$ tank and nested-reactance feedback amplifier.

### 4.2 Circuit Analysis

Small-signal and large-signal behavior of a nested-reactance feedback power amplifier are explained to develop a trade-offs in the design methodology.

#### 4.2.1 Small Signal Circuit Analysis

Figure 4.3 shows a single stage of a nested-reactance feedback PA and equivalent small-signal circuit model. The feedback capacitor across the transconductor
Figure 4.2: Branch currents in a nested-reactance feedback power amplifier at the resonance.

$g_m$ is denoted $C_\mu$ and incorporates the base-collector capacitance of the device. Input and output capacitors $C_i$ and $C_o$ isolate the device from input and output ports. As explained in Section 4.1, the $LC$ network forms a series parallel tank when $g_m = 0$ with an effective capacitance of $C_{eff} = C_i || C_o || C_\mu$ and resonates at $\omega_o = \sqrt{\frac{1}{LC_{eff}}}$. While this resonance suggests an open looking into the network, this section shows that paradoxically the return losses are minimized when $g_m > g_{m, crit}$.

The detailed development of the $S$-parameters are provided in Appendix A. The $S$-parameters are

$$S_{11} = S_{22} = \frac{-\alpha s^3 + (\beta - LC_i) s^2 + (-\gamma + \frac{L}{Z_o}) s}{\alpha s^3 + \beta s^2 + \gamma s + 1}, \quad (4.1a)$$

$$S_{21} = \frac{1 - LC_i s^2}{1 + LC_i s^2} \frac{(2\beta - LC_i) s^2 + \frac{L}{Z_o} s + 1}{\alpha s^3 + \beta s^2 + \gamma s + 1}, \quad \text{and} \quad (4.1b)$$

$$S_{12} = \frac{1}{1 + LC_i s^2} \frac{(2\beta - LC_i) s^2 + \frac{L}{Z_o} s + 1}{\alpha s^3 + \beta s^2 + \gamma s + 1}. \quad (4.1c)$$

where $\alpha = \frac{LC_i^2 Z_o}{2}$, $\beta = \frac{LC_i^2}{2C_{eff} g_m Z_o} + LC_i$ and $\gamma = \frac{C_\mu^2 Z_o}{2C_{eff}} + \frac{L}{2Z_o}$ are the
circuit parameters that determine the poles and zeros of the S-parameters.

![Small signal model](image)

**Figure 4.3:** Single stage of the nested-reactance feedback power amplifier and equivalent small-signal circuit model.

### Input and Output Return Loss

The input and output return loss are expressed in (4.1a). The minimum value of $S_{11}$ and $S_{22}$ occurs when the numerator of (4.1a) is minimized. This occurs at $\omega_{\text{notch}} = \sqrt{\frac{1}{C_{\text{eff}} L} - \frac{1}{(C_i Z_o)^2}}$ which is slightly smaller than $\omega_o$. Notably, for high voltage gain ($A_v = \frac{C_i}{C_{\mu}} \gg 1$), $\omega_{\text{notch}}$ approaches $\omega_o$.

Figure 4.4 shows the return loss at $\omega_o$ for various $g_m$ values. Small $g_m$ suggests that the network is open since $\beta$ dominates both numerator and denominator in (4.1a) and the circuit is simplified to a parallel LC structure which is open at $\omega_o$. For higher $g_m$ values, the real part of the input (output) impedance decreases
and the input and output impedance converges to

\[ Z_{in}(\omega_o) = Z_o \left( 1 + \frac{j \sqrt{C_{eff} L}}{Z_o (C_i - C_{eff})} \right) \]

\[ \approx Z_o + \frac{j}{\omega_o C_i} \text{ for } A_v \gg 1. \]  \hspace{1cm} (4.2)

While the real part of the impedance approaches 50 Ω, the imaginary part is inversely proportional to \( C_i \). The input and output matching is improved for larger \( C_i \) as shown in Figure 4.4. The \( g_m \) required for return loss better than 10 dB is defined as critical transconductance and is approximately

\[ g_{m,crit} = \frac{C_i}{C_{eff} Z_o} \]

\[ \approx \frac{A_v}{Z_o} \text{ for } A_v \gg 1. \]  \hspace{1cm} (4.3)

Figure 4.4: Effect of \( g_m \) on return loss. Higher \( g_m \) pushes the real part of the input impedance toward 50 Ω at both input and output ports from (4.2).

Figure 4.5 shows the contour plot of \( S_{11} \) and \( S_{22} \) from (4.1a) at 40 GHz for \( \frac{C_i}{C_\mu} \) and \( g_m \) while \( C_\mu = 100 fF \). \( L \) is adjusted properly to keep the tuning frequency
at 40 GHz. Increasing both $g_m$ and $\frac{C_i}{C_\mu}$ improves the return loss. For a given $\frac{C_i}{C_\mu} = 2$, any $g_m$ above $g_{m,crit}$ does not substantially improve the return loss.

**Figure 4.5:** Contour of return loss of the nested-reactance feedback PA at 40 GHz for various $g_m$ and $\frac{C_i}{C_\mu}$ ($C_\mu = 100fF$).

**Gain and Isolation**

From (4.1b), the peak value of $S_{21}$ occurs at

$$\omega_{peak} = \sqrt{\frac{1}{C_{eff}L} + \frac{1}{(C_iZ_o)^2}}$$

when the denominator of (4.1b) is minimized. Since $\omega_{peak}$ comes from $\alpha s^3 + \beta s^2 + \gamma s + 1$, it is common for both $S_{21}$ and $S_{12}$. However, the backward voltage gain, $\frac{1}{1 + LC_is^2}$, is much smaller than the forward voltage gain. As such the circuit’s isolation increases with its gain. For $g_m \gg g_{m,crit}$, $\beta \rightarrow LC_i$, simplifying

$$(2\beta - LC_i)s^2 + \frac{L}{Z_o}s + 1$$

to

$$(2\beta - LC_i)s^2 + \frac{L}{Z_o}s + 1$$

which has a local minimum at $\omega = \sqrt{\frac{1}{LC_i}}$.

Consequently, the pole at $\omega = \sqrt{\frac{1}{LC_i}}$ from $1 + LC_is^2$ is cancelled due to the numerator, $(2\beta - LC_i)s^2 + \frac{L}{Z_o}s + 1$.

Now, the $S_{11}$ notch frequency, $S_{21}$ peak frequency and nominal resonant frequency, $\omega_o$, are related through

$$\omega_{notch}^2 + \omega_{peak}^2 = \omega_o^2.$$  

(4.4)
For high $C_i$ values, it has been shown that the notch and peak approach $\omega_o$. At the resonant frequency, (4.1b) and (4.1c) are simplified to

\[
S_{21}(\omega_o) = \frac{C_i}{C_\mu}(1 + \frac{j}{-C_i Z_\omega \omega_o + \frac{Z_o}{L \omega_o}}) \quad \text{and} \quad (4.5a)
\]

\[
S_{12}(\omega_o) = \frac{C_{\text{eff}}}{C_i}(1 + \frac{j}{-C_i Z_\omega \omega_o + \frac{Z_o}{L \omega_o}}).
\]

Figure 4.6 shows the contour of the gain of a single stage nested-reactance feedback PA as a function of $g_m$ and $\frac{C_i}{C_\mu}$ at 40 GHz. Again, $C_\mu = 100fF$ and $L$ is adjusted properly to maintain a tuning frequency of 40 GHz. It shows improvement for higher $g_m$ and $\frac{C_i}{C_\mu}$.

**Figure 4.6**: Contour of gain (dB) of a single stage nested-reactance feedback PA at 40 GHz for various $g_m$ and $\frac{C_i}{C_\mu}$.

Figure 4.7 shows the $S$-parameters of a single stage nested-reactance feedback PA over frequency range of 80 GHz. The value of $C_i$, $C_\mu$ and $L$ are 200fF, 100fF and 300pH respectively to tune the circuit at 40 GHz. The Q of the circuit is

\[
Q = \frac{Z_o}{\omega_o L \sqrt{\frac{L}{C_{\text{eff}}}}}.
\]

Thus smaller inductor can make it more narrow band while smaller capacitor makes it wide band. In general, the return losses can presumably
be broadened using balanced architectures if necessary or staggering the return loss across multiple stages.

The above analysis is based on $C_\pi = C_s = 0$. While ignoring $C_s$ might be valid relative to $C_i$, $C_\pi$ is generally significant. Indeed, $C_\pi$ may be an order of magnitude larger than $C_i$ since $g_m$ is assumed large. The effect of $C_\pi$ on the small signal parameters is discussed in Appendix B.

\begin{figure}[h]
\centering
\includegraphics[width=\textwidth]{figure4.7.png}
\caption{Gain and isolation of an ideal single stage nested-reactance feedback PA. $C_i = 200fF, C_\mu = 100fF, L = 300pH$ and $g_m = 200mS$.}
\end{figure}

4.2.2 Large Signal Circuit Analysis

The large-signal behavior of a nested-reactance feedback power amplifier mainly depends on the active device biasing. However, the operation of this topology exhibits subtle differences in the theoretical efficiency and compression behavior since the amplifier does not require traditional input and output matching networks. From Section 4.1, the following observations are made at resonance.

1. The power delivered from the source is maximized when the input impedance is equal to the source impedance and $P_{in} = \frac{i_1^2(\omega_0).Z_o}{2} = \frac{V_s^2}{4Z_o}$

2. The power delivered to the load is $P_{out} = \frac{i_2^2(\omega_0).Z_o}{2} = \frac{V_s^2}{4Z_o}$ when the condition 1) is true.
3. The transducer power gain is defined as $G_T = \frac{P_{out}}{P_{in}} = A_v^2$ and depends to the first order only on the input and feedback capacitance.

The collector efficiency is defined as $\eta = \frac{P_{out}}{P_{dc}} = \frac{i_o^2 Z_o}{2V_{cc}I_c}$, where $V_{cc}$ is the collector bias and $i_o$ is the peak swing at the collector. For class-A operation, this simplifies to $\eta_{max} = \frac{i_o}{2I_c}$ since the maximum RF swing at the collector is equal to $V_{cc}$ [45]. Applying $A_v|i_i|$ and $(A_v + 1)|i_i|$ for the output current and collector current respectively, the maximum collector efficiency is

$$\eta_{max} = \frac{A_v}{2(A_v + 1)} \quad (4.6)$$

For high $A_v$, a nested-reactance feedback power amplifier has the same efficiency as a class A power amplifier since the underlying active device in the feedback is biased in class-A. A similar argument holds for other linear biasing classes, i.e. AB and B.

While the drain efficiency is no better than other amplifier classes, the nested-reactance feedback amplifier offers the possibility of achieving high efficiency at high power levels because in this topology the load line matching does not require high-Q impedance transformation. Additionally, the linearization effect of the feedback capacitor allows the circuit goes to higher power before gets into compression. For the proposed amplifier, the base-emitter voltage seen through a capacitive divider is $V_i = \frac{C_i}{C_i + C_\pi} V_i$ assuming a negligible effect from $C_\mu$. The bipolar base-emitter junction capacitance is composed of the depletion and diffusion capacitances $C_\pi = C_{\pi, \text{depl}} + C_{\pi, \text{diff}}$. However, the diffusion portion dominates the forward bias PN junction. Thus, $C_\pi \approx C_{\pi, \text{diff}} \approx g_m t_{bb}$, where $t_{bb}$ is the base transit time. As $g_m = \frac{I_c}{V_T}$ and $I_c = I_{ES} e^\frac{V_i}{V_T}$, $V_i$ equals $(1 + \frac{C_\pi}{C_i} e^{\frac{V_i}{V_T}}) V_\pi$. This equation is transcendental and can only be solved by numerical techniques. Intuitively, the $I_c$ should be a linear function of $V_i$ since $I_c$ is an exponential function of $V_\pi$ and $V_\pi$ is a natural log of $V_i$. Since this capacitor is increasing with the current density of the device, the voltage divide ratio is dynamically changing, resulting to a linear behavior of the output current versus the input voltage, $V_i$. This prevents the PA from going into compression quickly and the compression happens at higher level of input power. Figure 4.8 shows the rule of capacitive divider at high power levels.
This voltage division improves the $V_{1dB}$ compression point by a factor of $(1 + \frac{C_\pi}{C_i})$. A comprehensive analysis is addressed in [40].

**Figure 4.8:** Collector current with and without the effect of $C_i$. The current is more linear due to the effect of voltage division at the base-emitter node.

### 4.3 Circuit Design

Figure 4.9 shows the proposed nested-reactance power amplifier implemented in a 120-nm SiGe process. It contains three stages with progressive transistor scaling handle higher power levels and prevents each stage from entering compression.

**Table 4.1:** Passive elements of each stage with their predicted gain. The gain drops as the transistor size increases. This due to increase of $C_\mu$ while $C_i$ is fixed.

<table>
<thead>
<tr>
<th>Stage</th>
<th>$C_i$ (fF)</th>
<th>$C_\mu$ (fF)</th>
<th>$C_\pi$ (fF)</th>
<th>$L$ (pH)</th>
<th>Gain (dB)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>220</td>
<td>40</td>
<td>250</td>
<td>320</td>
<td>8.8</td>
</tr>
<tr>
<td>2</td>
<td>200</td>
<td>65</td>
<td>450</td>
<td>240</td>
<td>6.5</td>
</tr>
<tr>
<td>3</td>
<td>180</td>
<td>115</td>
<td>850</td>
<td>180</td>
<td>2.3</td>
</tr>
</tbody>
</table>

High-$f_t$ SiGe HBTs ($f_t/f_{max}$ of 210/200 GHz) suffer from low $BV_{CEO}$ of 1.7V, which limits the maximum collector voltage swing and power handling. A design
that presents low external base impedance to a power transistor may overcome $BV_{ceo}$ limitations. This can increase the effective collector breakdown voltage well beyond $BV_{ceo}$ [46]. The biasing circuit for this PA provides an impedance of 100-Ω from DC to the frequency of operation. This low impedance at the base of each transistor improves the breakdown voltage more toward the $BV_{cbo}$, a value of 5.1V [47]. In addition, the feedback behavior of the resistor prevents thermal runaway.

Figure 4.10 shows the simulated $S$-parameter values at 40 GHz as a function of $g_m$. Notably, beyond a transconductance of 200 mS there is no significant change in the $S$-parameter values. From (4.3), the $g_{m,crit}$ is 140 mS and for $g_m \geq g_{m,crit}$, the $S$-parameters are independent of the transconductance value.

Figure 4.11 shows the $S$-parameters of the three-stage nested-reactance feedback power amplifier. The PA has a peak gain of 15 dB at 38 GHz. Both $S_{21}$ and $S_{12}$ show same $\omega_{peak}$ frequency. This happens since $\omega_{peak}$ comes from $\alpha s^4 + \beta s^2 + \gamma s + 1$ and it is common for both $S_{21}$ and $S_{12}$. However, as discussed in 4.2.1, $A_v = \frac{C_i}{C_i} \mu$ and $\frac{C_{eff}}{C_i} \simeq (\frac{C_i}{C_i})^{-1}$, then the isolation is always $A_v^2$ times smaller than the gain, providing enough margin for the circuit stability. To check the circuit stability over the corner and temperature, the $\mu_{factor}$ has been calculated for typical, fast and slow corners at room, 0°C and 125°C respectively. The results are plotted in Figure 4.12 and show unconditional stability for frequencies above 36 GHz.
Figure 4.10: The $S$-parameters at 40 GHz for various transconductance show insignificant change for $g_m \geq 300 \text{mS}$, a value twice than $g_{m,\text{crit}}$.

Simulated large signal performance of the PA is presented in Figure 4.13. With a $V_{cc} = 2V$ and $I_{dc} = 4mA$ the PA reaches a maximum PAE of 20.1% and $P_{sat}$ of 20 dBm.

The time-domain collector-emitter voltage $V_{ce}$ and collector current $I_c$ of the third stage of the nested-reactance feedback PA are plotted in Figure 4.14 for an input power of 0 and 20 dBm at 40 GHz. The loadline impedance seen from the collector shows a value of $9.4\Omega$ at the tuned frequency. This indicates the voltage swing of the collector is $\sqrt{5.3}$ times smaller than the swing at the output, making the transistor less vulnerable to break down.

Quarter-wave transmission lines are used to bias the collector of each device. On-chip 10 pF MIM capacitors provide low impedance at $f_o$ to ground. Each capacitor takes an area of $130\mu m \times 90\mu m$. The self resonance frequency of the MIM caps are simulated and extracted using HFSS and is at 77 and 300 GHz.

4.4 Measurement Results

The PA is fabricated in a 120-nm SiGe BiCMOS process. Fig. 4.15 shows the die microphotograph. The circuit measures $1160\mu m$ by $900\mu m$ including pads.
Figure 4.11: Simulated S-parameters of the nested-reactance feedback power amplifier.

The nominal collector current bias for all three stages is 4 mA at 2.4 V collector voltage. The biasing favors class B operation to achieve higher efficiency.

The small signal measurement was performed with an Agilent E8361A two port power network analyzer at room temperature. Figure 4.16 and 4.17 show simulated and measured S-parameters of the PA.

Figure 4.18 shows the large signal measurement setup. Since the Agilent E8257D signal generator (PSG) output power is limited to 14 dBm for frequencies above 30 GHz, an external PA (MARKI A2050) is used to compensate for the cable loss. A 10-dB branch coupler (AG 87301) is used to sense the input and output power with an Agilent E4419B power meter. To ensure the power amplifier is not exhibiting any oscillation, a separate 10-dB branch coupler is used at the output node to feed an Agilent E4448A power spectrum analyzer (PSA). The table in Figure 4.18 shows the loss of each component and the final offset values for the input and output side.

Figure 4.19 shows the performance of the chip at 38 GHz with a $V_{cc}$ of 2.4 V and $I_{bias}$ of 4 mA. The PA achieves a PAE max of 20.05% and a Psat of 21.13 dBm at this operating condition. A maximum Psat of 23 dBm was reached for a Vcc of 3 V. Figure 4.20 and 4.21 plot the gain, $P_{sat}$ and PAE of the device for the
maximum PAE and maximum $P_{sat}$, respectively. In both cases the peak PAE and peak saturated output power occur at 38 GHz. The peak PAE is shown to be just over 20% for an output power of 19 dBm. The peak output power reaches 23 dBm at a PAE of over 10%. To the authors best knowledge, this is the highest output power from a single PA and the best PAE shown at 200 mW in a SiGe process at this band. The BW of the PA is defined based on 3-dB power roll off of its saturated power presented in Figure 4.21. This indicates a 5 GHz BW from 36-41 GHz.

Table 4.2 compares this work to prior state-of-the-art mm-wave PAs implemented in SiGe, Si CMOS and III-V processes. The combination of high output power and high efficiency place this work amongst the best demonstrations at mm-wave bands in Si/SiGe processes.

### 4.5 Chapter Summary

A Nested-Reactance Feedback (NeRF) power amplifier is presented based on a capacitive feedback at the transconductor and an inductor in the feed forward path. The PA has 3 stages and occupies 1160$\mu$m by 900$\mu$m including pads. The
Table 4.2: Performance Comparison of latest mm-wave PAs.

<table>
<thead>
<tr>
<th>Ref.</th>
<th>Freq. (GHz)</th>
<th>BW (GHz)</th>
<th>Gain (dB)</th>
<th>Psat (dBm)</th>
<th>PAE (%)</th>
<th>Technology</th>
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<tr>
<td>This work</td>
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<td>5</td>
<td>18.7</td>
<td>21.3</td>
<td>20.0</td>
<td>SiGe 120nm</td>
</tr>
<tr>
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<td>5</td>
<td>18.4</td>
<td>23</td>
<td>10.7</td>
<td>SiGe 120nm</td>
</tr>
<tr>
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<td>-</td>
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<td>36</td>
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</tbody>
</table>
Figure 4.13: Simulated large signal performance at 40GHz. The PA reaches a saturated output power of 20.5 dBm and a maximum PAE of 21%.

small signal gain of the PA has a peak of 18.7 dB at 38 GHz. A maximum PAE of 20.05% and $P_{sat}$ of 23 dBm was achieved for $V_{cc}$ of 2.4V and 3V respectively at 38 GHz. This is the highest output power from a single PA in SiGe process at Q-band. The PA performs over 5 GHz of bandwidth from 36-41 GHz.

Acknowledgments

Chapter 4 is mostly a reprint of the material as it appears in IEEE Transactions on Microwave Theory and Technology, vol. 60, pp. 1667-1675, June 2012, N. Kalantari; J. F. Buckwalter. This dissertation author was the primary author of these materials and co-author has approved the use of the material for this dissertation.
Figure 4.14: $V_{ce}$ and $I_c$ of the third stage of the nested-reactance feedback PA for $P_{in}=0$ and 20 dBm.

Figure 4.15: Die micro photograph of the Q-band nested-reactance feedback power amplifier.
Figure 4.16: Measured and simulated gain and isolation of the Q-band nested-reactance feedback power amplifier.

Figure 4.17: Measured and simulated return loss of the Q-band nested-reactance feedback power amplifier.
Figure 4.18: Large signal measurement setup. The 10-dB coupler at the output was used to check the signal tone at a spectrum analyzer. It makes sure the measured output power at the power meter is not due to any oscillation.

Figure 4.19: Large signal performance of the Q-band nested-reactance feedback PA at 38GHz for a Vcc=2.4 V. The PA achieves a PAE max of 20.05% and Psat of 21.13dBm.
**Figure 4.20:** Maximum PAE biasing condition ($V_{cc}=2.4\,v$, $I_{dc}=4\,mA$). The $P_{out}$ is at the PAE max while the gain is the 1dB compression point gain.

**Figure 4.21:** Maximum $P_{out}$ biasing condition ($V_{cc}=3\,v$, $I_{dc}=4\,mA$). The PAE is at the $P_{out}$ max while the gain is the 1dB compression point gain.
Chapter 5

A Multichannel Serial Link Receiver with Dual-loop Clock-and-data Recovery and Channel Equalization

5.1 Dual-Loop CDR

5.1.1 Architecture Review

Figure 5.1 shows the architecture of a dual-loop CDR, consisting of a PLL and CDR [32, 33, 52]. The PLL creates a quadrature clock at the data rate of the input data $D_{in}$ while the CDR tracks the data phase along each lane of the serial link. The data recovery loop is based on a phase detector (PD) \(^1\), a finite state machine (FSM) and a phase interpolator (PI) [52]. A bang-bang PD creates "up" and "down" signals based on the phase of the clock in respect to the input data [53]. The FSM filters the "up" and "down" signals inside a roll-over counter. The output of the roll-over counter is filtered in a digital proportional and integrator loop filter to create an $n$-bit binary code. The $n$-bit binary code is sent to the phase interpolator to select one out of $2^n$ phase to align the sampling clock $CK_{IQ}$.

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\(^1\)Here a binary, also known as bang-bang phase detector (!!PD) is used.
to the center of the input data $D_{in}$.

![Figure 5.1: The architecture of a dual loop CDR. The PLL generates the quadrature clock. The CDR loop consists of a binary phase detector, a finite state machine and a phase interpolator.](image)

### 5.1.2 Phase Interpolator

The main functionality of a phase interpolator is to combine quadrature clocks and creates different phases with fine steps. Figure 5.2 shows the basic architecture of a linear phase interpolator. The PLL generates the quadrature clock phases and provides these to a phase interpolator [34]. An $n$-bit phase interpolator creates $2^n$ different phases to cover one unit interval (UI). The two most significant bits determine the phase quadrant. The other $n-2$ bits divide each quadrant into $2^{n-2}$ sections. The phase-interpolated clock is defined as

$$ CK_{IQ} = \alpha I + (1-\alpha)Q $$ (5.1)
where $0 \leq \alpha \leq 1$. The following terminology is used throughout the paper:

- $\Phi$ is the phase difference between the $I$ and $Q$ clock. Ideally, $\Phi = \frac{\pi}{2}$ but this often varies with the frequency of operation complicating the implementation of wideband CDR loops.

- $\Delta$ is the ideal phase resolution; $\Delta = \frac{2\pi}{2^n}$. Uneven steps are exhibited in the phase interpolator as manifested in phase non-linearity.

- $k$ is the digital value of the phase code. $0 \leq k \leq 2^n - 1$.

- $\alpha (k)$ is weight of $I$ clock, where $\alpha (k) = \frac{k}{2^{n-2}}$ for $0 \leq k \leq 2^{n-2}$.

- $\theta(k)$ is the phase of $CK_{IQ}$ at phase code $k$.

For an ideal $I$ and $Q$ clock phase ($\Phi = \frac{\pi}{2}$) and clock peak swing of $V_o$, (5.1) is written as

$$CK_{IQ} = V_s \cos(\omega t - \theta)$$

where $V_s = V_o \sqrt{\alpha^2 + (1 - \alpha)^2}$ and $\theta (k) = \tan^{-1}\left(\frac{1-\alpha}{\alpha}\right)$.

The phase integral nonlinearity ($INL$) is the difference between $\theta$ and the ideal phase; i.e. $INL(k) = \theta(k) - k\Delta$. The phase differential nonlinearity ($DNL$) is the difference between adjacent discrete phases and $\Delta$; i.e. $DNL(k) = \theta(k + 1) - \theta(k) - \Delta$. Even for an ideal $IQ$ phase difference ($\Phi = \frac{\pi}{2}$), the phase steps are not equally spaced and the phase $INL$ and $DNL$ is non-zero. Additionally, the phase interpolated clock amplitude is not constant for all the phase codes and reaches its
minimum at $\frac{\sqrt{2}}{2}V_o$ when $I$ and $Q$ are equally weighted. This directly affects the random jitter generation in the CDR and is discussed in Section 5.2. In the next section, the impact of imperfect $IQ$ phases on $INL$ and $DNL$ is demonstrated.

### 5.1.3 Effect of $I/Q$ Mismatch on the Phase-Interpolated Clock

The precise relationship between $I$ and $Q$ phases is difficult to reach based only on circuit matching over a wide frequency range. Figure 5.3 shows the impact of $IQ$ phase mismatch. $CK_{IQ}$ is the sum of two vectors in complex domain with an amplitude of $V_o$ and an angle of $\Phi$. Then, (5.1) becomes

$$CK_{IQ} = \pm \alpha V_o + (1 - \alpha)V_o e^{j\Phi}$$

$$= V_s(\alpha, \Phi)e^{j\theta(\alpha, \Phi)}$$

(5.3)

where $V_s(\alpha, \Phi) = V_o(\sqrt{\alpha^2 + (1 - \alpha)^2} \pm 2\alpha(1 - \alpha) \cos \Phi)$ is the voltage swing and $\theta(\alpha, \Phi) = \tan^{-1}(\frac{(1-\alpha)\sin \Phi}{\pm \alpha + (1-\alpha) \cos \Phi})$ is the sampling clock phase. The $\pm$ sign refers to the 1st and 2nd quadrant where sign of $I$ changes. Both $V_s$ and $\theta$ exhibit a period

---

**Figure 5.3**: The non-ideal $IQ$ phase introducing non-equal $INL$ and $DNL$ in the $Ck_{IQ}$ phase.
Figure 5.4: Clock IQ phase mismatch and its effect on the amplitude, INL and DNL. A $\Delta \Phi = -15^\circ$ ($\Phi = 75^\circ$) increases the INL from $4^\circ$ to $18.2^\circ$.

The maximum and minimum of $V_s$ is $V_o$ and $V_o \sqrt{2(1 - \cos \Phi)}$. The minimum occurs at $\frac{\pi - \Phi}{2}$. \footnote{This is for $0 < \Phi < \frac{\pi}{2}$. For $\frac{\pi}{2} < \Phi \leq \pi$, the minimum happens at $\frac{\Phi}{2}$.}

The IQ phase mismatch degrades the phase linearity. The phase INL and DNL are

\[
\text{INL}(\alpha, \Phi) = \frac{\pi}{2} (1 \mp \alpha) - \tan^{-1} \frac{(1 - \alpha) \sin \Phi}{\pm \alpha + (1 - \alpha) \cos \Phi} \tag{5.4}
\]

and

\[
\text{DNL}(\alpha, \Phi) = \tan^{-1} \left( \frac{\mp (\alpha - \beta) \sin \Phi}{1 - (\alpha - \beta) + 2 \alpha \beta \pm (\alpha + \beta - 2 \alpha \beta) \cos \Phi} \right) - \Delta, \tag{5.5}
\]

where $\beta = \alpha - \frac{1}{2^{n-2}}$. Figure 5.4 shows the normalized clock amplitude and the INL and DNL as a function of phase code for an IQ phase mismatch of $0^\circ$ and $-15^\circ$ ($\Phi = 90^\circ$ and $\Phi = 75^\circ$). The amplitude reduction occurs at midpoints. This reduction is more severe at the presence of quadrature clock phase mismatch. With additional buffering, the amplitude is limited to prevent any amplitude variation. For $\Delta \Phi = 0^\circ$ the maximum INL is about $4^\circ$. For $\Delta \Phi = -15^\circ$, it increases to $18.2^\circ$. The same argument is valid for the phase DNL in $CK_{IQ}$. 

\[
\text{INL}_{\text{max}} = \frac{\sin \Phi}{1 - \cos \Phi} - \Delta, \tag{5.6}
\]
The INL of the phase interpolator is not a big of concern since it is suppressed by the large feedback loop gain. However, the DNL of the phase interpolator degrades the CDR jitter tolerance and BER performance [36].

5.1.4 Source Synchronous and Non-Synchronous Clocking

A serial link is source synchronous if the input data and PLL clock are generated from the same reference source\(^3\). Therefore, the phase difference between the input data and recovered clock remains constant over the time \((D_{in} \text{ and } CK_{IQ} \text{ in Figure 5.1})\). On the other hand, if the transmitter reference clock has a slight frequency difference- typically ten to hundreds parts per million- between \(D_{in}\) and \(CK_{IQ}\), the phase difference varies with time and is referred as a non-synchronous link. While locked to the input data, the phase of \(CK_{IQ}\) rotates to maintain the sampling clock in the middle of input data.

For non-source synchronous applications, dual-loop CDRs are specified to handle a minimum ppm offset of ±100 ppm. In case of spread spectrum clocking (SSC), CDRs need to track ±5000 ppm at 33 KHz [54] and require a second order loop filter [36] [55].

5.1.5 Slew Rate

The slew rate (SR) - or update rate - is the maximum rate at which the loop filter updates the phase interpolator to go through one UI worth of phase. An \(n\)-bit phase interpolator takes \(2^n\) steps to cover one UI. If \(F_{LF}\) is the rate at which the loop filter is clocked then the SR is \(F_{LF}\Delta\). For the loop filter shown in Figure 5.1 the \(F_{LF} = \frac{F_{PLL}}{m}\). Meanwhile, there is an \(m\)-bit counter in the loop. Thus the update rate is slowed down by a factor of \(2^m\). The input data transition density \((T_D)\) has a proportional effect on the updating procedure. Since an \(m\)-bit demux is used inside the loop filter, the overall transition density is \(mT_D\). Consequently, the \(SR\) of loop filter in Figure 5.1 is

\[
SR = \frac{T_D F_{PLL}}{2^m} \tag{5.6}
\]

\(^3\)Some authors refer to source synchronous systems as mesochronous.
for an update rate of ±1. Note the $m$ of transition density has canceled by $m$ in $F_{LF}$. The reader should note the $SR$ equation depends on the complexity of the digital loop. Equation (5.6) is defined based on digital filter in Figure 5.1. Similar equation is presented in [36].

Like the loop bandwidth ($LBW$) of an analog CDR, the slew rate sets the point at which jitter goes from being tracked to being attenuated. The slew rate also determines the maximum PPM difference between the reference clock and the incoming data that can be tracked without a second order loop. The maximum frequency tolerance in PPM is defined by multiplying the $SR$ by $\frac{10^6}{F_{PLL}}$. For example, consider a 10-bit counter for the loop filter shown in Figure 5.1. If the $T_D$ is 0.5 then the maximum frequency tolerance is $\frac{10^6}{F_{PLL}} \times \frac{0.5 F_{PLL}}{2^{10}} \approx 488 PPM$. For SSC condition, as explained in Section 5.1.4, a second order loop (proportional plus integrator) is required to track ±5000 PPM at 33 KHz.

### 5.1.6 Dithering

The steady state of the bang-bang CDR is a limit cycle whose amplitude and frequency is determined by the feedback loop delay [36]. A binary phase detector, by definition, creates "up" or "down" pulse even in the locked condition [53] [56]. Consequently, the recovered clock dithers around a bounded range and manifests as deterministic jitter.

In a conventional CDR with charge-pump and VCO, the dithering effect is attenuated as the phase detector immediately is applied to the charge-pump, loop filter and VCO. In a dual-loop CDR with digital filter and phase interpolator, the amplitude of dithering is magnified for two reasons. First, the loop is digital and the error signal goes through several clock cycles before adjusting the phase interpolator. Second, the phase interpolator has finite resolution. Ideally, the phase resolution is $\Delta = \frac{2\pi}{2^n}$. However, the actual phase resolution has been shown to be a function of $\alpha$ and $\Phi$. These factors define the overall dithering magnitude in a digitally-controlled CDR loop. If the input data and clock are truly synchronous,
then the dithering magnitude is defined as

\[ \theta_{\text{dither}} = \sum_{k=-D_f}^{D_f} DNL(k-1) + \Delta. \]  

(5.7)

D_f is called the dithering factor and relates to the CDR feedback loop latency. For the digital loop, D_f is defined by the number of re-timing stages inside the loop filter. Figure 5.5 illustrates how dithering causes clock jitter. Since the loop filter has three sequential stages, it requires three clock cycles to deliver the up/down signal from the PD to the phase interpolator. Thus D_f is 3. The effect of dithering on the recovered clock and retimed data is shown in Figure 5.5. Figure 5.6 shows the dither magnitude based on (5.7) for a 7-bit phase interpolator, a D_f of 4 and the IQ phase mismatch, ∆Φ, of 0° and −15°. The dither magnitude increases at the phase code midpoints similar to DNL. Dithering is undesirable and the main source of deterministic jitter in digitally controlled CDRs.
Figure 5.6: The magnitude of dither in degree for a 7-bit phase interpolator and $D_f = 4$. The IQ phase mismatch makes the magnitude larger and un-even over the phase code.

5.2 Analysis of Clock Jitter in Dual Loop CDRs

A dual-loop CDR generates random and deterministic jitter in the sampling signal due to the phase-interpolated clock. The jitter transfer function from the $CK_{IQ}$ to the recovered data has a high-pass response similar to the VCO noise in a PLL [57, 58]. Here, the recovered clock jitter on BER performance is discussed. Clock jitter has a direct effect on the jitter tolerance of the CDR and achievable BER. A comprehensive BER equation is derived as a function of IQ phase mismatch for given input data jitter.

5.2.1 Random Jitter

The main source of random jitter in the clock path is PLL phase noise and the additive noise of the phase interpolator. Also, any buffer after the phase-interpolated clock $CK_{IQ}$ contributes jitter. Figure 5.7 shows the source of random noise in the phase interpolator. The power spectral density (PSD) of thermal noise of resistor and NMOS differential pairs of I and Q branch are shown as $i_R^2$, $i_I^2$ and $i_Q^2$. We assume the MOSFET and resistor thermal noise are $4kT\gamma g_m$ and $\frac{4kT}{R}$,
Figure 5.7: Sources of random noise in phase interpolator. The conversion between voltage noise and timing jitter is a function of zero-crossing slope. Since the slope is a function of $\alpha$ and $\Phi$ so is the jitter.

respectively. The value for $\gamma$ is $\frac{2}{3}$ for long channel devices and increases for the short channel ones [28]. The current in the $I$ and $Q$ branch are a factor of $\alpha$ and $1 - \alpha$ of the tail current, $I_o$. Therefore, the differential drain noise contribution of the $I$ and $Q$ branches follow:

$$i_I^2 = 4kT\gamma\sqrt{2k_n\alpha I_o}$$  \hspace{1cm} (5.8a)$$

$$i_Q^2 = 4kT\gamma\sqrt{2k_n(1 - \alpha) I_o},$$  \hspace{1cm} (5.8b)$$

where $k_n = \mu_n C_{ox} \frac{W}{L}$. Since sampling occurs near the voltage threshold-crossing of the $C_{KiQ}$, we are most concerned with noise near the zero-crossing point when the current in the $I$ and $Q$ differential pair is equally divided between the positive and negative side. Therefore, the NMOS noise of $I$ and $Q$ branches are $\bar{i}_I^2 = \bar{i}_Q^2 = 4kT\gamma\sqrt{k_n\alpha I_o}$ and $\bar{i}_Q^2 = \bar{i}_Q^2 = 4kT\gamma\sqrt{k_n(1 - \alpha) I_o}$. Note the transistor mismatch is not considered here otherwise the above claim is not valid. The overall voltage
noise at the output of the phase interpolator is

\[ v_{PI}^2 = 2(i_I^2 + i_Q^2 + i_R^2)R^2 = 8kT \left( \gamma(\sqrt{\alpha} + \sqrt{1 - \alpha})\sqrt{k_nI_oR^2 + R} \right) \]  

(5.9)

Voltage noise is translated to timing jitter through the instantaneous \( CK_{IQ} \) slope at the zero-crossing. Dividing this voltage noise in (5.9) by the slope of the signal swing at the zero-crossing, the timing jitter is

\[ \sigma_{PI}^2 = \frac{v_{PI}^2}{|x'_0(\alpha, \Phi)|^2} = 8kT \frac{\gamma\sqrt{k_nI_o(\sqrt{\alpha} + \sqrt{1 - \alpha})R^2 + R}}{\omega^2V_o^2(\alpha^2 + (1 - \alpha)^2 \mp 2\alpha(1 - \alpha)\cos \Phi)}, \]  

(5.10)

where \( |x'_0(\alpha, \Phi)| = |\frac{1}{\omega V_o(\alpha, \Phi)}| \) from (5.1) and the \( \mp \) are used for \( \Phi \) below or above \( \frac{\pi}{2} \) respectively. The maximum noise occurs at the minimum slope for \( \alpha = 0.5 \). In other words, adding equal contributions of the I and Q clock reduces the slope of the interpolated signal as well as contributing the most noise and, consequently, the timing jitter is maximum. The maximum timing jitter is

\[ \sigma_{PI,max}^2 = 16kT \frac{2\sqrt{2}\gamma\sqrt{k_nI_oR^2 + R}}{\omega^2V_o^2(1 \mp \cos \Phi)} \]  

(5.11)

In the presence of PLL phase noise, the phase interpolator noise is independent of the PLL rms jitter on each of the I and Q inputs and the total jitter is

\[ \sigma_{clk}^2 = \sigma_{PLL}^2 + \sigma_{PI}^2. \]  

(5.12)

### 5.2.2 Deterministic Jitter

The deterministic jitter in a dual-loop CDR is a function of the phase resolution and dithering factor as discussed in Section 5.1.6. The magnitude of the deterministic jitter defines the mean value of the timing jitter. Converting (5.7) from phase to time domain,

\[ t_{\text{dither}} = \frac{\theta_{\text{dither}}}{2\pi} T_b \]  

(5.13)

where \( T_b \) is the bit period equivalent to one UI.
5.2.3 Total Jitter and BER Calculation

With the mean and standard deviation of clock jitter, a BER limit is derived. Figure 5.8(a) shows the data and clock jitter on an eye diagram with a data period of $T_b$. The ideal sampling time is in the center of the data eye where $t = \frac{T_b}{2}$. In the absence of clock jitter, the bit error rate is

$$BER = Q \left( \frac{T_b}{2\sigma_{data}} \right),$$

(5.14)

where the $Q$-function is defined as $Q(t) = \frac{1}{\sqrt{2\pi}} \int_{t}^{\infty} e^{-\frac{x^2}{2}} \, dx$ [29]. Equation (5.14) defines the BER due to the timing jitter of the data. The input data to CDR usually comes from the equalizer and includes timing jitter.

Clock jitter further reduces the sampling window margin and aggravates the probability of the error. Clock deterministic and random jitter calculated in the previous section introduces a mean shift and standard deviation in the overall PDF. The clock sampling edge is shifted by $\pm \frac{t_{dither}}{2}$. While the deterministic contribution to the clock shifts the mean value of the overall jitter, the random jitter added to the data jitter. Therefore, the overall standard deviation is $\sigma_{tot}^2 = \sigma_{data}^2 + \sigma_{clk}^2$.

For source synchronous condition, considering the change in the mean and standard deviation of the jitter, the BER is determined by

$$Q \left( \frac{T_b - t_{dither}}{2\sigma_{tot}} \right)$$

(5.15)
Figure 5.9: The BER vs clock IQ phase mismatch. The analytic simulation results are based on $\sigma_{\text{data}} = 50\text{mUI}$ for data jitter. The phase interpolator jitter calculated for $I_o = 2.4\text{mA}$, $R = 250\Omega$ and a $D_f = 4$. Case 1 is for data only jitter. Case 2 includes clock random jitter with zero dithering. Case 3 and 4 include dithering for 7 and 6 bit phase interpolator. Case 5 considers the maximum $INL$ instead of dithering.

In case of non-synchronous source clocks, (5.15) is valid so long as the frequency difference between the $D_{in}$ and $CK_{IQ}$ is less than the maximum frequency tolerance (488 PPM in this work). For higher frequency difference when a second order loop is required, the deterministic jitter is a function of phase interpolator $INL$.

Figure 5.9 shows the analytic simulation results of BER as a function of IQ phase mismatch for five different case study. The first line represents the BER for a random bit stream with only jitter on the data ($50\text{mUI}$) and no clock jitter. This represents an “ideal” receiver and the BER limits imposed by the data jitter. In the second case, the clock is corrupted by random jitter from a 7-bit phase interpolator with $250\Omega$ resistor and tail current of $2.4\text{mA}$. The margins to achieve a BER of $10^{-15}$ are reduced. The third and fourth cases add the deterministic clock jitter due to finite phase resolution and a $D_f$ of 4 for a 7 and 6-bit phase interpolator respectively. As expected, lower phase resolution comes with higher magnitude of dithering and worse BER. Finally, the fifth case shows the BER for a 7-bit phase interpolator where the maximum $INL$ is replacing the dithering.
magnitude. All the plots are based on (5.15) for various $IQ$ phase.

### 5.3 Circuit Design

The circuit was designed and fabricated in a standard 130 nm CMOS technology. It consists of four receiver channels that share one PLL. Each channel has a continuous time linear equalizer (CTLE)$^4$, data retimer and a phase interpolator. The PLL is shared between the four retiming circuits via the phase interpolators.

#### 5.3.1 CDR Design

![Diagram](image)

**Figure 5.10**: The dual loop CDR system level architecture. Two quadrature VCOs are used to cover a wide range of frequency. The clock divider after the PI allows the CDR locks to data rates as low as 100Mbps.

Figure 5.10 shows the detail of the PLL and CDR. The PLL consists of two quadrature VCOs that cover a frequency range of 3.2-5.2 and 5-7 GHz respectively. The 200 MHz frequency overlap guarantees coverage from 3.2-7 GHz. Each VCO is designed based on two identical coupled VCOs. Mirzaei derived the $IQ$ phase mismatch as $\Delta \Phi = -Q \left(1 + \frac{1}{m}\right) \frac{\Delta \omega}{\omega_0}$ where $m = \frac{I_c}{I_b}$ is the ratio of coupling and VCO currents and is called the coupling factor. $Q$ is the quality factor of the

---

$^4$ Also equalizer (EQ) is used in some places in this paper for CTLE.
tank and $\Delta \omega$ is the frequency difference between the free running frequency of
the quadrature VCOs [37]. To reduce the phase mismatch requires increasing the
coupling factor and reducing the quality factor. Figure 5.11 shows the simulated
phase noise of the PLL. The PLL locked at 6 GHz for a divider ratio of 40 and a
150 MHz reference clock.

In the CDR, high speed analog circuits are realized with current mode logic
(CML) that uses replica biasing shown in Figure 5.12. The replica biasing enforces
the circuit to have a voltage swing of $V_{\text{swing}} = IR = 600 \text{mV}$. The 100 $\mu A$
reference current is generated from a bandgap voltage over the same type of resistors used
in Figure 5.12. Consequently, $V_{\text{swing}}$ has a bandgap behavior which minimizes the
PVT variation.

Figure 5.13 shows the circuit detail of the phase interpolator. Two MSB
bits out of the 7 bits are used to define four quadrant and the mapping shown in
top right corner of Figure 5.13. The remaining 5 bits are split in 2 and 3 control
bits. Bits $< 2 : 0 >$ are used to select 8 binary coded reference voltages. Bits
$< 4 : 3 >$ select 1, 2, 3 or all 4 phase interpolator blocks of $I$ or $Q$. This way,
the biasing power of $I$ or $Q$ is divided into 32 different levels and they go opposite
direction of each other. The mapping of these five LSBs is shown in bottom right

![Figure 5.11](image-url)
Figure 5.12: The unit cell CML latch with the reference voltage and replica biasing circuitry.

corner of Figure 5.13.

Figure 5.14 shows circuit simulation of RMS jitter of the phase interpolator and compares to the analytic in equation (5.10) for a resistor value of $R = 250\Omega$ (4 parallel blocks), $I_o = 2.4\ mA$, input voltage swing of 600 mV (differential) at 6 GHz. Analytical and simulated results show reasonable agreement and suggest the random jitter varies between 100 fs and 200 fs.

The clock after the phase interpolator goes to a programmable divider with binary steps from 1 to 32. This is shown as $L$ in Figure 5.10. The minimum data rate the CDR can handle is $\frac{3.2\text{Gbps}}{32} = 100\text{Mbps}$. Therefore, the CDR performs over a wide range of 0.1-7 Gbps. This covers most of the standard in wireline datacom and telecom such as Ethernet, SONET, and SATA/SAS.

5.3.2 Equalizer Design

Transmission line loss arises from the series resistance of the conductor and shunt conductance of the dielectric material. Both are function of frequency since the skin effect increases the series resistance with the square root of frequency and the parallel conductance depends on the dielectric material and is roughly proportional to the frequency. The loss increases linearly with length and increases
Figure 5.13: The schematic of phase interpolator. Four identical cells are used for I and Q clocks. Each block can use 8 different biasing point. The overall effect is 32 linear level to define $\alpha$ in (5.1).

linearly with frequency when the loss tangent dominates [18].

A continuous time linear equalizer (CTLE) should have a transfer function equal to the inverse of the channel. The equalizer transfer function can be represented as a rational transfer function that synthesizes a high-pass filter, $CTLE(s) = \frac{A}{\prod m (s - z_i)} \prod n (s - p_i)$. As shown in Figure 5.15, the CTLE should create a unity gain transfer function if cascaded with the lossy channel. As the channel loss rolls off as a strong function of frequency, a higher-order CTLE is required. Although, higher-order CTLEs offer better channel compensation, they amplify high-frequency noise. Thus, there is always a trade-off between the loss compensation and the amplified high frequency noise power. A low power approach to the CTLE has been proposed by [59].

Figure 5.16 shows the schematic of the CTLE that consists of two cascaded CML buffer with capacitive degeneration. It is designed to compensate a maximum 23 dB channel loss at 3.5 GHz. Equation (5.16) provides the voltage transfer
Figure 5.14: The simulated RMS jitter of phase interpolator for three different IQ phase mismatch. Analytic simulation results are based on (5.10) for $I_o = 2.4mA$ and $R = 250\Omega$ at 6GHz. The circuit simulation was run with the same parameter.

function of the CTLE for each stage where $R_L$ and $R$ are the drain and source resistance respectively:

$$H(s) = \frac{g_m R_L}{1 + g_m R (1 + \frac{1}{R C s})}$$  \hspace{1cm} (5.16)

As seen, the zero and pole of the CTLE are located at $\frac{1}{RC}$ and $\frac{1 + g_m R}{RC}$. Each stage is biased such that the $g_m$ is equal to the inverse of the source resistor, therefore it puts the pole of the system at twice frequency of its zero. This provides

Figure 5.15: (a) Transfer function of a CTLE (b) Response of channel and CTLE
a 6dB of high frequency boost. Figure 5.16 has its $z_0$, $p_0$, $z_1$ and $p_1$ at 380, 760, 1000 and 2000 MHz respectively. That is for its maximum boost when $C_0$ and $C_1$ are set to 6 and 1.8 pF. These two stages provide an overall boost of 12 dB. The presence of a passive high pass filter before the 1st CTLE, provides an additional 5dB boost. Four control bits of the CTLE provides 16 different equalizer boost values. Code 0 is used for point blank and code 15 for 23 dB channel loss. Figure 5.17 shows the channel response along with the equalizer when set to maximum high frequency boost. The overall effect shows a 3-dB bandwidth up to 2.2 GHz. Figure 5.18 shows the simulated eye at the output of the channel and equalizer at 7 Gbps. The simulation was run in Agilent SystemVue when the transfer function of the CTLE was imported along with the measured $S$-parameter of the actual channel.

**Figure 5.16:** Schematic of the CTLE. It consists of two cascaded CML buffer with capacitive degeneration.
Figure 5.17: Simulated frequency response of channel, the CTLE and cascaded channel and the CTLE.

Figure 5.18: (a) Simulated eye diagram at 6 Gbps after 45-inch trance. The eye is closed (b) Simulated eye diagram after the CTLE. The eye is opened.

5.4 Measurement Results

Figure 5.19 shows the die photograph of the four-channel CDR. The chip was fabricated in 130nm CMOS and occupies 2.41 mm². An Agilent N4903A BERT and 86100C Digital Communication Analyzer (DCA) was used to measure the equalizer and the CDR performance using a PRBS-23 pattern. For source-synchronous measurements, the reference clock of the PLL was provided by a BERT. The PLL divider ratio was set to 40. Table 5.1 shows the detail DC current consumption of each individual block. The chip uses 1.2V from an external regulated power supply and the total power consumption of the chip was measured
at 271.5 mW. This indicates an overall of 67.9 mW per channel. For an aggregated data rate of 28 Gbps, the energy efficiency of the chip is recorded at 9.7 pJ per bit.

The CDR operates from 150 Mbps to a maximum data rate of 7.0 Gbps per channel. Figure 5.20 shows the eye diagram at both extreme case of 0.150 and 7 Gbps with a high-quality input signal.

5.4.1 Phase Interpolator and CDR Characterization

The quadrature phase of the CDR, \( \Phi \), was measured at room temperature and 90°C and the phase mismatch (\( \Delta \Phi \)) is shown in Figure 5.21. At room temperature, \( \Delta \Phi \) reaches a maximum of 14.3° at 5.25 GHz and minimum of 16.7° at 6.75 GHz. At 6 GHz, a perfect IQ of \( \Delta \Phi = 0 \) is observed. At 90°C case temperature, this frequency shifts to 6.3 GHz.

Figure 5.22 illustrates the simulated and measured phase DNL of the phase interpolator at 5.25, 6.0 and 6.75 GHz as a function of phase code. To have an accurate measurement, an Agilent 86108A precision waveform analyzer was
Table 5.1: DC current consumption of each individual block of the DUT. The supply voltage was 1.2 V. The data rate and energy efficiency is included at the end of the table.

<table>
<thead>
<tr>
<th>Block Name</th>
<th>Number</th>
<th>$I_{DC}/\text{Block}$</th>
<th>Total $I_{DC}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>PLL</td>
<td>1</td>
<td>33 mA</td>
<td>33 mA</td>
</tr>
<tr>
<td>PI, Clk Divider</td>
<td>4</td>
<td>8 mA</td>
<td>32 mA</td>
</tr>
<tr>
<td>Clk Buf. Chain</td>
<td>4</td>
<td>5.2 mA</td>
<td>20.8 mA</td>
</tr>
<tr>
<td>CDR</td>
<td>4</td>
<td>11.4 mA</td>
<td>45.6 mA</td>
</tr>
<tr>
<td>CTLE</td>
<td>4</td>
<td>23.7 mA</td>
<td>94.8 mA</td>
</tr>
<tr>
<td>Total $I_{DC}$</td>
<td>1</td>
<td>-</td>
<td>226.2 mA</td>
</tr>
<tr>
<td>Total $P_{DC}$</td>
<td>1</td>
<td>-</td>
<td>271.5 mW</td>
</tr>
<tr>
<td>Max. Data Rate</td>
<td>4</td>
<td>7 Gbps</td>
<td>28 Gbps</td>
</tr>
<tr>
<td>Energy per bit</td>
<td>-</td>
<td>-</td>
<td>9.7 pJ</td>
</tr>
</tbody>
</table>

used to measure the phase interpolator steps. The $rms$ jitter of this module is recorded as low as 100 fs which is less than 7% of $\Delta$ at 6.75 GHz. The minimum $DNL$ is recorded at 6 GHz where the phase mismatch was the lowest. At 5.25 and 6.75 GHz, the maximum $DNL$ is measured in the first and second quadrant, respectively. Both simulation and measured $DNL$ follows the prediction presented in (5.5). The overall $\Theta_{dither}$ is calculated and presented in Figure 5.23 for 5.25, 6 and 6.75 Gbps. The maximum $\Theta_{dither}$ can be used in (5.13) and (5.15) to predict the BER.

A measured bathtub curve for the above data rates is shown in Figure 5.24. The 6 Gbps plot has the highest margin due to a perfect $IQ$ phase whereas the other two data rates are limited in margins. This outcome is predicted in (5.15) and Figure 5.8.

Figure 5.25 shows the measured RMS jitter at 5.25, 6.0 and 6.75 Gbps. The shape of these measured results are in close agreement with the simulated and analytical results in Figure 5.14. The reader may wonder why the absolute values are quite higher then. This is due to the additional random noise through the several clock buffer chain and output drivers as there was no direct access to
Figure 5.20: (a) CDR output eye at 150 Mbps. This is the minimum data rate supported by Agilent N4903A BERT. (b) CDR output eye at 7 Gbps.

the output of the phase interpolator on chip.

5.4.2 Jitter Transfer Function and Jitter Tolerance

Figure 5.26 shows the measured jitter transfer function and jitter tolerance of the CDR. Jitter transfer function of a CDR represent the output jitter as the input jitter varied at different rates. Jitter tolerance, on the other hand, specifies how much input jitter a CDR loop must tolerate without causing the bit error rate [29]. The measured JTOL shows better margin on 6 GHz compare to 5.25 and 6.75 GHz. This indicates the phase interpolator nonlinearity degrades the JTOL and supports the analysis provided in Section 5.2.

The jitter transfer is measured when the input data is modulated with 500mUI sinusoidal jitter. The measured data shows that the dual-loop CDR exhibits a low-pass transfer function. Table 5.2 displays the predicted and measured DJ at frequencies 0.5, 1, 5 and 20 MHz. The effect of packaging and connectors from the actual DUT was de-embedded from the deterministic jitter (DJ) of the CDR. This was done by freezing the CDR phase and measuring the DJ. The measured DJ was then recorded at 16.3 ps at 6 Gbps. This data rate was selected since the PLL measured no IQ phase mismatch.

The ∆ is equally spaced along the PI for a value of $\frac{128}{125}$. For a 6 Gbps data rate $\Delta$ is 1.302 ps. The predicted DJ is then formulized as $DJ = DJ_f \Delta + DJ_0$ where $DJ_0$ is 16.3 ps. For jitter frequency below the LBW of the CDR, the CDR tracks
them and as such the dithering factor is measured quite long. This is expected as the CDR follows the input data properly. For jitter above the LBW of the CDR, on the other hand, the CDR is not fast enough to follow. Consequently, the jitter is filtered and CDR shows a lower number of dithering.

**Table 5.2:** Predicted and measured DJ of the CDR at the presence of input data jitter.

<table>
<thead>
<tr>
<th>Jitter Frequency</th>
<th>$D_f$</th>
<th>Predicted DJ</th>
<th>Measured DJ</th>
</tr>
</thead>
<tbody>
<tr>
<td>500 KHz</td>
<td>62</td>
<td>97.1 ps</td>
<td>99.0 ps</td>
</tr>
<tr>
<td>1 MHz</td>
<td>45</td>
<td>74.9 ps</td>
<td>79.0 ps</td>
</tr>
<tr>
<td>5 MHz</td>
<td>8</td>
<td>26.7 ps</td>
<td>29.2 ps</td>
</tr>
<tr>
<td>20 MHz</td>
<td>3</td>
<td>20.2 ps</td>
<td>21.1 ps</td>
</tr>
</tbody>
</table>

Phase interpolator linearity has no effect of CDR LBW and jitter transfer function. However, it degrades the jitter tolerance (JTOL) [36]. In detail, for frequency offsets less than the slew rate of the CDR, the JTOL is degraded by the worst $DNL$. 

**Figure 5.21:** PLL I/Q phase mismatch from ideal $\frac{\pi}{2}$. The measurement was done from 5 to 7 GHz at room and 90°C case temperature.
Figure 5.22: Simulated and measured $DNL$ at 5.25, 6 and 6.75 Gbps where the $IQ$ phase mismatch is approximately $15^\circ$, 0 and $-15^\circ$ respectively. An Agilent 86108A precision module was used for the measurement.
5.4.3 Equalizer Characterization

A 35-inch Nelco-4000 backplane plus two 5-inch line cards have been used for demonstrating equalizer performance. The measured channel response is shown in Figure 5.27 and has 23-dB loss at 3.5 GHz.

Figure 5.28 shows the test set up and plots the eye after the CTLE and CDR for four different channels at 7 Gbps with PRBS 23 pattern. The eye is completely closed after the channel at 7 Gbps. In all four channels, the CTLE opens the eye. The data eye after the CTLE exhibits high deterministic jitter. The CDR filters the jitter from the CTLE to lower the total jitter. Table 5.3 provides the jitter performance of the eye after CTLE and CDR after the signal attenuates by the 45-inch backplane. The relationship between the deterministic jitter \( DJ \) and random jitter \( RJ \) is generally provided based on a given BER. For a BER of \( 10^{-12} \), the total jitter \( TJ \) is

\[
TJ = DJ + 14 \cdot RJ. \tag{5.17}
\]

where 14 is the \( rms \) to peak-to-peak conversion factor for a BER of \( 10^{-12} \). For lower BER, the conversion factor increases. A more detailed discussion is provided in [29].

Figure 5.23: Predicted \( \Theta_{dither} \) from the measured DNL. The pattern follows the analytical prediction presented in Section 5.1.
Figure 5.24: Measured bathtub curve. The frequency with IQ phase mismatch show smaller error free window. At 6 Gbps the window is more open due to perfect IQ phase. The error free window is smaller for 5.25 and 6.75 Gbps due to IQ phase mismatch.

Before the CDR, the DJ is high while the RJ is low. Ideally, the DJ is eliminated by the CDR. However, the dual-loop CDR introduces DJ due to the IQ clock mismatch and dithering. The CDR eliminates around 33% of the DJ in all four channels at the cost of around 1.75 ps of random jitter. All four channels demonstrate a total jitter that is one-half of the original TJ.

Table 5.4 provides a comparison between this work and some recently published papers. A low energy efficiency of 9.7 pJ/bit and high data rate of 28 Gbps are highlight of its performance.

5.5 Chapter Summary

Dual-loop CDRs were demonstrated for energy efficient multilane serial links. An analysis of phase INL and DNL as a function of clock IQ phase mismatch is presented for dual loop CDRs and predicts the BER for synchronous and non-synchronous links. A four channel signal conditioning receiver for high-speed signal was designed and fabricated in 130 nm CMOS technology. All channel share a single PLL that generates and distributes quadrature clock phases to each
Figure 5.25: The measured RMS jitter for three different data rates. The overall RMS jitter due to device noise and dither factor. The 5.25 and 6.75 GHz have a phase mismatch of 14.3° and −16.7° respectively. Consequently they show higher jitter at 1st and 2nd quadrant.

channel for data recovery. The die occupies an area of 1930μm by 1250μm and consumes 67.9 mW per channel. The CDRs achieve a maximum data rate of 7 Gbps per channel for 0 and ±200 ppm clock frequency deviation. For an aggregated data rate of 28 Gbps the energy efficiency of the system is recorded at 9.7 pJ per bit. Analytical, simulated and measured results are corroborated.

Acknowledgments

Chapter 5, is in part mostly a reprint of the material as it appears IEEE Transaction on Circuit and Systems-I, 2013, N. Kalantari; J. F. Buckwalter. This dissertation author was the primary author of these materials and co-author has approved the use of the material for this dissertation.
Figure 5.26: (a) CDR jitter transfer at 6 GHz (b) CDR jitter tolerance at 5.25, 6 and 6.75 GHz
Figure 5.27: Measured channel response of 45-inch trace. It is a 35-inch Nelco-4000 backplane plus two 5-inch line cards.

Table 5.3: Jitter performance of the EQ and CDR after a 45-inch backplane at 7 Gbps.

<table>
<thead>
<tr>
<th>Output</th>
<th>$DJ (ps)$</th>
<th>$RJ (ps)$</th>
<th>$TJ (ps)$</th>
</tr>
</thead>
<tbody>
<tr>
<td>CTLE1</td>
<td>69.71</td>
<td>1.57</td>
<td>91.23</td>
</tr>
<tr>
<td>CDR1</td>
<td>19.82</td>
<td>1.71</td>
<td>43.41</td>
</tr>
<tr>
<td>CTLE2</td>
<td>63.85</td>
<td>1.62</td>
<td>85.71</td>
</tr>
<tr>
<td>CDR2</td>
<td>18.14</td>
<td>1.73</td>
<td>41.85</td>
</tr>
<tr>
<td>CTLE3</td>
<td>64.28</td>
<td>1.69</td>
<td>87.42</td>
</tr>
<tr>
<td>CDR3</td>
<td>17.85</td>
<td>1.85</td>
<td>51.14</td>
</tr>
<tr>
<td>CTLE4</td>
<td>69.98</td>
<td>1.57</td>
<td>91.70</td>
</tr>
<tr>
<td>CDR4</td>
<td>15.71</td>
<td>1.82</td>
<td>42.71</td>
</tr>
</tbody>
</table>
Figure 5.28: The 45-inch test bench schematic, the closed eye at the output of the channel and the performance of the CTLE and CDR of the four channel receiver. The Time and voltage per division are 25 ps and 85 mV respectively.
**Table 5.4**: Performance comparison of this work and some recently published papers.

<table>
<thead>
<tr>
<th>Reference</th>
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<th>Energy Efficiency (pJ/bit)</th>
<th>Area (mm²)</th>
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Chapter 6

Conclusion

Power amplifiers are essential blocks in any wireless system. Since the power amplifiers are the main power consumer, they get a great deal of attention. For high range applications such as cellular phones, the wireless systems use standalone PAs in III-V materials because they provide higher output power and better efficiency. Advancement in Si/SiGe has encouraged designers to integrate PAs along with the rest of the system in one die. The challenge of power efficiency and output power increases as the frequency enters the mm-wave band. The devices need to operate at frequencies closer to their $f_t, f_{max}$. Therefore, device maximum available power gain (MAG) drops which comes with lower power added efficiency (PAE) as a penalty. Additionally, faster devices come with lower breakdown voltage. Consequently, to achieve higher output power, device current should be increased. This requires larger device size in which the effect of parasitic elements are worse. Power combining is an alternative approach to get higher output power. However, due to losses associated with the power combining elements, the overall gain and efficiency of the system drop. Power combiners are mainly large in size and area consuming as well which is not desirable.

Another challenge at mm-wave band is passive elements. Capacitors, inductors and transmission lines are used for matching purposes in power amplifiers. At higher frequency, their losses go high and their quality factors drop. All these factors come with less efficient system. The first portion of this dissertation focus was on mm-wave power amplifiers in SiGe and the materials were presented in
Chapter 2, 3 and 4.

In Chapter 2, the author presented a Q-band Wilkinson power combined class-E power amplifier in 120 nm SiGe HBT process. It demonstrated with a maximum PAE of 18% at 45 GHz at a 1.2 V supply voltage and a maximum saturated output power of 19.4 dBm (87 mW) with a PAE of 14.4% at 42 GHz at 2.4 V supply voltage. The extracted PAE for each individual PA cell was calculated 22% and 19.8% for 1.2 V and 2.4 V supply voltage respectively.

Chapter 3 went over a W-band tapered constructive wave power amplifier. The PA was demonstrated in a 120 nm SiGe HBT process. The amplifier had a 3-dB bandwidth of 19 GHz from 91-110 GHz and maximum gain of 12.5 dB at 101 GHz. It reached a $O P_{1dB}$ of 4.9 dBm (3.1 mW) at 98 GHz. Saturated output power was measured 5.9 dBm (3.9 mW) at 97 GHz with a PAE of 7.2%. The compact chip occupied an active area including pads of 0.22 mm$^2$.

In Chapter 4 a new PA circuit was demonstrated to eliminate explicit input and output matching networks with a reactive feedback mechanism which allows high power and high efficiency. It takes advantage of $C_\mu$ as part of its matching network. Additionally, the dynamic feedback mechanism through the network input capacitance, $C_i$, and the device input capacitance, $C_\pi$, prevents the PA of going to early compression. Therefore, the PA achieved its maximum efficiency close to its saturated output power. The PA had three stages and occupied 1160 $\mu$m by 900 $\mu$m including pads. The small-signal gain of the PA had a peak of 18.7 dB at 38 GHz. A maximum PAE of 20% and of 23 dBm (200 mW) was achieved for of 2.4 and 3 V, respectively, at 38 GHz. This was the highest reported output power from a single-stage PA in the SiGe process at Q-band at the time of publication. The PA performed over 5 GHz of bandwidth from 36 to 41 GHz.

The second part of this dissertation focus was on high speed serial link. As the data rate goes higher the margin for jitter drops and the bit error rate increases. More channel equalization is required which comes with more power consumption and less energy efficiency per bit. Additionally, the signal integrity issues rise at higher frequencies as the speed limits are more severe on interconnects, packaging and channels compare to the chips. To avoid these issues, Parallel tran-
mission of serial links are suggested to increase the throughput. To avoid usage of VCOs for each link, dual loop CDRs with phase interpolators are recommended instead of the traditional approach. However, phase mismatch due to the circuit non-idealities increases the bit error rate (BER). In Chapter 5 an analysis of phase integral non-linearity (INL) and phase differential non-linearity (DNL) as a function of quadrature clock ($IQ$) phase mismatch was presented for dual loop CDRs. Jitter analysis for the random and deterministic sources were provided and the BER is predicted at the presence of clock $IQ$ phase mismatch. A 4-channel signal conditioner with channel equalizer and CDR for each link was designed and implemented in 130 nm CMOS technology and measures 1930 $\mu m$ by 1250 $\mu m$. The CDRs share one PLL through their phase interpolators. The CDRs operate from 100 Mbps to 7 Gbps. The aggregated data rate is recorded at 28 Gbps. The total power consumption of the chip was measured at 272 mW. That indicates an energy efficiency of 9.7 pJ per bit for the system. All the analytical, simulated and measured results were corroborated.

6.1 Recommendations for Future Work

At mm-wave, power amplifiers suffer from low output power and low efficiency. To have higher output power either bigger devices are used or power combining techniques are applied. Each approach faces higher loss due to the worse parasitic elements of big devices or losses associate with the passive power combiners. Spatial power combining can be used to avoid the on chip power combining loss. As another approach, since the silicon on isolater (SOI) technology is advancing, the designer can take advantage of the MOS devices with no bulk. This technology does not face the limits of body effect and active devices can be cascaded on top of each other. This looks like a series of voltage sources whose final stage can provide high swing and as such high output power.

For the high speed serial links, usage of IQ VCO gets more complicated at mm-wave for 40 and 100Gbps applications. usage of delay cell can produce a 90° phase shift in a clock to produce the quadrature clock. Analog feedback
techniques can be used to make sure the phase mismatch is minimized. As the speed of devices is improving, design and implementing the analog feedback loop should be manageable these days. This eliminates the difficult tasks of VCOs running at twice of the frequency of operation, divide-by-2 circuits or usage of coupled VCOs for quadrature clock generation.
Appendix A

Scattering Matrix of a NeRF Power Amplifier

The circuit in Figure 4.3 consists of two shunt-shunt admittance ($Y$) networks $Y_L$ and $Y_A$. The first network $Y_L$ is a series inductance;

$$Y_L = \frac{1}{sL} \begin{bmatrix} 1 & -1 \\ -1 & 1 \end{bmatrix}. \quad (A.1)$$

The second network $Y_A$ is the transconductor with capacitive feedback. The impact of the base-emitter capacitance is initially ignored to illustrate the basic circuit principles, i.e. $C_x = C_s = 0$. Later, these capacitances are discussed. For simplification, $C_i = C_o$.

$$Y_A = \begin{bmatrix} \frac{sC_i + g_m}{1 + \frac{g_m}{sC_i} + \frac{C_i}{C_\mu||C_i}} & -s(C_\mu||C_i) \frac{sC_i}{1 + \frac{sC_i}{g_m}} \\ -sC_i & \frac{g_m}{sC_i} + \frac{C_i}{C_\mu||C_i} \end{bmatrix} \quad (A.2)$$

From feedback theory, the voltage gain is defined as the ratio of feedback and input impedance, $1/sC_i$ when the output port is open. Therefore, the voltage gain is defined by $A_v = \frac{C_i}{C_\mu}$.

The frequency response of a single stage is determined from the shunt-shunt
interconnection of (A.1) and (A.2). Thus, \( Y_S = Y_L + Y_A \):

\[
Y_S = \begin{bmatrix}
\frac{1}{sL} + \frac{sC_i + g_m}{1 + \frac{gm}{sC_i} + \frac{C_i}{C_\mu}} & \frac{-1}{sL} - \frac{sC_\mu}{gm} \cdot \frac{sC_i}{1 + \frac{gm}{sC_i} + \frac{C_i}{C_\mu}} \\
\frac{-1}{sL} - sC_i - \frac{C_i}{C_\mu} \cdot \frac{sC_i + g_m}{1 + \frac{gm}{sC_i} + \frac{C_i}{C_\mu}} & \frac{1}{sL} + \frac{sC_i}{1 + \frac{gm}{sC_i} + \frac{C_i}{C_\mu}}
\end{bmatrix}
\]  \( \text{(A.3)} \)

For (A.3), it is assumed \( C_i \) is larger than \( C_\mu \). In other words, the voltage gain \( A_v \gg 1 \).

A \( Y \) to \( S \)-parameter transformation is applied to (A.3) [18].
Appendix B

Effect of $C_\pi$ on the S-parameters of a NeRF Power Amplifier

At the presence of $C_\pi$, the notch frequency for input and output return loss is

$$\omega_{\text{notch}} - S_{11} = \frac{\left( \frac{1}{C_i Z_o} - \frac{C_i Z_o}{C_{\text{eff},\pi}} \right) \omega_t}{1 - \frac{C_i}{C_{\text{eff},\pi}} - C_i Z_o \omega_t}$$  \hspace{1cm} (B.1a)$$

$$\omega_{\text{notch}} - S_{22} = \frac{\left( \frac{C_{\text{eff},\pi}}{C_i^2 Z_o} - \frac{C_{\text{eff},\pi} Z_o}{C_{\text{eff},\pi} Z_o} \right) \omega_t}{1 - \frac{C_{\text{eff},\pi}}{C_i} - C_{\text{eff},\pi} Z_o \omega_t}$$  \hspace{1cm} (B.1b)$$

where $\omega_t = \frac{g_m}{C_\pi}$ is the transit frequency of the active device and $C_{\text{eff},\pi} = (C_i + C_\pi) || C_o || C_\mu$. In both (B.1a) and (B.1b), the notch frequencies approach $\omega_{\text{notch}}$ for $\omega_t \gg \frac{1}{C_{\text{eff},\pi} Z_o}$. For low $\omega_t$, they split apart and complicate matching.

Figure B.1 shows the input and output matching of a single stage nested-reactance feedback PA with the presence of $C_\pi$. As $f_t$ increases, both values approach each other such that the return loss and the input and output is indistinguishable.

The presence of $C_\pi$ reduces the gain ($S_{21}$) since there is voltage division ratio between $C_i$ and $C_\pi$. Ignoring $C_\mu$ for simplicity, the $V_\pi = V_i \frac{C_i}{C_i + C_\pi}$. This indicates lower gain for higher $C_\pi$. This, however, has the advantage of keeping the active device from compression at higher output voltage swings.
Figure B.1: $S_{11}$ and $S_{22}$ in the presence of $C_\pi$. The PA is tuned to 40 GHz for $C_i = 200 \ fF$, $C_\mu = 100 \ fF$, $L = 300 \ pH$ and $g_m = 1 \ S$ where $C_\pi = \frac{g_m}{\omega_i}$. 
Appendix C

Peak to Peak and RMS Values of Phase-Interpolated Clock

Equation C.1 shows the total peak to peak jitter where $k$ is the conversion factor to go between RMS and peak to peak (e.g. $k = 14.06$ for $10^{-12}$BER).

$$J_{pp} = J_{pp,\text{det}} + J_{pp,\text{rnd}}$$
$$J_{pp} = D_f \times QE + k \times J_{rnd}$$ \hspace{1cm} (C.1)

For example, assume a $J_{rnd} = 1.5\text{ps}$, a $D_{\text{factor}} = 4$ and a $QE = \frac{1\text{UI}}{128} = 7.82\text{m UI}$. At 6 Gbps, the $J_{rnd}$ is equal to $8.9\text{m UI}$. Thus for a BER of $10^{-12}$, $J_{pp,\text{det}} = 4 \times 7.82\text{m} = 31.28\text{mUI}$ and $J_{pp,\text{rnd}} = 8.9\text{m} \times 14.06 = 126.5\text{mUI}$ making a total peak to peak jitter of $J_{pp} = 157.8\text{mUI}$. As it is seen, the random jitter is almost 80% of the total peak to peak jitter. Ignoring the random jitter from the phase interpolator and buffer chain, this is the jitter from the PLL. That means in dual loop CDRs, the PLL jitter dominates the peak to peak value.

However, some standards such as SONET, specify RMS jitter value rather than the peak to peak one. In this case the QE of the phase interpolator need to be converted to RMS. For a loop with a dithering factor of $D_f$ it can be assumed the code oscillates from $-\frac{D_f}{2}$ to $\frac{D_f}{2}$ with equal probability$^1$. Therefore, the total RMS value can be presented as:

$^1$Note the equation does not have any meaning for $i=0$ and is not part of the summation.
\[ J_{\text{rms, det}} = \sum_{i=-\frac{D_f}{2}}^{\frac{D_f}{2}} (P(i) \cdot (2|i| - 1) \cdot \frac{Q E}{2}) \]  

where \( P(i) = \frac{1}{D_f} \). For example, the RMS jitter of the above phase interpolator with a dithering factor of 4 is equal to \( \frac{1}{4} \cdot 3 \cdot \frac{1}{256} \) and \( \frac{1}{4} \cdot 1 \cdot \frac{1}{256} \) for \( \pm 2 \) and \( \pm 1 \) making a total \( J_{\text{rms, det}} = 4.4\text{mUI} \). Now the total RMS jitter is \( J_{\text{rms}} = \sqrt{J_{\text{rms, det}}^2 + J_{\text{rms, rnd}}^2} = \sqrt{4.4^2m + 8.9^2m} = 10\text{mUI} \).

Interestingly, the RMS contribution of the CDR is 44% of the total RMS value where as its peak to peak is less than 20%. This is a common characteristic of CDRs with QEs. Their RMS jitter is much bigger than their peak to peak. As such they have difficulties meeting the timing requirements for applications such as SONET.[ref Ron document]
Bibliography


