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April 26, 1962
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ABSTRACT

Presented here is a design for a wide-bandwidth gain-control stage used in a pulse amplifier, Model 10-03 ns, that has a maximum voltage gain of 10 and a rise time (10 to 90%) of 3 nsec. Circuitry is not complicated by compensation difficulties, which have been circumvented by placing the potentiometer at a very low impedance node, and by using low values of potentiometer resistance.
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The realization of a continuously variable gain control functioning over a wide band of frequencies often results in relatively complicated circuitry because of the compensation required. The parasitic capacitance and inductance of available potentiometers when they are used in such gain control circuits, have made compensation necessary, especially when used on a relatively high-impedance node of an amplifying stage. The design used here circumvents the compensation difficulty by placing the potentiometer at a very low-impedance node, and by using low values of potentiometer resistance (see Fig. 1).

The first transistor, $Q_1$, provides an impedance match to the source and isolates it from the following circuitry. The minimum bandwidth depends upon the capacitance to ground at the collector of $Q_1$ shunting the maximum resistance value obtained by a potentiometer setting that corresponds to the half-gain position. As shown in Fig. 1, the capacitance to ground is $C_{ob}$ of $Q_1$, plus the stray wiring capacitance and the capacitance of the potentiometer, a total of approximately 10 pF. The maximum resistance to ground is $(70 + R_{in})/4$, with $R_{in} \approx kT/qI_e$, or \approx 2.0 ohms. If the gain setting is either higher or lower, the resistance to ground is smaller, hence, the bandwidth is larger, being equal to $1/RC$. 

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The relatively high impedance collector node of $Q_2$ is available for driving any subsequent circuitry. The variation in gain is from

$$0.93 \approx \frac{70}{70 + R_{\text{in}}} \quad \text{to} \quad 0.27 \approx \frac{20}{70 + R_{\text{in}}}.$$

The gain-control stage shown was used with pulse amplifier designed for a maximum voltage gain of 10 and a rise time, 10 to 90%, of 3.0 nsec (Fig. 2). Adding the gain-control stage made no observable change in the rise time of the fixed-gain portion of the amplifier.

The amplifier circuit consists of a diode current-limiting section followed by two stages of amplification employing shunt feedback with $R_C$ loading. These amplifying stages drive a low-impedance load of $Q_5$, a common-base stage, which realizes a voltage gain of about 4 to the base of $Q_6$. The last two transistors are a pair of emitter followers that develop the output voltage into a load of 50 ohms.
REFERENCES


FIGURE LEGENDS

Fig. 1. Wide-bandwidth gain control with matched input, high-impedance output. Gain variation (+ or - pulses) is 0.27 to 0.93.

Fig. 2. Pulse amplifier Model 10-03 ns. The rise time is 3.0 nsec, with an output limited to a maximum + and - swing of 1.5 V into a 50-ohm load. All capacitors are 6.8 μF/30 V dry tantalum. At all points where supply voltages are shown, additional capacitors are used as needed for accurate bypassing. All leads are kept as short as possible. Q7 is in a low-capacitance heat sink. All resistors are 1/2 watt, unless otherwise noted. Gain is 3 to 10, continuously adjusting and noninverting. Maximum output: ±1.5 V.

Fig. 3. Wave shape of amplifier output.
200 mV/cm

(10 nsec/cm)

(2 nsec/cm)

→ Time
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