Full-Band Impulse-Radio Ultra Wideband Transceivers With Integrated ESD Protection

A Dissertation submitted in partial satisfaction of the requirements for the degree of
Doctor of Philosophy
in
Electrical Engineering

by

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June 2011

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ACKNOWLEDGEMENT

This dissertation is prepared under the careful direction of Prof. Albert Wang. I really appreciate his tremendous patience, constructive advising, endless encouragement and warm help not only on my academic but also on my life in the past years at the University of California, Riverside. He sets up a good example for my future life with his dedicated working attitude, strong motivation and energetic passion on science and technology.

I would like to thank Professor Roger Lake and Professor Sheldon Tan for serving on my PhD Committee and proving valuable suggestions on my PhD dissertation. In addition, I would like to give sincere thanks to all the members in the Lab for Integrated Circuits and Systems at UC Riverside: Mrs. Lin Lin, Mr. He Tang, Mr. Hui Zhao, Mr. Qiang Fang, Mr. Jian Liu, Mr. Zitao Shi, Mrs. Li Wang, Mr. Zongyu Dong and Ms. Chen Zhang. I also want to thank Dr. Xiaokang Guan and Dr. Siqiang Fan from Fairchild Semiconductor, Dr. Haolu Xie from Fujitsu Semiconductor, Dr. Guang Chen from Freescale Semiconductor, Dr. Qiong Wu from NXP Semiconductor and Dr. Bo Qin from CitrusCom Semiconductor. Thank you so much for all your supports, discussions and advices. I learned a lot from my friends over the past years both in research and daily life.

My deep thank goes to my whole family. This dissertation would not be possible without the love, understanding and supports from my family.

The author also wants to thank SMIC and GSMC for wafer fabrication, as well as Omnivision Technologies, Inc. and Skyworks Solutions, Inc. for offering internship.
To my family.
The past decade has witnessed rapid proliferation of wireless communications, which continues to enjoy a booming growth driven by unprecedented technology advances and strong consumer demands. New wireless technologies are being developed to provide people with high-speed low-cost multi-mode multi-task wireless communication environments with high quality of service (QoS). Of all the proposed wireless techniques, ultra wideband (UWB) is a promising technology, which becomes a front contender for various extremely high data throughput wireless applications, particularly for wireless video streaming and wireless sea-volume data transformation typically requiring a data speed up to several giga bit per second (Gbps).

This dissertation describes research and integrated circuit (IC) implementation of a single-full-band carrier-free impulse-radio ultra wideband (IR-UWB) system. The IR-UWB transceiver adopts a simple-most-digital architecture with low design complexity, aiming to achieve the whole IR-UWB system-on-a-chip (SoC) in standard
complementary metal-oxide-semiconductor (CMOS) process. Detail analysis for the IR-UWB system architecture is provided. Critical circuit building blocks, such as pulse generator (PG), BPSK modulation, receiver front-end low-noise amplifier (LNA) and correlator, are described both theoretically and experimentally.

Adequate on-chip electrostatic discharge (ESD) protection is required for all IC chips and ESD protection design for radio-frequency (RF) IC emerges as a challenging design task as semiconductor IC technologies continue to advance into the very-deep-sub-micron (VDSM) regime. ESD protection for IR-UWB ICs is more challenging compared with narrow band IC designs. In this thesis, a novel ESD-RFIC co-design technique for UWB ICs was developed and experimentally verified. The interactions between ESD protection unit and core UWB IC were thoroughly investigated. The IR-UWB transmitter, front-end LNA and correlator ICs were designed with full ESD protection using the new ESD-RFIC co-design technique in this work.
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Chapter 1
Introduction
1.1 Wireless Communication Technologies

Wireless communication technologies are being rapidly proliferated in our daily life, which continue to enjoy a booming growth in cellular telephony, wireless internet, wireless local/personal area network (WLAN/ WPAN), wireless sensor network, etc. Many new wireless technologies are being introduced in order to serve people with broadband, high data throughput, high speed, multi-mode multi-task communication system with high quality of service (QoS). The demands from consumer electronics are raised not only to have traditional voice or paging service but also to have sea-volume digital data streaming like high definition, uncompressed, real time video and multimedia service, etc.

Of many wireless communication solutions, ultra wideband (UWB) technology is the one at forefront which offers the possibility and potential to support extremely high data rate and throughput with high QoS.

1.2 UWB History, Motivation and Advantage

Unlike other new wireless technologies, UWB is not a newly introduced concept but was first brought out in the year of 1960s. Early UWB systems were developed mainly as radar/sensing/military-oriented surveillance tool because they could see through trees/houses and beneath ground surfaces. UWB is a spread spectrum technology. But, UWB has its own difference differing from conventional spread spectrum technologies. It achieves data transmission via time-domain impulse-radio with the pulse width as short as nano-second or pico-second.
The milestone for UWB applications was occurred in Feb 2002, when the Federal Communication Commission (FCC) issued a ruling that UWB could be used for civilian radar and safety applications [1]. Since then, the world of UWB has changed dramatically recently in both industry area and university research institutes.

Wireless communications have gone through rapid development in recent years. As an example, nowadays it is easy for people to use their cell phone to browse internet, to download/upload files, to watch real time TV channel, to have face to face network conference, and a lot more. Several trends are driving short-range wireless in general and ultra-wideband in particular [2]. First is the growing demand for wireless data capability in portable devices at higher bandwidth but lower in cost and power consumption than currently available. Second concern is the crowding spectrum that is segmented and licensed by regulatory parities in traditional ways. Third is the growth of high-speed wired access to the internet in enterprises, homes, and public spaces. Fourth will be shrinking semiconductor cost and power consumption for signal processing. Fundamentally speaking, UWB is a candidate solution for broadband short range, high speed and portable wireless applications with low cost, low power consumption, longer battery life and high QoS.

FCC defined the UWB as a signal with a fractional bandwidth greater than 0.2 or which occupies more than 500MHz of spectrum. The fractional bandwidth is defined as $2(f_H - f_L)/(f_H + f_L)$, where $f_H$ and $f_L$ are the upper and lower frequencies, respectively, measured at -10 dB below the peak emission point. To allow government and industry to conduct UWB testing, frequency spectrum from 3.1GHz to 10.6GHz was allocated for
communications use below specified power levels, while imaging was limited to below 960MHz, as seen in Fig. 1.1 below. From Fig. 1.1 we can know the emitting power is very low for UWB, which means a much longer battery life. For indoor systems, the average output power spectral density is limited to -41.3dBm/MHz, which complies with the long standing Part 15 general emission limit to successfully control radio interference [3].

![FCC EIRP Power Mask For Indoor/Outdoor UWB Applications](image)

**Fig. 1.1** FCC EIRP power mask for indoor/outdoor UWB applications.

Why UWB? Or, why not choose others? An intuitive view from Fig. 1.2 can tell us the UWB communication system won’t cause any interference to current wireless communication standard like GSM, WCDMA, EDGE, WiFi, Bluetooth, GPS, etc. In
other words, UWB has “noise-like” signal for other standards, which also means it has a good communication security.

![Fig. 1.2 PSD comparisons for current wireless communication standards.](image)

The most attractive part for UWB is its broad bandwidth from 3.1-10.6GHz. For consumer electronics applications, engineers always want to increase the channel throughput via all kinds of methods. This 7.5GHz bandwidth potentially boosts the wide applications for UWB. From Shannon channel capacity theory as shown in Equation 1.1, where $C$ is the maximum channel capacity (bps); $B$ is the channel bandwidth (Hz); $S/N$ is the signal to noise ratio also known as SNR we can tell, if we want to increase channel capacity, intuitively, one can either increase SNR or increase the bandwidth. UWB utilizes its wide bandwidth feature to linearly increase the channel capacity.

$$C = B \log(1 + \frac{S}{N})$$  \hspace{1cm} (1.1)
To emphasize UWB’s high channel capacity, we explore Fig 1.2 further trying to find out the channel capacity for some typical standards. For IEEE 802.11b, it has a rated operating range of 100 meters. In the 2.4GHz ISM band, there is about 80MHz of useable spectrum. Hence, in a circle with a radius of 100 meters, three 22MHz IEEE 802.11b systems can operate on a non-interfering basis, each offering a peak over-the-air speed of 11Mbps. The total aggregate speed of 33Mbps, divided by the area of the circle, yields a spatial capacity of 1Kbps/m² approximately. Bluetooth, in its low-power mode, has a rated 10 meter range and a peak over-the-air speed of 1Mbps. Studies have shown that approximately 10 Bluetooth “piconets” can operate simultaneously in the same 10 meter circle with minimal degradation yielding an aggregate speed of 10Mbps [3]. Dividing this speed by the area of the circle produces a spatial capacity of 30Kbps/m² approximately. IEEE 802.11a is projected to have an operating range of 50 meters and a peak speed of 54Mbps. Given the 200MHz of available spectrum within the lower part of the 5GHz U-NII band, 12 such systems can operate simultaneously within a 50-meter circle with minimal degradation, for an aggregate speed of 648Mbps. The projected spatial capacity of this system is therefore 83Kbps/m².

UWB systems vary widely in their projected capabilities, but one UWB technology developer has measured peak speeds of over 50Mbps at a range of 10 meters and projects that six such systems could operate within the same 10-meter radius circle with only minimal degradation. Following the same procedure, the projected spatial capacity for this system would be over 1Mbps/m². Fig. 1.3 shows previous discussion result, indicating UWB has extremely high spatial capacity.
Fig. 1.3 Spatial capacity comparisons: IEEE 802.11, Bluetooth, and UWB [2]. Beyond UWB’s attracting channel capacity and security, it also has potentially low complexity and low cost. Since UWB is a time-domain technology, it transmits extremely short pulses, there is no need to employ complicated RF mixing stage at transceiver, greatly reducing the system complexity and cost. What’s more, in term of applications, UWB has a very wide range from high speed wireless personal network to locating, tracking, sensor, surveillance, etc.

1.3 UWB Proposals

For the UWB standard, there are two competing proposals: 1) the Direct Sequence Spread Spectrum UWB (DSSS), supported by the UWB Forum, which includes Freescale Semiconductor and a number of other small companies. 2) The Multi-band OFDM Alliance (MBOA) standard, supported by a consortium of leading semiconductor and consumer electronics companies such as Intel, TI, ST Microelectronics, Panasonic, Philips, Sony, and many others. Both proposals exhibit competitive features and advantages of their own, from the view of technology and view of business.
1.3.1 MBOA Standard

The MBOA standard proposes a channelized UWB system [4] as shown in Fig. 1.4. It divides the UWB spectrum into five bands. Each band consists of multiple channels of 528MHz. The Group 1 band has three mandatory channels for standard and current operation, while the remaining band groups are reserved for future use. Due to the multi-band approach, it provides maximal flexibility to comply with future regulatory UWB standards in other parts of the world (e.g. ETSI in Europe and MPHPT in Japan). The MBOA proposal is based on a proven Orthogonal Frequency Division Multiplexing (OFDM) technology used in the WLAN, which enables a higher chance of “first-pass” designs and short design cycles. Since OFDM technology is adopted, usually carrier is employed for frequency shifting. This proposal is supported by large semiconductor and IT companies like Intel, TI, and Microsoft, which focus initially on the U.S. PC market segment according to the FCC allocations. The MBOA regards UWB as an immediate replacement for the USB/Firewire technologies and, perhaps with the use of standard RF CMOS IC technologies will enable the integration of multiple radio front-ends. On the long run, the MBOA has the vision to support multiple protocol baseband architectures for the utilization of cognitive radio, which has been heavily backed up by FCC in recent times [5].
1.3.2 DSSS Standard

The DS-UWB standard proposes to use a dual-band impulse radio spread spectrum approach [6], which employs transmission of short duration pulses (in the sub-nanosecond range), with a bandwidth greater than 1GHz. It utilizes almost all of the UWB spectrum allocation, with the exception of having a null band for the 5.2-5.8GHz WLAN, as shown in Fig. 1.5 below.

The main goal of the DS-UWB approach is to provide low-cost, ultra high-rate, and ultra low-power solutions for handheld devices, with the primary focus on the Japanese consumer market, where the CRL-UWB Consortium is actively involved. One of the key advantages of the DS-UWB standard over that of the MBOA is the ability to scale up to ultra high data rates (up to 1.32Gbps) without increasing baseband circuit
complexity and power consumption. The report in [6] showed that as the data rate increases from 100 or 200Mbps to 1.32Gbps, the increase of the gate count for a DS-UWB system would be negligible, as opposed to an expected 110% increase in gate count for the MBOA system (i.e. from 455K to 954K). This is mainly due to the need for a higher order modulation scheme (i.e. 16-QAM) in MBOA, which would require a higher order ADC (i.e. 6bits), Viterbi decoder, and FFT engine, to keep up with the data rate. In DS-UWB, a simple and efficient binary phase shift keying (BPSK) modulation based on variable length spreading codes is used for all data rates. An optional support of a quaternary bi-orthogonal keying (4BOK) modulation provides performance improvement, but at a small expense of increasing circuit complexity.

An overview of the MBOA and DS-UWB proposal is summarized in Table 1.1.

Table 1.1 Summary of UWB proposals.

<table>
<thead>
<tr>
<th>Proposal</th>
<th>Number of Bands</th>
<th>Bandwidth</th>
<th>Band Group</th>
<th>Modulation</th>
<th>Data Rates</th>
</tr>
</thead>
<tbody>
<tr>
<td>MBOA</td>
<td>3 (Mandatory)</td>
<td>528 MHz</td>
<td>3.168-4.752 GHz</td>
<td>QPSK</td>
<td>53.3, 80, 110, 160, 200, 320, 400, 480 Mbps</td>
</tr>
<tr>
<td></td>
<td>11 (Optional)</td>
<td></td>
<td>4.752-6.336 GHz</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>6.336-7.920 GHz</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>7.920-9.5047 GHz</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>9.504-10.560 GHz</td>
<td></td>
<td></td>
</tr>
<tr>
<td>DS-UWB</td>
<td>2</td>
<td>1.75 GHz</td>
<td>3.1-4.85 GHz</td>
<td>BPSK</td>
<td>28, 55, 110, 220, 500, 660, 1k, 1320 Mbps</td>
</tr>
<tr>
<td></td>
<td></td>
<td>3.5 GHz</td>
<td>6.2-9.7 GHz</td>
<td>or 4-BOK</td>
<td></td>
</tr>
</tbody>
</table>
1.4 Full-band Impulse-radio UWB Transceivers with Integrated ESD Protection

We’ve briefly introduced the two UWB potential standards. Both of them divide the whole spectrum (mainly 3.1GHz to 10.6GHz) into several sub-bands. In this thesis, we proposed a single-full-band carrier-free impulse-radio based UWB (IR-UWB) communication system circuit-level design and implementations. Here we employ the original idea for UWB transceiver, employing extremely short duration pulse to achieve pulse shaping and data transmission in the whole 7.5GHz bandwidth, as shown in Fig. 1.6.

![Fig. 1.6 Channel and bandwidth of the proposed IR-UWB.](image)

Design considerations, implementations and verifications were provided for critical blocks such as UWB pulse generator, UWB transmitter, UWB low noise amplifier (LNA) and UWB correlator. To enhance the design robustness, electrostatic discharge (ESD) devices were introduced and embedded in each design block. The interaction between the ESD device and core IC block was investigated. An IC-ESD co-design flow was introduced and implemented. The performance was confirmed from Si verifications.

The dissertation is composed as following. In Chapter 2, the IR-UWB system overview is provided with transceiver system architecture, transmitter, channel model and receiver. In Chapter 3, the design methodology for UWB pulse generator has been
described in detail, including critical design parameters with regard to FCC power mask. Si measurement confirms the performance of the UWB pulse generator. In Chapter 4, author shows the IR-UWB transmitter design architecture and flow. Full Si measurement and discussion are also well explained. In Chapter 5, UWB front-end LNA has been explored. LNA architecture and design concerns are described. Full Si characterization has been conducted. Chapter 6 provides the UWB correlator design. Correlator structure and simulation results are depicted. For UWB transmitter, UWB LNA and UWB correlator, the ESD-RFIC co-design methodology has been well explained and implemented. Full ESD testing results and the interaction between ESD and core IC are also well described.
Chapter 2
IR-UWB System Overview
IR-UWB technique can transmit extremely short impulse trains for highly efficient wireless communications. If using the carrier-free and single 7.5GHz full band UWB (3.1-10.6GHz) scheme, IR-UWB radio has the huge potential to not only achieve the desired multi-Gbps wireless data rate, but also realize IR-UWB system chip in CMOS with simple RF transceiver architecture, simple BPSK modulation and simple digital baseband. Apparently, single-band carrier-free IR-UWB is a competent technology to eventually realize high-performance, low-power and low-cost CMOS UWB SoCs [7]. Before we go to detail circuit-level block design for IR-UWB system, it is beneficial to introduce the IR-UWB from system point of view. In this chapter, a systematic overview of a single-full-band carrier-free impulse-radio based UWB application has been described, including transmitter, channel and receiver.

2.1 IR-UWB System Architecture

Impulse radio is a UWB digital data communication system for low power, narrow range and high speed application [8]. The brief transmitter and receiver structure for an IR-UWB application is shown in following Fig. 2.1 and Fig. 2.2, respectively.

Fig. 2.1 UWB transmitter architecture.
Fig. 2.1 describes the transmitter architecture for an IR-UWB system. The IR-UWB transmitter consists of a clock source, modulation, pulse shaping block and antenna. One of the great benefits for UWB transmitter relative to impulse radio is that there is no need to employ complex circuitry such as frequency synthesizers which contains phase locked loop (PLL), voltage controlled oscillators (VCO) and mixers [2]. What’s more, due to FCC’s EIRP power mask, the averaging emitting power from 3.1GHz to 10.6GHz is below -41.3dBm/MHz, which means the total emitted power is approximately 0.55mW. So, there will be no power amplifier (PA) needed to boost the emitting power. For PA, PLL, VCO and mixers, they are critical parts for conventional transmitters have complex structure; they are difficult to implement from design point of view and expensive from cost point of view. On the other hand, for an IR-UWB transmitter, the design cycle is short, it is moderately easy to implement and the cost is low especially for mass production for consumer electronics since there are no additional complex circuitry employed.

Fig. 2.2 UWB receiver top level architecture.

15
Fig. 2.2 shows the IR-UWB receiver architecture, containing receiver antenna, low noise amplifier (LNA), reference circuitry, correlator and analog to digital converter (ADC) and baseband (BB) digital signal processing (DSP). The reference circuit will generate the pulse template for direct converting in a multiplier, then the integrator serves as a low pass filter and then the signal will feed into ADC for further signal processing. From Fig. 2.2 we can see, the receiver structure is moderately simple and easy to implement. However, accurate synchronization, high speed correlation and digitization are still in need for applications for high QoS.

Based on the discussion above, we proposed a single-full-band, carrier-free, impulse-radio UWB system architecture as shown in Fig. 2.3 below. The transmitter is composed of IR-UWB pulse generator, IR-UWB BPSK modulation circuitry; the receiver consists of a full band IR-UWB LNA, IR-UWB pulse template generator, a correlation type demodulator, timing and power control circuitry and high speed low resolution ADC.

![Fig. 2.3 IR-UWB transceiver architecture.](image)
In following sections in the chapter, more detail will be introduced for IR-UWB transmitter, channel and receiver.

2.2 IR-UWB Transmitter

2.2.1 FCC EIRP Power Mask

All radio communication applications are subject to different regulations about how much power it can emit at output in a specific frequency band. The purpose is to prevent interference to other subscribers nearby or in same frequency band [9]. For UWB applications, as described in Fig. 1.1, FCC regulated the spectrum of UWB signaling. Table 2.1 shows the spectral mask mandated by FCC for indoor and outdoor UWB systems. The power spectrum density (PSD) of the emitted UWB signal must be well controlled to avoid confliction with FCC EIRP regulation for UWB applications.

<table>
<thead>
<tr>
<th>Frequency Band (GHz)</th>
<th>Indoor EIRP Limit (dBm/MHz)</th>
<th>Outdoor EIRP Limit (dBm/MHz)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0-0.96</td>
<td>-41.3</td>
<td>-41.3</td>
</tr>
<tr>
<td>0.96-1.61</td>
<td>-75.3</td>
<td>-75.3</td>
</tr>
<tr>
<td>1.61-1.99</td>
<td>-53.3</td>
<td>-63.3</td>
</tr>
<tr>
<td>1.99-3.1</td>
<td>-51.3</td>
<td>-61.3</td>
</tr>
<tr>
<td>3.1-10.6</td>
<td>-41.3</td>
<td>-41.3</td>
</tr>
<tr>
<td>&gt;10.6</td>
<td>-51.3</td>
<td>-61.3</td>
</tr>
</tbody>
</table>
2.2.2 IR-UWB Pulse Shaping

Since the PSD of IR-UWB emitted signal is directly related with pulse type, pulse width and amplitude, so, pulse shaping is critical for any IR-UWB applications. Pulse generator is the key circuit block in an IR-UWB system, which generates UWB impulse signal trains for both transmitting and receiving channels. Critical aspects for designing UWB PG ICs include the followings. Firstly, the UWB pulse width must be very short and well-controlled to ensure very high data rate up to Gbps. Secondly, the pulse shape should be optimized for the desired UWB power spectrum density (PSD). Thirdly, the generated UWB pulse trains must be complied with the FCC EIRP power mask while allowing maximum signal emission. Fourthly, low-power design is desirable for many mobile and hand-held applications. Fifthly, a CMOS based PG design is highly desirable for low-cost and low-power UWB SoC [10]. Potential UWB impulse waveforms include Gaussian pulse, Hermit pulse, Rayleigh pulse, chirp signal, etc. Among these candidates, Gaussian pulse and its derivatives are preferred because of its condensed PSD property and lower side-lobe compared to others [11].

Equation 2.1 and 2.2 show the zero order and first order Gaussian pulse mathematical expression in time domain, where \(A_0\) and \(A_1\) is amplitude parameter, \(\sigma\) is standard derivation also called time constant, \(t\) is time.

\[
G_0(t) = A_0 \left(\frac{1}{\sqrt{2\pi\sigma}}\right) \exp\left(-\frac{t^2}{2\sigma^2}\right) \tag{2.1}
\]

\[
G_1(t) = A_1 \left(\frac{-t}{\sqrt{2\pi\sigma^3}}\right) \exp\left(-\frac{t^2}{2\sigma^2}\right) \tag{2.2}
\]
For higher order Gaussian pulses, the time domain mathematical expression is shown in following Equation 2.3 where \( n \) is the order number.

\[
G_n(t) = -\frac{n-1}{\sigma^2}G_{n-2}(t) - \frac{t}{\sigma^2}G_{n-1}(t) \quad (n \geq 2)
\]  (2.3)

The power spectrum density of Gaussian waveform and its derivatives is shown in Equation 2.4, where \( T_f \) is the reciprocal of pulse repeating frequency.

\[
e_n(f) = \frac{A^2}{T_f} (2\pi f)^{2n} \exp\left[-(2\pi f\sigma)^2\right] \quad (n \geq 0)
\]  (2.4)

Fig. 2.4 and Fig. 2.5 show the Gaussian waveform and its higher order derivatives in time domain and PSD respectively.

![Gaussian pulse and its derivatives in time domain.](image-url)
Fig. 2.4 shows the time domain waveform for $0^{th}$-, $1^{st}$-, $2^{nd}$-, $5^{th}$- and $7^{th}$-order Gaussian waveform. As we can see from Fig. 2.5, for higher order Gaussian waveforms, the central frequency will move from baseband to high frequency end. And what's more, we prefer to have the center of PSD locating at around 6.85GHz, which is central point of 3.1GHz-10.6GHz. For example, from Fig. 2.5, $5^{th}$-order Gaussian pulse is a good candidate for UWB pulse shaping. However, different kind of UWB application might choose different kind of UWB pulses, it also depends on applications.

### 2.2.3 IR-UWB Modulation Scheme

The purpose of pulse shaping is to choose a proper waveform to carry the user information so that we can achieve data transmission. The function of modulation is to add user's data information into analog UWB pulse. In UWB systems there are several basic methods of modulation and they will be described in this section in detail.
Intuitively, there are two kinds of modulation, one is time based and the other is shape based.

\section*{A. Pulse Position Modulation}

Pulse position modulation (PPM) belongs to time based modulation. It is one of the most common modulation methods in the literature. Each pulse is delayed or sent in advance of a regular time scale. Then, a binary communication system can be established with a forward or backward shift in time. By specifying different time delays for each pulse, an M-art system can be created. For example, we can create the data by the delay parameter $\tau_i$ to create pulses $S_i$ as shown in Equation 2.5 where $t$ represents time.

$$s_i(t) = p(t - \tau_i) \quad (2.5)$$

To make it easy, if we only have $i=1$ and $i=0$, then we will have two symbols with $S_i(t)=p(t - \tau_i)$ and $S_0(t)=p(t - \tau_0)$.

The advantage of PPM mainly arises from its simplicity and the ease with which the delay may be controlled. On the other hand, for the UWB system extremely fine time control is necessary to modulate pulses to nano-second or pico-second accuracy.

\section*{B. Pulse Amplitude Modulation}

Pulse amplitude modulation (PAM) is a form of signal modulation where the message information is encoded in the amplitude of a series of signal pulses. For example, to employ zero order Gaussian pulse as pulse shaping, we can have following Equation 2.6 and 2.7 to standard for “0” and “1” respectively using PAM method.

$$S_0(t) = A_0 \left( \frac{1}{\sqrt{2\pi\sigma}} \right) \exp\left(-\frac{t^2}{2\sigma^2}\right) \quad (2.6)$$
In some PAM systems, the amplitude of each pulse is directly proportional to the instantaneous modulating-signal amplitude at the time the pulse occurs. In other PAM systems, the amplitude of each pulse is inversely proportional to the instantaneous modulating-signal amplitude at the time the pulse occurs. In still other systems, the intensity of each pulse depends on some characteristic of the modulating signal other than its strength, such as its instantaneous frequency or phase.

C. On-Off Keying

On-off keying (OOK) is similar with PAM discussed above. For UWB applications, it can be characterized as a type of pulse shape modulation where the shape parameter $s$ is either 0 or 1, as shown in Equation 2.8 as following

$$ s_i = \sigma_i p(t) \quad \sigma_i = 0 \text{ or } 1 $$

For example, the “on” pulse is created when $\sigma_i=1$ and the “off” pulse when $\sigma_i=0$, resulting $S_1=p(t)$ and $S_2=0$. The major difficulty of OOK is the presence of multipath, in which echoes of the original or other pulses make it difficult to determine the absence of a pulse. On-off keying is also a binary modulation method but it cannot be extended to an M-ary modulation method.

D. Binary Phase Shift Keying

Binary phase shift keying (BPSK) is the simplest form of phase shift keying (PSK). It employs two phases which are separated by $180^\circ$ in pulse and so can also be called as 2-PSK, or bi-phase modulation (BPM). BPM is easily understood as the
inversion of a particular pulse shape, and we take the following equation to create a binary system based on inversion of the basic pulse \( p(t) \).

\[
S_i = \sigma_i p(t) \quad \sigma_i = \pm 1
\]  

(2.9)

For a binary system the two resultant pulse shapes can be defined as \( S_1 = p(t) \) and \( S_2 = -p(t) \). One of the reasons for the use of bi-phase modulation is the 3-dB gain in power efficiency. What’s more, BPSK is an opposite modulation method and PPM is an orthogonal modulation method. For PPM, since it must always waste the time when pulses are not transmitted. If PPM delays by one pulse width, then BPSK can send twice the number of pulses and then it can achieve a system which, given all other things being equal, having twice the data rate. Another benefit of using BPSK is that the mean of \( \sigma \) is zero. Therefore, it has the benefit of removing the comb lines or spectral peaks.

Fig. 2.6 summaries the discussion above and demonstrates the time domain waveform for PPM, PAM, OOK and BPSK signals.

Fig. 2.6 Time domain waveform for PPM, PAM, OOK and BPSK.
2.3 UWB Channel Model

The propagation environment which the signal passes through from a transmitter to a receiver is referred to as the channel [9]. Due to the wideband nature for UWB applications, the propagation phenomena are different in lower band and higher band of spectrum [8].

The IEEE 802.15.TG3a has evaluated lots of indoor and indoor-outdoor channel models to determine which model is fit for the UWB channel characteristics. Among these models, the modified Saleh-Valenzuela model (SV) [12] is recommended by IEEE as a reference channel model [8]. For UWB channel model, due to UWB pulse’s fine delay resolution, the multipath arrivals are in clusters rather than in a continuum. UWB channel measurements also show that the fading amplitudes follow a lognormal or Nakagami distribution. IEEE 802.15.TG 3a gave the final report of WPAN (Wireless Personal Area Network) in Feb, 2003. It provides a detailed channel model for UWB communication systems.

The IEEE 802.15.3a’s channel gives a detailed description of UWB channel model and it is an important step for the research of UWB channels. A lot of work has been done [13-16] for and will be done to complete the channel model and localization so that it is much more precise and convenient for UWB communication system design. This thesis is focusing on design and implementation of UWB transceivers, for detail UWB channel models and indoor/outdoor measurements, the readers can refer to literature reference like [8, 9] and [12-14,17].
2.4 IR-UWB Receiver

Recall from Fig. 2.2 the author shows the IR-UWB receiver architecture. Let’s replot it with UWB pulse information in Fig. 2.7 as following.

![IR-UWB Receiver Diagram](image)

**Fig. 2.7 IR-UWB receiver top level structure.**

After the receiver antenna, LNA serves as the front end amplifier. There is a template reference circuit which generates the UWB pulse template which will feed into the multiplier in proceeding stage. Since for IR-UWB system, there is no carrier employed, in other words, there is no frequency shifting, so a simple time domain direction conversion should be enough for signal demodulation. The multiplier will take the reference input and radio frequency (RF) input and multiply them together to conduct a correlation type demodulation. An RC integrator block follows the multiplier serving as a low pass filter for signal processing, and then the output of integrator digitized by the high speed low resolution ADC circuit for digital signal processing or host applications. Synchronization, speed of correlator and power control should be well considered during actual design implementations.
Chapter 3
UWB Pulse Generator
3.1 UWB Pulse Generator Overview

Pulse generator is a critical block for IR-UWB system since it will generate the impulse for transmission at both transmitter and receiver. While simplifying the digital baseband design, RF design for 7.5GHz bandwidth full-band IR-UWB pulse generator (PG) is extremely challenging because one ought to simultaneously achieve full compliance with the FCC EIRP power emission requirement (-41.3dBm/MHz) and, preferably, full utilization of the available room under the FCC UWB power mask for both spectrum and power spectrum density (PSD). For example, it is preferred that a center frequency of 6.85GHz is designed upon, which means that the favored IR-UWB impulse width shall be less than one nanosecond. Designing fully-integrated, low-power, low-cost and sub-nanosecond CMOS PG across 7.5GHz is a clear technical challenge to any RF designer [11].

Many possible impulse waveforms may be used for IR-UWB signals, among which, Gaussian impulse is favored. References [18, 19] reported PG designs using step recovery diode and microstrip technique for pulse generation, which do not meet the integration, low-power and low cost requirements. Reference [20] reports a PG that up-converts the base band signal directly to the UWB frequency band using a fairly complicated topology at cost of power. [21] depicts a complex digital approach to generate 3ns 47pJ/pulse modulated pulses for a narrower band 3-5GHz transmitter that requires an off-chip high-pass filter for FCC compliance. [22] presents a Gaussian PG with complex calibration to produce accurate 1ns pulse that consumes a high power of 1.8nJ/pulse and has a large die size of 1.95mm². [23] discusses modulated 17ns PG for 7-
9GHz band with programmable carrier, where the bandwidth and pulse width limit the wireless data throughput. [24] describes a relatively simple 8-delay-cell 5th-derivative Gaussian pulse generator that consumes a power of 58pJ/pulse. [25] reports a 2nd-derivative Gaussian PG that requires on-chip balun and off-chip bandpass filter to produce FCC-compliant 1.5ns 63pJ/pulse pulses over 0.5-5GHz spectrum. A few high order Gaussian derivative PGs, such as a 5th-derivative Gaussian [26] and 7th-derivative Gaussian [27], are reported with good spectrum performance and FCC compliance. [28] presents a high order quasi-Gaussian PG using step recovery diode and discrete microstrip reflection network. [29] describes a complex VCO-based 1st-order UWB PG that consumes large power and size. [30] uses NAND/NOR gates to generate 0th-order Gaussian pulses. In [31], VCO is employed for UWB pulse shaping. [11] gave a good summary of UWB Gaussian and its higher order derivative PG from methodology and implementation point of view.

3.2 Design Concerns for Gaussian UWB PG

From discussion of section 2.2.2, we conclude that Gaussian pulse and its derivative are good candidates for UWB PG. In this section, the design concerns for UWB PG using Gaussian related waveform are well explored.

We replot FCC EIRP indoor mask as shown in Fig. 3.1. From FCC PSD mask point of view, several critical points were marked, which forms the “red cap” profile. They are: 1) cap top which is -41.3dBm/MHz over 3.1-10.6GHz; 2) Center frequency which locates at 6.85GHz; 3) cap bottom which locate at 3.1GHz and 10.6GHz with PSD
of -51.3dBm/MHz. The emitter power spectrum density of the UWB pulse train should be within this mask to comply with FCC’s rule.

Fig. 3.1 FCC EIRP mask with “cap” and design information.
Fig. 3.2 (a) UWB pulse time domain design factor_zero order Gaussian, (b) related PSD of zero order Gaussian waveform.

We replot Gaussian waveform in Fig. 3.2 (a) as an example for time domain critical design parameters for a UWB pulse. The pulse shape, pulse width and pulse amplitude are three dominant factors for time domain. The design of UWB PG will become challenging when the pulse width is shrinking into only hundreds of pico-second.

The related PSD for zero order Gaussian waveform is shown in Fig. 3.2 (b). As we can see, the center frequency for zero order Gaussian pulse is locating at frequency zero, with a frequency span of approximately 8.6GHz. The PSD peak is determined by the amplitude of time domain waveform.
Combine both Fig. 3.1 and Fig. 3.2, we can see, the time domain waveform and its PSD are closely related, or, they are mapping to each other. During design phase, both of them should be well considered. Among design parameters, two of them are well considered in this UWB PG design, they are optimum frequency (also called center frequency) and peak to peak pulse amplitude [21].

### 3.2.1 Optimum Frequency $f_{opt}$

Equation 2.4 shows the PSD equation for Gaussian and its $n^{th}$-order derivative waveform. Differentiating Equation 2.4 against $f$ yields the $f_{opt}$ shown in following Equation 3.1, where $n$ is the derivative order of Gaussian waveform and $\sigma$ is standard derivation also called time constant.

$$ f_{opt} = \frac{\sqrt{n}}{2\pi\sigma} \tag{3.1} $$

The optimum center frequency, $f_{opt}$, should be set near center of the FCC UWB spectrum of 3.1-10.6GHz, i.e., $f_{opt} \approx 6.85\text{GHz} - 7\text{GHz}$. This $f_{opt}$ should correspond to the maximum allowed PSD peak of -41.3dBm/MHz to ensure that a Gaussian waveform fully complies with the FCC EIRP power mask while emits the highest possible signal power. Clearly, $f_{opt}$ is proportional to the square root of $n$ and inversely proportional to $\sigma$. It suggests that higher order Gaussian derivatives are favored to move $f_{opt}$ toward higher frequency, which, however, lead to more sophisticated PG circuitry. On the other hand, as $\sigma$ decreases, $f_{opt}$ will move to higher frequency more efficiently. We plot the $f_{opt} \sim \sigma$ with different order number and get Fig. 3.3. What’s more, the pulse width $\tau$ for Gaussian waveform and its derivatives is directly related with the time constant parameter $\sigma$. So,
with a proper center frequency range, the UWB pulse width can also be determined. Assume a $f_{\text{opt}} \sim 6.85\text{GHz}$ to best utilize the FCC power mask, one can obtain the required UWB pulse width for different FCC-compliant $n^{\text{th}}$-derivative Gaussian pulses as summarized in Table 3.1. For example, for a preferred $5^{\text{th}}$-derivative Gaussian PG, a very short UWB pulse width of 408ps is required in PG design.

![Optimum Frequency vs. Time Constant Parameter](image)

Fig. 3.3 $f_{\text{opt}} \sim \sigma$ with different order numbers.

Table 3.1 Estimated pulse width with $f_{\text{opt}} \sim 7\text{GHz}$ for Gaussian & its derivatives.

<table>
<thead>
<tr>
<th>Derivative Order</th>
<th>0</th>
<th>1$^{\text{st}}$</th>
<th>2$^{\text{nd}}$</th>
<th>3$^{\text{rd}}$</th>
<th>4$^{\text{th}}$</th>
<th>5$^{\text{th}}$</th>
<th>6$^{\text{th}}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>$\sigma$ (pS)</td>
<td>--</td>
<td>23</td>
<td>32</td>
<td>39</td>
<td>45</td>
<td>51</td>
<td>56</td>
</tr>
<tr>
<td>$\tau$</td>
<td>5$\sigma$</td>
<td>6$\sigma$</td>
<td>7$\sigma$</td>
<td>7$\sigma$</td>
<td>7$\sigma$</td>
<td>8$\sigma$</td>
<td>6$\sigma$</td>
</tr>
<tr>
<td>$\tau$ (pS)</td>
<td>--</td>
<td>138</td>
<td>224</td>
<td>273</td>
<td>325</td>
<td>408</td>
<td>336</td>
</tr>
</tbody>
</table>
3.2.2 Peak to Peak Amplitude $V_{pp}$

Equation 2.4 in Chapter 2 shows the PSD expression for $n^{th}$-order Gaussian pulses. Submit Equation 3.1 into Equation 2.4, we will get following Equation 3.3.

$$e_n \bigg|_{\text{max}} = \frac{A_n^2}{T_f} \left( \frac{n}{\sigma^2} \right)^n \exp(-n)$$  \hspace{1cm} (3.3)

To find the peak to peak pulse amplitude $V_{pp}$ in time domain, a FCC-mask-aware approximated method can be employed. Assume little variation in PSD around $f_{opt}$, we take the integration of Equation 3.3 within 1MHz and the total power should be -41.3dBm. Equation 3.4 shows the discussion above.

$$\int_{1MHz} \frac{A_n^2}{T_f} \left( \frac{n}{\sigma^2} \right)^n \exp(-n) = -41.3dBm$$  \hspace{1cm} (3.4)

The integration will result Equation 3.5 where the amplitude coefficient $A_n$ can be obtained under a specific pulse repeating frequency ($1/T_f$) for Gaussian pulse and its derivatives.

$$A_n = 2.723 \times 10^{-7} \cdot \sqrt{T_f} \cdot \sigma^n \cdot \left( \frac{e}{n} \right)^{n/2}$$  \hspace{1cm} (3.5)

After we get the amplitude coefficient $A_n$, submit Equation 3.5 into Gaussian time domain expression such as Equation 2.1, we will get the peak to peak amplitude $V_{pp}$. This will give the designer an intuitive view for pulse amplitude.

Table 3.2 shows the peak to peak amplitude for Gaussian pulse and its derivatives using the approximation method and Matlab simulation. From the data we can see, the approximation method is very accurate.
Table 3.2 Comparison of approximated PG $V_{pp}$ with Matlab simulation.

<table>
<thead>
<tr>
<th>Derivative Order</th>
<th>1(^{st})</th>
<th>2(^{nd})</th>
<th>3(^{rd})</th>
<th>4(^{th})</th>
<th>5(^{th})</th>
<th>6(^{th})</th>
<th>7(^{th})</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{pp}$-Matlab (mV)</td>
<td>943</td>
<td>922</td>
<td>660</td>
<td>668</td>
<td>536</td>
<td>540</td>
<td>467</td>
</tr>
<tr>
<td>$V_{pp}$-Approx. (mV)</td>
<td>946</td>
<td>923</td>
<td>661</td>
<td>669</td>
<td>536</td>
<td>540</td>
<td>468</td>
</tr>
</tbody>
</table>

3.2.3 Other Design Parameters

In section 3.2.1 and 3.2.2, we explore two important design parameters for UWB PG implementation. During design, we should also pay attention to the roll-off of PSD curve. As already shown in Fig. 3.1, for indoor applications, there are two corners, locating at 3.1GHz and 10.6GHz with the power level of -51.3dBm/MHz. To fully comply with FCC power mask while achieve the highest emission power, the -10dB bandwidth, i.e., the PSD roll-off frequency corresponding to a -10dB drop from the FCC-allowed -41.3dBm/MHz limit, must be considered in Gaussian PG designs. Using previous equations, the -10dB corner frequencies ($f_{1,2}$) can be determined from following Equation 3.6 where $P_1=P_2=-51.3$dBm, $B=10^6(A^2/T_f)(2\pi)^2$, $D=-4\pi^2\sigma^2$.

$$P_{1,2} = B \cdot f_{1,2}^{2n} \cdot e^{Df_{1,2}^2} \quad (n \geq 0) \quad (3.6)$$

The hand calculated -10dB corners for $n^{th}$-derivative Gaussian pulse listed in Table 3.3 agree well with Matlab simulation as shown in Fig. 3.4. It readily observed that a 4\(^{th}\)-order Gaussian would slightly exceed the FCC EIRP mask; the 6\(^{th}\) and 7\(^{th}\)-derivative Gaussian pulses comply with FCC EIRP mask, however are inefficient in using FCC power mask and complex in circuitry; a 5\(^{th}\)-order Gaussian PG seems to be the best fit for IR-UWB, we mark the curve of 5\(^{th}\)-order Gaussian waveform in red color in Fig. 3.4.
Table 3.3 Estimated -10dB corner frequencies for \( n^{\text{th}} \)-order Gaussian PGs.

<table>
<thead>
<tr>
<th>Derivative Order</th>
<th>1(^{\text{st}})</th>
<th>2(^{\text{nd}})</th>
<th>3(^{\text{rd}})</th>
<th>4(^{\text{th}})</th>
<th>5(^{\text{th}})</th>
<th>6(^{\text{th}})</th>
<th>7(^{\text{th}})</th>
</tr>
</thead>
<tbody>
<tr>
<td>( f_1 ) (GHz)</td>
<td>1.34</td>
<td>2.5</td>
<td>3.15</td>
<td>3.57</td>
<td>3.87</td>
<td>4.1</td>
<td>4.29</td>
</tr>
<tr>
<td>( f_2 ) (GHz)</td>
<td>15.15</td>
<td>12.57</td>
<td>11.45</td>
<td>10.8</td>
<td>10.37</td>
<td>10.04</td>
<td>9.8</td>
</tr>
</tbody>
</table>

Besides roll-off corner frequency, the PSD is also affected by pulse repeating frequency (PRF). For higher PRF, the PSD might go beyond FCC EIRP mask. So, careful attention need to be paid when design UWB PG.

3.3 UWB PG Design

In previous section, we talked about the design concerns for UWB PG. In this section, we will give detail description how the Gaussian and its higher order derivatives
are generated from circuit level. Directly mapping equations to create $n^{th}$-derivative Gaussian PG circuit results in very complicated and practically infeasible PG circuitry. Instead, a novel approximate Gaussian pulse generation algorithm is proposed to design practical low-power low-cost $n^{th}$-derivative Gaussian PGs.

### 3.3.1 Zero-order Gaussian Waveform

For Gaussian waveform, there are two mainly ways to generate from circuit level, one is to generate it according to Gaussian expression as shown in Equation 2.1. For example, [22] reports a Gaussian pulse generator using MOSFET operating in sub-threshold region to generate Gaussian waveform, which is very difficult for accurate control particularly under PVT variations. Alternatively, there is another way to generate Gaussian waveform using approximating method, such as [11], [24], [26] etc. To ensure low-power and low-cost, we choose to use the approximate method and MOS inverter circuitry is used because the capacitive load charging and discharging function gives the exponent operation for Gaussian pulse [32]. The topology of the new Gaussian pulse generator is shown in Fig. 3.5.

From Fig. 3.5 we can see, the Gaussian pulse generator consists of two cascade stages: square waveform generation and Gaussian pulse formation. The input of Gaussian PG is either sinusoidal or square waveform. When there is an input, a square wave with sharp rising and falling edge is generated, which drives the delay cell block to generate another delayed square wave. The two square waves A and B will feed into the NOR or NAND block and an approximated Gaussian waveform is then generated. Fig. 3.6 shows the waveform at A, B and output.
The width and amplitude of this Gaussian impulse signal is determined by the rising and falling times of the input square wave and the inverted delay stage transistor channel length. To further increase the drive capabilities and shorten the rising and falling times, a series of inverters with increasing size for each step can be used as the square-wave generator. The delay time between them can be controlled by adjusting the delay cell. Fig. 3.7 shows the circuit schematic of the Gaussian PG.
3.3.2 1st-order and 2nd-order Gaussian Pulse Generator

In previous section we talked about how to generate Gaussian waveform using approximation method, in this section, the method for how to generate 1st-order and 2nd-order Gaussian waveform will be discussed.

1st-order and 2nd-order Gaussian PG are based on zero-order Gaussian waveform. To generate 1st-order/2nd-order Gaussian waveform, a first order/second order derivative circuitry can be employed at the output of zero order Gaussian pulse generator. Fig. 3.8 shows the block diagram how these pulses are generated.
Equation 3.7 and 3.8 shows the function of derivative circuit in Fig. 3.8. 1st-order and 2nd-order derivative can be obtained from the equations.

$$G_1(s) = G_0(s) \frac{R}{R + 1/sC} \approx G_0(s) \cdot sRC \quad (R << 1/sC)$$  \quad (3.7)

$$G_2(s) = I_0(s) \frac{sRL}{R + sL + 1/sC} \approx I_0(s) \cdot s^2RLC$$  \quad (3.8)

3.3.3 5th-order Gaussian Waveform

Based on discussion before, 5th-order Gaussian could be the best candidate for UWB PG [10-11]. The center frequency should be selected properly to ensure that the pulse waveform can not only comply with the FCC EIRP power emission mask of less than -41.3dBm/MHz, but also take full use of FCC emission power cap to allow longer transmission distance and higher data rate at given transmission distance. On the other hand, it also favors an optimal pulse waveform filling up the whole 3.1-10.6GHz bandwidth as much as possible, i.e., the high/low corner frequencies, corresponding to the -10dB roll-off points from the peak, close to the 3.1GHz and 10.6GHz corners for the
main portion of the FCC UWB spectrum. With the above features, PG designs must also balance between pulse width, power efficiency, power dissipation, etc.

Following the method described from section 3.2, we will get detail design parameters for 5th-order Gaussian PG. Equations (3.9) and (3.10) depict the time domain pulse waveform and its PSD for the 5th-order PG circuit.

\[ G_5(t) = A \frac{-15\sigma^5 t + 10\sigma^2 t^3 - t^5}{\sqrt{2\pi\sigma^11}} \exp\left(-\frac{t^2}{2\sigma^2}\right) \]  

(3.9)

\[ \varepsilon_5(f) = \frac{A^2}{T_f} (2\pi f)^{10} \exp\left[-(2\pi f \sigma)^2\right] \]  

(3.10)

Equations (3.9) and (3.10) suggest that there is an optimal frequency \( f_{\text{opt}} \), corresponding to the EIRP peak of -41.3dBm/MHz in the PSD. By differentiating (3.10) with respect to \( f \) and setting it to zero, we have:

\[ \varepsilon_{5,\text{max}} = \frac{A^2}{T_f} \left(\frac{5}{\sigma^2}\right)^5 e^{-5} \]  

(3.11)

\[ f_{\text{opt}} = \frac{\sqrt{5}}{2\pi\sigma} \]  

(3.12)

Hence, to make full use of FCC power mask, an optimal \( \sigma \approx 51\text{ps} \) is obtained. With the definition for the pulse width \( \tau \) being the period, across which the accumulated energy is 99.99% of that over an infinite time span of a single pulse, the pulse width of 5th-order Gaussian pulse is calculated as \( \tau \approx 8\sigma = 408\text{ps} \), which ensures simultaneously complying with and taking full use of the FCC EIRP power mask as discussed previously. Next, as mentioned in Equation 3.4, the peak pulse amplitude of \( V_{pp} \) is derived by integrating
Equation 3.11 at $f_{opt}$ within a 1MHz bandwidth and set it to -41.3dBm, the optimal amplitude parameter $A$ can be obtained. Then, substitute $A$ into Equation 3.9, the optimum $V_{pp}\approx 536.8mV$ is obtained at a PRF=100MHz.

Fig. 3.9 shows the diagram for the simple 5th-order Gaussian PG consisting of a square waveform generator, a single delay line with four inverters, four Gaussian PGs (GPG) and one output stage. The square waveform generator produces a square pulse with sharp rising and falling time, which feed into the delay line stage. The single delay line generates four inverted and delayed square waveforms successively. The delay time can be adjusted by sizing the inverter devices. The GPG cells are used to generate the four required Gaussian pulses with different phase, amplitude and arrival time. GPG1 and GPG3 are NAND gates; GPG2 and GPG4 are NOR gates; all were properly sized for the desired Gaussian waveforms. The last stage consists of two push-pull cells, which serve to combine the incoming pulses into the desired 5th-order Gaussian pulse waveforms with proper polarities.

![Fig. 3.9 Diagram for 5th-order Gaussian PG.](image-url)
Fig. 3.10 shows the schematic for the digital combination 5th-order Gaussian PG circuit. During operation, the push-pull structure helps to reduce the power consumption because, at any time, only one transistor conducts during pulse generation.

3.4 Si Measurement and Discussion

The fully integrated 5th-order Gaussian pulse generator circuit was designed and implemented in SMIC 0.18µm RFCMOS technology. Fig. 3.11 shows the layout and die photo of the 5th-order Gaussian pulse generator, occupying a very small Si area of ~0.2mm² (including all testing pads) due to its all-digital architecture. Full measurement was conducted using Cascade RF-1 Probing Station, Tektronix AWG 520 Arbitrary Waveform Generator, Agilent DSO81304B Infiniium Oscilloscope, Agilent 4448A PSA Series Spectrum Analyzer and Agilent 4156C Precision Semiconductor Parameter Analyzer. The pulse repeating frequency is 100MHz for measurement.
Fig. 3.11 Layout (left) and die photo (right) for $5^{th}$-order Gaussian PG.

Fig. 3.12 Measured $5^{th}$-order Gaussian pulse train (upper) and single pulse curve (lower) comparing with ideal $5^{th}$-order Gaussian waveform.
Fig. 3.12 gives the measured pulse train (upper) and its single pulse waveform (lower) in time domain, which shows near ideal 5th-order Gaussian pulse waveform as predicted. The measured pulse width for the 5th-order Gaussian waveform is about 418pS, reasonably close to the simulated $\tau \approx 408pS$. The peak to peak amplitude is about 533mV, also very close to the expected $V_{pp} = 536.8mV$. Fig. 3.13 shows the measured PSD for 5th-order Gaussian pulse train via spectrum analyzer.

![Measured PSD for 5th-order Gaussian pulse train at 100MHz PRF](image)

Fig. 3.13 Measured PSD for 5th-order Gaussian pulse train at 100MHz PRF.

The total power consumption for the UWB PG is only 0.05pJ/p-mV under 100MHz input PRF. The ultra low power consumption means long lasting battery life. The proposed 5th-order Gaussian PG is suitable for IR-UWB applications.

Extra care must be exercised in measuring such higher-order Gaussian pulse signals with extremely short pulse width, because any losses and other parasitic effects
associated with the testers, including test fixtures, may affect testing result, hence, we must take into full consideration of all such parasitic effects during measurement.

![Graph](image1.png)

(a)

![Graph](image2.png)

(b)

Fig. 3.14 (a) Cable loss reported by manufacture, (b) RF probe loss-data from manufacture.
In testing procedure, it was found that substantial losses exist for the testing cables (2.4mm female to male, 50GHz, SN 05604670), RF probe (CASCADE 8828C ACP-GSG-150) and adapters (2.4mm to SMA connector), for S-parameter measurement. For example, the measured S21 curves for the RF probe and adaptors used in this work show substantial losses that much be carefully calibrated during any RF measurement. Fig. 3.14 (a) and (b) show the cable and RF probe loss reported by manufacture, also shows the measured loss from adapter, respectively. During the measurement, the cable and RF probe loss should be well considered and de-embedded from raw data.

As we can see from the Si measurement result, the approximation method works well to produce a 5th-order Gaussian waveform with simple architecture and ultra low power consumption. Table 3.4 compares the state-of-the-art UWB PG in various performance metrics.

<table>
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<th>Ref.</th>
<th>n&lt;sup&gt;th&lt;/sup&gt;</th>
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<th>τ (nS)</th>
<th>Vpp (mV)</th>
<th>Power (pJ/p-mV)</th>
<th>Area (mm&lt;sup&gt;2&lt;/sup&gt;)</th>
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<td>0.5µm CMOS</td>
</tr>
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Table 3.4 Comparison of similar 5<sup>th</sup>-order Gaussian PGs.
Chapter 4
UWB Transmitter with ESD Protection
4.1 UWB Transmitter Overview

Transmitter (Tx) is a critical and important block for UWB transceiver chain, it has several functionalities: pulse mapping, modulation, emitting power level control, etc. In section 2.1, we described the architecture of UWB transmitter.

There have been many UWB transmitter designs of various types reported recently. For example, [33] reported a CMOS IR-UWB Tx with DBPSK modulation, which contains digital locked loop (DLL), complex pulse generator (PG), power amplifier (PA), balun, etc. Reference [34] described a CMOS IR-UWB Tx with time hopping pulse position modulation (TH-PPM), which utilizes voltage-controlled oscillator (VCO), voltage-controlled delay lines (VCDL) and multiplexer. [35] presented a CMOS IR-UWB Tx employing VCO, multiplexer, triangle PG with no modulation mechanism. [36] depicted a PPM modulated IR-UWB Tx with localization into consideration using PLL, low pass filter (LPF), varying gain amplifier (VGA), RF balun and mixer. [37] discussed an on-off keying (OOK) IR-UWB Tx for wireless personal area network (WPAN) applications consisting of PG and VCO. [38] presented a low frequency band driver amplifier included UWB Tx with Gaussian pulse shaping and BPSK modulation. [39] demonstrated a BPSK modulated IR-UWB Tx with 5th-order Gaussian PG and on-chip balun. [20] reported a discrete BPSK UWB Tx with Gaussian pulse shaping employing mixers, filters and PA, etc. [40] and [41] reported UWB Tx using on-chip inductors. [42] presented an OOK UWB pulse generator with digital edge combiner, current driver and LC on-chip filters.
In this thesis, a new 5kV ESD-protected IR-UWB Tx employing 5th-order Gaussian PG and BPSK modulation with simple architecture and low circuit design complexity has been explained in detail.

4.2 UWB Transmitter Design

The proposed IR-UWB Tx is shown in Fig. 4.1. The Tx consists of two main functional circuit portions: data modulation block and pulse shaping block. In the design, no inductor, buffer or amplifier is employed, which helps to achieve low design complexity, simple circuit architecture and most-digital CMOS design.

![Fig. 4.1 Proposed IR-UWB transmitter architecture.](image)

We’ll give detail description for BPSK modulation block and pulse shaping block in following.

4.2.1 BPSK Modulation

Modulation is an important function for IR-UWB system. The information data will be modulated into special impulse trains by the modulation circuit block for wireless transmission. From Fig. 4.1 we can see, a simple BPSK modulation scheme is employed. BPSK is sufficient for Gbps data rate, because the UWB Tx utilizes an ultra wide 7.5GHz wideband. Generally, modulation can be done before or after the pulse shaping block in a
transmitter. For example, in [34] [36] and [37], modulation circuitry was placed before the pulse generators; while in [38] and [39], the modulation is conducted after the pulse generator. Fig. 4.2 shows the BPSK modulation scheme implemented in this design. The BPSK scheme was realized full digitally utilizing AND gates and inverters. The input clock can be either sinusoidal or square waveform. First, the clock signal is modulated by the incoming information data. As shown in Fig. 4.2, when data=1, the signal path A works; when data=0, the signal path B operates. Second, the signal lines A and B will feed the pulses into the 0º and 180º phase shifted 5th-order Gaussian pulse generators, respectively.

![Functional diagram for BPSK modulation and 0º/180º 5th-order Gaussian PG.](image)

**Fig. 4.2** Functional diagram for BPSK modulation and 0º/180º 5th-order Gaussian PG.

### 4.2.2 0º/180º 5th-order Gaussian PG

In section 3.3.3, we gave detail description for 5th-order Gaussian PG generation. Since BPSK modulation is employed, 0º and 180º phase 5th-order Gaussian waveform need to be generated. Following the same methodology from section 3.3.3, a 180º phase 5th-order Gaussian waveform can be generated. Fig. 4.3 shows the diagram how to generate 180º phase 5th-order Gaussian waveform.
Fig. 4.3 Schematic for 180° phase 5th-order Gaussian PG.

From description above, we can see, for the proposed structure in Fig. 3.10 and Fig. 4.1 to 4.3, there is no single-to-differential circuitry like balun needed, greatly reduce the Tx design complexity, die area and cost.

4.3 IR-UWB and ESD Co-design Methodology

Adequate electrostatic discharge (ESD) protection is required for all IC chips and ESD protection design for RF IC has emerged as a challenging design task in recent years [43-48]. As the semiconductor IC technologies continue to advance into the very-deep-sub-micron (VDSM) regime, ICs become increasingly more susceptible to ESD damages [43]. On one hand, any ESD protection structure will induce extra parasitic effects, such as, parasitic capacitance ($C_{ESD}$), resistance ($R_{ESD}$), substrate noise coupling and self-generated noises, etc, which may significantly affect core IC performance. On the other
hand, RF ICs are extremely sensitive to any parasitic effects. Further, many RF ICs are for hand-held devices that requires much higher ESD protection robustness, which generally translates into larger ESD protection structure and more ESD-induced parasitic effects [45]. Consequently, RF ICs, particularly the RF signal pins, often have inadequate on-chip ESD protection to avoid circuit performance degradation, while module and system level ESD protection is widely used [44]. This is particularly true to UWB ICs used for Gbps wireless communications where a moderate IC performance degradation may result in significant bit error rates. Hence, a well-argued on-chip ESD protection structure should be designed to ensure both adequate ESD protection and minimized ESD-induced parasitic effects. In addition, since ESD-induced parasitic effect is inevitable and RF IC is extremely sensitive to any parasitic effect, careful ESD-RFIC co-design becomes critical to recover any IC performance degradation induced by ESD parasitic effects [45]. Since UWB has ultra wide frequency bandwidth, ESD-UWB is more challenging compared with relatively narrower band ESD-RFIC co-design because of the tougher design re-matching requirements, which is the case for the full-band (3.1-10.6GHz) IR-UWB Tx IC in this work.

In this thesis, the author proposed the ESD-RFIC co-design methodology, shown in the flow diagram in Fig. 4.4. As shown in Fig. 4.4, there are two main design paths for ESD-RFIC co-design: ESD protection unit design and RFIC design.
Fig. 4.4 ESD-RFIC co-design methodology flow.
For ESD protection unit design, designers should have target ESD specification with ESD protection level, leakage current, structure and area, etc. During ESD design phase, an optimum design should come with good ESDV with minimum leakage, proper layout and smallest area. Then, the ESD unit itself will be sent to fabrication. Fig. 4.5 shows the ESD testing pattern for parameter extraction. After fabrication, ESD dies should go under lab testing with S-parameter, NF and Transmission Line Pulse (TLP) testing for all kinds of ESD features. After making sure the ESD design target is satisfied, an extracted S-parameter file will be ready for RFIC designer use in RFIC co-design simulation.

![Fig. 4.5 GSG device test pattern used to extract $C_{ESD}$, $R_{ESD}$, S-parameter and noise figure of RF ESD protection structures with high accuracy [48].](image)

For RFIC simulation path, the designer should first design RFIC with targeted specifications. Then, the extracted ESD S-parameter file will be added into RFIC simulation, which usually will cause circuit degradation since parasitic capacitance, resistance and additional noise will be introduced by ESD unit. Then, circuit modification based on ESD-RFIC will be conducted, making sure the ESD protected circuit performance is coming back comparing with RFIC without ESD protection. After that, the ESD-RFIC circuitry will be sent to foundry for fabrication. After fabrication, a
comprehensive ESD-RFIC lab verification will be conducted, including full RFIC testing and ESD stressing. What’s more, the RFIC’s performance before and after ESD stress should also be verified to confirm feasibility of the design methodology.

4.4 IR-UWB Tx and ESD Co-design Implementation

The co-design philosophy proposed in section 4.3 was excised to design ESD-protected UWB Tx IC using the ESD-RFIC co-design methodology [45]. Firstly, the ESD protection structures, with targets for 2kV and 5kV HBM (human body model) ESD protection, were designed and optimized for minimum ESD-induced parasitic using a mixed-mode ESD simulation-design approach [46]. The optimized ESD protection structures were then fabricated in the foundry 0.18 µm CMOS process used in this work, and subsequently characterized for parasitic effects by S-parameter and noise figure (NF) measurements, as well as their ESD protection level using the transmission line pulse (TLP) ESD testing technique.
Fig. 4.6 I-V Curves from TLP testing reveal maximum sustainable current levels under ESD stressing: (a) 2kV and (b) 5kV.

Fig. 4.7 ESD protection scheme for the IR-UWB Tx IC.

Fig. 4.6 depicts the measured I-V characteristics by TLP testing for the two designed ESD protection structures, showing 1.3A and 3.5A ESD failure point, which
roughly corresponds to 1.95kV and 5.25kV HBM ESD protection levels, respectively. Next, the diode-type ESD protection structures were integrated to the UWB transmitter IC at the output port as illustrated in Fig. 4.7.

ESD-UWB Tx co-design were carefully conducted, taking into consideration of the already minimized ESD parasitic parameters, i.e., $C_{\text{ESD}} \approx 90 \text{fF}$ at 5GHz, to achieve whole-chip performance optimization for the ESD-protected UWB transmitter IC using our new ESD-RFIC co-design method [45]. The co-design technique allows importing the measured ESD-induced parasitic effects directly into the UWB Tx circuit using the n-port feature of the Cadence CAD tool. The co-design goal is to realize both on-chip ESD protection and UWB Tx circuit performance optimization simultaneously.

4.5 Measurement and Discussion

The ESD-protected IR-UWB transmitter was fabricated in SMIC 0.18µm RFCMOS technology. Fig. 4.8 shows the die photos for the fabricated IR-UWB Tx circuits without ESD and with ESD, respectively, for comparison study. ESD structure is locating in the red circle in the right photo of Fig. 4.8. The simple circuit architecture adopted for this UWB Tx IC does not use inductors, amplifiers or baluns on chip, hence, a very small die size of 0.25mm$^2$ for the whole UWB Tx IC was realized, including all testing pads.
Comprehensive measurements for the designed IR-UWB transmitter ICs, including time domain/frequency domain waveform and ESD protection unit characterization were conducted. Fig. 4.9 and 4.10 depict the measured Gaussian pulse trains for the 0º and 180º phase channels, respectively. The single pulse details obtained readily show that desired 5\textsuperscript{th}-order Gaussian derivative waveforms as designed. Clear BPSK modulation was achieved that ensures 0º and 180º phase signals. The 5\textsuperscript{th}-order Gaussian waveforms are achieved that match with simulation reasonably well. Compared to the near ideal 0º waveform, the less-than-ideal 180º waveform is attributed to the possible transistor mismatching effect due to the inaccurate foundry device models across the ultra wide 3.1-10.6GHz spectrum, resulting in less ideal waveform combination. Fig. 4.11 compares the measured 0º phase shifted 5\textsuperscript{th}-order Gaussian pulse signals generated by the transmitters with and without ESD protection in reference with the ideal 5\textsuperscript{th}-order Gaussian waveform from simulation. It clearly shows that the measured Gaussian waveforms match the ideal Gaussian pulse very well.
Fig. 4.9 Measured IR-UWB 5th-order Gaussian pulses in time domain for the 0º phase channel: (a) pulse train; (b) single pulse waveform.
Fig. 4.10 Measured IR-UWB $5^{th}$-order Gaussian pulses in time domain for the $180^\circ$ phase channel: (a) pulse train; (b) single pulse waveform.
Fig. 4.11 Measured 5th-order Gaussian pulses of designed PGs with/without ESD protection in comparison with ideal 5th-order Gaussian pulse.

Critically, due to careful ESD-RFIC co-design to eliminate the ESD-induced parasitic effects, the measured Gaussian waveform generated from the UWB transmitters with 5KV ESD protection does not show any performance degradation compared with the original circuit without ESD protection, which is a challenging goal for any RF ICs, particularly across the full wide 3.1-10.6GHz spectrum. The measured signal peak of $V_{pp} \approx 506$mV and pulse width of $\tau \approx 394$ps also match the simulation reasonably well. The circuit simplicity results in an ultra low power dissipation of $0.14$pJ/p-mV for the design.

Comprehensive ESD testing for RF ICs is tricky and involving. Complete full-chip ESD protection testing must follow a standard ESD zapping procedure: 1) All I/O pins must be stressed by ESD pulses against every other I/O pin, GND and $V_{DD}$ pads. 2) Each pad must be stressed with both positive and negative ESD pulses, i.e., I/O-to-GND
(or $V_{SS}$) positively and negatively (i.e., PS and NS modes), I/O-to-$V_{DD}$ positively and negatively (i.e., PD and ND modes), and $V_{DD}$-to-GND positively and negatively (i.e., DS and SD modes) [43]. 3) Key IC specs parameters should be evaluated after each ESD zapping step to check if any circuit degradation occurs due to ESD failure. This requires test of key circuit specs before and after each ESD zapping step. Any degradation beyond a pre-set margin after ESD stressing is considered that ESD failure occurs at the whole IC level regardless of the individual ESD device protection capability. Such a comprehensive ESD testing ensures proper evaluation of whole-chip ESD protection characterization.

In this work, the ESD-protected UWB Txs were tested for HBM-equivalent ESD protection using a TLP tester. As was shown in Figure 4.6(b), an individual ESD protection structure shows ~5.25KV ESD protection capability for stand-alone ESD device in TLP testing. However, individual ESD protection device capability does not necessarily guarantee the same level ESD protection at whole chip level. Complete full-chip ESD testing for the TXs was conducted, including I/O-GND, I/O-$V_{DD}$ and $V_{DD}$-GND power clamp protection, in both positive and negative ESD stressing modes as described previously. To properly determine chip-level ESD protection capability, key IC specs must be compared before and after ESD stressing tests.
Fig. 4.12 shows measured Gaussian waveforms for the Tx before ESD zapping and after ESD stressing right before the ESD failure threshold, which shows no visible degradation for the Gaussian waveforms up to 2.5kV ESD stressing. Six Tx samples were tested for ESD performance. Table 4.1 summarizes the ESD testing results for all ESD stressing modes, showing that the achieved whole-chip ESD protection level is about 2.5kV for all ESD testing modes. ESD failure analysis shows that the reason for the lower whole-chip Tx ESD protection level of 2.5kV, instead of 5kV tested ESD protection capability for individually designed and verified ESD protection devices, is that some metal lines in layout were too narrow, which burned out under ESD stressing. The layout mistake can be corrected accordingly.
Fig. 4.13 shows the die photo when ESD failure happens. Fig. 4.14 shows the TLP testing I-V curve for GND-VDD direction when ESD failure happens. Table 4.2 shows state-of-the-art UWB Tx design comparisons.

![Fig. 4.13 Die photo after ESD failure happens.](image)

![Fig. 4.14 TLP Testing I-V curve for GND-VDD direction.](image)
Table 4.1 Full-chip ESD protection level for IR-UWB Tx.

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Table 4.2 Comparison of state-of-the-art UWB Txs.

| Ref. | Mod. | Pulse Type      | Bandwidth (GHz) | PRF (MHz) | <i>t</i> (nS) | <i>V</i><sub>pp</sub> (mV) | Power (pJ/p-mV) | Area (mm<sup>2</sup>) | Tech. | ESDV (kV) |
|------|------|-----------------|-----------------|-----------|--------------|----------------|------------------|--------|-----------|
| [33] | DBPSK| -               | 3.1-5.15        | 36        | 1.75         | 640             | 1.29             | 0.4    | 0.18µm CMOS |
| [34] | PPM  | 5<sup>th</sup>-order Gaussian | -              | 50        | 0.75         | 300             | 1.53             | 0.5    | 0.18µm CMOS |
| [35] | -    | Gaussian Monocycle | 1.53-5.67      | 1160      | 0.28         | 123             | 0.09             | 0.03*  | 0.18µm CMOS |
| [36] | PPM  | -               | 6.93-8.43       | 60        | 0.26         | 200             | 34.42            | 5      | 0.25µm SiGe |
| [37] | OOK  | -               | 3.3-5.3         | 2         | 1            | 4900            | 0.02             | 0.19*  | 0.18µm CMOS |
| [38] | BPSK | Gaussian        | 3.1-4.5         | -         | 2            | 1200            | -                | 1.2    | 0.18µm CMOS |
| [39] | BPSK | 5<sup>th</sup>-order Gaussian | 3.1-10.6       | 100       | 0.75         | 72              | 0.46             | 0.36   | 0.13µm CMOS |
| This  | BPSK | 5<sup>th</sup>-order Gaussian | 3.1-10.6       | 100       | 0.39         | 506             | 0.14             | 0.25   | 0.18µm CMOS |

*Core circuit only.
Chapter 5
UWB LNA Design with ESD Protection
5.1 UWB LNA Overview

As described in section 2.4, low noise amplifier (LNA) is the first stage at IR-UWB receiver front-end, with the function of amplifying received signal while introducing as little noise as possible. In addition to general circuit specs, an LNA requires robust on-chip ESD protection since it is directly exposed to external world via the antenna. Design of ESD-protected UWB RF front-end ICs is a major challenge [49]. The UWB IC requires very high ESD protection, e.g., >8kV in human body model (HBM), because it is often used in hand-held consumer electronics. Consequently, RF ICs, particularly the RF signal pins, often have inadequate on-chip ESD protection to avoid circuit performance degradation, while module and system level ESD protection is widely used. In previous sections, the interactions between ESD protection structure and core RF circuit were well explained.

Several ESD protected wideband LNA designs were reported recently [51-56]. For example, [50] and [52] report 3-5GHz LNA with 1.5kV and 6.5kV ESD protection respectively. [51] describes a 1.7-13.6GHz common gate enhancement LNA with 4.25kV ESD protection. [53] presents a 2.7-9GHz 4kV ESD protected LNA with Chebyshev input matching network and cascode topology. [54] reports a resistive feedback 3.1-4.8GHz LNA with 1.36kV ESD protection. [55] discusses a Gm boosted two stage 3-10.35GHz LNA with 1kV ESD protection. [56] depicts a narrow band 5.8GHz LNA with 4kV ESD protection. Most reported LNA’s have partial ESD protection only. In addition, ESD-LNA co-design to simultaneously optimize LNA and ESD protection performance at full chip level has not been considered. For Gbps carrier-free full-band UWB
transceivers for mobile consumer electronics, it is desired to have 3.1-10.6GHz LNA with ultra robust ESD protection. In following sections in this chapter, the author proposed a fully integrated single-stage 3.1-10.6GHz UWB LNA with complete full-chip ESD protection beyond 8kV, for which ESD-RFIC co-design was carefully considered.

5.2 UWB LNA Design

Due to the ultra wideband nature, designing UWB LNA is very challenging compared with that for relatively narrow-band LNA for traditional frequency-domain RF transceivers. There are several critical design parameters for UWB LNA. Firstly, a broadband well matched 50Ohm termination should be achieved since the input of LNA will be connected to antenna directly. Secondly, enough gain and moderate noise figure with good flatness over 3.1GHz to 10.6GHz are required. Thirdly, good linearity is preferred. However, since the input of the CMOS LNA circuit is typically a capacitive node, the varying parasitic capacitance of transistors makes it extremely difficult to realize good broadband impedance matching without degrading the noise performance and power delivery efficiency, not to mention the parasitic from ESD protection unit [49].

5.2.1 Typical LNA Topology

There are several typical LNA topologies in term of their impedance matching methods. They are illustrated in Fig. 5.1 below.

Fig. 5.1 (a) shows a simple resistive termination topology, where the 50Ohm resistor \( R_m \) connects directly from the input transistor gate to ground. A reasonable broadband matching can be achieved for this structure; however, this structure is not appropriate for LNA applications since the \( R_m \) will introduce thermal noise to LNA and
also it will attenuate input signal level. Fig. 5.1 (b) shows a $1/g_m$ LNA topology where the desired 50Ohm input matching is achieved by biasing the transistor M1. This kind of topology has a broadband feature [57]. However, to achieve good matching, we should have $1/g_m=50$, which is usually different from that for optimum noise figure performance [58]. Fig. 5.1 (c) provides a source degeneration structure, which has very wide applications [59] and can achieve good noise figure [60]. This architecture is only good for narrow band applications. Fig. 5.4 (d) shows a shunt-series feedback topology suitable for broadband applications. In contrast to the open-loop architectures, this topology breaks-up the troublesome global negative feedback and achieves proper trade-off between source impedance matching and noise figure performance. Hence, this shunt-series topology is attractive to broadband LNA design.

![Typical LNA topologies](image)

**Fig. 5.1** Typical LNA topologies (a) resistive termination (b) $1/g_m$ termination (c) source degeneration (d) shunt-series feedback.

### 5.2.2 Single-Stage Full-Band UWB LNA Design

Fig. 5.2 shows the circuit topology for single-stage full-band UWB LNA. Shunt-series feedback is employed for broadband matching. The cascode stage eliminates Miller effect [61] and gives good isolation between input and output. Shunt peaking inductor $L_2$
is employed to compensate high frequency gain attenuation and also prevent leakage between output and VDD.

![Single-stage full-band UWB LNA architecture.](image)

To analyze input/output matching, a small signal analysis is conducted. Fig. 5.3 shows the small signal circuit for the circuit of Fig. 5.2.

![Small signal analysis for single-stage full-band UWB LNA.](image)
From small signal analysis, we can get following equations for input/output impedance.

\[
Z_{\text{in}} = \frac{v_i}{i_i} = \frac{Z_f + (Z_L / / R_z)}{1 + g_m (Z_L / / R_z) + (1 / Z_s)(Z_f + (Z_L / / R_z))}
\]  \hspace{1cm} (5.1)

\[
Z_{\text{out}} = \frac{v_o}{i_o} = \frac{Z_f + (Z_s / / R_s)}{1 + g_m (Z_s / / R_s) + (1 / Z_L)(Z_f + (Z_s / / R_s))}
\]  \hspace{1cm} (5.2)

where \( Z_f = 1/sC_f + sL_f + R_f \); \( Z_s = sL_1/(1/sC_{gs}) \); \( Z_L = r_o / // sL_2 \). Since a broadband matching from 3.1GHz to 10.6GHz is extremely difficult, approximation method is employed here. Suppose at the frequency range, \( L_1 \) resonates with \( C_{gs} \), \( R_f \) resonates with \( C_f \), then we will have \( Z_s \rightarrow \infty, Z_f = R_f \) and \( Z_L / / R_z \approx R_z \). Equation (5.1) will become to

\[
Z_{\text{in}} \approx \frac{R_f + R_z}{1 + g_m R_z}
\]  \hspace{1cm} (5.3)

Similar for \( Z_{\text{out}} \), we suppose under a specific frequency, \( Z_s \rightarrow \infty, Z_f = R_f, Z_L \rightarrow \infty \) then Equation (5.3) will become to

\[
Z_{\text{out}} \approx \frac{R_f + R_s}{1 + g_m R_s}
\]  \hspace{1cm} (5.4)

For application, we have \( R_z = R_s = 50 \text{ Ohm} \), to make \( Z_{\text{in}} \) and \( Z_{\text{out}} \) equal to 50Ohm also, then we will have following Equation 5.5 and 5.6 for input/output impedance matching for the UWB LNA.

\[
\frac{R_f + 50}{1 + 50g_m} = 50
\]  \hspace{1cm} (5.5)

\[
R_f = 2500g_m
\]  \hspace{1cm} (5.6)
Based on discussion above, by properly choosing the feedback resistor and transistor biasing of M0, 50Ohm input and output impedance matching will be achieved. The voltage gain of the circuit can be expressed as following:

$$A_v = \frac{v_o}{v_i} = \left(\frac{Z_L}{Z_f} + \left(\frac{Z_L}{R_s}\right)\right) \left(1 - g_m Z_f \right) \approx \frac{R_s \left(1 - g_m R_f \right)}{R_f + R_s} \approx -\frac{g_m R_f R_z}{R_f + R_s} \quad (5.7)$$

where $R_z = 50\text{Ohm}$. From Equation 5.7, the gain of the LNA is proportional with $g_m$ of transistor M1 and feedback resistor $R_f$.

To analyze the noise performance of the proposed UWB LNA, if we only consider noise from feedback resistor $R_f$ and transistor M0’s channel thermal noise while ignoring other noise source from the circuit, after calculation, we will have the noise factor equation as shown in following,

$$F = 1 + \frac{R_f}{R_s} \left(1 + \frac{g_m R_s}{1 - g_m R_f} \right)^2 + \frac{\gamma g_m}{\alpha R_s} \left(\frac{R_s + R_f}{1 - g_m R_f} \right)^2 \quad (5.8)$$

where $\alpha$ and $\gamma$ are process related parameters. From the noise factor equation we can see, the noise of the LNA has close relationship with biasing of the transistor M0 and feedback resistor $R_f$. For rough approximation, $g_m R_s >> 1$ and $g_m R_f >> 1$, then Equation 5.8 will become following

$$F \approx 1 + \frac{R_s}{R_f} + \frac{\gamma}{\alpha R_s} \frac{(R_s + R_f)^2}{g_m R_f^2} \quad (5.9)$$

Since the feedback topology is adopted, stability issue should be well considered. Actually, the first concern for an amplifier with feedback is to make sure it won’t become
an oscillator at anytime. Here we employ stability factor $K_f$ to evaluate the stability of the circuit. The stability factor equation is shown as following Equation 5.10:

$$K_f = \frac{1 + |S_{11}S_{22} - S_{12}S_{21}|^2 - |S_{11}|^2 - |S_{12}|^2}{2|S_{11}||S_{22}|}$$  \hspace{1cm} (5.10)

To make sure the circuit is unconditionally stable, $K_f > 1$ over 3.1GHz to 10.6GHz should be strictly satisfied.

Now we summarize our design concern for UWB LNA. Combine with Equation 5.6 to 5.10 together and the designer will can get a rough idea how to choose critical design parameters in the UWB LNA circuit. To have a high gain with low noise, a large $g_m$ is preferred. However, the larger $g_m$ is, the more current LNA circuit will consume. And a too large $g_m$ will degrade circuit linearity. Increasing feedback resistor $R_f$ will increase the gain while improve the noise figure, but a large $R_f$ will reduce the feedback and cause stability issue. What’s more, $g_m$ and $R_f$ are closely related to achieve good impedance matching. Hence, design trade-off between gain, impedance matching, NF, power dissipation, linearity and stability is critical to overall LNA performance.

5.3 LNA-ESD Co-design

In chapter 4 the author already described the methodology and design for ESD-RFIC co-design. In this thesis, a complete full-chip ESD protection scheme for the UWB LNA is adopted. As shown in Fig. 5.4, the complete ESD protection scheme consists of diode ESD protection for input to VDD and input to ground (GND), as well as a diode-string power clamp between VDD and GND, respectively. No ESD protection at output is needed for LNA because it will be integrated into our UWB receiver chip.
To minimize ESD induced parasitic effects and predict ESD protection at LNA circuit level, a mixed-mode ESD simulation-design methodology was used to optimize ESD protection design at circuit level [46]. Since the UWB transceiver is designed for handheld consumer electronics, extremely robust and full-chip ESD protection, i.e., ~8kV for input protection and ~15kV for power line protection was our ESD design target. Since high ESD robustness normally requires larger ESD protection structure that hence introduces more ESD parasitic effects, which will adversely affect LNA circuit performance, ESD-LNA co-design becomes essential to ensure simultaneous design optimization of both ESD protection and LNA circuit performance [45].

In this work, although mixed-mode ESD simulation was exercised to minimize ESD-induced parasitic and predict ESD design performance, it is apparent that the high ESD protection requirement of 8kV/15kV will inevitably affect LNA circuit. We adopt a unique direct S-parameter insertion technique [45] and [62] for ESD-LNA whole-chip
simulation and optimization. Let’s briefly restate the ESD-RFIC design flow shown in Fig. 4.4 specialized for LNA as following. Firstly, ESD protection structures are optimized for minimum parasitic by mixed-mode ESD simulation. Secondly, the ESD structures are fabricated. Thirdly, complete RF characterization for the ESD structures is conducted to extract all ESD parasitic parameters. Fourthly, the LNA is designed to meet its design specs. Fifthly, whole-chip ESD-LNA simulation is conducted to evaluate any LNA circuit degradation due to the added ESD parasitic, mainly the impedance matching corruption that may affect every LNA specs. Finally, ESD-LNA co-design is performed that typically involves I/O impedance re-matching tune-up to recover most ESD-induced circuit degradation for the LNA. The ultimate design goal is to ensure simultaneous whole-chip design optimization of both LNA specs and ESD protection performance.

For design comparison, design splits for LNA without ESD protection and with diode and ggNMOS ESD protection were designed in this work. In general, the traditional ggNMOS is large and its ESD parasitic effect is so strong that the resulted circuit degradation cannot be recovered even using ESD-RFIC co-design. On the other hand, optimized diode ESD structures can still introduce parasitic effects to the LNA, however, its negative impacts on LNA circuit performance may be largely suppressed by careful ESD-LNA co-design.

5.4 Measurement and Discussions

The ESD-protected UWB LNAs were implemented in GSMC 0.18μm RFCMOS process. Fig. 5.5 shows the layout and die photo of the UWB LNA without ESD and with
ESD, respectively. Complete measurements were conducted including S-parameter, NF, linearity and ESD TLP testing.
5.4.1 UWB LNA w/o ESD Si Measurement

For the UWB LNA without ESD protection, Fig. 5.6 shows the on-wafer probing result for S-parameter measurement. As we can see, the UWB LNA achieves a flat gain with a maximum S21=10.9dB@8.85GHz. It also gives good S11<-10dB for broadband matching. The reverse isolation is evaluated by S12, which is less than -18.9dB over the full UWB band. For 3.1GHz to 7.8GHz, S22<-10dB; for 7.8GHz to 10.6GHz, S22<-5.2dB. Since S22 can be properly adjusted by the proceeding stage, it is not a primary concern.
Noise figure measurement is shown in Fig. 5.7. From Fig. 5.7 we can see, the UWB LNA achieves a minimum NF=4.98dB. The reason why the NF is higher than
expected might come from several sources. First, the foundry preliminary RF PDK model is mainly developed for low-GHz operation, they are not very accurate for high frequency up to 10GHz, which actually has broad impacts on this UWB LNA design. In addition, the extra cable adaptors used in our testing set-ups might also affect the testing system calibration, though careful calibration was well conducted for noise figure analyzer.

Fig. 5.8 gives the measured result for P1-dB and K-factor. The UWB LNA achieves a P1-dB=2.88dBm@7GHz. Since feedback topology is employed, circuit stability should be considered. Measurement shows a $K_f > 1.58$ over 3.1GHz to 10.6GHz, which means the circuitry is unconditionally stable.

Fig. 5.9 is the measured group delay for the UWB LNA that shows reasonably good group delay of approximate 100±35pS across the full 3.1-10.6GHz bandwidth. While group delay is inevitable for ultra wideband circuits, a relatively constant group delay is preferred for UWB IC to avoid signal distortion.
For power consumption, the UWB LNA consumes about 15.2mA from 1.8V power supply, which means the total power consumption is 27.4mW. The power consumption is high since the gain of the UWB LNA is directly related with $g_m$, the higher gain means more current draw from power supply. The total die area is approximately 0.48mm² including all the testing pads for the LNA without ESD.

5.4.2 UWB LNA w/ ESD Si Measurement and Discussion

Following the same procedure, LNAs with ESD protection have been measured. Fig. 5.10 shows the measured S21 for LNA splits, and it clearly shows that the large ggNMOS ESD device significantly affects the LNA gain by as much as 45.9%. This is because the ggNMOS has a large parasitic capacitance around 1.1pF@5GHz, the re-matching technology cannot bring the degradation back with such large parasitic. On the other hand, using optimized diode ESD structure successfully minimized the LNA gain degradation due to ESD-LNA co-design as expected.
Fig. 5.10 Measured S21 from LNA w/o ESD, LNA w/ diode ESD optimized and LNA w/ ggNMOS ESD.

The LNA input reflection (S11) was also significantly affected by the large ggNMOS ESD structure, which increases from S11~ -21.8dB for nominal LNA without ESD to S11~ -4.38dB at center frequency, i.e., about 80% degradation, which was then largely reduced to S11~ -14.8dB when using the diode ESD structure. Fig. 5.11 shows the measured S11. As we can see, even with re-matching, due to the parasitic from ESD device, the S11 performance still has some degradation from the LNA without ESD. The measured reverse isolation for the LNA using optimized diode ESD structure is better than -20.6dB across the full 3.1-10.6GHz bandwidth.

Fig. 5.12 depicts the measured NF for the LNA design splits readily shows that using ggNMOS ESD protection seriously increases the LNA noise behavior, mainly due to the impedance matching corruption. On the other hand, co-design using optimized diode ESD protection structure almost completely eliminated the extra noises induced by the ggNMOS ESD structure. The extracted NF ranges from 4.98dB to 7.37dB across the
3.1-10.6GHz spectrum, which is higher than expected. The reason has been explored in previous section.

Fig. 5.11 Measured S11 performances for LNA splits.

Fig. 5.12 Measured NF performances for LNA splits.

Complete ESD characterization for LNA circuits using Transmission Line Pulse TLP testing (Barth Model 4002). In section 4.5 the author already described the ESD
testing procedure designer should follow, which also applied to LNA testing. Fig. 5.13 depicts typical S21 curves measured for the ESD-protected LNA circuit before and after ESD stressing (but immediately prior to ESD failure threshold), which shows no noticeable gain degradation before any ESD failure occurs to the LNA. Six LNA samples are tested by TLP stressing up to the ESD failure threshold.

![Measured LNA S21 before and right after 8.25kV ESD stressing.](image)

Fig. 5.13 Measured LNA S21 before and right after 8.25kV ESD stressing.

Fig. 5.14 shows the TLP testing I-V curve (I/O-VDD and VDD-GND) as an example, which give about 5.75A and more than 10A ESD failure point, which equals to 8.63kV and more than 15kV respectively. Figure 5.15 shows the die photo right after ESD failure taken from microscope. Device damage can be seen from microscope.
Table 5.1 summarizes the ESD testing results for all ESD stressing modes. It is observed that all input signal pin can sustain at least 8.25kV HBM ESD stressing under all ESD stressing modes. The ESD power clamp passed 9.38kV HBM ESD protection level. To the best of author's acknowledge, the designed LNA is the highest whole-chip ESD protection result reported for UWB LNA's. Table 5.2 compares the reported ESD
protected UWB LNA with state-of-the-art in similar category, which shows that this
design prevails in many aspects, e.g., ESD protection level, gain flatness and linearity, etc.

Table 5.1 Full-chip ESD protection level for UWB LNA.

<table>
<thead>
<tr>
<th>I/O-V_{DD}</th>
<th>V_{DD}-I/O</th>
<th>I/O-GND</th>
<th>GND-I/O</th>
<th>V_{DD}-GND</th>
<th>GND-V_{DD}</th>
</tr>
</thead>
<tbody>
<tr>
<td>8.63kV</td>
<td>8.25kV</td>
<td>8.25kV</td>
<td>8.25kV</td>
<td>&gt;15kV</td>
<td>9.38kV</td>
</tr>
</tbody>
</table>

Table 5.2 Comparison of similar ESD protected UWB LNAs.

<table>
<thead>
<tr>
<th>Ref</th>
<th>Freq. (GHz)</th>
<th>S21 (dB)</th>
<th>NF (dB)</th>
<th>S11 (dB)</th>
<th>P_{1-dB} (dBm)</th>
<th>ESDV (kV)</th>
</tr>
</thead>
<tbody>
<tr>
<td>[50]</td>
<td>3-5</td>
<td>26</td>
<td>4</td>
<td>-11</td>
<td>-22.7</td>
<td>1.5</td>
</tr>
<tr>
<td>[51]</td>
<td>3.1-10.6</td>
<td>15.4</td>
<td>-</td>
<td>-6</td>
<td>-11.2</td>
<td>4.25</td>
</tr>
<tr>
<td>[52]</td>
<td>3-5</td>
<td>11.8</td>
<td>2.1-3</td>
<td>-9</td>
<td>-15.1</td>
<td>6.5</td>
</tr>
<tr>
<td>[53]</td>
<td>2.7-9</td>
<td>10</td>
<td>3.2-5</td>
<td>-10</td>
<td>-10</td>
<td>4</td>
</tr>
<tr>
<td>[54]</td>
<td>3.1-4.8</td>
<td>16.5</td>
<td>4.5</td>
<td>-8</td>
<td>-4.3</td>
<td>1.36</td>
</tr>
<tr>
<td>[55]</td>
<td>3-10.35</td>
<td>11</td>
<td>3.3-11.4</td>
<td>-8.3</td>
<td>-14</td>
<td>1</td>
</tr>
<tr>
<td>[56]</td>
<td>5.8</td>
<td>18</td>
<td>1.85</td>
<td>-16</td>
<td>-11</td>
<td>4</td>
</tr>
<tr>
<td>This</td>
<td>3.1-10.6</td>
<td>10.9</td>
<td>4.98-7.37</td>
<td>-10</td>
<td>2.88</td>
<td>&gt;8.25</td>
</tr>
</tbody>
</table>
Chapter 6
UWB Correlator Design with ESD Protection
6.1 UWB Correlator Overview

A correlator is critical circuit block in the receiving channel of any IR-UWB transceiver IC chips. In IR-UWB systems, correlator is the following stage right after LNA. Recently, research on developing correlator or multiplier for UWB IC has attracted significant attentions [63-71]. Reference [63] gives a good summary for various analog multiplier topologies and compares their advantage and disadvantage. [64-66] gives a fully integrated IR-UWB correlator implemented in CMOS or BiCMOS, composing of a multiplier and integrator. [67] proposed a UWB correlator composed of a Gilbert cell, common mode feedforward circuit, capacitor load and buffer. [68] proposed a low power analog multiplier in CMOS. [69]-[72] described various kind of UWB correlators for GHz applications.

![UWB Correlator block diagram](image_url)

Fig. 6.1 UWB Correlator block diagram.

The receiver architecture of IR-UWB has been shown in Fig. 2.7 in Chapter 2. The functionality of the correlator is to achieve direct conversion/demodulation for the received signal; it is composing of a correlation type multiplier and a low pass filter. Fig.
6.1 shows the block diagram for UWB correlator. From the figure we can see, for an IR-UWB correlator, it achieve following functions. First, it performs a direction conversion without frequency shifting. There are two inputs for multiplier, one is reference impulse template and the other is RF input signal after LNA. This is a correlation type demodulation. Then, a RC integrator will be following stage performing as a low pass filter to prepare the signal for further ADC processing. The multiplier has a differential input/output to ensure signal quality. The detail correlator architecture is shown in Fig. 6.2 as following. Here the pulse shape in the figure is just an example since in real applications, the pulse type of the RF input and template reference of the correlator is determined by pulse shaping.

Fig. 6.2 UWB Correlator detail block diagram.
6.2 IR-UWB Correlator Design with ESD Protection

The proposed IR-UWB correlator is based on topology from reference [64-68], and ESD-RFIC co-design methodology is implemented to ensure high quality performance. Fig. 6.3 shows the circuitry of the correlator.

![Diagram of UWB Correlator](image)

Fig. 6.3 Schematic for the UWB Correlator core circuit.

For the schematic in Fig. 6.3, the lower part is a UWB multiplier, upper part is RC integrator and buffer. For the multiplier, transistors P1-P4 are in saturation region, while other transistors N1-N4 and M1-M4 are biased in linear region for a low power application [64-66, 68]. For transistor P1/2, N1/2 and M1/2 we have following I-V equation:

\[
i_{p1} = \frac{1}{2} K_p (V_{DD} - L(t) - I(t) - |V_{THP}|)^2 [1 + \lambda (V_{DD} - V_{P1})]
\]  

(6.1)
\[ i_{P2} = \frac{1}{2} K_p (V_{DD} - L(t) + I(t) - |V_{THP}|)^2 [1 + \lambda (V_{DD} - V_{P2})] \quad (6.2) \]

\[ i_{N1} = K_N [(r(t) + r(t) - V_{P1} - V_{THN})(V_{O1} - V_{P1}) - \frac{1}{2} (V_{O1} - V_{P1})^2] \quad (6.3) \]

\[ i_{N2} = K_N [(r(t) - r(t) - V_{O1} - V_{THN})(V_{P2} - V_{O1}) - \frac{1}{2} (V_{P2} - V_{O1})^2] \quad (6.4) \]

\[ i_{M1} = K_M \left[ (V_b - V_{THM}) V_{P1} - \frac{1}{2} V_{P1}^2 \right] \quad (6.5) \]

\[ i_{M2} = K_M \left[ (V_b - V_{THM}) V_{P2} - \frac{1}{2} V_{P2}^2 \right] \quad (6.6) \]

In addition, we have \( i_{M1} = i_{P1} + i_{N1}, \) \( i_{M2} = i_{P2} - i_{N2} \) and \( i_{N1} \approx i_{N2} \). Solve above equation, we’ll get following Equation 6.7.

\[ V_{O1} - V_{O2} \approx C \frac{K_p}{K_M K_N} r(t) I(t) \quad (6.7) \]

where \( C \) is a constant coefficient. From above equation we can see, the circuitry achieves the multiplication of two input signals.

Transfer function of the first-order RC integrator in Fig. 6.3 can be derived as following equation,

\[ H(s) = \frac{1}{(1 + R_1 / R_2) + R_2 C s} \quad (6.8) \]

By properly select the value of \( R_1, R_2 \) and \( C \), a bandwidth of 180~200MHz can be achieved.
For the single to differential convertor, we employed a capacitor compensated balun [39]. Fig. 6.4 shows the schematic of the balun.

![Schematic of the single to differential balun.](image)

From small signal analysis of the Fig. 6.4 we will have following equations:

\[
V_{outp}(s) = \frac{V_m(s)}{1 + \frac{1}{Z_s\left(g_m + sC_{gs}\right)}} \tag{6.9}
\]

\[
V_{outn}(s) = V_{in}(s) \cdot \frac{Z_d\left(sC_{gd} - g_m/Z_s\left(g_m + sC_{gs}\right)\right)}{1 + \frac{1}{Z_s\left(g_m + sC_{gs}\right)}} \tag{6.10}
\]

where \(Z_d = (R_d + sL_d) || \frac{1}{sC_{gd}}\) and \(Z_s = (R_s + sL_s) || \frac{1}{sC_{gs}}\). By carefully choosing \(R_s = R_d\), \(L_s = L_d\) and \(C_{gd} = C_c\), one can make \(Z_d = Z_s\). Submit this into Equation 6.10 and we can have following equation:
\[ V_{out}(s) = V_{in}(s) \cdot \frac{sC_{gd}Z_s - 1}{1 + 1/Z_s(g_m + sC_{gs})} \quad (6.11) \]

By satisfying \( sC_{gd}Z_s << 1 \), we will have the final expression for \( V_{out}(s) \).

\[ V_{out}(s) = \frac{-V_{in}(s)}{1 + 1/Z_s(g_m + sC_{gs})} = -V_{outp}(s) \quad (6.12) \]

From above derivation we can achieve the single to differential conversion for the input signal. During the design, phase difference of the two output (\( V_{outp} \) and \( V_{outn} \)) should be well considered, an ideal 180° should be expected over all the 3.1GHz to 10.6GHz.

To achieve robust design, ESD protection is embedded. Careful ESD-RFIC co-design was applied to the IR-UWB correlator. The co-design procedure is implemented as described in Chapter 4. Fig. 6.5 shows the diagram of ESD protected correlator. Since the RF input of the correlator is directly from LNA, so there is no necessary to have any ESD protection. The template reference input and output are well ESD protected. The input/output ESD protection also serves as the VDD-GND power clamp.

![Fig. 6.5 ESD protected Correlator block diagram.](image)
6.3 Simulation Result for ESD Protected IR-UWB Correlator

Zero order Gaussian waveform is employed for pulse shaping and reference template generation in the correlator design. To demonstrate the feasibility of the correlator, the two inputs of the multiplier take the same zero order Gaussian waveform.

First, the performance of the balun is provided. Fig. 6.6 shows the time domain performance of the balun itself.

![Fig. 6.6 Time domain waveform of balun input/output.](image)

The phase error and gain error of the $V_{outp}$ and $V_{outn}$ is shown as Fig. 6.7. From the figure we can see, the phase error is 2.3º and the gain error is 0.74dB from 3.1GHz-10.6GHz, which allows a good single to differential signal conversion.
Fig. 6.6 (a) Phase error of the balun over 3.1GHz-10.6GHz, (b) Gain error of the balun over 3.1GHz-10.6GHz.

Fig. 6.7 (a)-(d) shows the time domain waveform of each node in correlator simulation result.
Fig. 6.7 (a)-(d) Time domain waveform of each stage in Correlator.
Fig. 6.7 (a) shows the zero order Gaussian waveform which feeds into the single to differential convertor. Fig. 6.7 (b) shows the signal after single to differential convertor. As we can see, the balun achieves good single to differential conversion. Fig. 6.7 (c) shows the output of multiplier, which is the multiplication of two input Gaussian waveform train. Fig. 6.7 (d) shows the final output of the RC integrator. This output is well enough for a high speed low resolution ADC to conduct further signal processing.

Although correlator is the proceeding stage of LNA, the noise of the correlator is also of concern. Fig. 6.8 shows the NF of the correlator. From the figure we can see, the correlator has a NF from 12.7dB to 14.3dB over 3.1GHz to 10.6GHz.

![Fig. 6.8 NF simulation result for the UWB Correlator.](image)

Fig. 6.8 NF simulation result for the UWB Correlator.
Fig. 6.9 gives the 1-dB compression point of the RF input port of the correlator. It shows the P1-dB is larger than 7.95dBm for 3.1GHz to 10.6GHz.

![Fig. 6.9 RF port P1-dB simulaiton result of the Correlator.](image)

ESD-RFIC co-design has been implemented on this correlator. Fig. 6.5 already shows the block diagram for the ESD protected design. When the ESD unit is added to the correlator, due to the parasitic effect, it will degrade the correlator performance. By applying the re-matching methodology mentioned in Chapter 4 and 5, the performance degradation has been maximally corrected. Fig. 6.10 shows the correlator performance with regards to ESD protection. As shown in Fig. 6.10 (a) and (b), when the ESD unit is added to circuitry, the output of the correlator will drop from 158mV to 113mV, which is about 28.5% performance degradation. After re-matching, the performance is brought back to 140mV, which is very close to 158mV original performance.
Fig. 6.10 Simulation result for Correlator w/o ESD, w/ ESD before and after ESD re-matching: (a) pulse train; (b) single enlarged pulse.
Chapter 7
Conclusions
7.1 Summary

This dissertation presents design and analysis of a single-full-band carrier-free impulse-radio based UWB transceiver system, including IR-UWB system analysis, circuit architectures, IC design and characterization, ESD protection design for UWB IC and a new ESD-RFIC co-design methodology for UWB ICs.

For IR-UWB transmitter, the author proposed a new approximation method to design Gaussian pulse generators with various orders. A 5th-order Gaussian PG circuit featuring single delay line and pulse combination techniques was developed for IR-UWB transceiver optimization. A comprehensive UWB Gaussian PG circuit design procedure concerning pulse width, pulse peak to peak amplitude and frequency corner, etc., is described. The proposed UWB Gaussian PG design methods can simplify design complexity, while ensure IR-UWB IC performance. A most-digital BPSK modulation technique was proposed that generate the required 180° pulse directly by the pulse generator without employing any additional single-to-differential convertor. This IR-UWB transmitter is fully ESD protected up to 2.5kV in HBM model. Full Si measurement and characterization were conducted. The proposed whole IR-UWB transmitter can be achieved most digitally and easily be implemented in CMOS technologies. The new IR-UWB transmitter achieves the design targets of simple and most-digital architecture, low power, low cost, ultra high speed (Gbps), high ESD robustness and being SoC ready.

The IR-UWB receiver consists of a LNA and correlator. The 7.5GHz UWB LNA utilizes a single-full-band single-stage shunt-series feedback LNA topology to achieve a
flat gain and NF over the full UWB band. The LNA is fully ESD protected up to 8.25kV. The correlator adopts a multiplier plus integrator topology. The IR-UWB receiver was fully verified in Silicon.

The proposed IR-UWB transceiver IC was designed using a new ESD-RFIC co-design technique developed by the author to ensure whole-chip UWB IC and ESD protection performance optimization simultaneously.

7.2 Future Work

Several design challenges for IR-UWB IC designs may be studied in future. First, the critical circuit blocks for transmitter and receiver were designed and characterized separately in this work. Systematic UWB IC integration should be investigated to achieve good UWB SoC performance. For example, the receiver integration of LNA, correlator and timing control must be carefully considered to ensure UWB receiver SoC design optimization. The interconnection between various circuit blocks must be optimized. Second, possible interference from 5GHz WLAN should be carefully considered. Third, timing control such as synchronization between transmitter and receiver is extremely critical for the IR-UWB transceiver ICs for Gbps, which should be further investigated. Fourth, the antenna is certainly an important and integral part of any UWB transceiver system, which requires significant research efforts to achieve integration with UWB ICs and system performance. Last, but certainly not the least, full-chip robust ESD protection for UWB SoC deserves further research to ensure both high ESD protection level and Gbps data rate for future wireless video and data streaming applications.
REFERENCE


