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Ultra-low-loss Ta$_2$O$_5$-core/SiO$_2$-clad planar waveguides on Si substrates

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1. INTRODUCTION

An increasing number of systems and applications depend on photonics for transmission and signal processing. This includes data centers, communications systems, environmental sensing, radar, lidar, and microwave signal generation. Such systems increasingly rely on monolithic integration of traditionally bulk optical components onto the chip scale to significantly reduce power and cost while simultaneously maintaining the requisite performance specifications at high production volumes. A critical aspect to meeting these challenges is the loss of the waveguide on the integrated optic platform, along with the capability of designing a wide range of passive and active optical elements while providing compatibility with low-cost, highly manufacturable processes, such as those found in CMOS. In this article, we report the demonstration of a record low propagation loss of $3 \pm 1$ dB/m across the entire telecommunications C-band for a CMOS-compatible Ta$_2$O$_5$-core/SiO$_2$-clad planar waveguide. The waveguide design, fabrication process, and optical frequency domain reflectometry characterization of the waveguide propagation loss and group index are described in detail. The losses and dispersion properties of this platform enable the integration of a wide variety of linear and nonlinear optical components on-chip, as well as integration with active rare-earth components for lasers and amplifiers and additionally silicon photonic integrated devices. This opens up new integration possibilities within the data communications, microwave photonics, high bandwidth electrical RF systems, sensing, and optical signal processing applications and research communities.

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Ultra-low-loss Si$_3$N$_4$-core/SiO$_2$-clad planar waveguides (ULLWs) on silicon provide the basis of an integration platform allowing for a broad variety of exceptional active and passive photonics components, such as on-chip erbium-doped lasers [1], ultra-high-$Q$ resonators [2], sidewall Bragg grating filters [3], and arrayed waveguide grating routers [4]. Such a platform is able to take advantage of the high index contrast between silica and silicon nitride to create waveguides that possess sub-millimeter bend radii and sub-dB/cm losses simultaneously. These characteristics enable applications previously supported only by fiber-based components to now be realized with a photonic integrated circuit (PIC) at a lower cost point and a smaller packaging footprint. Example applications include tunable optical true time delays for broadband phased array antennas [5–7], optical gyroscope rotational velocity sensors [8], and programmable dispersion compensating lattice filters [9].

However, the Si$_3$N$_4$-core-based platform possesses certain limitations that can be addressed through the substitution of Ta$_2$O$_5$ as a core material, as described in this work. For example, nonlinear optical processes on photonic chips can be used to generate and process signals all-optically with speeds far superior to electronics. For the best performance, such nonlinear processes generally require high mode confinement and dispersion engineering for phase matching [10,11]. Due to its high tensile film stress, depositing thick (>300 nm) layers of Si$_3$N$_4$ without cracking has historically proven to be a considerable fabrication challenge [10]. Furthermore, optical absorption in the 1.52 μm wavelength region due to nitrogen–hydrogen (N–H) bond resonances (hydrogen being an undesired impurity incorporated into the Si$_3$N$_4$ and SiO$_2$ films during fabrication) creates a “floor” on the lowest achievable optical loss within the C-band [12].

Tantalum pentoxide (Ta$_2$O$_5$) is a CMOS-compatible material [13,14] that presents the opportunity to address both the requirements for nonlinear interactions and the fundamental loss limitations of Si$_3$N$_4$ as a waveguide core material, while at the same time preserving a high index contrast that allows for small bend radii (the refractive index of Ta$_2$O$_5$ at 1550 nm is roughly the same as Si$_3$N$_4$, 2.05). Investigation of the nonlinear refractive index of Ta$_2$O$_5$ has shown that it has an order of magnitude higher value than that of silica ($7.2 \times 10^{-19}$ m$^2$/W for Ta$_2$O$_5$ [15] versus $2.2 \times 10^{-20}$ m$^2$/W for SiO$_2$ [16]) and is greater than that of Si$_3$N$_4$ ($2.4 \times 10^{-19}$ m$^2$/W [16]), which allows for a shorter length of interaction and thus a reduced device footprint when
compared to both fiber and Si₃N₄-core based waveguides for achieving nonlinear applications such as optical switching. Due to the material’s extremely large bandgap value (3.8 eV), two-photon absorption (TPA) and TPA-induced free-carrier absorption are of little to no concern when operating Ta₂O₅-based devices at high powers [17–19]. These important material parameters when considering waveguide design optimizations are summarized below in Table 1.

Furthermore, the broadband transparent nature of the material means that it is suitable for wavelengths spanning the ultraviolet to the long-wavelength infrared (300–8000 nm) [20]. Finally, due to the low value of film stress of Ta₂O₅ when compared to a Si₃N₄-core-based alternative (100 MPa for Ta₂O₅ versus 800 MPa for stoichiometric LPCVD Si₃O₄), fabricating thick, high mode confinement waveguides will be less of a fabrication challenge [21]. As well as the aforementioned benefits concerning nonlinear signal generation and processing, such a high confinement factor waveguide design would be advantageous in the development of active devices that leverage rare-earth ion dopants [22,23].

Attempts to date at reducing the loss of Ta₂O₅-core-based waveguides have focused on the core deposition and subsequent anneal steps of the fabrication process [24,25]. In [24], the authors employed a sputter deposition technique for the core region of their Ta₂O₅-core/SiO₂-clad waveguides, with an O₂ atmosphere anneal protocol immediately following. Their 400 nm thick waveguides were processed into ring resonator structures that showed a propagation loss of 1.5 dB/cm at wavelengths near 1550 nm. In [25], the authors incorporated a mixture of SiO₂ and Ta₂O₅ within the core region of their SiO₂-clad waveguide structures. Such a mixture allowed for a much higher maximum anneal temperature before the crystallization of the Ta₂O₅ than previously possible (1100°C versus 650°C) [26]. The resulting propagation loss was measured by applying the cutback method in waveguides with lengths between 2.7 and 23.9 cm. The 1.5 μm thick core waveguides displayed a loss of 6 dB/m at a wavelength of 1550 nm. Both of these loss values are most likely dominated by the large degree of waveguide sidewall scattering incurred during their reactive ion-based etching process.

In this paper, we report on record low propagation losses for Ta₂O₅-core/SiO₂-clad planar waveguides across the entire C-band over the lengths of complete spiral delays. Our structures demonstrate loss that is both lower than the state of the art for a Ta₂O₅-core waveguide [25] and that demonstrated by an Si₃N₄-core waveguide of an equivalent geometry [27]. We achieve these losses with refined core deposition and anneal processes, as well as through an optimized waveguide geometry and the resulting required etching protocol. We begin with an overview of the waveguide design and fabrication process. We then show optical backscattering reflectometry (OBR) characterization results from spiral waveguide delays. The group index and propagation loss of the waveguide structures are then reported.

### 2. WAVEGUIDE DESIGN

The cross-sectional geometry and material stack for our waveguides follow the loss reduction and photonic integration approach reported in [27] and [28]. With Si₃N₄ and Ta₂O₅ having roughly equivalent optical indexes of refraction, the majority of waveguide design rules for Si₃N₄ core structures will also apply to waveguides featuring a Ta₂O₅ core. In general, when designing a waveguide cross section to minimize loss, there is an inherent compromise between optical confinement and core/cladding interfacial scattering loss. This trade-off manifests itself as an optimization between the lowest possible waveguide bend radius (as a practical matter, taking into account the given available on-chip PIC real estate) and the largest reduction in interfacial scattering loss contributions. When taking into account nonlinear applications, a high degree of optical confinement within the waveguide core is desirable, but this design parameter comes at the expense of an acute sensitivity to waveguide core sidewall scattering.

For planar waveguides, the roughness value at the waveguide sidewall due to optimized dry etching is typically an order of magnitude larger than that of the roughness value for the deposited top/bottom interfaces (1–10 nm versus <1 nm on average). This implies that the optimum lowest-loss single-mode core geometry for a given bend radius has the highest single-mode aspect ratio (width:thickness). Here, we choose a 90 nm Ta₂O₅ core thickness, with a width of 2.8 μm (the widest possible single-mode core width for the given core thickness). This high aspect ratio design (width:thickness > 10:1) ensures the waveguide will support only a single spatial mode in the C-band, while at the same time allowing tight (<1 mm, with no additional loss penalty) bends. Figure 1(a) gives a schematic representation of the cross section of the waveguide, while Fig. 1(b) shows the simulated (FIMMWAVE by Photon Design) transverse electric (TE) polarized optical mode profile for the 1590 nm wavelength.

The transverse magnetic (TM) -polarized mode for such a geometry will have a lower confinement factor within the waveguide core (larger modal cross-sectional area) and thus a larger critical bend radius. The critical bend radius is defined as the

| Table 1. Material Parameters for Ta₂O₅, Si₃N₄, and SiO₂ |
|-----------------------------|-------------|-----------------------------|
| Material | Refractive Index (n) [λ = 1550 nm] | Nonlinear Refractive Index (n₂) [m²/W] | Experimental Bandgap (E₀) [eV] |
| Ta₂O₅ | 2.05 | 7.2 × 10⁻¹⁹ | 4.4 |
| Si₃N₄ | 2.05 | 2.4 × 10⁻¹⁹ | 5.3 |
| SiO₂ | 1.44 | 2.2 × 10⁻²⁰ | 9 |

![Fig. 1. (a) Cross-sectional geometry of the final Ta₂O₅-core/SiO₂-clad waveguide. The thermal SiO₂ lower cladding, Ta₂O₅ core, and sputtered SiO₂ upper claddings layers are 15 μm, 90 nm, and 1.1 μm thick, respectively. The width of the Ta₂O₅ core is 2.8 μm. (b) Simulated optical mode profile of the fundamental TE waveguide mode at the 1.55 μm wavelength. The calculated modal intensity diameters (1/e²) are 2.7 μm in the horizontal by 1.1 μm in the vertical. These dimensions were confirmed experimentally through facet imaging utilizing an infrared camera. The calculated core confinement factor (Γ) is 0.15 and the effective index (nₑff) is 1.474.](image-url)
radius at which the total propagation loss is dominated by the contribution from bend loss, rather than from the material or interfacial scattering losses. As a result of this bend limitation, combined with the maximum available field size of our lithography system, we consider in this work only TE-polarized light for waveguide design and loss measurements.

We designed the thickness of the upper and lower SiO₂ claddings as 1.1 and 15 μm, respectively. A thicker upper cladding layer would, in principle, result in a lower propagation loss, but in practice, even 2 μm thick sputter-deposited layers show a drastic decrease in film quality due to the incorporation of additional deleterious scattering centers. The 15 μm lower SiO₂ cladding ensures that the design is unaffected by leakage loss from the Si substrate.

3. DEVICE FABRICATION AND PROPAGATION LOSS CHARACTERIZATION

To test the optical loss of these waveguides, we designed and fabricated 10 m long Archimedean spiral delays with an innermost minimum bend radius of 2 mm and 0.7 m long spiral delays consisting of Bézier curves having a minimum bend radius of 760 μm and a central loop mirror structure. Figures 2(a) and 2(b) below give a schematic representation of both structures.

A. Waveguide Fabrication

Figures 3(a)–3(d) gives a graphical representation of the entirety of the Ta₂O₅ waveguide fabrication process.

Waveguide fabrication begins with a 1 mm thick, 100 mm diameter silicon substrate upon which 15 μm of silica is thermally grown by wet oxidation for the lower cladding. Next, 90 nm of Ta₂O₅ is deposited by sputter deposition. This 90 nm layer is then patterned using a photoreist mask by 248 nm stepper lithography and an optimized CH₃/CF₄/O₂ inductively coupled plasma etch. The etching chamber had CH₃/CF₄/O₂ gas flows of 35/5/10 cm³/min, a pressure of 0.5 Pa, an RF source power of 500 W, and an RF bias of 50 W. This etching chamber is regularly used to etch various other materials (including Si, GaN, and InP) as part of our shared fabrication space, so if catastrophic contamination were to occur it would manifest during our loss measurements. Figures 4(a)–4(c) show atomic force microscopy (AFM) measurements of the waveguide core top and sidewalls and an optical micrograph of the bus and outermost waveguides (yellow in color) of the 10 m long Archimedean spiral.

Fig. 2. (a) Schematic representation of a fabricated die featuring the 10 m long Archimedean spiral with a 2 mm minimum bend radius (at the innermost turn-around section). The outermost bend radius was 10 mm. (b) Schematic representation of a fabricated die containing the 0.7 m long spiral delay, with Bézier curves connecting the straight sections. The minimum bend radius of the Bézier curves was 760 μm, while the outermost radius was 1.7 mm. The loop mirror structure can be seen within the spiral center. Both designs in (a) and (b) also feature 21 mm long straight waveguides as auxiliary test structures.

Fig. 3. (a)–(d) Schematic overview of the fabrication process for the waveguides discussed within this paper. All of the processes we employ within this work (including the deposition and etch steps of the Ta₂O₅ material) are CMOS compatible.
means of assessing the impact of annealing on both the core and cladding materials. Once the initial testing has completed, we anneal the samples in a furnace containing a 3.0 SLPM \( \text{N}_2 \) flow at 300°C for 3 h. With an \( \text{Si}_3\text{N}_4 \) core material, the nominal anneal temperatures routinely reach 1100°C [12]. This allows for maximum reduction in hydrogen-impurity-related absorption loss [29]. However, the \( \text{Ta}_2\text{O}_5 \) material limits the maximum attainable anneal temperature here, as \( \text{Ta}_2\text{O}_5 \) crystallizes and catastrophically increases in loss. In accordance with the work presented in [26], we determined this point to be temperatures above 650°C. Our final 300°C 3 h annealing protocol was experimentally found to be the optimum temperature/time combination for our sputter-deposited samples. After this final processing step, we then re-characterize the propagation loss.

B. Propagation Loss Characterization by Optical Backscattering Reflectometry

In order to quantify the propagation loss of the \( \text{Ta}_2\text{O}_5 \) waveguides, we utilize the coherent optical frequency domain reflectometry (OFDR) technique using a commercially available system (Luna Inc. OBR 4400) [12,30]. In the OFDR technique, a continuous-wave laser source is scanned over several tens of nm in wavelength (1535–1600 nm in this case), giving a micron-level spatial resolution of the waveguide delay. It is important to note that the OFDR propagation loss measurement is independent of the excess loss and loss uncertainty incurred during fiber-to-chip coupling and is thus more accurate for very low losses than the commonly used cut-back technique. Additionally, over long length spans, OFDR provides optical attenuation versus propagation distance that captures the loss variability caused by localized variations within the fabrication process. This loss variability can be attributed to imperfections, including those due to failed lithography sections of the waveguide core or to flaws such as micron-sized clusters within the nominally homogenous sputter-deposited upper \( \text{SiO}_2 \) cladding. Figure 5 shows reflection amplitude data measured for one of the 0.7 m long spiral delays consisting of Bézier curves having minimum bend radii of 760 \( \mu \text{m} \) and a central loop mirror structure. Before the OBR scan, the fiber-to-chip coupling and launched polarization are optimized using the OBR source laser, a 3-paddle polarizer, and an infrared camera mounted on a microscope above the sample. The leftmost peak (near 0 m in distance) is the coupling interface between the fiber and the chip edge. The right peak (near 0.7 m in distance) is the reflection from the on-chip loop mirror structure. It is through this distance relationship that we measured the group index of the waveguide to be 1.55, which agrees with our optical mode simulations and is roughly comparable to that as measured in an \( \text{Si}_3\text{N}_4 \) core waveguide of a similar geometry [27]. Figure 6 shows the mean and standard deviation of the spectral dependence of the propagation loss within 3 separate die of 10 m long Archimedean spirals. As is shown, even the un-annealed samples display a lower loss across the C-band than the previously recorded lowest-loss \( \text{Ta}_2\text{O}_5 \)-core waveguide designs [25]. After annealing, the loss is even further reduced to lower than that demonstrated by an \( \text{Si}_3\text{N}_4 \) core waveguide of an equivalent geometry [27]. Due to various scattering events caused by the imperfect nature of the sputtered upper cladding above the entirety of the 10 m spiral, the annealed samples display an irregular standard deviation over the whole of the wavelength range. Such a yield issue is a remaining challenge of fabricating extremely long, ultra-low-loss waveguides.

4. CONCLUSIONS

In conclusion, we have demonstrated record low measured propagation losses for \( \text{Ta}_2\text{O}_5 \)-core/\( \text{SiO}_2 \)-clad planar waveguides across the full telecommunications C-band. Our design achieves lower loss than any other reported \( \text{Ta}_2\text{O}_5 \)-core waveguide to the best of our knowledge and also simultaneously lower loss than that demonstrated by an \( \text{Si}_3\text{N}_4 \)-core waveguide of an equivalent geometry. Our fabrication method, which leverages sputter
deposition of the Ta2O5 core and SiO2 cladding, greatly reduces the incorporation of deleterious hydrogen during the waveguide construction. This approach can be extended to waveguides with even thinner cores, further lowering the expected absolute propagation loss values through a reduction of sidewall scattering loss. Because Ta2O5 does not exhibit the material absorption of Si3N4 in the C-band, these waveguides could be used for low-loss, high confinement factor designs. Low sidewall scattering loss could be maintained by shallowly etching the core. An initial design for such a low-loss high confinement geometry could consist of a 1.0 μm thick Ta2O5 core layer, surrounded by a SiO2 cladding. Lateral confinement would be accomplished through a 90 nm shallow etch of a 2.8 μm wide waveguide. Such an approach can furthermore facilitate the combination of deeply etched, small bend radius waveguides and shallowly etched ultra-low-loss waveguides on a single chip. Additionally, due to its CMOS compatibility, Ta2O5 can readily be used as a replacement for Si3N4 in current delay-based applications (gyroscopes, true-time delays, low-loss high confinement optical waveguides with less than 0.1 dB/m propagation loss fabricated with wafer bonding), Opt. Express 24, 24090–24101 (2011).


