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Quasi-optical network analyzers and high-reliability RF MEMS switched capacitors

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Quasi-Optical Network Analyzers and High-Reliability RF MEMS Switched Capacitors

A dissertation submitted in partial satisfaction of the requirements for the degree Doctor of Philosophy

in

Electrical Engineering (Electronic Circuits and Systems)

by

Alex Grichener

Committee in charge:

Professor Gabriel M. Rebeiz, Chair
Professor Lawrence E. Larson, Co-Chair
Professor Gert Cauwenberghs
Professor Brian Keating
Professor Kevin B. Quest

2011
The dissertation of Alex Grichener is approved, and it is acceptable in quality and form for publication on microfilm and electronically:

Co-Chair

Chair

University of California, San Diego

2011
DEDICATION

To my grandfathers Aron Shuster and Yakov Grichener.
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and Gabriel M. Rebeiz. The dissertation author was the primary investigator and author of this material.
VITA AND PUBLICATIONS

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<tr>
<td>1999 - 2003</td>
<td>B. S. in Electrical Engineering and Mathematics, Tufts University, Boston, MA, USA</td>
</tr>
<tr>
<td>2003 - 2004</td>
<td>Electrical Engineer with National Radio Astronomy Observatory, Charlottesville, VA, USA</td>
</tr>
<tr>
<td>2004 - 2005</td>
<td>M. S. in Electrical Engineering, University of Michigan, Ann Arbor, MI, USA</td>
</tr>
<tr>
<td>2006 - 2007</td>
<td>Electrical Engineer with Goodrich Sensor Systems, Burnsville, MN, USA</td>
</tr>
<tr>
<td>2007 - 2011</td>
<td>Ph. D. in Electrical Engineering, University of California, San Diego, USA</td>
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ABSTRACT OF THE DISSERTATION

Quasi-Optical Network Analyzers and High-Reliability RF MEMS Switched Capacitors

by

Alex Grichener

Doctor of Philosophy in Electrical Engineering (Electronic Circuits and Systems)

University of California, San Diego, 2011

Professor Gabriel M. Rebeiz, Chair
Professor Lawrence E. Larson, Co-Chair

The thesis first presents a 2-port quasi-optical scalar network analyzer consisting of a transmitter and receiver both built in planar technology. The network analyzer is based on a Schottky-diode mixer integrated inside a planar antenna and fed differentially by a CPW transmission line. The antenna is placed on an extended hemispherical high-resistivity silicon substrate lens. The LO signal is swept from 3-5 GHz and high-order harmonic mixing in both up- and down-conversion mode is used to realize the 15-50 GHz RF bandwidth. The network analyzer resulted in a dynamic range of greater than 40 dB and was successfully used to measure a frequency selective surface with a second-order bandpass response. Furthermore, the system was built with circuits and
components for easy scaling to millimeter-wave frequencies which is the primary mo-
tivation for this work. The application areas for a millimeter and submillimeter-wave
network analyzer include material characterization and art diagnostics.

The second project presents several RF MEMS switched capacitors designed for
high-reliability operation and suitable for tunable filters and reconfigurable networks.
The first switched-capacitor resulted in a digital capacitance ratio of 5 and an analog
capacitance ratio of 5-9. The analog tuning of the down-state capacitance is enhanced
by a positive vertical stress gradient in the the beam, making it ideal for applications that
require precision tuning. A thick electroplated beam (4-4.5 µm) resulted in Q greater
than 100 at C to X-band frequencies, switching times of 30-50 µs, and power handling
of 0.6-1.1 W. The design also minimized charging in the dielectric, resulting in excellent
reliability performance even under hot-switched and high power (1 W) conditions. The
second switched-capacitor was designed without any dielectric to minimize charging.
The device was hot-switched at 1 W of RF power for greater than 11 billion cycles with
virtually no change in the C-V curve.

The final project presents a 7-channel channelizer based on the mammalian
cochlea. The cochlea is an amazing channelizing filter, covering three decades of band-
width with over 3,000 channels in a very small physical space. Using a simplified me-
chanical cochlear model and its electrical analogue, a design method is demonstrated
for RF and microwave channelizers that retains the desirable features of the cochlea in-
cluding the ability to cascade a large number of channels (for multiple-octave frequency
coverage), and a high-order stop-band rejection. A 6-pole response is synthesized in
each channel using the top-C coupled topology. A constant absolute 3 dB bandwidth
of around 4.3 MHz and an insertion loss of around 3.9 dB is measured in each channel.
A high isolation (greater than 35 dB) is achieved between adjacent channels. A reflec-
tion loss of greater than 15 dB is measured at the input port over the entire channel-
izer bandwidth. Application areas for the demonstrated channelizer include wideband,
contiguous-channel receivers for signal intelligence or spectral analysis.
Chapter 1

Introduction

1.1 Millimeter-Wave Planar Integrated Technology

The millimeter-wave frequency range covers from 30 to 300 GHz and the submillimeter (also known as the terahertz) frequency range covers from 300 GHz to 3-10 THz. Millimeter-wave applications include automotive radars, communication systems, traffic control, and industrial process control [2–4]. In the submillimeter frequency range, applications extend to radio astronomy, plasma fusion diagnostics, and terahertz time-domain spectroscopy (for gas and molecular line spectroscopy) [5, 6]. Terahertz technology also has many applications in biology and medicine including in vivo and in vitro tissue identification and disease detection [7]. One significant advantage of millimeter-waves over microwaves is the increase in antenna gain (narrower beamwidth) for a given aperture size, since antenna gain scales as $f^2$. For imaging applications, narrower beamwidths result in higher imaging resolution (smaller pixel size).

Another advantage of a smaller wavelength is that it allows the realization of smaller circuits and smaller antennas for a given antenna gain. Traditionally, millimeter-wave systems have been implemented with waveguide components which require precision machining and are relatively expensive to manufacture. Also because components (such as antennas, mixers, amplifiers, etc.) are individually manufactured and then connected with sections of waveguide, millimeter-wave systems tend to be bulky, expensive, and lossy. The alternative is to utilize integrated circuit processing techniques to real-
Figure 1.1: Cross section view of three different planar transmission line geometries. 
(a) Microstrip, (b) coplanar waveguide, and (c) grounded coplanar waveguide.

ize an entire system monolithically on a single semiconductor substrate. Such a system promises to be low-cost, light, and compact. Several mm-wave and THz receivers have been implemented using planar techniques based on GaAs, InP, and even SiGe BiCMOS circuits [8–16].

One challenge with planar systems is the high loss associated with the transmission lines. Coplanar waveguide (CPW) and microstrip lines are most commonly used to propagate electromagnetic waves in planar circuits (Fig. 1.1). CPW lines have the added advantage that they allow easy series and parallel connections and do not require via holes (for ungrounded CPW) [17]. In CPW the electromagnetic fields are confined partly in the air and partly in the dielectric and the fundamental mode propagating in CPW lines is quasi-TEM. However if the ground to ground spacing is too wide then quasi-TEM propagation does not take place and is disturbed by line radiation resulting in increased losses. This maximum ground to ground spacing is approximately $\lambda_d/10$ where $\lambda_d$ is the dielectric wavelength. Also, in comparison to microstrip, CPW lines suffer from higher conductor losses because the current distribution is along the edges of the central conductor and of the grounds. For these reasons it is important to eliminate the need to propagate millimeter-wave signals through long transmission lines. This can be done by tightly integrating the mixer element with the antenna which allows the system to mix the RF and LO signals directly at the antenna.

One challenge with planar antennas at millimeter-wave frequencies is the potential for power loss into substrate modes resulting in poor radiation patterns. The thickness required to avoid excessive substrate mode power loss is typically less than $0.1\lambda_d$ for dipoles and $0.25\lambda_d$ for slot antennas [18]. At millimeter-wave frequencies,
this results in excessively thin substrates which are fragile and difficult to implement practically. One technique to avoid substrate modes is based on an idea from the optical domain, and was introduced by Rutledge and Muha in 1981 [19]: the dielectric lens. The antenna substrate is placed directly on the back of a dielectric lens. If the dielectric constant of the lens is close to that of the antenna substrate, then substrate modes will not exist. The additional effect is that antennas placed on dielectric lenses tend to radiate most of their power into the dielectric lens side, which can then be focused by the lens surface, and increases their overall radiation efficiency. The ratio of powers radiated into the dielectric and into the air is approximately $\frac{\varepsilon_r^3}{2}$ for elementary slot and dipole-type antennas, where $\varepsilon_r$ is the relative dielectric constant of the lens. For silicon ($\varepsilon_r = 11.7$), this means that only 2% of the power is radiated into the air. The dielectric lens is an attractive solution for millimeter-wave antennas, since it provides mechanical rigidity and a thermal heat sink. In addition, dielectric lenses can produce high quality Gaussian-beams which are useful for efficient coupling to a quasi-optical system.

A dielectric lens can be shaped to focus the rays of the feeding antenna to result in high-directivity patterns. As shown in Fig. 1.2(a), 1.2(b), and 1.2(c), the dielectric lens comes in three main geometric configurations, the hemispherical, the hyperhemispherical, and the elliptical [20]. In the case of the hemispherical lens, the antenna pattern does not experience any focusing but is simply transmitted through the lens. A hyperhemispherical lens is a hemispherical lens which has been extended such that the feed antenna is located at a distance of $\frac{R}{n}$ from the hemispherical center, where $R$ is the radius of the hemisphere and $n$ is the index of refraction of the lens. Such a geometric configuration bends the rays radiated by the integrated antenna towards the broadside direction, thereby sharpening the pattern and effectively increasing the gain of the integrated antenna by $n^2$. The hyperhemispherical lens is capable of coupling well to a Gaussian-beam system, but couples well to a converging beam and not to a planar equiphase front. An elliptical lens, on the other hand, couples well to a planar equiphase front. An integrated antenna that is placed at the focus of the elliptical lens will result in a far-field pattern with a main-beam that is diffraction limited by the aperture of the lens. In ray analysis, an elliptical dielectric lens with a point source at its more distant focus, refracts the emitted rays so that they emerge parallel to each other [21]. The diffraction-
Figure 1.2: Three main dielectric lens configurations are (a) hemispherical, (b) hyperhemispherical, and (c) elliptical. Each configuration can be synthesized with the extended hemispherical lens by varying extension length $L$ in (d).
limited patterns have been verified for a simple dipole antenna [22], a double-dipole antenna [23], a double-slot antenna [24], a log-periodic and spiral antenna [25], and for a sinuous antenna [26]. The main difference in the measured patterns between these antennas is in the sidelobe and cross-polarization levels.

A novel way of realizing different lens shapes is with an extended hemispherical lens which is a hemispherical lens (with radius $R$) and an attached rectangular extension of length $L$, as shown in Fig. 1.2(d). Note that the hyperhemispherical lens is a special case of the extended hemispherical lens. Filipovic presented a full analysis and characterization of extended hemispherical lenses [20]. He showed from a geometrical interpretation that there exists a specific extension length that effectively synthesized an elliptical lens. Using a ray-optics and field-integration formulation, he presented universal design curves, including the directivity, "Gaussicity", and reflection loss as a function of extension length. The term "Gaussicity" is defined as the coupling efficiency of a far-field pattern of an antenna to the far-field pattern of a Gaussian-beam.

Fundamental diode mixers require 1-10 mW amount of local oscillator (LO) power which may be difficult to generate and distribute at high millimeter-wave frequencies. One solution is to inject the LO into each mixer through the antennas using a quasi-optical technique [27] as shown in Fig. 1.3(a). However, this requires precision manufacturing and alignments and results in a bulky and a nonplanar solution. An-
other approach, based on high-n harmonic mixers and multipliers, uses a LO signal at a frequency which is a submultiple of the radio frequency (RF) signal (Fig. 1.3(b)). In general the mixing process becomes less efficient as the harmonic number increases. Page has shown that the conversion efficiency of a variable resistor multiplier is limited to $1/n^2$ where $n$ is the multiplication factor [28]. A more efficient mixer and multiplier can be made using a variable capacitance diode, which utilizes the nonlinearity of the capacitance-voltage curve. The well-known Manley and Rowe relations prove that the efficiency of an ideal varactor can be 100% [29, 30]. In practice, the series resistance of a diode and the inability to exactly match all the embedding impedances will considerably reduce the conversion efficiency. Also, variable capacitance diode designs are often limited to narrowband operation.

Wideband operation is best achieved with variable resistor diodes which utilize the nonlinearity of the current-voltage curve to generate harmonic mixing and multiplication. For example, monolithic broadband balanced doublers have been demonstrated in the literature using variable resistor diodes [31, 32]. The University of Virginia has developed several diode chips suitable for millimeter wave applications. The diodes are well matched and exhibit a reduced parasitic capacitance due to the surface channel fabrication procedure. The conventional approach to mixer design in the millimeter-wave region has been to mount a whisker contacted diode in a waveguide mixer block. Unfortunately these mixers may require multiple waveguides with different dimensions and can become very complicated to build, especially at higher frequencies. Millimeter-wave antennas with mixing elements placed directly at the terminals can be designed without the need for a complex waveguide system and result in receivers with very small dimensions [10–12]. Mixing antennas of this type can be designed to work into the terahertz region without mechanical limits.

1.2 RF MEMS Technology

Micro-Electro-Mechanical-Systems (MEMS) is the integration of mechanical elements, sensors, and actuators on a common substrate using micro-fabrication processes. MEMS devices vary in size from less than a micron to as large as several
millimeters and are fabricated using standard "micro-machining" techniques. MEMS technology originated in the 1970s and has quickly become a very diverse field leading to the miniaturization of accelerometers, gyroscopes, pressure sensors, temperature sensors, bio-sensors, and more. MEMS devices designed to operate at RF to mm-wave frequencies (0.1 to 100 GHz) are called RF MEMS. Due to its outstanding performance, RF MEMS has immense potential for commercial and defense applications. Essentially, a RF MEMS device uses mechanical movement of a suspended beam to achieve an impedance change in a transmission line. The forces required to achieve this mechanical displacement can be obtained using electrostatic, magnetostatic, piezoelectric, or thermal designs. Electrostatic actuation is the most commonly used due to its simplicity, compact size, and low power consumption.

There are two main categories of RF MEMS switches: metal-contact and capacitive-contact. Metal contact switches present a near open circuit in the up-state (due to their low up-state capacitance) and a near short circuit in the down-state (due to their low series resistance), and have been demonstrated from DC-100 GHz with excellent performance. Capacitive-contact switches on the other hand, use a metal-to-dielectric contact to achieve a variable capacitance ratio. Capacitive-contact switches with a high capacitance ratio (20-150) are called capacitive switches and are mostly used as On/Off switches in applications such as phase shifters and switching networks. A picture of a series capacitive switch developed by Lincoln Laboratory and its associated circuit model is shown in Fig. 1.4. Capacitive-contact switches with a medium capacitance ratio (3-10) are called switched capacitors and are ideal devices for tunable filters, loaded-line phase shifters, and reconfigurable matching networks from 500 MHz to 100 GHz [33, 34].

RF MEMS switches have certain key advantages over PIN diodes and FET switches that include:

1. Very low insertion loss: Since suspended metal structures are used for conduction instead of semiconductors, RF MEMS switches show very low loss, about 0.05-0.2 dB from 1-100 GHz.

2. Very high linearity: MEMS switches exhibit very high linearity which result in very low intermodulation products (about 30-60 dB better than FET switches or PIN
3. Extremely low power consumption: Although a high actuation voltage (20-100 V) is required for the electrostatic actuation of MEMS switches, there is very little current consumption leading to a very low DC power dissipation.

4. Very high isolation: MEMS metal-contact switches have air as a dielectric, and therefore have a very small off-state capacitance ($C_u=2-16$ fF) resulting in very high isolation up to 40 GHz.

These advantages along with IC-processing compatibility make RF MEMS an enabling technology for low cost and high performance systems in both military and commercial applications such as phase shifters, wide-band tunable/switchable filters, reconfigurable matching networks, reconfigurable array antennas, and satellite communications [35–37]. However, despite the superior performance, there remain key challenges that have to be overcome before RF MEMS becomes commercially viable. One of the biggest challenges that the RF MEMS community has been working hard to solve is in improving the reliability performance of MEMS-based structures. Great progress has been made in demonstrating devices that can survive very high-cycle ($>1B$) reliability tests. For example, the capacitive switch developed by Lincoln Laboratory (Fig. 1.4) has demonstrated $>300B$ cycles [38]. Still it is hard to achieve such reliability performance across process variations introduced by different foundries. In capacitive-contact switches, dielectric charging remains the key factor leading to device failure in
long-term reliability tests [39].

1.3 Multiplexers and Channelizers

Many wideband communication systems depend on channelization, where a RF signal is subdivided into several signals, each with a smaller bandwidth. This process of multiplexing is accomplished with a multiplexing filter or a *multiplexer*. Channelization is used in communication systems to allow a receiver, transmitter, or antenna to simultaneously accommodate multiple signals or channels. If the channels inside the multiplexer are contiguous (adjacent to each other in frequency) then the multiplexer is often times referred to as a channelizer [40, 41]. Systems using a front-end channelizer promise high receiver performance over a large bandwidth in a small size with low cost.

Take for example a wideband heterodyne digital receiver, in which the IF signal is converted to the digital domain with an analog to digital converter (ADC). The sampling rate of a traditional Nyquist ADC must be at least twice that of the instantaneous bandwidth of the signal. With present-day commercially available ADCs, this limits the signal bandwidth to about 1 GHz. Also, a very fast ADC may not be suitable as it is expensive and consumes a lot of power. The alternative is to use an analog channelizing filter and an array of low sampling rate and low-bit ADCs as shown in Fig. 1.5. This results in a relatively low-cost and low-power digital receiver with simultaneous detection over the entire receiver bandwidth. Also, since the channelizer reduces adjacent-channel interference, the ADC’s spurious-free dynamic range (SFDR) requirement, and thus number of required bits, is also significantly reduced [42, 43].

Channelizers composed of multi-mode high-Q waveguide filters are used in many satellite and military applications [44–46]. But when implemented with high-order filters, the channelizer becomes very complex requiring extensive optimization with a large number of variables. The size and mass of such a channelizer can also quickly become excessive. With the advent of computer aided design (CAD), large optimization problems become possible but are still time consuming and lack a coherent design methodology.

Some loss in a channelizer is tolerable as the noise figure in a receiver is mostly
10

**Figure 1.5:** Receiver application of channelizing filter.

governed by the front-end section which precedes the channelizer. The extra loss can always be compensated for by cascading amplifiers after the channelizer. This opens up the channelizer design space to circuits with lower-Q components. Previous work has demonstrated RF channelizers based on an equivalent circuit of a mamalian cochlea [47–49]. The circuit was implemented with surface mount technology (SMT) on a printed circuit board (PCB). The cochlear-like channelizer lends itself well to a theoretical model and a coherent design and optimization methodology. It also offers the possibility of cascading an unlimited number of channels together, each with an arbitrary number of poles.

### 1.4 Thesis Overview

Chapter 2 presents a 2-port quasi-optical scalar network analyzer built in planar technology. Both the transmitter and receiver are based on a Schottky-diode mixer integrated inside a planar antenna and fed differentially by a CPW transmission line. The receiver differs from the transmitter in that it has an additional IF path with appropriate low-pass filtering. The antenna is placed on an extended hemispherical silicon lens in order to eliminate power loss to substrate modes and to boost the antenna directivity. The LO signal is swept from 3-5 GHz and high-order harmonic mixing in both up- and down-conversion mode is used to realize the 15-50 GHz RF bandwidth. The hardware was designed to be scalable to sub-millimeter wave frequencies. The network analyzer resulted in a dynamic range of greater than 40 dB and was successfully used to measure
a series of frequency selective surfaces.

Chapter 3 presents RF MEMS switched capacitors suitable for tunable filters and reconfigurable networks. The switched capacitor results in a digital capacitance ratio of 5 and an analog capacitance ratio of 5-9. The analog tuning capability makes it an ideal device for tunable filters where precision tuning is required. Furthermore, the effect of a vertical stress gradient in the beam on the electromechanical performance of the switch is well characterized. It is found that a slight positive stress gradient increases the tuning range of the down-state capacitance and is therefore desirable. The design also minimizes charging in the dielectric, resulting in excellent reliability performance even under hot-switched and high power (1 W) conditions.

Chapter 4 presents a lumped-element cochlear-based channelizer with a 6th order channel filter response. Seven channel filters, each with a 4.3 MHz 3 dB bandwidth, are designed to cover the 60-90 MHz bandwidth. A high isolation (greater than 35 dB) is achieved between adjacent channels, and a reflection loss of greater than 15 dB is measured at the input port over the entire channelizer bandwidth. Both lumped and printed capacitors are used to implement the channel filters such that the 2% error tolerance in the lumped capacitors is compensated for.
Chapter 2

Quasi-Optical Network Analyzer Scalable to Terahertz Frequencies

2.1 Introduction

Network analyzers (both cabled and quasi-optical) operating to 67 GHz typically offer extensive functionality and high dynamic range but at the expense of circuit complexity, size, and cost [50]. The typical network analysis scheme uses a phase-locked loop to synthesize a LO frequency in the range of 2-4 GHz which is then up-converted to a single RF frequency through a series of analog doublers and filters (to reduce the harmonic content). In the receiver, fundamental mixing and $3^{rd}$ harmonic mixing is generally used to down-convert the RF to an IF frequency. In this work we demonstrate a different and much simpler approach for scalar network analysis up to 50 GHz. The scheme uses high-order harmonic mixing to transmit and receive multiple RF frequencies at the same time. The RF frequencies are prime harmonic multiples of the LO frequency and are each down-converted to independent IF channels in the receiver. Prime multiples are used to prevent aliasing where more than one RF signal falls onto the same IF. Such a network analysis is particularly useful in the higher millimeter-wave and terahertz frequency range because it relies on high-order harmonic multiplication and mixing. With this in mind, the circuits were designed so as to be easily scalable to terahertz frequencies.
The transmitter and receiver each consist of a planar antenna integrated with a distributed matching network and a planar Schottky-diode. Planar-based network analyzers offer an attractive advantage over the waveguide-based systems at millimeter-wave frequencies because they are smaller, lighter, and less expensive to build and can be easily produced in large numbers for low-cost applications. A potential antenna candidate for excellent millimeter-wave performance is the double-slot antenna. This antenna was first proposed by Kerr et al. [51] and later improved with a CPW transmission-line between the slot antennas instead of a microstrip line [10]. When the slot antenna is placed on an extended hemispherical high-resistivity silicon substrate lens, it results in high gain patterns and high Gaussian coupling efficiency [20]. Another antenna which offers an excellent wideband planar feed for the silicon lens is the sinuous antenna [26]. We have demonstrated a quasi-optical network analyzer with excellent performance using both antennas.

2.2 Design

A diagram of the quasi-optical network analyzer is shown in Fig. 2.1(a). The two-lens quasi-optical system is designed to shape the waist of the radiated Gaussian-beam in order to result in minimum path loss in the network analyzer [39]. A high-level schematic of the receiver and of the transmitter is shown in Figures 2.1(b) and 2.1(c) respectively. The planar circuits are shown inside the dashed boxes and are each realized with a printed circuit board. Two external signal generators are used to provide the LO to the transmitter and to the receiver. The IF output of the receiver is amplified with a low-noise amplifier and then detected and digitized with an external spectrum analyzer. In this way, the hardware is able to measure the magnitude of the transmission coefficient ($S_{21}$) of a device under test (DUT) that is placed between the transmitter and receiver in the path of the RF transmission. A through calibration is achieved by measuring the magnitude of the received power level with the DUT and without the DUT.

The transmitter LO frequency (referred to as $LO_T$) and the receiver LO frequency ($LO_R$) track each other while maintaining a constant frequency offset of $\Delta f$. Harmonics of the $LO_T$ frequency are radiated by the transmitter and picked-up by the
receiver where they mix with harmonics of the $LO_R$ frequency and are down-converted to harmonics of $\Delta f$. The chosen frequency plan for the network analyzer is illustrated in Fig. 2.2. The two LO signals are swept from 3-5 GHz with a constant 10 MHz offset resulting in all harmonics of 10 MHz showing up in the IF. For example, an IF of 30 MHz results from the mixing product of $LO_T \times 3$ (RF) and $LO_R \times 3$, and an IF of 40 MHz results from the mixing product of $LO_T \times 4$ (RF) and $LO_R \times 4$ as well as $LO_T \times 2$ (RF) and $LO_R \times 4$. Therefore, in order to avoid multiple RF signals from falling on top of each other in the IF, only the prime harmonics of $LO_T$ are used for the RF.

Fig. 2.3(a) and Fig. 2.3(b) show the top-metal layout of the receiver PCB based on the double-slot antenna and the sinuous antenna, respectively. Fig. 2.3(c) shows the cross-sectional view of the receiver. The antenna metal layer is fabricated on top of a 0.635 mm thick RT/duroid [52] 6010 substrate ($\epsilon_r = 10.2$), and a high-resistivity silicon lens ($\epsilon_r = 11.7$) with radius $R=12$ mm is fixed centrally on the bottom of the board. The planar antenna is extended to a distance of $L=3.94$ mm behind the hemispherical center of the lens, between the hyperhemispherical and elliptical position ($L/R=0.33$), and results in the peak antenna directivity. The dielectric lens approach also eliminates the power loss to substrate modes and makes the pattern unidirectional into the lens with minimal power radiated to the back-side. No matching-cap layer on the silicon lens is used.

The receiver circuit is implemented differentially which requires external 180° hybrids for the LO and for the IF signals. All transmission lines on the printed circuit board (PCB) are implemented in coplanar waveguide. The LO and IF signals are combined with a diplexer circuit shown in Fig. 2.4. Narrow bridges etched on the bottom metal and connected to the top metal with via holes, are used to equalize the ground potentials of the CPW. Also, the PCB is designed to sit inside a package on a metallic lip and has a bottom ground plane covering the area that directly contacts the lip.

The diplexer is designed to pass a 3-5 GHz LO signal from port 1 to port 2 and a 50-110 MHz IF signal from port 2 to port 3. An off-chip high-pass filter is used to block the IF signal from coupling into port 1. The IF network consists of a 5-section low-pass CPW filter with a corner frequency of 1.2 GHz. The filter is synthesized with alternating low (28 $\Omega$) and high (108 $\Omega$) impedance sections and the corresponding CPW geometry.
Figure 2.1: (a) Quasi-optical setup and schematic of (b) receiver and (c) transmitter.
Figure 2.2: Frequency scanning scheme for the quasi-optical network analyzer.
Figure 2.3: Top view of receiver PCB layout showing the LO/IF diplexer and (a) double-slot antenna, (b) sinuous antenna (grey is metal and white is slot) and (b) cross-section view of receiver showing the silicon lens attached to the bottom side of the PCB with dimensions in mm.
**Figure 2.4:** Layout of diplexer showing top and bottom metal and via holes with dimensions in \( \mu \text{m} \).
Figure 2.5: Simulated S-parameters of (a) LO path and (b) IF path.
is obtained from LineCalc. The diplexer was simulated in Sonnet [53] and the resulting S-parameters are plotted in Fig. 2.5. The diplexer has a 1 dB IF bandwidth of 450 MHz and a LO insertion loss of < 1 dB from 3-5 GHz. The isolation $S_{31}$ is 20 dB or higher for most of the 3-5 GHz band.

### 2.2.1 Antenna design

The network analyzer was implemented with two types of planar antennas: double-slot and sinuous. The double-slot was chosen as a reference antenna as it has been extensively characterized on a silicon lens [20]. The sinuous antenna was chosen for its excellent wideband performance [26]. The antennas are shown in Fig. 2.6 with the white area representing the metal and the grey representing the slot. The voltage sources in the drawing depict the impedance port across which the diode is connected. In the case of the double-slot antenna, the LO signal is fed to the diode through a pair of 6-pole low-pass filters which consist of alternating low (32 $\Omega$) and high (87 $\Omega$) impedance sections and are designed with a corner frequency of 15 GHz. The filter’s S-parameters were simulated in IE3D [54] (Fig. 2.7) and the resulting short-circuit rejection at 30 GHz is around 18 dB. In the case of the sinuous antenna, the LO signal is fed to the diode directly through the arms of the antenna. The sinuous antenna exhibits a natural low-pass filter response, passing the LO/IF frequencies and rejecting the RF frequencies at its external ports.

The length of the slot antenna controls the H-plane pattern and the separation between the slots controls the E-plane pattern. The slots are $l = 0.28\lambda_0$ long and spaced $s = 0.16\lambda_0$ apart where $\lambda_0 = 10$ mm is the free-space wavelength at 30 GHz. A sinusoidal magnetic current distribution in the slot is assumed with $\lambda_g = \lambda_0/\sqrt{\varepsilon_m}$ where $\varepsilon_m = (1+\varepsilon_r)/2$ and $\varepsilon_r = 11.7$. The slot antenna is used near its second resonance which provides a wideband self impedance on a silicon substrate. The distance between the slots is chosen to be $s = \lambda_d/2$ where $\lambda_d = \lambda_0/\sqrt{\varepsilon_r}$. This results in an array factor of $\text{AF}=2 \cos(\pi/2 \cos \theta)$ inside the silicon lens which gives a zero at $\theta = 0^\circ$ and $\theta = 180^\circ$.

The layout of the sinuous antenna is shown in Fig. 2.6(b), with a switch-backed curvature defined by the expression
Figure 2.6: (a) Layout of double-slot antenna and input low-pass filters and (b) layout of sinuous antenna (grey is slot and white is metal).
\[ \phi = (-1)^k \sin \left[ \pi \frac{\ln (r/R_k)}{\ln \tau} \right] \pm \delta \] (2.1)

where \((r, \phi)\) are the cylindrical coordinates of the curve, \(R_k\) is the inner radius of the \(k\)th cell, \(\tau\) is the scaling ratio for each successive cell (such that \(R_{k+1} = \tau R_k\)), and \(\alpha\) and \(\delta\) define the angular dimensions of each arm. The sinuous antenna shown in Fig. 2.6(b) is a basic 4-arm design with each arm composed of 11 cells.

The sinuous antenna supports a traveling wave that radiates efficiently when the length of a single cell, \(L_k\), is an odd multiple of one-half guided wavelength, \(\lambda_g\), and the current at the end of the cell has reversed phase and direction relative to the start of the cell. Thus, the two sections of traveling-wave current combine coherently, and the cell radiates a linearly polarized field. The radius of the active cell is approximately \(R_{k,active} = 2\lambda_g/3\pi\). The length and radius of the 11\(^{th}\) cell is illustrated as an example in Fig. 2.6(b). The antenna design results in a 4:1 bandwidth with a maximum frequency of 40 GHz, corresponding to a minimum guided wavelength of \(\lambda_{g,min} = 3\) mm. This sets the minimum radius of the first cell as follows: \(R_1 = \lambda_{g,min}/3\pi = 0.32\) mm. However, in order to make room for the diode, the first cell was partially filled in and this was
expected to slightly lower the maximum frequency of the antenna.

The theoretical input impedance of a sinuous antenna is given by $Z_{in} = \eta_m / \sqrt{2} = 106 \, \Omega$ where $\eta_m = \eta_0 / \sqrt{\varepsilon_m}$ [26]. However, it is known that the input impedance on a dielectric half-space will exhibit log-periodic fluctuations around the theoretical value with $R_{in}$ oscillating between 50-160 $\Omega$ and $X_{in}$ oscillating between $\pm 50 j \, \Omega$ [26]. The two arms connected to the diode terminals radiate in phase and thus both contribute to the same linear polarization. The other two arms are not utilized in this design and are terminated with a 100 $\Omega$ resistor soldered to the back-side of the PCB (with via-holes providing the connection to the front-side pads).

It is expected that the sinuous antenna has a directivity into the lens of around 12 dB, while the directivity of the double-slot antenna into the lens ranges from 8.5-12 dB through the 15-50 GHz range (since it was designed to resonate at 30 GHz). In order to boost the directivity, both antennas are placed on an extended hemispherical lens which moves the antenna by a certain extension length, $L$, behind the hemispherical center of the lens. It is known that a hyperhemispherical lens can be approximated with $L/R=0.29$ (where $R$ is the radius of the lens) and an elliptical lens can be approximated with $L/R=0.39$ [20]. Extending the antenna to the hyperhemispherical position effectively increases the directivity of the integrated antenna by $n^2$ (where $n$ is the index of refraction of the lens), and further extending it to the elliptical position results in a far-field pattern with a main-beam that is diffraction limited by the aperture. The diffraction limited (or peak) directivity is achieved at an extension length $L_{pk}$ that is somewhere between the hyperhemispherical and elliptical positions. The precise location of $L_{pk}$ is dependent on the $R/\lambda_0$ ratio. The higher $R/\lambda_0$, the closer $L_{pk}$ is to the elliptical position. For the given frequency range of the network analyzer the $R/\lambda_0$ ratio is relatively small (0.6-2.0 for 15-50 GHz) which results in peak directivity attained close to the hyperhemispherical position beyond which the gain remains fairly flat.

The diffraction limited directivity can be calculated using the standard equation, $D = 4\pi A_e / \lambda^2$, where $A_e$ is the effective aperture area of the lens and is approximately 85% of the physical aperture area [20]. Based on this calculation, the directivity of the planar antenna on the extended hemispherical lens is expected to vary from 11-21 dB for the 15-50 GHz bandwidth.
Table 2.1: MA4E2037 Diode Parameters

<table>
<thead>
<tr>
<th>$C_{j0}$ (fF)</th>
<th>$C_p$ (fF)</th>
<th>$R_s$ (Ω)</th>
<th>$I_s$ (fA)</th>
<th>$\eta$</th>
</tr>
</thead>
<tbody>
<tr>
<td>20</td>
<td>30</td>
<td>4</td>
<td>50</td>
<td>1.15</td>
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</table>

2.2.2 High-n harmonic mixer and multiplier design

A single-ended GaAs Schottky-diode from M/A-COM (model MA4E2037) is used as a high-order harmonic multiplier in the transmitter and a high-order harmonic mixer in the receiver. The key diode parameters are given in Table 2.1. The total diode capacitance (junction capacitance plus the parasitic capacitance) is 50 fF. The diode series resistance is 4 Ω and the forward voltage at 1 mA of dc current is 0.7 V. The ideality factor, $\eta$, and the reverse saturation current, $I_s$, were verified by curve fitting the calculated dc I-V curve to the measured. The figure-of-merit cutoff frequency ($f_c = 1/2\pi R_s C_T$) is approximately 750 GHz.

The diode forms the center conductor of the CPW-line and is placed in series between the two slots (across port 1 in Fig. 2.6(a)) and between the two sinuous arms (across port 1 in Fig. 2.6(b)). The impedance environment of the diode inside the double-slot antenna is shown with a schematic in Fig. 2.8(a). Each diode terminal sees an impedance of $Z_{e,ds}$, which includes the short section of CPW line ($Z_{CPW}$) in series with the self and mutual impedance of the slot antenna ($Z_{11} + Z_{12}$) in series with the impedance of the low-pass filter ($Z_{LPF}$). Since the diode is in series with the CPW-line, the equivalent diode embedding impedance is $2Z_{e,ds}$ as shown in Fig. 2.8(b). Note that at low frequencies the diode sees two 50 Ω resistors in series and therefore $2Z_{e,ds} = 100$ Ω at the IF and LO frequencies.

The double-slot antenna shown in Fig. 2.6(a) was simulated in IE3D on top of a silicon half-space. Port 1 was configured as a horizontal (in-plane) internal port and used to determine the diode embedding impedance, $2Z_{e,ds}$. The resulting impedance is plotted on a 100 Ω Smith chart in Fig. 2.9 and remains with a VSWR<2 from 20-40 GHz ($2Z_{e,ds} = 50$ Ω at 30 GHz). It must be noted that $2Z_{e,ds}$ does not include the effect of a reflection at the silicon-air interface and therefore is only an approximation.
Figure 2.8: (a) Circuit model representing the impedance environment inside the double-slot antenna and (b) the equivalent embedding impedance seen by the diode.

Figure 2.9: Simulated diode embedding impedance inside the double-slot antenna $(2Z_{e,ds})$ plotted on a 100 $\Omega$ Smith chart from 0-39 GHz.
Figure 2.10: Circuit model of the (a) multiplier and (b) mixer used in harmonic balance simulations.

Harmonic balance simulations were performed in ADS [55] using two different diode embedding impedances: $2Z_e = 2Z_{e,ds}$, and $2Z_e = 100 \ \Omega$. The 100 $\Omega$ impedance was used because it is an ideal approximation of the sinuous antenna input impedance and thus provides a good baseline case to compare with the impedance of the double-slot antenna (see Fig. 2.9). The multiplier and mixer circuit used in the harmonic balance simulation is shown in Fig. 2.10. The available LO power in the multiplier and in the mixer is given by

$$P_{LO,avail} = \frac{|V_{LO}|^2}{8\text{Re}\{2Z_e\}} = \frac{|V_{LO}|^2}{8 \times 100}$$  \hspace{1cm} (2.2)

and the available RF power in the mixer is given by

$$P_{RF,avail} = \frac{|V_{ANT}|^2}{8\text{Re}\{2Z_e\}}$$  \hspace{1cm} (2.3)

The RF power at the $n^{th}$ harmonic absorbed by the RF load in the multiplier is given by

$$P_{RF}(n) = \frac{|V_{RF}(n)|^2}{2} \text{Re}\left\{\frac{1}{2Z_e}\right\}$$  \hspace{1cm} (2.4)

and the IF power at the $(m,-1)$ mixing product absorbed by the IF load in the mixer is given by

$$P_{IF}(m, -1) = \frac{|V_{IF}(m, -1)|^2}{2} \text{Re}\left\{\frac{1}{2Z_e}\right\} = \frac{|V_{IF}(m, -1)|^2}{2 \times 100}$$  \hspace{1cm} (2.5)

The conversion loss of the multiplier and mixer can then be calculated using $L_{MULT}(n) = P_{RF}(n)/P_{LO,avail}$, and $L_{MIX}(m, -1) = P_{IF}(m, -1)/P_{RF,avail}$. 
Table 2.2: Simulated diode impedances as a function of available LO power with LO frequency fixed at 4.0 GHz

<table>
<thead>
<tr>
<th>$P_{LO}$ (dBm)</th>
<th>$Z_{in,LO}$ (Ω)</th>
<th>$Z_{out,IF}$ (Ω)</th>
<th>$Z_{in,20GHz}$ (Ω)</th>
<th>$Z_{in,28GHz}$ (Ω)</th>
<th>$Z_{in,44GHz}$ (Ω)</th>
</tr>
</thead>
<tbody>
<tr>
<td>5</td>
<td>201-j78</td>
<td>163</td>
<td>55-j75</td>
<td>34-j63</td>
<td>17-j46</td>
</tr>
<tr>
<td>10</td>
<td>90-j19</td>
<td>102</td>
<td>50-j50</td>
<td>34-j46</td>
<td>19-j36</td>
</tr>
<tr>
<td>15</td>
<td>49-j17</td>
<td>73</td>
<td>43-j35</td>
<td>31-j35</td>
<td>18-j29</td>
</tr>
</tbody>
</table>

Table 2.2 lists the simulated input impedance of the mixer at the RF and LO frequency, and the output impedance at the IF frequency for three different available LO power levels at each of the three harmonic multiples. The LO frequency is fixed at 4 GHz. As expected, the capacitance of the diode drives the RF impedance down with frequency. Also, as expected, the LO input impedance and the IF output impedance decrease as a function of LO power. Since the diode embedding impedance at both the LO and IF frequencies is 100 Ω, it is seen from the table that the best input and output match results at an LO power of 10 dBm.

The simulated multiplier and mixer conversion gain as a function of available LO power (for a 100 Ω embedding impedance) is plotted in Figures 2.11(a) and 2.11(b) respectively. Simulations show that the minimum conversion loss in the multiplier and in the mixer is achieved at an LO power of 12 dBm and 9 dBm respectively. With the LO power fixed at the optimum value in both the multiplier and the mixer, Fig. 2.12 presents the simulated conversion gain as a function of RF frequency. Simulations show that the conversion loss of the multiplier is 10-15 dB higher than the conversion loss of the mixer.

The reason the simulated conversion loss shows significant variation over LO power and RF frequency is due to multiple conversion paths interfering with one another. This is best illustrated with an example. Suppose an RF signal is located at the lower sideband of the 5th LO harmonic. It can be down-converted to the IF directly using the 5th LO harmonic (this conversion path can be expressed as $5 \rightarrow 0$) or it can be first down-converted to the lower sideband of the 3rd LO harmonic using the 2nd LO harmonic and
Figure 2.11: Simulated (a) multiplier conversion gain and (b) mixer conversion gain as a function of available LO power.
Figure 2.12: Simulated multiplier and mixer conversion gain as a function of RF frequency for two different diode embedding impedances. The LO power in the multiplier is fixed at 12 dBm and the LO power in the mixer is fixed at 9 dBm. The LO frequency is swept from 3-5 GHz.

Figure 2.13: A simplified illustration showing two different down-conversion paths.
then to the IF using the $3^{rd}$ LO harmonic ($5 \rightarrow 3 \rightarrow 0$). These two conversion paths are shown graphically in Fig. 2.13. In fact, there are three more conversion paths involving two frequency conversion steps, namely, $5 \rightarrow 4 \rightarrow 0$, $5 \rightarrow 2 \rightarrow 0$, and $5 \rightarrow 1 \rightarrow 0$. Also, adding to these are all conversion paths involving three frequency conversion steps, as well as four frequency conversion steps, and so on. As the LO power or frequency is changed, the magnitude and phase of every conversion path changes resulting in some paths reinforcing each other while others cancel. This effect is more dependent on the LO power (Fig. 2.11) than on the LO frequency (Fig. 2.12). Also, as expected, the variation of conversion loss over the LO frequency and with a fixed LO power is minimal for a frequency independent embedding impedance equal to 100 $\Omega$.

### 2.2.3 Mixer excess noise and dynamic range

Fig. 2.14 presents the schematic of the receiver and the associated noise figure and loss/gain of each element. $F_{MIX}$ denotes the excess noise figure of the mixer. The main contribution of the mixer noise is the diode shot noise (proportional to the DC bias current). Another component of the mixer noise is the phase noise of the LO (IF away from the carrier). The total noise figure of the mixer is the product of the mixer’s excess noise figure and its conversion loss ($F_{MIX} \times L_{MIX}$). Thus the equivalent noise figure of the entire receiver is given by

$$F_{REC} = L_{MIX} \left[ F_{MIX} + (F'_{LNA} - 1) + \frac{(F_{SA} - 1)}{G'_{LNA}} \right]$$

(2.6)

where $F_{SA}$ (17 dB) is the noise figure of the spectrum analyzer, and $F'_{LNA}$ (3.3 dB) and $G'_{LNA}$ (40 dB) are the noise figure and gain of the LNA respectively (with the IF losses included as shown in Fig. 2.14). The IF losses ($L_{IF}$) in the receiver are low ($\sim 1.5$ dB) and have little effect on the noise analysis.

Since the spectrum analyzer noise figure is reduced by the large gain of the LNA, the receiver noise figure can be approximated by $F_{REC} \approx L_{MIX} \left(F_{MIX} + (F'_{LNA} - 1)\right)$. The noise power at the output of the receiver can then be related to the input noise power by
Equation 2.7 can be used to extract $F_{MIX}$ from a measurement of $N_{out}$ (since $N_{in}$, $G'_{LNA}$, and $F'_{LNA}$ are all known quantities). In this way, the excess noise figure of the mixer was measured as a function of LO power and is plotted in Fig. 2.15. Since $F_{MIX} \gg F'_{LNA}$ for a LO power greater than 5 dBm, the output noise power can be approximated with

$$N_{out} \approx N_{in} G'_{LNA} F_{MIX}. \quad (2.8)$$

The schematic in Fig. 2.16 illustrates the signal path from the input of the net-
Figure 2.16: Schematic of the quasi-optical network analyzer showing all system losses.

work analyzer to the output. The output signal power can be expressed as

\[ S_{\text{out}} = S_{\text{in}} \left( \frac{G_{\text{LNA}}}{L_{\text{TOTAL}}} \right) \]  

(2.9)

where \( L_{\text{TOTAL}} = L_{\text{LO}}L_{\text{MULT}}L_{\text{RF}}L_{\text{MIX}}L_{\text{IF}} \). The output signal-to-noise ratio can then be expressed in terms of the input signal-to-noise ratio as

\[ \frac{S_{\text{out}}}{N_{\text{out}}} = \frac{S_{\text{in}}}{N_{\text{in}}} \frac{1}{L_{\text{TOTAL}}F_{\text{MIX}}} \]  

(2.10)

The total loss and the measured excess noise figure of the mixer are listed in Table 2.3 for the three harmonic multiples (and their associated RF bandwidth) used in the network analysis scheme. The total loss includes the loss at the RF, LO, and IF (listed in Table 2.3) as well as the conversion loss of the multiplier and mixer (plotted in Fig. 2.12). The calculated RF loss includes \( 2 \times 0.4 \) dB of back-side radiated power loss of the silicon lens (\( 2 \times \) because there are two silicon lenses), \( 2 \times 1.8 \) dB of reflection loss at the silicon-air interface, \( 2 \times 0.4 \) dB of Gaussian coupling loss, and \( 2 \times 0.1 \) dB of absorption loss inside the silicon lens. It is assumed that the input signal power is 16 dBm and the input noise power is -144 dBm (which is the equivalent thermal noise power of a room temperature load in a 1 kHz bandwidth) resulting in a 160 dB input signal-to-noise ratio. The output signal-to-noise ratio can then be calculated with (2.10) and is listed in Table 2.3 for each \( n \). The calculations show that a dynamic range of \( > 50 \) dB can be achieved up to 50 GHz in a 1 kHz IF bandwidth.

2.3 Measurements

A picture of a fabricated and packaged receiver is shown in Fig. 2.17 (both top and bottom view). A zoom-in on the central region of the receiver shows the diode
Table 2.3: Expected output signal-to-noise ratio in a 1 kHz IF bandwidth (all losses and ratios expressed in dB). $L_{\text{MULT}}$ and $L_{\text{MIX}}$ values are shown in Fig. 2.12.

<table>
<thead>
<tr>
<th>n</th>
<th>RF (GHz)</th>
<th>$L_{RF}$</th>
<th>$L_{LO}$</th>
<th>$L_{IF}$</th>
<th>$L_{TOTAL}$</th>
<th>$F_{MIX}$</th>
<th>$S_{in}/N_{in}$</th>
<th>$S_{out}/N_{out}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>5</td>
<td>15-25</td>
<td>5.4</td>
<td>2.5</td>
<td>1.5</td>
<td>58</td>
<td>20</td>
<td>160</td>
<td>82</td>
</tr>
<tr>
<td>7</td>
<td>25-35</td>
<td>5.4</td>
<td>2.5</td>
<td>1.5</td>
<td>67</td>
<td>20</td>
<td>160</td>
<td>73</td>
</tr>
<tr>
<td>11</td>
<td>35-50</td>
<td>5.4</td>
<td>2.5</td>
<td>1.5</td>
<td>85</td>
<td>20</td>
<td>160</td>
<td>55</td>
</tr>
</tbody>
</table>

soldered in the middle of a double-slot antenna. The LO and IF interface to the PCB is done with flange mount SMA connectors as shown. The silicon lens is held in-place, on the bottom-side of the PCB, with nylon rods. A thin layer of dielectric paste (with a permittivity similar to that of silicon) is used at the interface of the lens and PCB to minimize air gaps.

### 2.3.1 Antenna measurements

Antenna pattern measurements were done on a double-slot and sinuous antenna inside a packaged receiver by dc biasing the diode and using it as a video detector. Fig. 2.18 shows the measured E- and H-plane patterns (both the co-polarization and cross-polarization components) of the double-slot antenna from 18-40 GHz and of the sinuous antenna from 18-28 GHz. Because the highest frequency cell in the sinuous antenna was filled in to make room for the diode, the antenna radiates above 30 GHz mostly from the gap at the feed resulting in high cross-polarization levels. Also slightly higher cross-polarization levels are measured below 20 GHz for both antennas because of the contribution from the CPW lines. Below 20 GHz the CPW line radiates since its ground to ground spacing ($W+2G$) is on the order of $\lambda_d/5$. The resulting received RF power is passed directly to the diode as it is not filtered at these frequencies by the sinuous antenna or by the low-pass filters connected to the double-slot antenna.

A forward pattern directivity was extracted from measurements with [56]
Figure 2.17: (a) Top view of packaged receiver showing double-slot antenna with integrated diode, and (b) bottom view showing silicon lens pressed against bottom-side of PCB.
\[
D \approx \frac{32400}{\theta_{3dB-E}\theta_{3dB-H}}
\]  
(2.11)

and also calculated with

\[
D = \frac{4\pi A_e}{\lambda^2}
\]  
(2.12)

where the effective aperture, \( A_e \), was estimated to be 85% of the physical aperture. Both directivities are plotted in Fig. 2.19 for a double-slot antenna resonant at 30 GHz. Good agreement is seen between the measured and calculated directivities.

2.3.2 Conversion-loss measurements

Block diagrams of the transmitter and receiver used in the conversion-loss measurements are shown in Fig. 2.20. In the double-slot or sinuous based transmitter setup, a source connected to a 180° hybrid is used to generate the differential LO signal. Bias-Ts are used to provide a DC path to the diode so that it is able to self bias. In the receiver setup, two external high-pass filters are used to block the IF signal from coupling into the LO path. Also, a splitter/combiner is used to combine the differential IF signal before it is passed to the LNA and the spectrum analyzer.

In the up-conversion measurement setup, a double-slot based transmitter was positioned about 1 meter away from a horn based receiver and the RF output signal, \( S_{RFout} \), was measured as a function of the LO input signal, \( S_{LOin} \) (Fig. 2.20(a)). In the down-conversion measurement setup, a horn based transmitter was positioned about 1 meter away from a double-slot based receiver and the IF output signal, \( S_{IFout} \), was measured as a function of the RF input signal, \( S_{RFin} \) (Fig. 2.20(b)). Given the gains and losses of the system, the measured output signals can be expressed in terms of the input signals as

\[
S_{RFout} = S_{LOin} \times \frac{G_{friis}G_{horn}}{L_{LO}L_{lens}L_{MULT}}
\]  
(2.13)

\[
S_{IFout} = S_{RFin} \times \frac{G_{horn}G_{friis}G_{LNA}}{L_{lens}L_{MIX}L_{IF}}
\]  
(2.14)
Figure 2.18: Measured pattern measurements for double-slot and sinuous antennas showing the co-polarization and cross-polarization components for both the E- and H-plane cuts at 18, 28, 34, and 40 GHz.
Figure 2.19: Simulated and measured directivity as a function of frequency for a double-slot antenna on a silicon lens.

where $G_{\text{horn}}$ is the gain of the standard gain horn (20 dB at 30 GHz), and $G_{\text{friis}} = A_e/(4\pi R^2)$ which assumes $A_e = 0.85 \times A_p$ (where $A_p$ is the physical aperture area of the lens), and $L_{\text{lens}}$ is the RF loss of the antenna (includes the back-side radiated power loss, absorption loss, and reflection loss of the silicon lens). The conversion loss of the mixer and multiplier can thus be extracted from measurements as follows:

$$L_{\text{MULT}} = \frac{S_{\text{LOin}}G_{\text{friis}}G_{\text{horn}}}{S_{\text{RFout}} L_{\text{LO}} L_{\text{lens}}}$$ (2.15)

$$L_{\text{MIX}} = \frac{S_{\text{RFin}}G_{\text{horn}}G_{\text{friis}}G_{\text{LNA}}}{S_{\text{IFout}} L_{\text{IF}} L_{\text{lens}}}$$ (2.16)

The conversion gain was measured as a function of LO power available at the input of the transmitter/receiver with the LO frequency fixed. Figures 2.21(a), 2.21(b), and 2.21(c) show the measured and simulated conversion gain for three different LO harmonics. The measurement was done using the double-slot based transmitter/receiver and the simulation was performed with a harmonic balance simulation of the circuit in Fig. 2.8 using the simulated embedding impedance of the double-slot antenna. A slightly different LO frequency was used for each harmonic multiple in order to avoid suck-outs at particular frequencies caused by destructive interference of the multiple conversion paths. Such suck-outs can be seen in Fig. 2.22 which plots the measured
Figure 2.20: Schematic of sinuous or double-slot (a) transmitter and (b) receiver test setups and (c) horn-based network analyzer.
and simulated conversion gain as a function of RF frequency with the LO power fixed at 12.5 dBm. Overall, good agreement is seen between simulation and measurement across all harmonic multiples.

Fig. 2.23 shows the measured IF power referred to the diode terminals, calculated with $S_{IF\text{diode}} = (S_{IF\text{out}} L_{IF}) / G_{LNA}$, as a function of RF power available at the diode terminals, calculated with $S_{RF\text{diode}} = (S_{RF\text{in}} G_{\text{horn}} G_{\text{friis}}) / L_{RF}$. As expected, a near-perfect linear relationship is measured between the diode RF input power and the diode IF output power, showing that the diode can handle -14 dBm without saturation due to the high LO power used (10 dBm).

2.3.3 FSS measurements

In order to characterize the performance of the quasi-optical network analyzer, a frequency selective surface (FSS) was designed and used as the DUT. The FSS consists of a $n \times n$ array of unit cells, each consisting of dual-polarized half-wavelength slots as shown in Figures 2.24(a) and 2.24(c). The metal layer is fabricated on top of a 0.25 mm thick RT/duroid [52] 5880 substrate ($\epsilon_r = 2.2$). The FSS can be modeled by a parallel LC tank which passes the normally incident RF at the resonant frequency of the slot, and rejects as a short off resonance. Two substrates can be cascaded together, separated with an air gap of length $s$ as shown in Fig. 2.24(b), to give a second-order filter response with sharper roll-off as compared to the single resonator. The substrate slightly loads the FSS resulting in a slightly shorter slot length given by $l_s = (1 / \sqrt{\epsilon_m}) \times \lambda_0/2 = 0.8 \times \lambda_0/2$ where $\epsilon_m = (1 + \epsilon_r)/2$ and $\epsilon_r = 2.2$.

An infinite two-dimensional array of unit cells with various resonant frequencies was simulated in HFSS. The infinite array was synthesized through the use of PEC and PMC walls around a single unit cell. A simplified model of the 1-pole FSS is a single shunt LC resonator implemented as a 2-port and loaded at both ports with the free space impedance $\eta_0$ as shown in Fig. 2.25(a). The simulated 3 dB fractional bandwidth of the 1-pole FSS can be used to calculate a loaded quality factor ($Q_L = 1/\Delta_{3dB}$) which can be used to calculate the lumped element values and the susceptance parameter of the equivalent LC resonator by
Figure 2.21: Simulated and measured conversion gain as a function of LO power: (a) n=5 and (b) n=7.
Two lumped-element LC resonators separated by an admittance inverter implemented with a quarter-wavelength transmission line as shown in Fig. 2.25(b), can be used to realize a 2-pole filter response. In order to achieve the same response with an FSS, two layers should be cascaded as shown in Fig. 2.24(b), and the space in between them used as the quarter-wavelength section of transmission line. The impedance of each quarter-wavelength section is determined by the value of the associated J-inverter which depends on the g-values of the prototype 2-pole Chebyshev filter, the susceptance parameter $b$, and the filter’s fractional bandwidth $\Delta$, as follows:

\[
Z_1 = \frac{1}{J_{0,1}} = \sqrt{\frac{g_0 g_1 \eta_0}{b \Delta}}
\]

(2.20)
Figure 2.22: Simulated and measured conversion gain for (a) multiplier and (b) mixer as a function of RF frequency. The LO frequency is swept from 3-5 GHz.
Figure 2.23: Measured down-converted IF power as a function of available RF power (both powers are referred to the diode terminals). The LO power in the mixer is fixed at 10 dBm.

\[ Z_2 = \frac{1}{J_{1,2}} = \frac{1}{\Delta} \sqrt{\frac{g_1 g_2}{b^2}} \]  \hspace{1cm} (2.21)

\[ Z_3 = \frac{1}{J_{2,3}} = \sqrt{\frac{g_2 g_3 \eta_0}{b\Delta}} \]  \hspace{1cm} (2.22)

A 1-pole FSS at 30 GHz was simulated in HFSS in a 2-port configuration. The simulated \( S_{21} \) was used to extract \( Q_L = 6 \) resulting in \( b = 0.03 \) which was used in 2.20, 2.21, and 2.22 to calculate the impedance of each quarter-wavelength section. It turns out that for a fractional bandwidth or around 10% (\( \Delta = 0.1 \)), the impedance of each transmission line section evaluates to a value close to \( \eta_0 \). This means that a simple implementation of the 2-pole FSS is to use two layers separated by a quarter-wavelength air gap. The separation \( s \) can then be tuned slightly in HFSS to result in the desired filter response. Using this technique, a 2-pole FSS was designed at 20, 30, and 40 GHz and the resulting dimensions are summarized in Table 2.4.

A picture of the fabricated frequency selective surface is shown in Fig. 2.26. The assembly process in action of a 2-pole FSS is shown in Fig. 2.26(a). Alignment holes which accept nylon screws are drilled around the perimeter of both FSS layers. Nylon washers are used to implement an adjustable air gap of 1-3 mm between the two layers.
Figure 2.24: (a) Layout of a single unit cell which when cascaded in a (c) $n \times n$ two-dimensional array creates a frequency selective surface (grey is metal and white is slot). (b) A cross-section view of a 2-pole FSS.

Table 2.4: Parameters summarizing three different 2-pole FSS designs.

<table>
<thead>
<tr>
<th>$f_0$ (GHz)</th>
<th>$\lambda_0/2$ (mm)</th>
<th>n×n</th>
<th>s (mm)</th>
<th>L (mm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>20</td>
<td>7.5</td>
<td>11×11</td>
<td>2.4</td>
<td>82.50</td>
</tr>
<tr>
<td>30</td>
<td>5</td>
<td>16×16</td>
<td>1.8</td>
<td>80.00</td>
</tr>
<tr>
<td>40</td>
<td>3.75</td>
<td>21×21</td>
<td>2.4</td>
<td>78.75</td>
</tr>
</tbody>
</table>
Figure 2.25: Circuit model of (a) 1-pole FSS and (b) 2-pole FSS.

For mechanical support, the FSS is screwed into a thick board with metal on both sides. During measurements, the metal of the support board is covered with absorber.

The quasi-optical network analyzer was assembled as shown in Fig. 2.1 but without the objective lenses (for a simpler test setup). The assembled FSS was used as the DUT and positioned half-way between the transmitter and receiver which were spaced approximately 1 meter apart. At this distance, the FSS appears in the far-field of both the transmitter and receiver resulting in a RF wave with an equi-phase front at the surface of the FSS. The Friis transmission between two identical antenna apertures can be expressed as

$$\frac{P_r}{P_t} = \left(\frac{A_e}{R\lambda}\right)^2$$

and evaluates to -34 to -24 dB at 15 to 50 GHz for R=1 m, where $A_e$ is the effective lens aperture area (estimated at 85% of the physical area).

A picture of the complete setup with the FSS positioned in-between the transmitter and receiver is shown in Fig. 2.27(a). Absorber is used in the setup to minimize reflections. A calibration sample was also fabricated which consisted of an identical FSS support fixture but with the FSS area removed as shown in Fig. 2.27(b). Also, two versions of the network analyzer were assembled and characterized, one with a transmitter and receiver based on the double-slot antenna (Fig. 2.3(a)) and another based on
Figure 2.26: (a) Picture showing top-metal of two FSS layers, with the bottom one containing holes around the perimeter which are aligned to the nylon screws in the top one, allowing (b) the two FSS layers to be fastened together while still separated by an air gap.
the sinuous antenna (Fig. 2.3(b)).

To achieve a calibrated $S_{21}$ measurement, the RF signal power was measured through the FSS (stored as variable $S_{IF_{out,FSS}}$), and through the calibration sample (stored as variable $S_{IF_{out, hole}}$), resulting in $S_{21} = S_{IF_{out,FSS}}/S_{IF_{out, hole}}$. The measurement sequence consisted of sweeping the transmitter LO frequency, $LO_T$, and the receiver LO frequency, $LO_R$, from 3-5 GHz with a constant 10 MHz offset between the two. At each frequency step, IF signals were measured at 50, 70, and 110 MHz corresponding to the mixing products generated by $5 \times LO_T$ (15-25 GHz), $7 \times LO_T$ (21-35 GHz), and $11 \times LO_T$ (33-55 GHz) RF signals, respectively. The IF bandwidth was set to 1 Hz. The entire measurement sequence was automated with a computer.

The measured and simulated $S_{21}$ of three different 2-pole frequency selective surfaces are shown in Figures 2.28, 2.29, and 2.30. Each FSS was measured with the double-slot and sinuous based network analyzer, and also with a horn based network analyzer (shown schematically in Fig. 2.20(c)). The quasi-optical network analyzer measurement and the horn measurement are in excellent agreement with each other and with the HFSS simulation. The measured insertion loss is <1 dB at the center frequency of each FSS. A measurement of the 30 GHz FSS (Fig. 2.29) shows the extent of the network analyzer’s dynamic range in the high-frequency portion of the spectrum. The double-slot based network analyzer is able to measure close to -45 dB of rejection at 43 GHz.

One discrepancy is that in the lower frequency range a higher rejection is simulated than what is measured for the 30 GHz and 40 GHz FSS. This is especially pronounced in the measurement of the 40 GHz FSS. The reason for this is that around 20 GHz, the half-power beamwidth of the lens antenna is double what it is around 40 GHz. This means that at 20 GHz only a small portion of the radiated RF energy goes through the FSS, and the rest is dissipated in the absorber. However, the absorber is not perfect and some of the energy is scattered resulting in coupling between the transmitter and receiver. The coupling level increases as the directivity of the antennas decreases, and is the reason why the rejection around 20 GHz is worse for the lens-based network analyzer (where the directivity is $\sim 14$ dB) as compared to the horn-based network analyzer (where the directivity is $\sim 20$ dB).
Figure 2.27: Picture of quasi-optical network analyzer setup with the (a) FSS and (b) calibration sample placed in between the transmitter and receiver.
As expected, the double-slot based network analyzer performs slightly better near 30 GHz, the design frequency of the DS planar antenna. This can be seen in the measured response of the 20 GHz FSS (Fig. 2.28) which shows the double-slot based NA measurement in better agreement with the horn measurement around 30 GHz as compared to the sinuous measurement. However, overall, the double-slot based and the sinuous based network analyzer result in similar performance, and no significant advantage is seen in using one over the other. The reason for this is that, first, the directivity of the antenna is mostly determined by the size of the silicon lens and not by the exact planar antenna design. Second, although the sinuous antenna theoretically results in a more stable antenna input impedance over the RF bandwidth as compared to the double-slot antenna, the double-slot antennas has a very wide-band impedance with a VSWR < 1.7 at 20-40 GHz. Also, even small fluctuations in antenna impedance can result in large fluctuations in conversion loss over frequency due to constructive and destructive interference of the multiple conversion paths, and both the sinuous and double-slot antenna have these fluctuations. Therefore, when more than one harmonic multiple is used at the same time in high-order harmonic multiplication and mixing, it becomes too difficult to define an optimal diode embedding impedance. One embedding impedance may be optimal over a specific frequency range and with a specific harmonic multiple but it may result in poor conversion loss at another frequency range using another harmonic multiple.

2.4 Conclusion

A wide-band quasi-optical network analyzer has been successfully demonstrated in the microwave frequency range using hardware and high-order harmonic mixing schemes that are extendable to millimeter-wave frequencies. The network analyzer is based on a double-slot antenna with an integrated Schottky-diode mixer placed on an extended hemispherical silicon lens. The hardware is planar and results in a compact and low-cost solution particularly if scaled to higher millimeter-wave and terahertz frequencies. In order to verify its performance, the network analyzer was used to measure 2-pole frequency selective surfaces centered at 20, 30, and 40 GHz, and the measured
Figure 2.28: Measured and simulated $S_{21}$ of 2-pole frequency selective surface centered at 20 GHz.
Figure 2.29: Measured and simulated $S_{21}$ of 2-pole frequency selective surface centered at 30 GHz.
Figure 2.30: Measured and simulated $S_{21}$ of 2-pole frequency selective surface centered at 40 GHz.
results are in excellent agreement with a horn-based system.

Chapter 2, in part, is currently being prepared for submission for publication of the material. Alex Grichener and Gabriel M. Rebeiz. The dissertation author was the primary investigator and author of this material. This chapter also includes material published in IEEE MTT-S Int. Microwave Symposium, 2011. Alex Grichener, and Gabriel M. Rebeiz. The dissertation author was the primary investigator and author of this material.
Chapter 3

High-Reliability RF MEMS Switched Capacitors

3.1 Introduction

RF MEMS switches and switched-capacitors have emerged as a high performance technology with very low loss and high linearity for use in switching networks, impedance matching networks, tunable filters, and phase shifters [35]. In particular, the Radant MEMS metal-contact switch and the MIT-Lincoln Laboratories and Raytheon capacitive switches have all shown excellent reliability (> 100 B cycles) and power handling (> 1 W). Metal-contact switches result in medium-Q (50-100) tunable networks due to their 1-2 Ω contact resistance. Capacitive switches, on the other hand, have a resistance of 0.25-0.5 Ω and result in high-Q (100-200) tunable circuits at 1-6 GHz. These devices can be arrayed with fixed capacitors in a switched-capacitor bank, which is an essential variable impedance element in a tunable network.

This chapter presents an RF MEMS switched-capacitor that is based on a thick metal process which is ideal for 1-10 GHz applications. The research studies the effect of cantilever beam thickness and associated vertical stress gradient, and the effect of incident RF power on the resulting device performance. Also, the chapter advances a deeper understanding of various charging mechanisms at work and their effect on switch reliability. The design allows for the switched-capacitor to be operated with no applied
electric field across the dielectric layer and therefore, has resulted in high reliability operation under high RF power. A capacitance ratio of 5-9 is achieved, and part of this capacitance region is obtained using an analog regime, thereby allowing fine capacitance control which is essential for tunable filters. The RF MEMS switched-capacitor has a high Q (> 200 at 5 GHz) and has been used in several high-Q tunable filters with excellent performance [57,58]. The last section presents another cantilever device which bypasses dielectric charging altogether by featuring a dielectric-less switched capacitor design which exhibits ultra-reliable operation but at the expense of a lower capacitance ratio of around 2.

3.2 Design

Figure 3.1 presents the top view and cross-section of the RF MEMS switched capacitor. The device is based on a thick electroplated cantilever with an isolated actuation electrode. When a voltage $V_s$ (> $V_{pi}$, the pull-in voltage) is applied to the actuation electrode, the cantilever beam is pulled-down and touches the RF electrode, resulting in a capacitance ratio of 5. However, the capacitance ratio can be increased to 7-9 by increasing $V_s$ or by applying a small voltage $V_h$ to the RF electrode ($\leq$ 10 V). This results in a movement of the cantilever which brings the beam tip closer to the dielectric and increases the contact area (zipping effect).

There are many degrees of freedom in the cantilever design depending on the requirements. The spring constant, $k$, is mostly dependent on the cantilever thickness and length as $k \propto (t_b/L)^3$. Since a higher spring constant is desirable for a robust mechanical design, the length of the cantilever was limited to less than 200 $\mu$m. It is possible to increase the thickness of a long cantilever and maintain the same spring constant, but this results in a large structure and consequently a slower switching speed. The width of the cantilever was also limited to less than 200 $\mu$m in order to prevent excessive curling (due to a vertical stress gradient) at the corners of the beam tip.

Once the area of the cantilever beam is chosen, the overlap area between the beam and the DC electrode as well as the RF electrode is determined. A larger overlap with the RF electrode will result in a higher capacitance but at the expense of a smaller
Figure 3.1: Top view (top), cross section in up-state (middle), and cross section in down-state (bottom) of switched-capacitor with z-axis expanded $\times 10$ (all dimensions given in $\mu m$).
overlap with the DC electrode resulting in a higher pull-in voltage. The air gap $g_0$ is a straightforward compromise between the capacitance ratio and the pull-in voltage given by $V_{pi} = \sqrt{\frac{8kq_0^3}{27\varepsilon_0A}}$.

The device with dimensions shown in Figure 3.1 was achieved with a requirement of a maximum DC operating voltage of 80 V, $C_u/C_d = 50/250$ fF (with 10-30% analog tuning of $C_d$), a switching time of less than 50 $\mu$s, and excellent yield for a vertical stress gradient in the cantilever beam of +/- 2 MPa/µm. Also, since many different parameters depend on the beam thickness (such as electrical/mechanical $Q$, switching time, power handling, spring constant, etc.), the thickness was limited to a range of 3.5-4.5 µm due to the plating process. For example, an important trade-off is while a thicker device results in shorter switching times and higher power handling, it also has a higher pull-in voltage and a smaller analog tunable range.

The resulting device is $140 \times 160$ µm$^2$ with an air gap of 1.5 µm and an RF overlap area of $36 \times 160$ µm$^2$. At 2-4 GHz, eight cantilevers can be used in parallel to result in a total capacitance of 0.4/2.0 pF [58]. This solution is mechanically more robust and with higher yield than using two cantilevers which are 4 times larger in area (slower switching speed, greater sensitivity to stress gradients, etc.).

Figure 3.2 presents the simulated spring constant, resonance frequency, mechanical $Q$, pull-in voltage ($V_{pi}$) and release voltage ($V_r$), and pull-in time ($t_{pi}$) and release time ($t_r$), as a function of beam thickness. A Young’s Modulus of 35 GPa taken from prior measurements on electroplated gold [59] is used in all mechanical simulations. Two spring constants are plotted: 1) $k_n$ (natural spring constant) defined as displacement at the tip due to a distributed force over the entire beam and 2) $k_a$ (actuation spring constant) defined as displacement at the tip due to a distributed force above the actuation electrode. The natural spring constant is used to solve for the release time when no voltage is applied and the tip is touching the RF electrode. The actuation spring constant is used to solve for the pull-in time.

The damping force encountered by the $96 \times 160$ µm$^2$ gold plate was simulated with Coventorware [60] with a correction for the Knudsen number (0.045) which effectively lowered the viscosity by 20% [35]. Also edge correction was used for the three moving edges to model the corner-turning resistance. The resulting damping coeffi-
Figure 3.2: Simulated electromechanical parameters plotted as a function of beam thickness.
The simulated pull-in and release voltages are almost identical because the device does not actually collapse down to the actuation electrode but is stopped when the tip touches the dielectric. For the given design, the increase in damping with displacement [35] results in a slightly longer pull-in time. Therefore (3.2) will slightly underestimate the pull-in time.

\[
m_n \frac{d^2 x}{dt^2} + b \frac{dx}{dt} + k_n x = 0 \quad \text{(release)}
\]

\[
m_a \frac{d^2 x}{dt^2} + b \frac{dx}{dt} + k_a x = \frac{1}{2} \frac{\varepsilon_0 A V_s^2}{(g_0 - x)^2} \quad \text{(pull-in)}
\]
Figure 3.3 shows the simulated $C-V_s$ curves for a cantilever beam with no stress gradient. In these simulations, an $\epsilon_r = 7.0$ was used for the dielectric and results in a down-state capacitance of 322 fF. An $\epsilon_{eff} \approx 1.0$ can then be extracted using $C_d = \epsilon_{eff} \epsilon_0 A/t_d$. The reason $\epsilon_{eff}$ is low is because, as will be seen later in the simulated down-state profile (Fig. 3.6(a)), the beam is not flush with the dielectric in the down-state and the resulting air gap significantly degrades $C_d$. Simulations also show that for each thickness, a $\Delta V_s$ of 20 V above the pull-in voltage (Fig. 3.3) corresponds to a change in the electrostatic force ($\Delta F_e$) of around 150 $\mu N$. This increases $C_d$ by 85-47 fF in a 3.5-4.5 $\mu$m device, respectively. As expected, a thinner device results in a lower $k$ and a larger tuning range in the down-state position.

### 3.2.1 Vertical Stress Gradient Effects

The cantilever beam curls upwards or downwards depending on the stress gradient polarity. For a two-layer beam, the deflection at the tip due to a stress gradient is given by [35]

$$\Delta z = \frac{3 \Delta \sigma L^2}{4 E'}$$  \hspace{1cm} (3.3)

where $\Delta \sigma = (\sigma_{top} - \sigma_{bottom})/t_b$ is the stepped stress gradient and $E' = E/(1 - \nu)$ is the effective Young’s Modulus calculated using Poisson’s ratio for gold ($\nu = 0.42$). The simulated deflection (using Coventorware) in the x-direction for $t_b = 4 \mu m$ and $\Delta \sigma = +/− 2$ MPa/$\mu$m is shown in Fig. 3.4. Table 3.1 presents the calculated tip deflection using (3.3) and the simulated tip deflection averaged across the width of the cantilever beam ($\Delta \bar{z}$). Excellent agreement is seen between (3.3) and Coventorware.

FEM simulations show that a stress gradient in the cantilever beam can significantly impact the resulting $C-V$ curve. Figures 3.5(a) and 3.5(b) show the $C-V_s$ and $C-V_h$ curves of a 4.0 $\mu$m thick beam with three different stress gradients. A downward curl (negative $\Delta \sigma$) results in a significant depreciation of the down-state capacitance and poor tuning with $V_s$ and $V_h$ (a partial collapse of the beam occurs at $V_h = 6$ V). An upward curl, on the other hand, results in a high down-state capacitance with an excellent linear tuning range with both $V_s$ and $V_h$. 
Table 3.1: Calculated and simulated tip deflection and up-state capacitance as a function of \( \Delta \sigma \)

<table>
<thead>
<tr>
<th>( \Delta \sigma ) (MPa/( \mu \text{m} ))</th>
<th>Calc. ( \Delta z ) (( \mu \text{m} ))</th>
<th>Sim. ( \Delta \bar{z} ) (( \mu \text{m} ))</th>
<th>Sim. ( C_u ) (fF)</th>
</tr>
</thead>
<tbody>
<tr>
<td>-2</td>
<td>-0.5</td>
<td>-0.5</td>
<td>53.6</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>41.8</td>
</tr>
<tr>
<td>+2</td>
<td>+0.5</td>
<td>+0.5</td>
<td>33.6</td>
</tr>
</tbody>
</table>

Simulated cross-sections of a 4.0 \( \mu \text{m} \) beam with three different stress gradients (Fig. 3.6(a)) show that an upward curled beam is most flush with the dielectric in the down-state (although the corners at the beam tip are slightly lifted which is why the initial \( C_d \) is not higher), and therefore can be deformed more easily with an electrostatic force at the actuation electrode (\( V_s \)) or at the RF electrode (\( V_h \)). A beam with a downward curl, on the other hand, makes a larger angle with the dielectric in the down-state and therefore results in a smaller down-state capacitance and tuning range. The cross-section of a beam with an upward curl (\( \Delta \sigma = +2 \text{ MPa/\( \mu \text{m} \)} \)) pulled-down with different voltage combinations is shown in Figure 3.6(b).
Figure 3.5: Simulated cantilever (a) $C-V_s$ curves with hysteresis, and (b) $C-V_h$ curves with hysteresis where $\Delta \sigma$ is in the range of -2 to 2 MPa/$\mu$m and $t_b = 4.0 \mu$m.
Figure 3.6: Simulated down-state profile of a 4.0 µm thick beam with z-axis expanded ×25 where (a) ∆σ = −2, 0, +2 MPa/µm and (b) ∆σ = +2 MPa/µm with different $V_s$ and $V_h$ applied.
3.3 Fabrication

The RF MEMS devices are fabricated on a 500 $\mu$m-thick quartz substrate and are implemented in a CPW configuration. First, a SiCr layer (1200 Å) is sputtered and patterned to form the high resistance bias lines. Second, a metal layer consisting of Ti/Au (200 Å/3000 Å) is sputtered and patterned to form the bottom electrodes. A Si$_3$N$_4$ layer (0.15 $\mu$m) is then deposited with PECVD and patterned with RIE to form the dielectric layer. A PMMA layer (1.5 $\mu$m) is coated as the sacrificial and patterned with RIE. Next, a second metal layer consisting of Ti/Au/Ti (200 Å/3000 Å/200 Å) is sputtered and selectively electroplated to form the 3.5-4.5 $\mu$m thick beams. Finally, the second metal is etched, the cantilevers are released in a standard photoresist stripper, and the sample is dried in a CO$_2$ critical point dryer. The fabricated devices are shown in Fig. 3.7. As seen in the 1-port configuration, the $V_h$ pad is DC isolated from the CPW ground using a large MIM capacitor (14.5 pF).

3.4 Measurements

3.4.1 RF

The device circuit models are shown in Fig. 3.8 and the corresponding measured and fitted S-parameters are shown in Fig. 3.9. For a flat beam, the fitted up-state capac-
Figure 3.8: Circuit model of (a) 1-port and (b) 2-port device.

The relationship between the measured and simulated capacitance and vertical stress gradient is shown in Fig. 3.10. It is seen that the measured $C_u$ is 37-53 fF, and is in excellent agreement with simulations. The $Q$ is calculated from the measured $S_{11}$ of a 1-port device which does not yield accurate results for $Q$ greater than 100 (see error bars in Fig. 3.8). An $R_s$ of around 0.5 $\Omega$ is extracted from the measurements, and is dominated by the loss of the RF electrode which is 0.3 $\mu m$ thick.

$C-V$ curves were obtained by fitting the measured S-parameters to the circuit models. As predicted by FEM simulations, the down-state capacitance tuning slope is enhanced with a positive stress gradient (upward curl) and a thinner beam (Fig. 3.12). Measurements also show that the 4.0 $\mu m$ cantilever pulls-in at 54 V while the 4.5 $\mu m$ cantilever pulls-in at 65 V which is in excellent agreement with the simulated pull-in voltages (Fig. 3.2).
Figure 3.9: Measured and fitted S-parameters of (a) 1-port and (b) 2-port device.
Figure 3.10: Measured and simulated up- and down-state capacitance (and resulting ratio) as a function of stress gradient.

Figure 3.11: Extracted up- and down-state $Q$ with error bars.
Figure 3.12: (a) Measured $C-V_s$ curves with hysteresis where $t_b = 4.0 \, \mu m$ and $\Delta \sigma = 0, +1 \, \text{MPa}/\mu m$ and where $t_b = 4.5 \, \mu m$ and $\Delta \sigma = +1 \, \text{MPa}/\mu m$ and (b) measured $C-V_h$ curves with hysteresis where $t_b = 4.0, 4.5 \, \mu m$ and $\Delta \sigma = +1 \, \text{MPa}/\mu m$. 
3.4.2 Mechanical Measurements

The setup in Fig. 3.13 can be adapted to different mechanical measurements. For the mechanical resonance frequency and $Q$ measurement, the function generator is used to excite the cantilever beam with a sinusoidal voltage and a DC offset voltage. This results in an amplitude modulation (AM) for an RF signal passing through the 2-port device and the resulting spectrum is detected using a spectrum analyzer [35].

The resonance frequency and $Q$ are extracted by fitting the measured AM response to a normalized second-order system (Fig. 3.14, Table 3.2). Note that the extracted $Q$ is the actuation $Q_a$ since the device is being displaced with a voltage at the actuation electrode. The extracted $Q_a$ is lower than simulated for a 3.5 $\mu$m beam, and higher than simulated for a 4.5 $\mu$m beam. The discrepancy is due to stress gradients in the fabricated devices and the resulting gap deviation from $g_0$.

To measure the switching time, a 2-port device was hot switched with a 50% duty cycle uni-polar square waveform and the resulting power detector output was used to record the switching dynamics (Fig. 3.15, Table 3.2). Overall there is good agreement between measured and calculated release times, while the measured pull-in times are 20-40% longer than calculated for reasons discussed in Section 3.2.

Table 3.2: Measured resonance frequency, $Q_a$, and switching times as a function of beam thickness

<table>
<thead>
<tr>
<th>$t_b$ ($\mu$m)</th>
<th>$f_0$ (kHz)</th>
<th>$Q_a$</th>
<th>$t_r$ ($\mu$s)</th>
<th>$t_{pi}$ ($\mu$s) ($V_s = 1.2 \times V_{pi}$)</th>
</tr>
</thead>
<tbody>
<tr>
<td>3.5</td>
<td>29</td>
<td>0.30</td>
<td>60</td>
<td>46</td>
</tr>
<tr>
<td>4.0</td>
<td>33</td>
<td>0.90</td>
<td>54</td>
<td>42</td>
</tr>
<tr>
<td>4.5</td>
<td>36</td>
<td>1.80</td>
<td>30</td>
<td>34</td>
</tr>
</tbody>
</table>

3.4.3 Power Handling

RF power incident on a 2-port device induces an effective $V_h$ which is plotted in Fig. 3.16(a) for both the up- and down-state positions. This rms voltage generates an
Figure 3.13: Core measurement setup used for resonance frequency, switching time, power, and reliability measurements.

Figure 3.14: Measured and fitted mechanical gain as a function of excitation frequency for three different beam thicknesses.
Figure 3.15: (a) Measured release time shown for \( t_b = 3.5-4.5 \mu m \) and (b) measured pull-in time \( (t_b = 4.0 \mu m) \) shown for \( V_s/V_p = 1.00-1.25 \).
electrostatic force on the cantilever and decreases both its pull-in and release voltage. It also increases the release switching time. These are plotted in Fig. 3.16 as a function of the incident power level at 10 GHz. It is seen that a 4-4.5 µm device can handle 0.6-1.1 W before failing to release in a hot-switched condition.

3.4.4 $V_{pi}$ vs. Temperature

The temperature stability of a device ($t_b = 4.0 \mu m$) was studied by measuring the change in the pull-in voltage as a function of temperature (Fig. 3.17). Measurements show the pull-in voltage decrease by 3 V with a 100° C change in temperature. This is most likely due to gold softening at the higher temperatures leading to a decrease in the spring constant.

3.4.5 Reliability Tests

The reliability of the device was studied with a setup similar to one used by Blondy et al. (Fig. 3.13) [61]. The response of a device hot switched with three different bias waveforms (shown in Fig. 3.18) applied to the actuation electrode was measured using a RF power detector connected to an oscilloscope. The incident RF power was limited to 100 mW so as not to induce a $V_{h}(\text{rms})$. Every bias waveform included two successive triangular pulses of opposite polarity (each 15 ms wide), which allowed for an automated detection (with the help of a PC) of both the positive and negative pull-in and release voltage. The triangular pulses were applied at a frequency of 1 Hz and therefore lasted for 3% of the time. The other 97% of the bias waveform, depending on the specific experiment, consisted of one of the following: 1) $V_s = 0$ (discharge mode), 2) Unipolar $V_s > V_{pi}$ (unipolar charge mode), 3) Bipolar $V_s > V_{pi}$ (bipolar charge mode). In this way the evolution of $V_{pi}$ and $V_r$ could be automatically recorded under different biasing conditions.

Charging effects induced by a unipolar voltage at the actuation electrode (with $V_h = 0$) were characterized by measuring the evolution of $V_{pi}$ and $V_r$. To get a baseline, the setup was run in discharge mode for the first half hour, and the switch was then pulled-down with a unipolar $V_s$ (Fig. 3.20(a)). The steady decrease of $V_{pi}$ and $V_r$ is
Figure 3.16: (a) Calculated effective $V_h$(rms) in the up-state and down-state positions, and measured (b) release voltage and (c) release time for $t_b = 3.5-4.5 \, \mu m$ as a function of incident RF power at 10 GHz.
Figure 3.17: Measured pull-in voltage as a function of temperature ($t_b = 4.0 \mu m$). Data from [1].

Figure 3.18: Three typical bias conditions that allow for an automatic recording (with the use of narrow triangular pulses) of the evolution of $V_{pi}$ and $V_r$. 
Figure 3.19: Two charging mechanisms shown: bulk charging in the quartz substrate and top charging in the dielectric.

indicative of bulk charging which is caused by the injection of positive charge by the electrode, into the quartz substrate. This is different from top charging which is caused by the injection of negative surface charge by the cantilever beam into the dielectric, as shown in Fig. 3.19. The change in $V_{pi}$ and $V_r$ can be fitted to a Curie-Von Schweidler equation [61] as

$$\Delta V = A \times (t/t_0)^n$$

with $A = 0.6$ V, $t_0 = 1$ s, and $n = 0.3$.

Figure 3.20(a) shows that after around 5 hours of charging, and a shift of 11-12 V in $V_{pi}$ and $V_r$, the switch quickly recovers to a steady-state condition when released. The short recovery time constant is further evidence of bulk charging where the path from the charge traps to the closest conductor is relatively short as compared to top charging [62, 63]. However it is seen that the switch does not recover to its original pull-in and release voltages which is indicative of additional charging mechanisms with much slower discharge time constants, such as surface charging due to humidity in the surrounding ambient atmosphere [64].

In a similar fashion, the evolution of $V_{pi}$ and $V_r$ due to a bipolar voltage at the actuation electrode (with $V_h = 0$) were measured and fitted with $A = 0.8$ V, $t_0 = 1$ s, and $n = 0.2$ (Fig. 3.20(b)). Note that the pull-in and release voltages nearly recover to their original levels. The excellent fit to the given exponentials is consistent with previous charging measurements in dielectric-less capacitive RF MEMS [61].

The voltage shift, $V_D$, for a given duty cycle, $D$, can be expressed as $V_D = V_{100\%} \times D$ where $V_{100\%}$ is the voltage shift due to a 100% duty cycle [61]. Also, an
Figure 3.20: Evolution of measured and fitted pull-in and release voltage when the device is pulled-down with (a) uni-polar $V_s$ and (b) bi-polar $V_s$. 
Figure 3.21: Simulated electric field distribution in air gap and quartz substrate of switch in down-state position with 60 V applied to actuation electrode and with RF electrode and beam grounded.

Extrapolation of the Curie-Von fit allows for a prediction of the switch lifetime: if only substrate charging is considered for the case of unipolar actuation then it would take 24 days for $V_r$ to fall to zero (stuck down) with a 100% duty cycle and 240 days with a 50% duty cycle. The values are 24 and 768 years, respectively, for bipolar actuation.

A 2-D electrostatic simulation of the electric field distribution with $V_s = 60$ V was performed using Maxwell SV [65]. Fig. 3.21 shows that most of the electric field is contained inside the air gap between the beam and the actuation electrode. However, the field also expands several microns into the substrate underneath the edge of the electrode. The simulated field magnitude in this region is 10-30 MV/m which is sufficient to induce charge injection.

Charging effects produced by a unipolar and bipolar voltage ($V_h \leq 10$ V) at the RF electrode was also studied. Figure 3.22 shows the evolution of the pull-in voltage when the switch is pulled-down with a bi-polar $V_s$, and with $V_h = 10$ V uni-polar and $V_h = 10$ V bi-polar. Before the application of a $V_h$, the switch was left in the down-state with a bipolar $V_s$ for over 2 hours in order to allow substrate charging to stabilize so that the effect of a $V_h$ could be studied nearly independently of substrate charging. The measurement shows that a unipolar $V_h$ causes the $V_{pi}$ to increase by almost 2 V before stabilizing at the 4 hour mark, while a bipolar $V_h$ does not result in a significant shift of $V_{pi}$. This demonstrates the importance of using only a bipolar voltage at the RF electrode.
Figure 3.22: Evolution of measured pull-in voltage when the device is pulled-down with a bi-polar $V_s$ and $V_h = 10$ V: uni-polar and bi-polar.

PECVD $\text{Si}_3\text{N}_4$ introduces a high density of charge traps associated with silicon dangling bonds [66]. An increase in the pull-in voltage suggests an injection of top charge into the dielectric which sets up an electric field that directly opposes the applied field. It is important to note that all charging experiments were performed in ambient atmosphere. In contrast to bulk charging, surface charging can be significantly impacted by humidity [62], and $\text{Si}_3\text{N}_4$ is susceptible to moisture-related surface charging. This is unexpected because $\text{Si}_3\text{N}_4$ is generally hydrophobic. However, it can be made hydrophilic after aggressive surface treatments such as oxygen plasma cleaning [67] which was the case with devices used here. For the time duration that the dielectric is subjected to $V_h$, the accumulation of injected charge can be modeled as [66]

$$Q = \sum_j Q^j \left[ 1 - \exp \left( -t / \tau^j \right) \right]$$

(3.5)

where $\tau^j$ is the charging time constant of the $j_{th}$ species of trap, and $Q^j$ is the corresponding steady-state charge density and is related to $V_h$ by

$$Q^j = Q^j_0 \exp \left( V_h / V^j_0 \right)$$

(3.6)

where $Q^j_0$ and $V^j_0$ are fitting parameters for each species of trap. The voltage shift that results from the trapped charge sheet is given by
\[ \Delta V = \frac{Qh}{\varepsilon_0 \varepsilon_r} \]  

(3.7)

where \( h \) is the distance between the bottom electrode and the charge sheet (typically a fitted parameter). Since \( V_h \) was limited to 10 V, the charge time constants of the nitride are seen most clearly by measuring the shift in the release voltage. Fig. 3.23 shows the measured release voltage immediately dropping to 16 V with an application of \( V_h = 10 \text{ V uni-polar} \) (this is expected), and then slowly rising to 45 V. As before, \( V_h \) is applied to a switch that has been pulled-down with a bipolar \( V_s \) for at least several hours. It follows from (3.5), (3.6), and (3.7) that the change in the release voltage can be fitted to \( \Delta V = \sum_j V_j \left[ 1 - \exp \left( -\frac{t}{\tau_j} \right) \right] \). A good fit is achieved with two species of charge traps (where \( V_1/V_2 = 12/15 \text{ V} \) and \( \tau_1/\tau_2 = 0.2/2.2 \text{ hours} \)) as shown in Fig. 3.23.

Charging also leads to a change in the down-state capacitance over time. Fig. 3.24 shows the measured change in \( C_d \) for each of the four voltage combinations studied previously. It is seen that the application of a bipolar \( V_s \) (\( V_h = 0 \)), and also a bipolar \( V_s \) and \( V_h \) results in a stable down-state capacitance over time. As expected, bulk charging due to a unipolar \( V_s \) acts to increase the down-state capacitance, while top charging due to a unipolar \( V_h \) acts to decrease the down-state capacitance.

Several high-cycle tests were performed with different bias waveforms. The first test was performed in ambient atmosphere using the standard setup (Fig. 3.13). A 4.5 \( \mu m \) device was hot-switched with 29 dBm of incident RF power at 10 GHz with a
**Figure 3.24:** Evolution of measured down-state capacitance when the device is pulled-down with (a) bi-polar $V_s$ and uni-polar $V_s$, and (b) bi-polar $V_s$ and $V_h = 10$ V uni-polar and $V_h = 10$ V bi-polar.
Figure 3.25: Power detector output recorded at beginning and end of reliability test.

4 kHz 50% duty cycle unipolar bias waveform of amplitude 1.1 times $V_{pa}$ (the beam and RF electrode were DC grounded). It is known that incident RF power can accelerate charging by raising the temperature of the MEMS device [68]. The bias waveform and power detector output were monitored on an oscilloscope and are shown in Fig. 3.25 at the start of the test and after 17 days of continuous switching (a total of 6 billion cycles). $C-V_s$ curves, measured before and after the high-cycle test, showed a 15% increase in the up-state capacitance which is attributed to substrate charging, and a 10% decrease in the down-state capacitance which is attributed to the accumulation of contaminants in the area where the beam touches the dielectric.

A second high-cycle test was again performed in ambient atmosphere with another 4.5 $\mu$m device. The device was hot-switched with 29 dBm of incident RF power at 12 GHz. The main difference was that the bias waveform used was bi-polar (8 kHz switching frequency, 50% duty cycle, and amplitude equal to 1.2 times $V_{pi}$). The device switched for 15.5 days (10.5 billion cycles) before a similar drift of the power detector voltage was observed as in the previous test.
3.5 Dielectric-less Design

The top view and cross section of the capacitive switch are presented in Fig. 3.26. The structure is cantilever-based with an air gap in both the up- and down-state positions. When a voltage is applied between the cantilever and the bottom electrode, the cantilever moves down until the dimples make contact with the landing pads which are electrically isolated from the electrode.

Electro-mechanical simulations of the structure above were performed using Coventorware. The results show an up-state capacitance of 85 fF, a down-state capacitance of 155 fF (capacitance ratio of 1.82), and a pull-in voltage of 37 V.

The switches are fabricated on a 500 \( \mu \text{m} \)-thick glass substrate, and are implemented in a CPW line. First, the bottom metal layer consisting of Ti/Au (200 Å/5000 Å) is evaporated and patterned to form the bottom electrodes. Next, a 1.5 \( \mu \text{m} \) thick SiO\(_2\) layer is deposited with PECVD as the sacrificial layer and patterned with RIE. The SiO\(_2\) is then etched again with RIE to a depth of 0.4 \( \mu \text{m} \) at the dimple locations. Next, a second metal layer consisting of Ti/Au/Ti (200 Å/1000 Å/150 Å) is sputtered and selectively electroplated (5 \( \mu \text{m} \)) to form the cantilevers. Finally, the second metal is etched,
the cantilevers are released in BHF, and the sample is dried in a CO$_2$ critical point dryer.

Two of the switch configurations that were fabricated are shown in Fig. 3.27. The first device is a 1-port switched-capacitor, and the second device is a 2-port switched-capacitor in a series configuration. As the pictures show, each switch is attached to a short section of CPW line (about 160 $\mu$m) at the input port and at the output port (if it is a 2-port configuration).

### 3.5.1 Measurements

A 1-port capacitive switch implemented in a CPW line, such as the one shown in Figure 3.27(a), was measured from 0.5 to 40 GHz in the up- and down-state positions. The actuation voltage was 35 V. The dimensions of this particular switch are exactly those shown in Figure 3.26. The up- and down-state capacitance were extracted by fitting the simulated $S_{11}$ of the equivalent model shown in Figure 3.28(a), to the measured $S_{11}$. Note that most of the inductance in the model physically comes from the two relatively thin arms connecting the anchors to the moving cantilever. Figure 3.28(b) shows the measured and simulated $S_{11}$ of the switch in both states. The extracted capacitance ratio is 1.90.

The formula for the quality factor of a series capacitor is:

$$Q = \frac{\text{Imag}(Z_{in})}{\text{Real}(Z_{in})}$$  \hspace{1cm} (3.8)

where $Z_{in}$ is the impedance of the switch and can be calculated from the measured $S_{11}$. However, the $S_{11}$ measurement includes a bit of CPW transmission line (as seen in the equivalent model in Figure 3.28(a)). For the final quality factor calculation, the purely reactive component of the line has been subtracted from $\text{Imag}(Z_{in})$. Whereas $\text{Real}(Z_{in})$ includes both the loss of the switch and the loss of the line (since it is very hard to separate the two), thus giving a fairly conservative estimate of the quality factor. The resulting quality factor and reactance of the switch are shown in Table 3.3 for three different frequency points.

The measured Q is very high due to the thick gold cantilever and the wide bottom electrode. As is well known, the thickness of standard fixed-fixed varactors is about 0.5-1.5 $\mu$m (and not 5 $\mu$m as in this case) which has limited their Q to about 100-200 at
Figure 3.27: Picture of a switched capacitor in series with the CPW implemented as (a) 1-port and (b) 2-port.
Figure 3.28: (a) Circuit model of a 1-port dielectric-less capacitor and (b) measured and simulated $S_{11}$ of a 1-port switched capacitor in the up- and down-state.

Figure 3.29: Measured capacitance vs. voltage curve of a 1-port switched capacitor.
Table 3.3: De-embedded reactance and quality factor vs. frequency for a 1-port switched-capacitor with \( C_u = 91 \) fF and \( C_d = 173 \) fF.

<table>
<thead>
<tr>
<th>Frequency (GHz)</th>
<th>Up-state X (Ω)</th>
<th>Up-state Q</th>
<th>Down-state X (Ω)</th>
<th>Down-state Q</th>
</tr>
</thead>
<tbody>
<tr>
<td>10</td>
<td>-169j</td>
<td>450</td>
<td>-86j</td>
<td>350</td>
</tr>
<tr>
<td>15</td>
<td>-108j</td>
<td>400</td>
<td>-52j</td>
<td>225</td>
</tr>
<tr>
<td>20</td>
<td>-76j</td>
<td>225</td>
<td>-34j</td>
<td>90</td>
</tr>
</tbody>
</table>

10-30 GHz. It must be stated that the Q is determined from \( S_{11} \) measurements and this does not yield an accurate result for \( Q > 100 \). Still, the results are consistent in that the extracted Q falls with frequency as \( 1/f \) and also falls with capacitance as \( 1/C \) (as expected).

Figure 3.29 shows the extracted capacitance versus voltage curve for the 1-port capacitive switch. The measured pull-down voltage is 31 V and is 6 V lower than the simulated pull-down voltage. The extracted spring constant of the cantilever beam is 115 N/m.

The effective mass of the cantilever is 1.2 \( \mu g \). Knowing \( k \) and \( m \), the mechanical resonant frequency \( f_0 \) of the cantilever is determined by \( 2\pi f_0 = \sqrt{k/m} \) and is 50 KHz. Assuming a cantilever with a relatively small damping coefficient (\( Q_m > 1 \)), the calculated switching time is given by [35]:

\[
t_s \simeq 3.67 \frac{V_p}{V_s 2\pi f_0}
\]

where \( V_p \) is the pull-down voltage and \( V_s \) is the actuation voltage. For a pull-down voltage of 31 V and an actuation voltage of 35 V the switching time is 10 \( \mu s \).

A 2-port capacitive switch, such as the one shown in Figure 3.27(b), was measured from 2 to 18 GHz, with an actuation voltage of 50 V. The switch dimensions are as shown in Figure 3.26 except the length of the cantilever was decreased from 80 \( \mu m \) to 70 \( \mu m \) and the width of the cutout for the landing pad was increased from 25 \( \mu m \) to 30 \( \mu m \). The network analyzer internal bias-T did not allow a voltage higher than 40 V, and prevented us from measuring this device up to 40 GHz in the down-state position.
Figure 3.30: (a) Circuit model for a 2-port switched capacitor and (b) measured and simulated S-parameters of a 2-port switched capacitor in the up- and down-state.

The simulated S-parameters of the equivalent circuit model shown in Figure 3.30(a) are plotted versus the measured S-parameters in the up-state and in the down-state in Figure 3.30(b). The extracted capacitance ratio is 1.51.

Table 3.4 lists the extracted capacitances for the two different kinds of fabricated switches, as well as their operating down-state voltage (this voltage was always chosen to be higher than the switch’s pull-down voltage). The measured up- and down-state capacitance of the 1-port switch agree fairly well with the simulated values from section II. Also, the up-state capacitance is directly proportional to the cantilever-to-electrode overlap area, as expected.

However, the results show that the capacitance ratio of the 2-port switch is significantly lower than that of the 1-port switch. This may be due to differences in dimple heights due to fabrication errors, and some upward curling of the cantilever beams due
Table 3.4: Summary of extracted up- and down-state capacitance for two fabricated switched-capacitors.

<table>
<thead>
<tr>
<th>Switch type</th>
<th>Overlap area (µm²)</th>
<th>C_{up} (fF)</th>
<th>C_{down} (fF)</th>
<th>Ratio</th>
<th>Operating Voltage</th>
</tr>
</thead>
<tbody>
<tr>
<td>1-port</td>
<td>12,200</td>
<td>91</td>
<td>173</td>
<td>1.90</td>
<td>35</td>
</tr>
<tr>
<td>2-port</td>
<td>10,450</td>
<td>78</td>
<td>118</td>
<td>1.51</td>
<td>50</td>
</tr>
</tbody>
</table>

Figure 3.31: Switching speed and reliability measurement test setup.

to a stress gradient in the 5 µm thick gold beams.

The test setup for measuring the switching speed of a 2-port device is shown in Figure 3.31. A square unipolar voltage waveform is used to actuate the device. The reflected power is blocked by the 20 dB isolator and does not affect the measurement. The output RF power is measured with a diode detector.

The switching speed of a 2-port capacitive switch, such as the one shown in Figure 3.27(b), was measured with this test setup. The switch was actuated at a rate of 10 KHz using a 0-35 V unipolar voltage and injected with 1 W of RF power at 8 GHz. Both the actuation voltage and the output voltage of the diode detector are plotted in Figure 3.32 during the up-to-down and down-to-up switch transitions. The plots show that the switching speed of this device is 8 µs which agrees with the calculated value
from the previous section.

The 2-port switch went through reliability testing in the test setup depicted in Figure 3.31. The device was hot switched with 10 KHz, 0-50 V square waveform and with 1 W of RF power at 8 GHz ($X_{up}=-250j$ at this frequency). The actuating square waveform and the detected output power were monitored on an oscilloscope. The device switched for over 11 billion cycles (> 12 days of continuous switching) with no failure. The reliability testing was ceased because the test setup could not be reserved for a longer period of time.

Figure 3.33 shows the extracted capacitance versus voltage curve for the 2-port capacitive switch before and after reliability testing. The capacitance ratio has remained 1.51. Measurements indicate that the S-parameters have also remained nearly the same.

### 3.6 Conclusion

This chapter has demonstrated a cantilever based RF MEMS switched capacitor with digital and analog tuning capabilities which is ideal for 1-10 GHz applications. The design features two independent electrodes under the beam, allowing for precise control of the capacitance, resulting in an up-state, and down-state capacitance of 50 fF/250 fF. A beam with a positive stress gradient (upward curl) has been found to be more flush with the dielectric in the down-state position resulting in a tunable capacitance ratio of 5-9. Measurements also showed that a beam thickness of 4-4.5 $\mu m$ is optimal and results in a pull-in voltage of 50-65 V, a switching time of less than 50 $\mu s$, and a $Q$ greater than 200 at 5 GHz. The power handling was limited by an induced $V_{bh}$(rms) which caused the switch to not release in hot-switched conditions with greater than 1.1 W of incident RF power at 10 GHz ($t_b = 4.5 \mu m$). Also, an investigation of the various charging mechanisms revealed that a bipolar voltage at the actuation electrode minimizes bulk substrate charging and a bipolar voltage at the RF electrode ($\leq 10$ V) minimizes top charging in the dielectric layer. Separating the electrodes also allows the device to be operated with a relatively low electric field across the dielectric. This results in high reliability performance with greater than 10 B cycles demonstrated under hot switched and high power conditions.
Figure 3.32: Actuation voltage and detected power level vs. time for up-to-down (a) and down-to-up (b) capacitive switch transitions.
Figure 3.33: Measured capacitance vs. voltage curve of a 2-port switched capacitor before and after reliability testing.

A dielectric-less RF MEMS switched capacitor has also been demonstrated. A capacitance ratio of 1.9 has been achieved for a switch implemented in a 1-port configuration. The switch shows a pull-down voltage of 31 V, and a switching speed of 8 \( \mu \)s. The thick gold cantilever and wide bottom electrode structure results in a \( Q > 225 \) at X to Ku-band frequencies. The device was hot switched with 1 W of RF power at 8 GHz for \( > 11 \) billion cycles with no failure and with little change in the C-V curve.

Chapter 3, in part, is mostly a reprint of the material as it appears in IEEE Transactions Microwave Theory and Techniques, October 2010. Alex Grichener and Gabriel M. Rebeiz. The dissertation author was the primary investigator and author of this material. This chapter also includes material published in IEEE MTT-S Int. Microwave Symposium, 2008. Alex Grichener, Balaji Lakshminarayanan, and Gabriel M. Rebeiz. The dissertation author was the primary investigator and author of this material. This chapter also includes material published in IEEE MTT-S Int. Microwave Symposium, 2006. Alex Grichener, Denis Mercier, and Gabriel M. Rebeiz. The dissertation author was the primary investigator and author of this material.
Chapter 4

A 60-90 MHz 7-Channel Cochlea-Based Channelizer

4.1 Introduction

Cochlear channelizers are passive wideband contiguous channel multiplexers whose operation are based on the mammalian cochlea. The cochlea is an electro mechanical transducer located in the inner ear that converts acoustical energy (sound waves) into nerve impulses sent to the brain, resulting in hearing [69–71]. The cochlear channelizer circuit topology is derived from an electrical-mechanical analogy of the basilar membrane. The result is a discretized, non-uniform transmission line arranged with the highest frequency ($f_N$) channel near the input and the lowest frequency ($f_1$) channel at the end of the channelizer manifold (Fig. 4.1). The channels are coupled using a manifold composed of inductors. Previously, single-order cochlear channelizers were first demonstrated for both constant fractional bandwidth and constant absolute bandwidth channels at 20-90 MHz [47].

The impedance behavior of each channel filter over the entire bandwidth is an important parameter. In particular, the input impedance of the channel filter should behave as a series resonator and appear resistive in its passband, capacitive at frequencies below its passband, and inductive above its passband. At far above and below its center frequency, a channel should appear as an open circuit. A channelizer composed of
such filters will have an equivalent circuit shown in Fig. 4.2 at the center frequency $f_0$ of one of the middle channels $Z_0$. The channels with a center frequency higher than $f_0$ will appear capacitive, and together with the inductive manifold will form an up-converting ladder matching network, transforming the channel impedance, $Z_{ch}$, to the required input impedance of the channelizer, $Z_{in}$. The up-converting network therefore requires that the input impedance $Z_{ch}$ of the resonant filter be smaller than the terminal impedance $Z_{in}$ which is usually 50 $\Omega$.

There are not many realizable RF filters that behave as near-ideal series resonant circuits at their input ports, over a wide bandwidth. Two filter topologies that can satisfy this requirement are the tubular and top-C coupled topologies, shown in Fig 4.3. The main difference between the two circuits is the inductor position. In the tubular topology, the inductor is placed in series and in the top-C coupled topology, the inductor is placed in shunt. Galbraith et al. [48] demonstrated a 3-pole channelizer based on the tubular topology. The channelizer covered 0.18-1.13 GHz with 10 constant fractional bandwidth channels and resulted in 1.1 dB of insertion loss and 20 dB adjacent-channel isolation.
Ou et al. [72] demonstrated a 20-90 MHz 26-channel 6-pole channelizer, also based on the tubular topology, with part constant absolute bandwidth channels of 1.40 MHz and part constant fractional bandwidth channels of 4.5%. The channelizer resulted in 4-7 dB of insertion loss and > 40 dB adjacent-channel isolation.

In the previous work, the tubular topology was chosen because it results in lower levels of magnetic coupling between physically adjacent channels. This allows for a more compact printed circuit board layout. However, if the coupling between inductors is minimized then the top-C coupled topology can offer an attractive alternative over the tubular topology. One advantage of the top-C coupled topology is that it offers more flexibility in choosing the channel filter’s input impedance, $Z_{ch}$, which should be in the range of 5 to 20 Ω to result in reasonable component values and good input return loss over the channelizer bandwidth [47]. Depending on the channelizer requirements, the ideal channel impedance may change within this range. A tubular implementation of the 60-90 MHz channelizer is only realizable if the input impedance of each channel is limited to < 10 Ω. A higher channel impedance would require higher reactance values of the inductors ($X_L > 150$) at the channel’s center frequency. This is hard to achieve with lumped inductors which suffer from parasitic capacitance effects. The top-C coupled topology results in reasonable inductor values for the entire 5-20 Ω range of $Z_{ch}$. In other words, a smaller inductor value is required in the top-C coupled topology as compared to the tubular topology for a given value of $Z_{ch}$. This extra degree of freedom
allows a wider range of requirements to be satisfied with a wider range of physically realizable channelizer circuits. For example, it is easier to achieve a good wide-band input impedance match in a channelizer that is based on the top-C coupled topology.

In this chapter we present a 60-90 MHz 7-channel 6-pole channelizer based on the top-C coupled topology with 5 MHz wide constant absolute bandwidth channels that resulted in 4 dB of insertion loss and > 40 dB adjacent-channel isolation. The cross-coupling between the inductors was minimized by an optimized layout which oriented neighboring inductors orthogonal to one another.

4.2 Design

The channelizer design procedure consists of choosing the desired frequency range, the filter order and bandwidth for each channel, and the crossover point for adjacent channels. The crossover point is chosen to be 3 dB below each channel’s maximum response. This empirical values provides the required amount of inter-channel coupling for the cochlea-like response and achieves a wideband input match by absorbing nearly all of the power in the total channelizer bandwidth. It is important to note that, in the finite resonator Q case, the crossover point will drop due to the introduction of filter insertion loss and the rounded-off filter edges. An example of this effect is illustrated with three simulated contiguous 6-pole filter responses shown in Fig. 4.4. As soon as loss is introduced to the filter resonators (and the unloaded resonator Q goes to 150), the crossover points decrease from -3 dB to -6 dB.

In order to cover the 60-90 MHz bandwidth with 7 channels, where the center frequency of the first channel is at 60 MHz and the center frequency of the seventh channel is at 90 MHz, the channel filters are designed to result in a 3 dB absolute bandwidth (ABW$_{3dB}$) of 5 MHz and to crossover at the -3 dB point (in the lossless case) as illustrated with channels 5, 6, and 7 in Fig. 4.4. Each channel filter is designed based on a Chebyshev (equal-ripple) response. A smaller ripple results in a filter response that is less sensitive to variations in component values because the six poles are bunched up closer together on the Smith chart. For this reason the ripple level is chosen to be < 0.01. As shown in Fig. 4.4, the channel-to-channel isolation is defined as the
Figure 4.4: Ideal response of three contiguous 6-pole filters for the case of $Q = \infty$ and $Q = 150$. The ideal -3 dB crossover point drops to -6 dB for the case of $Q = 150$.

difference between the transmission response of any two adjacent channels. To satisfy requirements it was necessary to design the filters to give a stopband attenuation at the center frequency of both adjacent channels of $> 40 \text{ dB}$. For the required passband ripple $R \text{ dB}$, the minimum stopband attenuation $S \text{ dB}$ at $\Omega = \Omega_S$, the degree of a Chebyshev lowpass prototype, can be found by [73]

$$n \geq \cosh^{-1} \sqrt{\frac{10^{0.58} - 1}{10^{0.58} + 1}} \Omega_S.$$  \hspace{1cm} (4.1)

For a ripple level of 0.01 dB and an attenuation level of 40 dB 5 MHz off the center frequency of a channel filter, the calculated $n$ is 5.5. This means that in order to satisfy the channel-to-channel isolation requirement, at a minimum a 6\textsuperscript{th} order channel filter is required. For a filter with a finite $Q$, the loss, $\Delta L$, increases with the number of poles as follows:

$$\Delta L = \frac{4.343}{Q} \sum_{i=1}^{n} g_i (\text{dB})$$ \hspace{1cm} (4.2)

where $g_i$ are the element values of the low-pass prototype and $Q$ is the quality factor of the unloaded resonator.

Once the filter order has been determined, Equation 4.1 can be rearranged (with
\( n = 6 \) to calculate \( \Omega_3 = 1.2 \) which can in turn be used to calculate the absolute ripple bandwidth of each filter with

\[
ABW_{RdB} = \frac{ABW_{3dB}}{\Omega_3},
\]

which evaluates to 4.2 MHz.

To synthesize each channel filter, one starts with the prototype bandpass filter shown in Fig. 4.5(a), whose circuit elements are given by

\[
L_{si} = \frac{Z_{ch}g_i}{\Delta \omega_0} \quad (i \text{ is odd}) \tag{4.4}
\]

\[
C_{si} = \frac{\Delta}{\omega_0 Z_{ch} g_i} \quad (i \text{ is odd}) \tag{4.5}
\]

and,

\[
L_{pi} = \frac{\Delta Z_{ch}}{\omega_0 g_i} \quad (i \text{ is even}) \tag{4.6}
\]

\[
C_{pi} = \frac{g_i}{\Delta \omega_0 Z_{ch}} \quad (i \text{ is even}) \tag{4.7}
\]

and \( R_7 = Z_{ch} \times g_7 \), where \( \Delta = (\omega_2 - \omega_1)/\omega_0 \) is the fractional bandwidth of the filter with \( \omega_0 = \sqrt{\omega_1 \omega_2} \). The passband corner frequencies, \( \omega_2 \) and \( \omega_1 \), are given by the absolute ripple bandwidth (where \( \omega_2 - \omega_1 = ABW_{RdB} \)). It was found that an input impedance of \( Z_{ch} = 15 \Omega \) (kept the same for all seven channel filters) results in reasonable component values and good input return loss over the channelizer bandwidth.

Next, the circuit in Fig. 4.5(a) is transformed to one consisting of only shunt resonators, each having an identical capacitance \( C \) and inductance \( L \) (Fig. 4.5(b)) which may be chosen arbitrarily. This transformation is enabled by immittance inverters implemented by Pi and L-networks of capacitors. The immittance inverter parameters are given by

\[
J_{0,1} = \sqrt{\frac{C}{L_{s1}}} \tag{4.8}
\]
Figure 4.5: Channel filter schematics showing network transformations used to arrive at the final top-C coupled topology.
\[ J_{6,7} = \sqrt{\frac{C}{C_{p6}R_7Z_0}} \]  
(4.9)

\[ J_{i,i+1} = \sqrt{\frac{C^2}{L_{si}C_{p(i+1)}}} \quad (i \text{ is odd}) \]  
(4.10)

\[ J_{i,i+1} = \sqrt{\frac{C^2}{C_{pi}L_{s(i+1)}}} \quad (i \text{ is even}) \]  
(4.11)

where \( Z_0 = 50 \ \Omega \) is the output impedance of each filter. A 169 nH inductor is chosen at every shunt resonator of the transformed circuit (Fig. 4.5(b)) and at every channel. This inductance value, \( L \), yields a high-Q and \( X_L < 100 \) over the channelizer bandwidth which makes it less sensitive to parasitic capacitance effects. From this, the shunt resonator capacitance, \( C \), used in Equations 4.8-4.11 is given by \( C = 1/(\omega_0^2 L) \).

The immittance inverters at the input and output of the channel filters are implemented with \( L \)-networks of capacitors with values given by

\[ C_{msi} = \frac{J_{i,i+1}}{\omega_0 \sqrt{1 - (J_{i,i+1}Z_{ch})^2}} \quad (i = 0, 6), \]  
(4.12)

\[ C_{mpi} = \frac{J_{i,i+1}}{\omega_0^2 C_{msi}} \quad (i = 0, 6). \]  
(4.13)

Whereas the other immittance inverters (located between two shunt resonators) are implemented with \( \Pi \)-networks of capacitors with values given by

\[ C_{mi} = \frac{J_{i,i+1}}{\omega_0} \quad (i = 1, 2, 3, 4, 5). \]  
(4.14)

In the final transformation shown in the circuit in Fig. 4.5(c), all the negative capacitances are absorbed by the shunt resonator capacitors. The resulting capacitance of the first shunt capacitor is given by \( C_0 = C - C_{mp0} - C_{m0} \), and of the next four shunt capacitors is given by \( C_i = C - C_{mi} - C_{m(i+1)} \) (where \( i=1,2,3,4 \), and of the last shunt capacitor is given by \( C_5 = C - C_{mp6} - C_{m5} \). The required capacitance values vary from 0.5 to 30 pF across the entire channelizer. This completes the transformation to the top-C coupled topology.
Once all seven individual channel filters have been designed, they can be integrated into the channelizer circuit shown in Fig. 4.6. The manifold inductors can be calculated with

$$L_m(n) = L_0 e^{a(1-\frac{n}{N})}, \quad 1 \leq n \leq N$$

where $n$ is the channel number and $N$ is the total number of channels (in this design $N=7$). A good starting point for $L_m(n)$ is given in [47] and yields a reactance of 5-8 Ω at the center frequency of the lowest frequency channel. To satisfy this condition, $L_0=22$ nH and $a=0.1$, which results in a very gradual inductance change through the manifold. Thus each manifold inductor can be approximated with a single 22 nH inductor.

The first and last channel by definition are missing one adjacent channel, and therefore need extra components to provide the impedance match to the input of the channelizer. Channel 7 uses a matching capacitor $C_m=22$ pF and the input manifold inductor $L_m(7)$ for the step-up matching network, and channel 1 uses a dummy channel (channel $e$) to resonate out the capacitive input impedance of channel 1 at its center frequency.

### 4.2.1 Layout and Tuning

The circuit is implemented in microstrip using a 0.787 mm thick RT/duroid 5880 [52] substrate ($\epsilon_r = 2.2$), two 53.3-µm-thick copper layers, and 0.38 mm diameter plated...
thru-hole vias. Since the lumped capacitors are only available in discrete values, the shunt capacitance in the channel filters is realized with a combination of lumped-element capacitors and parallel-plate capacitors composed of the microstrip top metal layer and the ground plane layer. An $\epsilon_r = 2.2$ substrate was chosen since it results in a very stable dielectric constant and accurate parallel-plate capacitance, at the expense of a physically large board size (13.1 inches $\times$ 14.7 inches). The channel filters use surface-mount technology (SMT) devices, including Coilcraft Spring air core inductors and Dielectric Laboratories multilayer capacitors, all with $\pm 2\%$ or better tolerance. The channel filter inductors (Maxi Spring [74]) were chosen for their high-Q (135-200) and the manifold inductors (Mini Spring [75]) were chosen for their small size. The SMT capacitors have a Q of greater than 500 at 60-90 MHz.

A picture of the 7-channel cochlea-like channelizer is shown in Fig. 4.7. An extra channel "e" is used as a dummy channel to provide an appropriate impedance load to channel 1 at its center frequency. The output of each channel is routed to an edge-launch SMA connector using a 50 $\Omega$ transmission line. Previously designed test circuits identified magnetic coupling between inductors as the main source of cross-talk within the same channel filter and between two different channel filters. To minimize this cross-talk, adjacent channel filters are placed on the opposite sides of the manifold and any two adjacent inductors (in the same channel or in different channels) are positioned perpendicular to one another. For an added measure to reduce cross-talk between channels, metal strips with plated-thru via holes to ground are placed between physically adjacent channels to allow metal dividers (one or two inches tall) to be placed on top. However, the metal dividers were not used as the perpendicular arrangement of the inductors provided the necessary reduction in electromagnetic coupling.

A close-up picture of an individual channel filter with its corresponding circuit model is shown in Fig. 4.8. The shunt capacitances, $C_0$ through $C_5$, are implemented using a combination of parallel-plate capacitors and lumped SMT capacitors (pointed out with black arrows in Fig. 4.8(a)) which are grounded using via-holes. This is done in order to have more precise control over the shunt capacitance as the lumped capacitors are only available in discreet values. Circuit models from Modelithics CLR Library [76] are used in the simulation for all components. Each channel layout, including
component pads, printed parallel-plate capacitors, transmission-lines and surface-mount
ports, are first simulated in Sonnet. The resulting S-parameters are exported into ADS
and simulated together with the Modelithics lumped-element models. The SMT models
for the inductors and capacitors include the component pads and parasitic capacitance
to ground which gets absorbed into the filter design.

The simulation methods described above are used to design the individual channel
filters independently of one another. Once this is done, the channels are combined
into the overall channelizer (Fig. 4.6) and simulated in ADS. Inside the channelizer,
the channel filter responses would have changed to due to the additional loading of the
adjacent channel filters and the inductive manifold. To achieve the desired channelizer
response several rounds of tuning and optimization were needed. This is done by chang-
ing the values of the series and shunt capacitors (while keeping the inductor values the
same) inside the channel filters. The manifold inductors offer another degree of free-
dom for tuning the circuit. The manifold inductors ended up being tuned to 35.5 nH
from their initial value of 22 nH. The goal of the tuning process was to achieve the de-
sired center frequency, bandwidth, and adjacent-channel rejection, while maintaining a
reflection loss of better than 15 dB over the channelizer bandwidth.

4.3 Measurements

The channelizer’s S-parameters are measured using an Agilent E5071B vector
network analyzer. A two-port short-open-load-thru coaxial line calibration sets the ref-
erence planes at the coaxial connectors. Each channel’s transmission response is mea-
sured by connecting the VNA to the channelizer input (port 0) and to the \( n^{th} \) channel
output (port n) with all other channels terminated with a 50 \( \Omega \) load \((S_{n,0})\). The channel-
izer’s input reflection coefficient \((S_{0,0})\) is obtained in the same way (each channel output
terminated with 50 \( \Omega \)).

The measured and simulated s-parameters for all seven channels are shown in
Fig. 4.9. A summary of the measured results is presented in Table 4.1. The channels
have an average 3 dB bandwidth of 4.3 MHz. The crossover point between adjacent
channels is around 5 dB and the average 5 dB bandwidth (or crossover bandwidth)
Figure 4.7: Picture of fabricated 7-channel channelizer with adjacent inductors positioned perpendicular to one another to minimize crosstalk.

Figure 4.8: (a) Close-up picture of a channel filter and (b) its corresponding circuit model.
Table 4.1: Measured channelizer specifications.

<table>
<thead>
<tr>
<th>Ch</th>
<th>$f_n$ (MHz)</th>
<th>$\Delta_{3dB}$ (MHz)</th>
<th>$\Delta_{5dB}$ (MHz)</th>
<th>I.L. (dB)</th>
<th>$R_{n+1}$ (dB)</th>
<th>$R_{n-1}$ (dB)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>60.5</td>
<td>4.2</td>
<td>–</td>
<td>3.7</td>
<td>39</td>
<td>–</td>
</tr>
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<td>3.9</td>
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is 4.9 MHz. The measured insertion loss is around 3.9 dB and the adjacent channel rejection is greater than 35 dB across all channels (for both the upper and lower stop bands). The measured reflection loss is greater than 15 dB over the entire channelizer bandwidth. To achieve this, some amount of post-fabrication tuning was required. The tuning was mainly done by adding small pieces of copper tape to the printed parallel plate capacitors.

A single channel’s (ch. 4) measured transmission response and group delay are shown in Fig. 4.10, along with the simulated response for a stand-alone 6-pole filter with the topology shown in Fig. 4.8(b). Compared with the stand-alone filter, the channelizer response has slightly higher rejection and an altered phase response. This results in an additional 30 ns of group delay at the center of channel 4. The additional delay is mostly due to the manifold and is proportional to the channel’s distance from the input port.

A careful inspection of the measured transmission response in Fig. 4.9(a) shows for channels 1, 3, and 5 a slight "hump" at the center frequency of channels 3, 5, and 7, respectively. Since the odd numbered channels are physically adjacent, the "humps" in the transmission coefficient are the result of electromagnetic coupling between physically adjacent channels. This coupling was further characterized by measuring the
Figure 4.9: Measured and simulated (a) transmission coefficient ($S_{n,0}$) and (b) reflection coefficient ($S_{0,0}$) of each channel.
**Figure 4.10**: Simulated and measured transmission response (top) and group delay (bottom) of channel 4 of the seven-channel channelizer and the corresponding simulated response of channel 4 as a stand-alone six-pole filter

transmission response between different pairs of channels (Fig. 4.11). The measured transmission coefficient between channels 1 and 2 closely follows the stopband skirts of both channels and is the result inter-channel coupling through the manifold (which was also simulated). However, there is negligible coupling through the manifold between channels 1 and 3 and yet this coupling is measured at the -50 dB level and is due to magnetic coupling between physically adjacent channels. The slight coupling between channels 1 and 4 is the result of energy coupling from channel 1 to channel 2 through the manifold and then magnetically coupling into channel 4.

### 4.4 Conclusion

This chapter presents a 7-channel channelizer from 60 to 90 MHz based on the mammalian cochlea. Each channel filter contains 6 poles and is based on the top-C coupled topology. The channelizer results in 4 dB insertion loss in each channel, and greater than 35 dB isolation between adjacent channels. The design is scalable and can be extended to cover 20-200 MHz for wideband EW applications.

Chapter 4, in part, has been accepted for publication of the material as it may appear in IEEE Biomedical Circuits and Systems, 2011. Alex Grichener, Yu-Chin Ou,
Figure 4.11: Measured and simulated $S_{1,0}$ and isolation between channel 1 and adjacent channels ($S_{1,m}$).

and Gabriel M. Rebeiz. The dissertation author was the primary investigator and author of this material.
Chapter 5
Conclusion

The thesis presents a quasi-optical network analyzer, high reliability RF MEMS switched capacitors, and a 7-channel channelizer from 60-90 MHz.

Chapter 2 presents a microwave quasi-optical network analyzer which has been successfully demonstrated using hardware and high-order harmonic mixing schemes that are extendable to millimeter-wave frequencies. The network analyzer is based on a planar antenna with an integrated Schottky-diode mixer placed on an extended hemispherical silicon lens. The hardware is monolithic and results in a compact and low-cost solution particularly if scaled to millimeter-wave frequencies. In order to check its performance, the network analyzer was used to measure a frequency selective surface, and the measured result is in excellent agreement with simulation.

Chapter 3 presents a cantilever based RF MEMS switched capacitor with digital and analog tuning capabilities which is ideal for 1-10 GHz applications. The design features two independent electrodes under the beam, allowing for precise control of the capacitance, resulting in an up-state, and down-state capacitance of 50 fF/250 fF. A beam with a positive stress gradient (upward curl) has been found to be more flush with the dielectric in the down-state position resulting in a tunable capacitance ratio of 5-9. Measurements also showed that a beam thickness of 4-4.5 µm is optimal and results in a pull-in voltage of 50-65 V, a switching time of less than 50 µs, and a $Q$ greater than 200 at 5 GHz. The power handling was limited by an induced $V_{h}(\text{rms})$ which caused the switch to not release in hot-switched conditions with greater than 1.1 W of incident...
RF power at 10 GHz ($t_b = 4.5 \mu m$). Also, an investigation of the various charging mechanisms revealed that a bipolar voltage at the actuation electrode minimizes bulk substrate charging and a bipolar voltage at the RF electrode ($\leq 10$ V) minimizes top charging in the dielectric layer. Separating the electrodes also allows the device to be operated with a relatively low electric field across the dielectric. This results in high reliability performance with greater than 10 B cycles demonstrated under hot switched and high power conditions.

Chapter 4 presents a 7 channel channelizer from 60-90 MHz based on the mammalian cochlea. Each channel is a 6th-order lumped-element filter implemented in the top-C coupled topology. The measurements show a constant absolute 3 dB bandwidth of around 4.3 MHz for each channel, and a greater than 35 dB adjacent channel rejection. The measured insertion loss, on the average, is less than 4 dB and the measured reflection loss is greater than 15 dB over the entire channelizer bandwidth. The agreement between simulation and measurements is excellent. The channelizer has both commercial and military applications in high-performance wideband communication systems.
Bibliography


