Lawrence Berkeley National Laboratory
Recent Work

Title
HISTOGRAMMING MEMORY PERIPHERAL DEVICE FOR COMPUTER SYSTEMS

Permalink
https://escholarship.org/uc/item/7ck4m0f9

Author
Meng, John.

Publication Date
1980-05-01
HISTOGRAMMING MEMORY PERIPHERAL DEVICE FOR COMPUTER SYSTEMS

John Meng

May 1980

Prepared for the U.S. Department of Energy under Contract W-7405-ENG-48
DISCLAIMER

This document was prepared as an account of work sponsored by the United States Government. While this document is believed to contain correct information, neither the United States Government nor any agency thereof, nor the Regents of the University of California, nor any of their employees, makes any warranty, express or implied, or assumes any legal responsibility for the accuracy, completeness, or usefulness of any information, apparatus, product, or process disclosed, or represents that its use would not infringe privately owned rights. Reference herein to any specific commercial product, process, or service by its trade name, trademark, manufacturer, or otherwise, does not necessarily constitute or imply its endorsement, recommendation, or favoring by the United States Government or any agency thereof, or the Regents of the University of California. The views and opinions of authors expressed herein do not necessarily state or reflect those of the United States Government or any agency thereof or the Regents of the University of California.
HISTOGRAMMING MEMORY PERIPHERAL DEVICE
FOR COMPUTER SYSTEMS

John Meng*
Lawrence Berkeley Laboratory
University of California
Berkeley, CA 94720

INTRODUCTION

Fast histogramming memory has been implemented as a peripheral device for a Nuclear Science ModComp IV data analysis system. The memory consists of four blocks, each containing 8192 24-bit words. The computer interface is a standard high-speed serial connection, making it specific to no single computer system, but instead making it easily usable on any system containing this high-speed serial capability. Connection to the host computer is accomplished via five 125 coaxial cables attached to BNC connectors on the rear panel of the unit. The cables must be approximately equal in length, although differential lengths of as much as 7 meters may be tolerable.

The unit contains three subsystems as shown in block drawing B1. (ADC's are not included as an integral part of the unit.) The serial interface unit effects communications between the host computer and the storage control subsystem. The storage control subsystem communicates directly with the four independent memory subsystems, passing along detailed control signals and compacting memory data for shipment back to the serial subsystems.

The memory subsystems are four independent units, each implementing the add-one facility and buffering data and control signals to and from the four semiconductor "stacks."

* This work was supported by the Physical Research Division of the Department of Energy under Contract No. W-7405-ENG-48.
SERIAL INTERFACE

This subsystem (B4) is an implementation of an earlier serial link using more modern integrated circuits. Specifically, the 74198 8-bit bidirectional shift register is used along with various shottky TTL devices (H1). The use of shottky devices desensitizes the circuitry to differential delays between clock and data signals which might be introduced by normal TTL devices. Logic drawing H1 details the shift register and input/output buffers. Handshaking logic is detailed on H2. The block drawing including both of these is B4. Referring to the top of H1, the clock-in signal (CKIN) is passed through three 74S04 buffer stages and a line-driver to emerge as the clock out signal (CKO). It is tapped in mid-chain to drive the shift clock for the 74198's. The PARELL signal is a single clock pulse generated when the shift register is to be loaded in parallel for data transmission back to the host system. The PARELD signal switches the mode of the shift registers to enable parallel loading during the PARELL pulse. Twenty four of the shift register bits are data (DFO-DF23; DTO-DT23). Bits DCO-DC2 are a control code. Bits DEO-DE1 are not used in this system.

At the bottom of H1 is the serial data path. The STROUT signal selects the data out source to be either data in (DAIN) or the output of the shift register (DF23).

Drawing H2 is handshaking and control for the serial data interface of H1. The clock-in signal (CKINA) retrigger a one-shot every clock pulse during a burst, and its output remains true during the entire clock burst. The capacitor from CKPERN to PCAP prevents incomplete firing of the one-shot for short drive pulses. At the end of the clock period, CKPER goes false and triggers a CKEND pulse to be used to signal stable data at the shift register outputs during a data-receive cycle. This
signal indicates the completion of a cycle during data transmission. The remainder of H2 is dedicated to a data transmission cycle.

The REQI signal triggers the transfer of data from a selected memory location to the host computer. The rising edge of REQI sets a flip-flop to start the cycle. The flip-flop is reset at the end of the cycle by the clock-end pulse (CKEND) AND'ed with with STROUT. STROUT is true while the computer has given the memory system control of the serial link.

The RQ signal from the flip-flop causes REQ, the bidirectional handshaking line to the computer, to be driven to about 1 volt. RQAN simultaneously goes low. The computer grants control by forcing REQ to about .1 volt, turning off collector current to the first transistor of the pair and consequently releasing RQAN. This sets SROUT true. RQ must be high to enable SROUT. RQ going high triggers a parallel-load sequence by setting the PARELL flip-flop. PARELD goes true to switch the shift registers into parallel-load mode. PARELL (the parallel-load strobe) is high just prior to PARELD. PARELD going high sets LDCKN low, resetting PARELL, and after a short delay resetting PARELS. The edge of PARELL (resetting) strobes data into the shift registers. PARELD is delayed sufficiently by the two inverters to allow parallel loading to occur before switching back to serial-shift mode.

The front-panel CLEAR pushbutton is used to initialize the REQ loop and the parallel-load loop, either of which may be placed into unrecoverable states during power interruptions.

**MEMORY CONTROL SUBSYSTEM**

The memory control subsystem (B3, H3-H5) performs several functions. First, it remembers which 8-k block of memory (and which 4-k half of that block) are under current scrutiny by the host computer system (H3).
Second, it decodes commands to initiate read and write operations to the selected memory (H3). Third, it multiplexes data from the four memory subsystems, connecting the proper one to the shift register data input line (H4). Fourth, it remembers an address, incrementing when desired to allow convenient transfers of contiguous blocks of storage (H5). Finally, this subsystem contains the master four-phase clock used to synchronize operations of the four independent memory subsystems. Driving each memory subsystem with a different phase of the clock staggers large parallel data-switching operations to reduce the system's noise-generation ability, thereby eliminating potential crosstalk problems.

As mentioned earlier, the CKEND pulse occurs when shift register data is stable. On H3, CKENDN (the low-true version of CKEND) is used to strobe data bits DCO-DC2 into a decoder. Six of the possible eight outputs are used as follows:

- **Code: 1 - Initialize**
  - Reset data bits DFO-DF11 into the address holding flip-flops (H3).

- **2 - Write Initiate**
  - Strobe data bits DFO-DF11 into the address holding register (H5).

- **3 - Write**
  - Trigger a memory write cycle at the address specified by Code 2. Data bits DFO - DF23 are written to memory. At the end of the write cycle, the address holding register is incremented by the RESIT signal (H3) returning at completion.
4 - Read Initiate

Strobe address bits DFO – DF11 into the address holding register. Trigger a memory read cycle and increment the memory address holding register at completion.

5 - Read

Trigger an operation identical to that triggered by Code 4, except do not load the address holding register.

6 - Select

Strobe data bits DF21 – DF23 into a holding register (H-3), selecting a single 4-k block of memory. Each memory plane is 8k words. DF23 is used as the most significant address bit. DF21-DF22 are decoded to select one of the four planes.

With the exceptions of Select (Code 6) and Initialize (Code 1) each of the above operations results in an echo back to the host computer. The write initiate signal, through logic which guarantees no overlap between the CKEND signal and the REQI signal, triggers an immediate response. The others rely on the end of a memory cycle (RESTAN – RESTDN) to trigger the echo. Read operations (Codes 4,5) echo the data word from memory. Bits MS21 – MS22 (H-3) select one of the four memory data busses for connection to the shift register parallel inputs via the multiplexer on H4.
MEMORY SUBSYSTEM CONTROL

The memory subsystem hardware (H6-H9) is duplicated four times, once for each 8k phase. To avoid having to duplicate these drawings four times, the logic signals are written with a ~ inserted in place of the A, B, C or D. This also specifies the physical location of the logic on the wire-wrap board.

Two masters (an ADC and the serial interface) must have interleaved access to each memory. These requests (ADCREQA and MEMSL~) appear in the upper left corner of H6. Upon being accepted, they are strobed, each into its own flip-flop. The flip-flops drive a priority encoder which guarantees that only one gets control of the memory. The ADC has top priority. Upon selection of either the serial interface or the ADC, data, address and control paths are set up for the memory (B-2). Control setups (chip select, read/write) are handled via the logic shown on H6.

Two sections of a multiplexer are used to steer the correct inputs to the read/write line (RNW~) and to the chip select control (CYRST~).

During a serial-interface triggered cycle, only one memory chip select is required (either read or write). During an ADC cycle, two are required— one to read and one to write. A single three-bit counter in conjunction with four flip-flops is used to control these functions.

If AD^TROL (H6) goes high, it clocks the setting of the first flip-flop. This forces (via QNTP^) the second flip-flop into the reset state. When this flip-flop is reset, CYRN^ goes low, resetting the first flip-flop. This sets QNTP^ high, enabling the eventual clocked setting of the second flip-flop.

CYRN^ drives (through a multiplexer section) the reset line of the three-bit counter. When CYRN^ is reset, the reset line (CYRST^) releases
and the counter can start counting. Its count clock is one phase of the system clock, and counting occurs on the trailing edge of the clock pulse. The first clock pulse sets CHIPS\(^\wedge\) true, generating a chip select. At the beginning of the next clock, DOS\(^\wedge\) is generated to strobe data from memory into a holding register (H7). The end of this second clock pulse turns off the chip select and enables the incrementing of the data (RNW\(^\wedge\)H). This signal also switches the memory read/write signal (RNW\(^\wedge\)) to write (via the multiplexer).

Data counting is strobed by a clock phase two later than that used to generate the chip select (PHA+2). The next clock pulse (PHA) once again turns on the chip select enable (CHIPS\(^\wedge\)). This chip select is for the write cycle. An extra data output strobe and data count are generated at the end of this cycle, but they have no effect. The next clock pulse turns off the chip select enable and the data count enable, but sets CYSTOP\(^\wedge\). CYSTOP\(^\wedge\) sets the control flip-flop which in turn forces the reset line on the control counter (CYRST\(^\wedge\)) to hold the counter reset. The rising edge of CYRN\(^\wedge\) also triggers a reset pulse for the ADC.

A serial interface cycle is not dissimilar to an ADC cycle, except the stop signal comes from the second bit of the counter (RNW\(^\wedge\)H) instead of from the third bit. The result is a single chip select. RNW\(^\wedge\)H is pulsed, but the data register is not counted because the control counter is reset by the rising edge of RNW\(^\wedge\)H, long before PHA+2 occurs. The read/write line is driven from the serial interface (SIWRT) instead of from the control counter.

Data bits from the ADC (AD\(^\wedge\)14 - AD\(^\wedge\)2 on H9) are buffered through exclusive-or's to allow selection of either high-or-low-true logic. The routing bit (AD\(^\wedge\)2), ADC-ready line (ADCRDY\(^\wedge\)) and ADC reset line (ADCRST\(^\wedge\)) are all individually controlled in similar fashion from the DIP switch.
located on the logic board. Settling time for ADC data lines is switch setable from the rear panel in order to accommodate both slow and fast ADC's.

MEMORY PLANES

The memory planes are provided as four independent PC boards, drawing 21X2562 S-1. The memory chips are SEMI 4200 static 4kx1 RAM's. They are clocked devices, drawing little power until the chip select signal goes true. Consequently the memory is normally cool to the touch. These devices use three power supplies, however-- +5V, +12V and -5V-- and the chip select signal is +12 volts driven to ground. Terminators for the chip select are provided on each memory plane.

REFERENCES


2. Drawing Package #21X448, UCLBL.
This report was done with support from the Department of Energy. Any conclusions or opinions expressed in this report represent solely those of the author(s) and not necessarily those of The Regents of the University of California, the Lawrence Berkeley Laboratory or the Department of Energy.

Reference to a company or product name does not imply approval or recommendation of the product by the University of California or the U.S. Department of Energy to the exclusion of others that may be suitable.