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A MODULAR 125 PS
RESOLUTION TIME INTERVAL DIGITIZER
FOR 10 MHz STOP BURST RATE AND 33 MS RANGE

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Abstract

A high resolution multiple stop time interval digitizer is described. It is capable of resolving stop burst rates of up to 10 MHz with an incremental resolution of 125 ps within a range of 33 ns. The digitizer consists of five CAMAC modules and uses a standard CAMAC crate and controller. All the functions and ranges are completely computer controlled. Any two subsequent stop pulses in a burst can be resolved within 100 ns due to a new dual interpolation technique employed. The accuracy is maintained by a high stability 125 MHz reference clock. Up to 151 stop events can be stored in a 48-bit, 10 MHz derandomizing storage register before the digitizer overflows. The experimental data are also given.

Introduction

Time-of-flight digitizers are widely used in experimental high energy nuclear physics and laser rangings. Basically, they are high resolution fast multiple stop clocks covering time ranges from a microsecond to tens of milliseconds. Each time cycle is initiated by a start pulse. Stop pulses are generated as various particles hit detectors. The digitizer has to resolve the time interval between the start and any of the stops in a very short time in order to be ready for another stop event as soon as possible. Any single stop in a burst that is accepted within the time range will be digitized within a time interval which we will refer to as the "stop deadtime". During this interval other stop signals will be rejected. Therefore, deadtime has to be small, especially when high stop rates are expected. Most digitizers that have been reported thus far, offer either a high time resolution (100 ps) but long stop deadtimes (5 μs) or high stop burst rate capability (10 MHz) but relatively low resolution (1 ns). An additional common problem all multiple stop digitizers share is a lack of a fast and reasonably large temporary register for the data. A direct transfer of stop burst data between the digitizer and even the fastest processors is still too slow resulting in high stop event losses. In this paper a time-of-flight digitizer is described (further on referred to as Digitizer) that combines a high time resolution (125 ps) with low stop deadtime (100 ns). In addition, the Digitizer has a 151-stage fast derandomizing register for storing 48-bit words at the rates exceeding 10 MHz. The digitizer covers time ranges from 8 μs up to 33 ns. Any range length can be computer programmed in 8 μs steps. The Digitizer system consists of 5 CAMAC modules and uses a standard CAMAC crate and controller.

The circuits employed in fast systems dissipate a lot of power. Thermal problems are quite serious, especially in a CAMAC environment. The Digitizer was designed to use a minimum of fast discrete and fast integrated circuits.

Each of the five Digitizer modules was made to perform the assigned functions with a minimum of wired interconnections in order to simplify servicing and reduce crosstalk. The modules and their basic functions are:

- Clock and Calibrator Module. This module contains a high stability oven controlled 125 MHz clock reference and clock pulse shaping circuitry. Also it comprises a precision time marker generator for testing the Digitizer.
- Dual Interpolator. This is an analog module for the synchronization of the external input start and stop signal with the 125 MHz clock. A new dual interpolation method is used. The stretching of the small fraction of the clock pulse at the beginning and the end of the measured time interval takes place twice, each time by a factor of eight. A great reduction in interpolation deadtime is thus achieved. The interpolator resolves the measured time intervals to 1/64th of the clock pulse period (125 ps), requiring an average of 100 ns for the conversion.
- Fast Logic Module. This module contains fast ECL logic circuits, counters and registers, for the digitizing of the analog signals provided by the dual interpolator. Also, it contains input circuits and fast storage for the 18 external tag signals. Tags serve for identification of the individual stop pulses, accepted by the Digitizer.
- Slow Logic Module. This module contains the bulk of the logic circuits, that perform the counting, arithmetic operations and derandomizing of data. Also, it stores the computer instructions via CAMAC (such as the Digitizer's range, conversion deadtime and enable time), displays all the data, and provides the transfer of data to the FIFO register.
- FIFO Register. This register is a fast derandomizing data storage. It can store 128 words of 48-bit data from the Slow Logic Module at the rates exceeding 10 MHz. The register output can be read via CAMAC at the rates and times independent of the input data rates. A standard CAMAC Crate Controller is required for communication between the Digitizer and the available processor.

Digitizer System Description

Typical application of the Digitizer is for nuclear time-of-flight measurements. A pick-off from the accelerator pulse provides the start signal to the Digitizer. The shower of nuclear particles spread out during the time-of-flight, hits one or more detectors and generates a burst of stop pulses. A sequence of such events is illustrated in Fig. 1. The general block diagram of the Digitizer is shown in Fig. 2 and Fig. 3. Only a start pulse, coincident with the external start enable pulse will be accepted by the Digitizer. From the leading edge of the start pulse, the stop times can be resolved in 125 ps increments throughout the preselected time range $T_R$ in Fig. 1. Start busy signal is available for the monitoring and external timing. During the $T_R$ no other start input can be accepted. The time range length is determined by the status of the 12-bit Range Register (Fig. 2). It can be reloaded by a CAMAC command at any time. At the beginning of each start cycle, the content of the Range Register (RR) is read.

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into the Range Counter (RC). RC is advanced by counting the 8 ns long clock pulses generated from 125 MHz Master Counter (MC2). The range time ends when RC is overrun. A master clear pulse is then generated, restoring the Digitizer to the initial conditions. A new start pulse can then be accepted.

Each time the Digitizer accepts a start pulse, the gated Deadtime Clock is started, having the clock period determined by the length $T_D$ of a delay line DL. Also, an Enable/Deadtime counter (EC) is loaded from Enable Register (ER). The number of deadtime clock pulses that are needed to bring DC to zero is equal to the content of the ER. At this point the stop input of the Digitizer is internally enabled and a Stop Enable signal output is available for external timing. DC and ER have a 12-bit range and if a 100 ns deadtime clock period was selected by using the right length of DL, the enable time covers a range from 100 ns to 0.4 ms in 100 ns increments.

When enabled, the Digitizer will accept stop pulses which are coincident with the stop enable signal at the input of the dual interpolator. $S_p$ in Fig. 1 will thus be the first accepted stop pulse. Stop input circuit remains busy and cannot accept other stops for the duration of the valid stop signal. An average time of 100 ns is needed to digitize the "first stop" interval ($T_s$) in the Master Counter (MC) and the "Coarse" Counter (CC) and the "Fine" Counter (FC), and transfer the data into the corresponding registers (MR, CR and IR). A "First stop" system tag is also generated and strobed into registers along with $T_s$ marking the beginning of each stop pulse burst after a new start.

The valid stop output is most useful in calculating statistical corrections for the losses, especially at high stop pulse rates. Fixed stop deadtime of constant duration that the Digitizer provides simplifies the calculation of the correction. Longer Digitizer stop deadtimes are often needed, when additional information describing a particular stop pulse is to be strobed into the registers along with the digital time information. External 18 tag inputs are available for recording the amplitude of the stop signal and its detector number in the Tag latch (TL). The minimum stop deadtime of 100 ns can be made longer by the deadtime counter. The deadtime clock is started once for each valid stop and Deadtime Register (DR) data is strobed into the DC. The valid stop time will be increased by 100 ns for each of the DC clock pulses counted. The deadtime range is 12 bits, the same as the enable time range. The deadtime can be changed any time if DR is reloaded by a new CAMAC command.

In Fig. 1, only the stops $S_p$ to $S_m$ met the acceptance conditions. They were tagged and quickly shifted through the registers. There are three groups of fast demultiplexing registers that also gradually perform some arithmetic functions to be described later (Figs. 2 and 3). Each transfer requires less than 100 ns. A Summing Counter (SC) (the third register stage) delivers each completed stop event to the 128-stage FIFO register for fast storage in 48-bit words.

The CAMAC readout from FIFO to a computer is comparatively slow for the high stop event rates that the Digitizer can provide. There is a high probability of having some stop events rejected because of the register space shortage. Any stop event that cannot be transferred because all of the registers are busy will have the valid stop time (and thus the deadtime) stretched beyond the preset stop deadtime. Such stop event will be eventually transferred into the register, but along with a 'buffer full' system tag. The average deadtime of the tagged stop burst is longer than the deadtime of one that is untagged. The incomplete burst can be either rejected or the appropriate statistical corrections made.

**Dual Interpolation Principle**

Interpolation techniques are often used for digitizing time intervals which are smaller than the full reference clock pulse and therefore can not be resolved by simple counting (see the Refs.). An example of single interpolation is shown in Fig. 4, line 4, where an interval $T_{ab}$ $T_o$ is stretched and then digitized, pacator is charged by a constant current for a duration of the time interval $T_{ab}$ $T_o$. At point b which is coincident with a clock pulse, the charging current is turned off. The capacitor is then brought to its initial level by a discharging current which is K times smaller than the charge current. The resulting stretched time interval $T_{bc}$ is therefore K times longer than $T_{ab}$ $T_o$. $T_{bc}$ can be digitized by counting the number of clock pulse periods. The time resolution in digitizing $T_{ab}$ is thus increased by a factor of K. High resolutions can be achieved by using either higher clock frequencies and/or a large K, but the conversion time may be prohibitively long.

In order to shorten the conversion time, a new dual interpolation technique is used. Interval $T_{ab}$ $T_o$ is first stretched $K_o$ times into a "coarse" interval $T_{bc}$. $K_o$ is low enough so that the maximum conversion time is short. The small time interval $T_{cd}$ (line 5) between the end of $T_{bc}$ and the second following clock pulse is stretched once again by a factor $K_F$ into a "fine" interval $T_{de}$. $T_{de}$ is digitized by counting $N=T_{de}$ $T_o$ clock pulses. Each fraction of the "coarse" interval that equals $T_{bc}$ is thus worth $K_F$ "fine" clock pulses. Since each fraction of $T_{ab}$ that equals $T_o$ is worth $K_C$ clock periods, each "fine" count is equivalent to $T_o$ $T_o$ $K_C$.

The net result is equivalent to an interpolation, where $T_{ab}$ $T_o$ would be stretched by a factor $K=K_C K_F$, and then digitized by counting $N=T_{ab}$ $T_o$ clock pulses. Each count then represents an increment of $T_o$ $K_C$.

The total conversion time $T_o$ that would be required for such a single interpolation is

$$T_s=(1+K)(T_{ab} T_o/2),$$

where $T_o/2$ is a constant, selected to reduce the conversion time and

$$K=K_C K_F$$

$K_C$ and $K_F$ are the "coarse" and the "fine" conversion ratios. The dual interpolation as illustrated in Fig. 4 (lines 4 and 6) that would give the same resolution as the single interpolation in Eq. 1 requires a total conversion time of

$$T_s=(1+K_C K_F)(T_{ab} T_o),$$

where

$$T_o=(1+K_C T_{ab} T_o)+(1+K_F T_{cd})$$

(3)
The dual interpolation conversion time is thus shorter by the ratio $T_s/T_d$. The worst case is when $(T_{ab} - T_o) = T_{cd}$, giving the ratio

$$T_s/T_d = (K_C + K_F)/K_C + (K_F^2 + K_C^2 - 2K_C K_F)$$  \hspace{1cm} (4)

Eq. (4) has a maximum when $d(T_s/T_d) / dK_C = 0$, i.e.,

$$K_C_{max} = K_F_{max} = \sqrt{R}$$  \hspace{1cm} (5)

These are the optimum $K_C$ and $K_F$ for the shortest dual conversion. Eq. (4) then becomes

$$(T_s/T_d)_{max} = (K+1)/2\sqrt{K+1} \cdot \frac{1}{2\sqrt{K}} \text{ (when } K \text{ is large)}$$  \hspace{1cm} (6)

When a "fine" conversion starts, the "coarse" conversion is already completed. The next "coarse" conversion of a new event can start even if the "fine" conversion of the previous event is still in progress. The total conversion time is then only slightly longer than a single "coarse" conversion. The total conversion time is thus further reduced almost by a factor of two:

$$(T_s/T_d)_c = (K+1)/2\sqrt{K+2}$$  \hspace{1cm} (7)

The resolution required by the digitizer described in this report was 125 ps. A clock frequency of 125 MHz was selected, i.e. $T_o = 8$ ns. Therefore $K=64$, thus if $K_C = K_F = 8$, we find $(T_s/T_d)_c = 6.5$. The total dual interpolation time is therefore 6.5 times shorter than a conventional single interpolation with the same $T_o$.

Due to the very short conversion time there is no need for two separate start and stop interpolators. The same dual interpolator performs both start and stop conversions by feeding both start and stop pulses into the same input. Virtual immunity to the temperature change is thus achieved because the interpolator is self-tracking. For the same reason, large variations in stop pulse burst rates do not affect the stability of the measurement. If separate interpolators are used, a significant time drift may result if there is a large difference between start and stop signal rates.

In Fig. 4 a start pulse is shown, at the point $a$, followed by a stop pulse at $f$. The measured time interval $T_{af}$ can be split into three fractions.

$$T_{af} = T_{ab} + T_{bg} + T_{fg}$$  \hspace{1cm} (8)

$T_{ab}$ is the fraction of $T_{af}$ between the leading edge of the start pulse and the second following clock pulse at $b$, and $T_{fg}$ is the fraction between the leading edge of the stop pulse and the second following clock pulse at $g$. The acceptance of the start pulse and later on of the stop pulse will cause two "coarse" - "fine" conversions in the dual interpolator. In order to shorten the "coarse" conversion time, the conversion start is delayed by $T_o/2$ (see line 4) so that

$$T_{ab} - T_o/2 = K_C (T_{bd} - T_{cd})$$  \hspace{1cm} (9)

$T_{bd}$ is the "coarse" gate signal spanning a total of $N_{bd}$ full clock intervals, $T_{cd}$ (line 6) is the time fraction between the end of the "coarse" start conversion and the second following "coarse" clock pulse.

$$T_{cd} - T_o/2 = K_F T_{de}$$  \hspace{1cm} (10)

$T_{de}$ is the "fine" start gate signal, digitizing $N_{de}$ "fine" clock pulses. The stop pulse, accepted at the point $f$, will be followed by a similar sequence of pulses:

$$T_{fg} - T_o/2 = K_C (T_{gi} - T_{hi})$$  \hspace{1cm} (11)

$$T_{hi} - T_o/2 = T_{ik}$$  \hspace{1cm} (12)

Combining Eqs. 9 to 12, the Eq. 8 becomes

$$T_{af} - T_o = (N_{AF} - N_{dg}) - (N_{gi} - N_{bd}) / K_C (N_{ik} - N_{de}) / K_F$$  \hspace{1cm} (13)

At the point $b$ the clock pulses are enabled until the digitizer is master cleared at the end of the preset time range. The counting of the clock pulses during the "real" time interval $T_{fg}$ is shared by the auxiliary counter (MC) and the Master Counter (MC) in Fig. 2. AC starts first to count only 8 initial clock pulses during the period $T_A$ and then switches the counting to MC. AC also generates a carry signal in the space half-way across $T_A$ which adds missing 8 counts to MC in advance. Thus MC idles during $T_A$ following each accepted event, allowing the strobing of data from it (waveform 21) into the Master Register (MR). MC, resuming the counting after each $T_A$, retains thus the correct digital reference to the initial start point $b$. Transfer of data follows from the "Coarse" Counter (CC) into the "Coarse" Register (CR) and from the "Fine" Counter (FC) into the "Fine" Register (FR) as soon as the counting is completed, in order to enable the interpolator for a new stop event.

The second shift of the data follows immediately. MR transfers the data into the Second Register (SR) (Fig. 3). CR transfers $N_{bd}$ into the "Coarse" Start Register ($CS_{tr}$) and FR transfers $N_{de}$ into the "Fine" Start Register ($FS_{tr}$), where they remain stored for the rest of the preset time range.

After a stop pulse is accepted, MC switches the counting to AC at the point $g$ (lines 12 and 13 in Fig. 4). MC contains at $g$ a total of $N_{AC} + N_{dg}$ counts, which is then transferred into SR by thestrobe $N_{sp}$.

The missing $N_{gi}$ pulses are then added to MC and the counting in MC resumed at the point $j$ (line 13). $N_{gi}$ "coarse" stop counts are transferred from CC into CR by the strobe pulse $C_{sp}$ and $N_{ik}$ "fine" stop counts are strobed from FC into FR by the strobe pulse $F_{sp}$. CR, MR and FR are again immediately cleared, and the interpolator enabled for the new stop event. The next rapid data transfer follows: $N_{AC} + N_{dg}$ is strobed from MR into the Second Register (SR), $N_{gi}$ from CR into the "Coarse" Stop Register ($CS_{tr}$), and $N_{ik}$ from FR into the "Fine" Stop Register ($FS_{tr}$).

The data transfer between the register is shorter than the interpolation time. The flow of events is thus derandomizing the high rate of stop events. Now the registers contain all the data needed for the computation of Eq. 13. The incremental resolution of 125 ps can be obtained by selecting $K_C = 2 \cdot C^{-1} = 8$ and
$K_f = 2^{R_f} = 8$. Eq. 13 can be rewritten into

$$T_{af} = \left(\frac{N + N_{bd}}{K} \right)^* \frac{(N + N_{bd})/K - C}{N_{bd}/K} - \left(\frac{2 + 2K - 1}{K} K_f\right)$$

(14)

$N_{bd}$ and $N_{de}$ are the complements of $N_{bd}$ and $N_{de}$, and

$N_{gd} = N_{gb}$ is the complement of $N_{gb}$. Only adding operations are required since the last term is a constant. The "fine" stop is added to the complement of the "fine" start in the "Fine" Adder (FA), and the "coarse" stop is added to the complement of the "coarse" start in the "Coarse" Adder (CA). Then FA is added to the complement of CA in the Second Adder (SA). Finally, SA and SC data is strobed into a register in the Summing Counter (SC). The registers SR, CS, and FS are now free for the next stop event.

The Summing Counter (SC) is the third fast derandomizing register stage. It contains a synchronous counter where SR data is strobed, and also has a register storing the result of the interpolation from SA. SC output is the final result of computing the Eq. 14. The total measured start/stop interval is given by a 28-bit word, covering a range of up to 32 ms with a resolution of 1/8 ns. In addition, 18 tag bits are strobed along with the time information, since each register stage contains also an 18-bit tag section. 18 external connectors can be used either for tag signals or for any information regarding a particular stop event. Tags should be strobed into Tag Latch (TL) a few nanoseconds after a stop event was accepted. The tag data propagates from register along with the time data.

Two more "system" tags are also generated. A "first stop" tag marks the first stop event in a burst after each new start. A "register full" tag marks each stop event whose transfer was delayed because the registers were busy. The deadtime of such a stop event is longer than the preset deadtime, which may greatly complicate data statistics. The two "system" tags define when and where the pile-up occurred so that the whole burst may be eliminated by the computer if necessary.

The SC is followed by a "first-in-first-out" (FIFO) register (FR). 128 words of 48-bit data can be stored in FR at the rates exceeding 10 MHz. The FR readout takes two 24-bit CAMAC cycles for each event. The FR can also be overwritten by CAMAC commands for testing or for the storage of data.

A number of manual controls and LED displays makes it easy to monitor and check the operation of the Time Digitizer. Also, fast NIM output signals are provided for the external timing of the input logic and tagging.

Experimental Results

The digitizer can derandomize and process time events at average rates close to 10 MHz. Its storage capacity of 131 events is adequate for single long stop bursts. However, to avoid losses the data should be transferred to a processor at a rate equal to the average digitizer input rates. The processor storage capacity should be very large even if only a fraction of the digitizer's range is used at a time. To cover only one millisecond of the time range, a storage capacity of $8 \times 10^6$ words would be required. In our case, only a 4,096-channel memory was available.
middle of the channel as indicated by the symmetry of the peak. The position of the peak shifts slightly from stop to stop. At the stop No. 10 the peak is evenly distributed into the two adjacent channels, indicating half a channel (62.5 ps) shift. If the frequency ratio of the Digitizer's 125 MHz reference oscillator and the 50 MHz marker generator reference were exactly 2.5, no shift of the stop pulses should occur. Therefore, the accumulated 62.5 ps shift over 7 stop intervals (covering 35 ps) indicates the difference between the two reference frequencies of about $2 \times 6^\circ$.

Fig. 9 shows the same setting as in Fig. 7 except for the reduced stop enable time. The number of stop pulses per burst has increased accordingly. In this case, the rate of the stop pulses exceeded the maximum rate at which they can be stored into the memory. The registers of the Digitizer begin to fill up from the stop No. 14. The stop deadtimes are increased by the time the registers are busy. The loss of some stops results (seen as the blurred portion of the valid stop waveform in Fig. 9). Some of the stops are transferred into the memory during the stop enable time leaving only 13 stop spaces free at the beginning of each burst. The distribution of the first 13 stops therefore remains unchanged. Only three additional stops were accepted out of 16 that actually appeared at the stop input of the Digitizer during the interval between the stop No. 14 and the end of the range.

Conclusions

The Digitizer was not tested so far in a time-of-flight experiment. However, the laboratory measurements confirm the expected inherent stability of the Digitizer due to the single interpolator being used at both the start and the stop of the measured time interval. Virtually no time drift was observed when a delay-line generated time interval was measured for several days. Also, no significant drift was observed when stop burst rate varied, again because the same interpolator processes both the start and stop events. Dual interpolation results in excellent averaging of measured intervals, permitting a large margin in misalignment of the interpolator before the time peak resolution is affected. Based on these results, one could build an even faster multiple stop digitizer by increasing the reference clock frequency to 250 MHz. The minimum stop deadtime would be reduced to 50 ns and the incremental resolution increased to 62.5 ps.

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References


Fig. 1 TIME-OF-FLIGHT DIGITIZER BASIC TIMING DIAGRAM

Fig. 7 5.12μs REPETITION RATE STOP BURST

Fig. 8 DISTRIBUTION OF STOP BURST FROM Fig. 7 (STOPS ARE SEPARATED BY 8ns TO AVOID OVERLAP)
RESOLUTION: 125ps/CHANNEL
Fig. 4 TIME-OF-FLIGHT DIGITIZER DUAL INTERPOLATION TIMING DIAGRAM

Fig. 5 256ns REPETITION RATE STOP BURST