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Advances in N-path Filtering for Broadband Tunable and Interference Robust Reception

A dissertation submitted in partial satisfaction of the requirements for the degree
Doctor of Philosophy

in

Electrical Engineering (Electronic Circuits and Systems)

by

Chris Michael Thomas

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Professor Lawrence E. Larson, Chair
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Professor Todd P. Coleman

2015
The dissertation of Chris Michael Thomas is approved, and it is acceptable in quality and form for publication on microfilm and electronically:

Co-Chair

Chair

University of California, San Diego

2015
DEDICATION

To my parents and family.
Begin at the beginning,
and go on till you come to the end; then stop.
—Lewis Carroll, *Alice in Wonderland*
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Technology Meeting (BCTM). The dissertation author was the primary researcher and the first author listed in these publications with exception to BCTM in which he is co-author. He performed the research which forms the basis of these chapters. The text of Chapter 5 gives an over-view of a full system that performs signal separation and classification with research contributions from Prof. Gert Cauwenberghs and his students Chul Kim and Siddharth Joshi. The channelizer presented in Chapter 5 was designed by Dr. Hao Li with test setup design and measurement performed by the dissertation author.
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ABSTRACT OF THE DISSERTATION

Advances in N-path Filtering for Broadband Tunable and Interference Robust Reception

by

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This research aims at creating broadband tunable, fully integrated filters for the application of cognitive radio and signal classification receivers. The approach under study is the N-path filter technique which is capable of translating a baseband impedance to a reference frequency creating a tunable filter. The traditional N-path filter suffers from fundamental architectural limitations, namely: a trade-off between insertion loss and out-of-band rejection, reference clock feed-through, and jammer power handling limitations.

In the first approach, the fundamental trade-off of the traditional N-path filter between insertion loss and out-of-band rejection is improved by a transmission line (T-line)
N-path filter technique. The T-line N-path filter ideally absorbs the parasitic capacitance of the N-path filter into a synthetic transmission line, improving insertion loss. Moreover, the out-of-band rejection is improved by further low-pass filtering. A transmission line N-path filter was implemented in a 65 nm CMOS process that achieves a tunable band-pass filter with tunable pass-band range of 0.1-to-1.6 GHz, less than 5 dB insertion loss, 30 dB to 50 dB out-of-band rejection, in-band IIP3 of +29 dBm, and IP1dB out-of-band jammer tolerance of +11 dBm.

In the second approach, a pseudorandom clocking scheme for an N-path bandpass filter is presented, which lowers the LO leakage to the filter’s input and output. Measurements of a 65 nm CMOS prototype from 100 MHz to 1.4 GHz demonstrate 15 dB out-of-band rejection, P1dB of +0 dBm, in-band IIP3 of +22 dBm, out-of-band jammer tolerance of +11 dBm, and LO leakage improvement of 10 dB to 15 dB with magnitude ranging from -60 dBm to -80 dBm.

Lastly, a GaN HEMT bandpass N-path filter is demonstrated for high jammer tolerance. Measurements from 50 MHz to 300 MHz of a series architecture implemented in hybrid form with Cree bare die in 400 nm technology demonstrate a IP1dB of +10 dBm, IIP3 of +24.6 dBm, and a IP1dB out-of-band jammer tolerance of +17 dBm.

As an example application for the tunable front-end filter, a signal classification receiver (Cognitive radio Low-energy signal Analysis Senor IC - DARPA CLASIC program) topology is presented. The CLASIC receiver is a multi-antenna receiver that channelizes, separates, and then classifies signals within a band of interest. A key building block of the CLASIC receiver is the baseband channelizer that allows for parallel signal separation in the following stages in the receiver. Measurements were performed on a 1-to-16 BiCMOS channelizer to demonstrate feasibility.

Current research avenues and potential future investigations are reviewed in the conclusion.
Chapter 1

Introduction

1.1 Spectrum Resources and Transceiver Complexity

Cellular receiver complexity has grown with multi-band, multi-standard coverage (GSM, WCDMA, LTE, GPS, etc.) [10]. For example, current cellular receivers cover at least a dozen bands in the main transceiver. Demand for higher data rates and the corresponding increased bandwidths of standards (for example, 20 MHz LTE or 100 MHz carrier aggregated LTE) pushes the need for adding more bands. An illustration of the complexity of the transceiver is shown in Fig. 1.1 with multiple transmitters and receivers to service each band. Adding further complexity, a separately located replica multi-band receiver is often utilized providing received signal spatial diversity to insure reception or increase data rates (Fig. 1.1). The broad multi-band nature of the receiver renders the receiver susceptible to out-of-desired-band jammers which may desensitize the receiver.

Cellular communication systems often employ frequency-division duplexed transceivers (FDD) which use a single antenna to transmit (Tx) in one band while receiving (Rx) in a separate band. For FDD, self-jamming is a serious concern and places strict performance criterion on the transceiver (illustrated in Fig. 1.2(a)). For example, a W-CDMA FDD transceiver can transmit a maximum power of +24 dBm while trying to receive a signal at sensitivity around -114 dBm giving a necessary dynamic range of 138 dB - completely impractical. To help provide isolation between the transmitter and receiver, an off-chip three-port duplexer is often used for each FDD band serviced. A
duplexer can provide 55 dB isolation between the Rx and Tx reducing the required dynamic range to a more reasonable 83 dB. Beyond the isolation provided by the duplexer, further filtering is often required - namely, SAW filters.

The cellular receiver employs multiple off-chip SAW filters for band selectivity. An example current cellular receiver is shown in Fig. 1.3 with transceiver and off-chip duplexer and SAW filter banks. The growing number of off-chip components increases the size of the design and cost making the possibility of servicing further bands less feasible.

To address spectrum over-crowding, the Federal Communications Commission (FCC) released the cognitive radio (CR) (IEEE 802.22) standard allowing for wireless regional area networks (WRANs) to utilize unoccupied commercial TV broadcast bands for communication. A CR should be capable of identifying unused spectrum by primary users and dynamically adapting to use the available spectrum. One of the major challenges of CR systems is co-existence with existing TV systems. An existing nearby TV systems may desensitize the CR which may receive a jammer as large as -8 dBm while trying to receive a signal at -102 dBm sensitivity (illustrated in Fig. 1.2(b)).

The growing number of off-chip components suggests the need for a fully integrated filter with low in-band insertion loss and distortion, and high out-of-band jammer rejection. Moreover, beyond full integration, the filter should be broadband tunable to allow for frequency agility that is needed in CR systems. Full transceiver integration and agility demands a monolithic CMOS wideband tunable filter.

The following sections describe the mechanism of receiver desensitization, introduces the N-path filter as a potential solution, and gives an overview of the current state-of-the-art of N-path filtering and its limitations.
Figure 1.1: Example smart phone with multiple transmitters and receivers, off-chip filters, and diversity antenna with multi-band receiver [1].
Figure 1.2: Example jammer sources: (a) Illustration of transmitter leakage into receiver path for FDD systems. (b) Illustration of near-by transmitting TV tower desensitizing a cognitive radio.
Figure 1.3: Components on the top side of iPhone 5s Printed Circuit Board (PCB) [2].
1.2 Mechanisms of Receiver Desensitization

Receiver desensitization, meaning the sensitivity is degraded, due to an out-of-band jammer is attributed to multiple factors: second-order distortion, third-order distortion, and reciprocal mixing. Each mechanism of receiver desensitization is described in the following sections.

1.2.1 Second-order Distortion

For direct-conversion receivers, where the desired signal band is directly down-converted and centered at DC, the receiver’s second-order distortion plays a critical role in the overall sensitivity. A modulated signal appearing out-of-band at any frequency will create intermodulation distortion through the receiver’s finite IIP2 and corrupt the desired baseband signal. The mechanism for the desired signal corruption is illustrated in Fig. 1.4 with the out-of-band modulated signal power of $P_{jam}$ and corresponding baseband distortion. The input referred distortion power due to the out-of-band jammer is given by

$$PN_{im2} (dBm) = 2(P_{jam} - F_{atten}) - 6 - IIP2,$$

(1.1)

where $F_{atten}$ is the attenuation of the front-end filter in $dB$, and 6 is a correction factor [11].

The second-order distortion of the receiver is generally dominated by the down-converting mixer and is a strong function of device mismatches. The LNA generally does not contribute to the second-order distortion as a DC blocking capacitor is often inserted between the LNA and down-converting mixer. In general, front-end filtering before the down-convorctor is needed in full-duplex systems for the case of maximum transmit power. With calibration techniques added, impressive IIP2 performance can be achieved in the range of IIP2 = +90 dBm [11].

1.2.2 Cross-modulation Distortion

If the receiver is in the presence of a strong continuous wave (CW) blocker near the receive band (for example, from a nearby AM broadcast) as well as an out-of-band
modulated jammer (for example, the full duplex Tx signal), due to the finite third-order intermodulation distortion of the receiver, the modulated jammer and CW signal cross-modulate creating in-band distortion as shown in Fig. 1.5. The input referred distortion power due to cross-modulation is given by

\[ PN_{cm} (dBm) = 2 (P_{jam} - F_{atten}) + (P_{cw} - F_{atten}) - 2IIP3, \]  

(1.2)

where \( P_{cw} \) is the power of the CW blocker [11].

The cross-modulation performance of the receiver is affected by the IIP3 performance of the LNA. The IIP3 performance of the CMOS LNA may be improved by using linearity enhancement techniques such as modified derivative superposition (MDS) method [12] or the active post distortion (APD) method [13]; however, limitations in the down-converter generally require further off-chip filtering.

### 1.2.3 Reciprocal Mixing of Down-converter Phase Noise and Jammer

The down-converting reference oscillator (LO) will have a corresponding phase noise. An out-of-band jammer will mix with the LO phase noise at the jammer frequency offset creating noise at DC overlapping the desired signal as shown in Fig. 1.6. The input referred noise power due to reciprocal mixing of a jammer and LO phase noise is given by

\[ PN_{rpmix} (dBm) = (P_{jam} - F_{atten}) + PN_{osc} (\Delta f_{jam-LO}) + 10\log (BW), \]  

(1.3)

where \( PN_{osc} (\Delta f_{jam-LO}) \) is the down-converting oscillator phase noise at the jammer offset, and \( BW \) is the signal bandwidth.
Figure 1.4: Mechanism of desensitization through receiver IIP2 and modulated jammer.
Figure 1.5: Mechanism of desensitization through receiver IIP3 and modulated jammer with CW.
Figure 1.6: Mechanism of desensitization through receiver LO phase noise and jammer.
1.2.4 Receiver Sensitivity Calculation

The total input referred noise power, which limits the receiver sensitivity, is given by

\[ PN_{\text{sensitivity}} \ (dBm) = 10 \log \left( 10^{PN_{th}/10} + 10^{PN_a/10} \\
+ 10^{PN_{cm}/10} \\
+ 10^{PN_{md2}/10} \\
+ 10^{PN_{rpmix}/10} \right), \quad (1.4) \]

where \( PN_{th} \) is the thermal noise floor power given by \( 10 \log (KTB10^3) \), and \( PN_a \) is the added receiver noise power given by \( 10 \log (KTF10^3) \) (where \( F \) is the receiver NF).

A typical cellular receiver jammer handling specification, as an example, is the GSM out-of-band jammer tolerance requirement of 0 dBm. Using (1.4) and given typical receiver specifications of NF = 5 dB, IIP2 = +50 dBm, and oscillator phase noise of -162 dBc/Hz at the jammer offset, a front-end out-of-band filtering of at least +30 dB is needed to meet a receiver sensitivity of -90 dBm.

1.3 Broadband Tunable Filter: The N-path Filter

Recently, due to the rapid development of CMOS technology, the N-path filter, a technique known since the 1960’s [14, 15], has been investigated as a potential front-end filtering solution replacing the multiple off-chip filters (Fig. 1.7(a)) with a single tunable filter (Fig. 1.7(b)). The N-path filter utilizes a passive mixer to translate a baseband impedance to the mixer switching frequency, creating a broadband tunable, highly linear filter [4].

The intuitive operation of the N-path filter is shown in Fig. 1.8. A passive mixer down-converts an input current with a desired signal near the switching frequency \( (F_{RF} \approx F_{LO}) \) and an out-of-band jammer far from the desired signal to baseband. The input current is mixed down to baseband in which the down-converted current is applied to a low-pass impedance. The desired signal down-converted current will see a high impedance and will generate a baseband voltage component related to the desired input signal current. However, the down-converted out-of-band jammer will see a low
impedance and will not create a voltage component related to the out-of-band jammer. The baseband desired signal voltage is then translated to the input of the passive mixer creating a desired signal voltage. The overall effect of the mixing operation of the N-path filter is that the baseband impedance is translated to the switching frequency at the input of the mixer creating a broadband tunable filter when placed in shunt to the input of a broadband LNA.

A single-ended N-path filter driven by N-phase non-overlapping clocks \((LO_i (t) - LO_N (t))\) is shown in Fig. 1.9. The time domain input current is down-converted (multiplied) by the time domain clock \((LO (t)_i\) with \(i = 1 \text{ to } N\) creating a baseband current \(I_{BB} (t)_i\). The baseband current is then filtered by the complex baseband impedance by convolving the time domain signal of \(Z_{BB} (t)\) with \(I_{BB} (t)_i\), creating a baseband voltage \(V_{BB} (t)_i\). Finally, the baseband voltage is then up-converted creating an input voltage component given by

\[
V_{RF} (t) = \sum_{i=1}^{N} LO_i (t) \cdot \{ [LO_i (t) \cdot I_{RF} (t)] \ast Z_{BB} (t) \},
\]

where \(N\) is the number of phases of the clock, \(LO_i\) is the \(i^{th}\) clock out of \(N\) total, and \(Z_{BB}\) is the baseband impedance. The time domain input voltage expression can be converted to the frequency domain giving

\[
V_{RF} (\omega) = N \sum_{m=-\infty}^{\infty} \sum_{n=-\infty}^{\infty} a_n a_m I_{RF} (\omega - (n + m) \omega_{LO}) \cdot Z_{BB} (\omega - n\omega_{LO}),
\]

where \(|a_n| = |\sin (n \pi / N) / (n\pi)|\) is the magnitude of the Fourier coefficient for a non-overlapping clock (period \(T\) and pulse width of \(T/N\)) [4], \(\omega_{LO}\) is the clock frequency, and \((n + m) = kN\) where \(k\) is an integer.

The single-ended N-path filter’s input impedance \(Z_{in} (\omega)\), assuming an infinite source port impedance, is given by [4]

\[
Z_{in} (\omega) = R_{on} + N \sum_{n=-\infty}^{+\infty} |a_n|^2 Z_{bb} (\omega - n\omega_{LO}).
\]

From (1.7), the N-path filter translates a baseband impedance to harmonics of the clock switching frequency. With the baseband impedance equivalent to a low-pass parallel RC, the N-path filter creates a high-Q, center frequency tunable band-pass filter.
From (1.6), spectrum located near harmonics of the clock can fold into the desired band, termed “harmonic folding”. More specifically, according to (1.6), the nearest folding frequency to $\omega_{LO}$ is given by $(N - 1) F_{LO}$. Additionally, according to (1.7), the baseband impedance is up-converted to harmonics of the clock with magnitude scaled by a sinc function termed “harmonic replicas”. The harmonic folding and harmonic replicas are illustrated in Fig. 1.10 [4] and may be problematic for broadband applications. Multi-phase N-path filters help alleviate harmonic folding [4, 16–18]. However, the multiphase clock generation limits the maximum frequency of operation since a higher number of phases requires the digital logic, which may be limited by the process technology, to operate at a higher frequency.

In the last few years, significant progress has been made implementing the N-path filter. For full duplex, a baseband N-path notch filter to reject the down-converted out-of-band jammer was designed in [5]. For fixed band GSM, a 4-phase N-path band-pass filter before and after the LNA was presented in [6] with an on-chip narrow-band balun to provide filtering of harmonic folding. Multi-phase N-path filters alleviate harmonic folding and have become popular for broadband tunable designs [4, 16–18]. Active higher order gyrator based N-path filters have been known since the 1970’s [19, 20] and revitalized recently in [7, 21] for RF front-end applications.
Figure 1.7: Front-end filtering methods: (a) Multiple off-chip SAW filter approach. (b) Tunable filter approach [3].
Figure 1.8: Operation of the N-path filter translating the baseband impedance to the input at the switching frequency.
Figure 1.9: Single-ended N-path filter.
Figure 1.10: Frequency translation of baseband impedance and harmonic folding (with $M = N$ phases) from [4].
1.3.1 Baseband Notch Filtering

One of the first implementations of N-path filtering for SAW-less full duplex transceivers was presented in [5] to remove the down-converted TX jammer that may compress the baseband amplifiers as depicted in Fig. 1.11(a). A DC notch is created by the input impedance of a transimpedance amplifier (TIA) as in Fig. 1.11(b) and placed as the baseband impedance of an N-path filter, creating an up-converted impedance notch at the N-path filter switching frequency. The N-path filter with baseband TIA is placed in a full duplex direct-conversion receiver preceding the baseband TIA to create a “sink” at the down-converted TX frequency (Fig. 1.12(c)). The schematic implementation of the full receiver is shown in Fig. 1.12(d). The receiver was fabricated in a 0.18μm CMOS technology and improved the triple beat and IIP2 performance each by 6.5 dB. The limiting factor of out-of-band jammer power handling of this approach is the front-end LNA which experiences no on-chip filtering. Moreover, the design is not suitable for multi-band coverage as there is no front-end tunable filter.

1.3.2 A GSM Receiver with N-path Filtering

The first published SAW-less receiver intended for fixed-band GSM was presented in [6]. To improve the LNA compression meeting the 0 dBm out-of-band jammer specification of GSM, a band-pass N-path filter is placed before and after an LNA as shown in Fig. 1.13. A narrow-band balun is designed on chip to interface with the antenna and differential LNA while alleviating harmonic folding of the input signal at harmonics of the N-path filter clock into the desired band (described in the following section). The chip was fabricated in a 65 nm CMOS technology and achieves an out-of-band blocker NF less than +12 dB with a 0 dBm jammer (below the +15 dB 3GPP limit). The limitations with this approach are the fixed frequency, limited rejection provided by the filtering, and filter order roll-off.
Figure 1.11: (a) Saw-less receiver mixer linearity degradation due to TX leakage [5]. (b) An active sink consisting of a passive mixer and TIA [5].
Figure 1.12: (c) Sink in a direct-conversion receiver [5]. (d) Schematic implementation [5].
Figure 1.13: (a) High Q band-pass N-path filter implemented with MOS switches (N = 4) [6]. (b) Fixed band receiver with front end N-path filters [6].
1.3.3 Active N-path Filtering

A traditional N-path filter with a baseband low-pass capacitive load translates the first-order baseband impedance to a 2\textsuperscript{nd} order band-pass at the filter’s input/output with limited out-of-band rejection roll-off. Active higher order gyrator based N-path filters have been known since the 1970’s [19, 20] and recently revitalized in [7, 21] for RF front-end applications. The gyrator allows for multiple N-path filters to be cascaded. Additionally, an effective series inductance and capacitance is created between the cascaded N-path filter stages, creating a higher order filter (illustrated in Fig. 1.14). A 6\textsuperscript{th} order band-pass filter with two resonators separated by a series LC is shown in Fig. 1.14(a). Due to the excessive size of the series resonating inductor, an active series LC may be created using two shunt resonators and a gyrator as shown in Fig. 1.14(b). In Fig. 1.14(c), the 6\textsuperscript{th} order band-pass filter of 1.14(a) is implemented with the active gyrator series LC and the shunt LC resonators are replaced by the switched capacitor counterpart in Fig. 1.14(d).

In [7], the 6\textsuperscript{th} order band-pass filter was implemented in a 65 nm CMOS technology achieving a 0.1-to-1.2 GHz tuning range, +7 dBm P1dB blocker ($\Delta f = 50$ MHz) compression, and 59 dB out-of-band rejection. The limitation of the active gyrator approach is the compression of the active amplifiers of the gyrator. The power consumption and noise performance of the gyrators is similar to a resistive feedback LNA which is a strong function of the device transconductance ($g_m$). Recent active higher order gyrator N-path filters have demonstrated NF’s less than 3 dB [7].
Figure 1.14: (a) A $6^{th}$ order LC BPF [7]. (b) Two gyrators to synthesize a series LC [7]. (c) Substitution of the series active gyrator [7]. (d) Implementation using the switched capacitor N-path counterpart [7].
1.3.4 Summary of N-path Filter Limitations

The core of the traditional N-path filter is a passive mixer that suffers from the common ailments of direct-conversion receivers. The following is a brief overview of the common issues of the traditional N-path filter. An N-path filter suffers from an in-band signal image that is common in frequency mixers and requires a quadrature mixer [22]. Figure 1.15(a) illustrates the issue of the signal image folding on top of the desired signal. Figure 1.15(b) illustrates the issue of harmonic folding of spectrum at harmonics of the driving clock into the desired band. Harmonic folding may be alleviated by increasing the number of clock phases with the nearest folding frequency given by \((N-1)\ \text{LO}\) as previously described. Figure 1.15(c) illustrates a modulated out-of-band jammer corrupting the in-band desired signal through second-order distortion and follows the trend of (1.1). Second-order distortion may be alleviated by using differential architectures as well as symmetrical layout techniques. Figure 1.16(d) illustrates the issue of multiple harmonic passbands, in-band insertion loss, and limited out-of-band rejection.

This dissertation presents a transmission line N-path filter technique in Chapter 2 that improves the fundamental trade-off between out-of-band rejection and in-band insertion loss of the traditional N-path filter. Figure 1.16(e) illustrates the clock feed-through issue of the traditional N-path filter that appears at the center of the desired band. Chapter 3 presents a pseudo-random N-path filter clocking technique that alleviates clock feed-through. Figure 1.16(f) illustrates the issue of third-order distortion of an in-band signal due to the non-linear channel ON resistance. Figure 1.17(g) illustrates the issue of reciprocal mixing of an out-of-band jammer and the phase noise of the reference oscillator into the desired band. The reciprocal mixing of the N-path filter follows (1.3) as previously described.
Figure 1.15: Limitations (a) Signal image folding. (b) Harmonic folding of spectrum into desired band. (c) Modulated jammer and second-order distortion corrupting the in-band signal.
Figure 1.16: Limitations cont. (d) Harmonic passbands, insertion loss, and limited out-of-band rejection. (e) Issue of clock feed-through. (f) Finite third-order linearity.
Figure 1.17: Limitations cont. (g) Reciprocal mixing of phase noise and out-of-band jammer.
1.4 Summary

This chapter gave a brief overview of the history and current state-of-the-art of N-path filtering for receiver RF-front-end filtering. The N-path filter’s characteristics such as impedance translation, harmonic folding, limited rejection and filter order, and compression of active designs were covered. This dissertation next presents a passive transmission line N-path filter approach that ideally improves insertion loss and out-of-band rejection. Secondly, a pseudorandom clocking scheme is presented that reduces the spurious LO leakage. Third, an implementation of a N-path filter in GaN technology to improve jammer power handling is presented. Finally, a broadband signal classification receiver application is presented that takes advantage of N-path front-end filtering techniques.

Chapter 2 reviews the fundamental limitations of the traditional N-path filter in terms of insertion loss and out-of-band rejection. A transmission line N-path filter technique is analyzed that ideally improves the in-band insertion loss and out-of-band rejection. Two designs were implemented in a 65 nm CMOS technology (one with and without a broadband LNA). The design achieves broadband tuning from 0.1-to-1.6 GHz, less than 5 dB insertion loss across the tuning range, 30 dB to 50 dB out-of-band rejection, in-band IIP3 of +29 dBm, and a +11 dBm IP1dB out-of-band jammer tolerance.

Chapter 3 reviews the issue of clock feed-through and spurious emissions of the N-path filter. A pseudorandom clocking scheme is shown that reduces the spurious LO leakage and the theory of its operation discussed. A design was fabricated in a 65 nm CMOS technology that achieves a tuning range of 0.1-to-1.4 GHz and 10-to-15 dB LO spurious leakage improvement at a magnitude of -60 to -80 dBm.

Chapter 4 reviews the compression limitations of conventional CMOS technology. A first implementation of a GaN N-path filter is shown implemented in a 400 nm Cree GaN HEMPT technology. The design achieves a tuning range of 50-to-300 MHz, in-band P1dB of +10 dBm, in-band IIP3 of +24.6 dBm, and a IP1dB out-of-band jammer tolerance of +17 dBm.

Chapter 5 presents measurement results of a 1-to-16 baseband channelizer for an application of a broadband signal separation and classification receiver.
Chapter 6 summarizes the dissertation and outlines future research possibilities.
Chapter 2

The Transmission Line N-path Filter

2.1 Introduction

The traditional N-path filter’s (Fig. 2.1) high-frequency performance is limited by the switch shunt parasitic capacitance, which increases the in-band insertion loss, and the switch resistance, which limits the out-of-band rejection. Additionally, the traditional passive N-path filter’s transfer function is generally limited to two poles, reducing the filter’s effectiveness for spectrally near-by jammers. Moreover, the switch parasitic capacitance creates a frequency offset, shifting the peak band-pass response to a lower frequency [23]. Recent work has demonstrated higher order active gyrator N-path filter approaches [7, 21]; however, due to the active nature of the designs, the power handling is still limited by the compression of the gyrators composed of resistive feedback amplifiers.

This chapter presents the analysis and design of an improved transmission line N-path filter (T-line N-path filter) approach, which absorbs the shunt switch parasitic capacitance of the N-path filter into a synthetic transmission line, reducing in-band insertion loss and increasing out-of-band rejection through further out-of-band low-pass filtering [3, 8]. The in-band P1dB compression, in-band IIP3, and out-of-band jammer P1dB blocker tolerance are all improved compared to previous active approaches, while ideally improving insertion loss and providing higher order out-of-band rejection. First, the background and fundamental limitations of the traditional N-path filter are reviewed. The following section then introduces the T-line N-path filter and derives the defining
filter characteristics. Finally, measurement results of a T-line N-path filter fabricated in a 65 nm CMOS process are presented and conclusions are drawn.

2.2 Limitations of the Traditional N-path Filter

2.2.1 Traditional N-path Filter Approaches

A single-ended band-pass N-path filter driven by N-phase non-overlapping clocks is shown in Fig. 2.1(a) with port impedances \( R_s \) and \( R_L \), baseband impedance \( Z_{bb}(\omega) \), shunt parasitic capacitance \( C_{par} \), and switch resistance \( R_{on} \). The input impedance \( Z_{in}(\omega) \), assuming an infinite source impedance (\( R_s = \infty \)) and neglecting parasitic capacitance, is [4]

\[
Z_{in}(\omega) = R_{on} + N \sum_{n=-\infty}^{+\infty} |a_n|^2 Z_{bb}(\omega - n\omega_{LO}),
\]

(2.1)

where \( N \) is the number of clock phases, \( |a_n| = \left| \sin \left( \frac{n\pi}{N} \right) / (n\pi) \right| \) is the magnitude of the Fourier coefficient for a non-overlapping clock (period \( T \) and pulse width of \( T/N \)) [4], and \( \omega_{LO} \) is the clock frequency. With \( Z_{bb}(\omega) = 1/(j\omega C_{bb}) \), the transfer function of the circuit of Fig. 2.1(a) is a tunable band-pass filter, with poles located near integer multiples of \( \omega_{LO} \) and a 3 dB BW of approximately \( 2/(C_{bb}NR_s) \).

An approximate Linear Time Invariant (LTI) lumped-element model of the filter at frequencies near \( \omega_{LO} \) is shown in Fig. 2.1(b), where

\[
L_{res} \approx N |a_1|^2 / \left( C_{bb}\omega_{LO}^2 \right),
\]

(2.2)

and

\[
C_{res} \approx C_{bb} / \left( N |a_1|^2 \right)
\]

(2.3)

similar to [24]. A shunt impedance \( Z_{sh} \) is added to model the loss of the input signal that is up-converted to harmonics of the clock and dissipated at the port impedance, \( Z_p \), as described in [25–28] (Fig. 2.1(b) and Fig. 2.1(d)). In [28], \( Z_{sh} \) is given by

\[
Z_{sh} (\omega_o + \Delta\omega) = \left( \sum_{g=-\infty}^{\infty} \frac{|a_{(1-gN)}|^2}{|a_1|^2} \cdot \frac{1}{Z_p((1-gN)\omega_o + \Delta\omega)} \right)^{-1},
\]

(2.4)
where \( Z_p = R_s \parallel R_L \parallel (1/sNC_{\text{par}}) + R_{\text{on}} \) and \( Z_{\text{sh}} \) is evaluated at a frequency offset \( \Delta \omega \). When the port impedance \( Z_p \) is purely real, \( Z_{\text{sh}} \) reduces to

\[
Z_{\text{sh}} = R_{\text{sh}} = (R_a + R_{\text{on}}) \left\{ \frac{\text{sinc}^2 \left( \frac{\pi}{N} \right)}{1 - \text{sinc}^2 \left( \frac{\pi}{N} \right)} \right\},
\]

(2.5)

where \( R_a = R_s \parallel R_L \) [27]. More exact expressions are given in [24]. The lumped equivalent circuit model is limited, since periodic harmonic replicas, frequency folding, and finite source impedance effects are not modeled. A transmission-line-based model that models the periodicity of the N-path filter at harmonics of \( \omega_{\text{LO}} \) is given in [29, 30]. A higher-order Linear Time Variant (LTV) state-space analysis, which takes into account memory effects, similar to [24], is required to model a reactive source impedance. Recently, the filter transfer function using second-order state-space analysis of a single shunt N-path filter, which assumes a source inductance, has been derived in [31]. The various equivalent circuit models for the N-path filter trade off model complexity with accuracy.
Figure 2.1: "Shunt switch" N-path architecture (a) with lumped approximation (b) and "series switch" N-path architecture (c) with lumped approximation (d).
2.2.2 Trade-off Between Insertion Loss and Out-of-band Rejection

There are two implementations of the traditional N-path band-pass filter: a “shunt” and a “series” architecture. Fig. 2.1(a) illustrates the shunt band-pass filter architecture, where the peak in-band gain near $\omega_{LO}$ (from the model of Fig. 2.1(b)) is

$$s_{21}^{\text{peak sh}}(s) \approx \frac{G_{o \text{ sh}}}{1 + \frac{s}{\omega_{p1 \text{ sh}}}}$$

(2.6)

where

$$G_{o \text{ sh}} = \frac{2}{R_s / (R_{on} + Z_{sh}) + 2}$$

(2.7)

$$\omega_{p1 \text{ sh}} = \frac{R_s / (R_{on} + Z_{sh}) + 2}{NC_{par} R_s}$$

(2.8)

and assuming $R_s = R_L$. The out-of-band gain of the shunt filter architecture, which is ideally zero, is limited to approximately $s_{21}^{\text{out-of-band sh}}(s) \approx 2R_{on}/R_s$.

Fig. 2.1(c) illustrates the series filter architecture. The peak in-band gain (from the model of Fig. 2.1(d)) is

$$s_{21}^{\text{peak ser}}(s) \approx \frac{G_{o \text{ ser}}}{1 + \frac{s}{\omega_{p1 \text{ ser}}}(1 + \frac{s}{\omega_{p2 \text{ ser}}})}$$

(2.9)

where

$$G_{o \text{ ser}} = \left(1 + \frac{R_{on} / R_s}{1 + R_{on} / Z_{sh}}\right)\left(1 + \frac{R_{on} / Z_{sh} + R_s / Z_{sh}}{NC_{par} R_s (1 + R_{on} / Z_{sh})}\right)$$

(2.10)

$$\omega_{p1 \text{ ser}} = \frac{1 + R_{on} / Z_{sh} + R_s / Z_{sh}}{NC_{par} R_s (1 + R_{on} / Z_{sh})}$$

(2.11)

$$\omega_{p2 \text{ ser}} = \frac{1 + R_{on} / R_s}{NC_{par} R_{on}^2}$$

(2.12)

and $Z_p = R_s || (1/sNC_{par}) + R_{on}$ to calculate $Z_{sh}$ from (2.4). For $Z_{sh}$ approaching infinity, $\omega_{p1}$ of the series architecture (2.11) is a factor of two lower than the shunt architecture (2.8) leading to increased insertion loss at higher frequency. By contrast, the out-of-band gain of the series architecture approaches zero at high frequency (Fig. 2.1(d)).

A comparison of simulation and calculation results of the in-band insertion loss and out-of-band rejection as a function of transistor switch width is shown in Fig. 2.2 and Fig. 2.3, respectively. The in-band insertion loss of the shunt architecture is superior to that of the series architecture due to the series architecture’s in-path series switch.
resistance and double the device parasitics. Conversely, the out-of-band rejection of the series architecture is superior, since the switch resistance is not in series with the baseband capacitance (or, equivalently, not in series with the shunt resonator as depicted in Fig. 2.1(d)). Considering the shunt architecture, the out-of-band rejection may be improved by increasing the device width; however, the in-band insertion loss will, correspondingly, increase due to increased parasitics. The simulation highlights the fundamental limitation of the traditional N-path filter - optimization of the high frequency out-of-band rejection and in-band insertion loss is in conflict.
Figure 2.2: Simulated (black) and calculated (dashed gray) filter in-band insertion loss as a function of transistor width (LO = 2 GHz, N = 8, $C_{bb} = 20$ pF, $R_s = 50$ Ω, $L_g = 65$ nm).
Figure 2.3: Simulated (black) and calculated (dashed gray) filter out-of-band rejection as a function of transistor width at a 1 GHz offset (LO = 2 GHz, N = 8, $C_{bb} = 20$ pF, $R_s = 50$ Ω, $L_g = 65$ nm).
2.2.3 Pass-band Frequency Shift due to Parasitic Capacitance

The switch parasitic capacitance of the N-path filter also shifts the center $\omega_o$ of the pass-band to a lower frequency [32]. From Fig. 2.4, the frequency of the peak of the pass-band is

$$\omega_o \approx \frac{1}{\sqrt{L_{res} (C_{res} + NC_{par})}} = \frac{1}{\sqrt{\frac{C_{par}^N |a_1|^2 + C_{bb}}{C_{bb} \omega_{LO}^2}}}. \tag{2.13}$$

Equation (2.13) predicts that as $C_{par}$ increases, the peak will shift to a lower frequency. Moreover, from (2.13), increasing $C_{bb}$ minimizes the effect of the parasitic capacitance with a resulting decreased bandwidth and increased chip area. More exact expressions for the peak shift in frequency that include complex source impedance harmonic folding are given in [32].

The simulated shunt band-pass architecture transfer function for differing device widths is shown in Fig. 2.4, and a comparison of the offset between the shunt and series architectures is shown in Fig. 2.5. As expected, the frequency shift of the series architecture is larger than the shunt architecture due to approximately twice the parasitic capacitance (Fig. 2.5). For narrow-band applications, the frequency offset may be problematic (Fig. 2.4).

The traditional N-path filter’s high frequency performance is limited by its insertion loss and out-of-band rejection in which the optimization of both metrics is in conflict. Moreover, the parasitic capacitance creates an undesired frequency shift limiting narrow-band performance. While process scaling may improve the performance by reduced parasitic capacitance and lower device switch resistance, the aggressively scaled device break-down limits the switch gate clock voltage swing, limiting jammer power handling capabilities due to device compression. An approach that ideally removes the trade-off between insertion loss and out-of-band rejection is desired.
Figure 2.4: Simulated frequency response of a shunt band-pass N-path filter, illustrating the effect of switch parasitics on center frequency shift and insertion loss (LO = 2 GHz, N = 8, $C_{bb} = 20$ pF, $R_s = 50$ Ω, $L_g = 65$ nm).
Figure 2.5: Simulated band center offset from $f_{LO}$ as a function of transistor width (LO = 2 GHz, $N = 8$, $C_{bb} = 20$ pF, $R_s = 50$ Ω, $L_g = 65$ nm).
2.3 Distributed Transmission Line N-path Filter

To improve the high-frequency performance, the switch parasitic capacitance of the N-path filter can be incorporated into a synthetic transmission line, broad-banding the filter response significantly [3, 8]. The distributed transmission line N-path filter is shown in Fig. 2.6. The total inductance $L$, may be chosen to provide a characteristic impedance of $R_s = \sqrt{L/(NC_{par})}$ with each inductor of value $L/K$ and the resulting transmission line cut-off frequency is $f_c \approx K/(\pi \sqrt{L/(NC_{par})})$, where $K$ is the total number of stages as shown in Fig. 2.6. The improvement in in-band insertion loss, out-of-band rejection, noise analysis, and parasitic effects are analyzed in the following sections.

2.3.1 In-band Insertion Loss and Poles of the T-Line N-path

To model the behavior of the T-line N-path filter, the following derivations use a lumped equivalent-circuit model using (2.2-2.5). The model includes device parasitic capacitance ($C_{par}$), the resistive losses of the T-line inductor due to the finite $Q$ ($R_{ind}$), self-resonance parasitic capacitance of the T-line inductance ($C_{self-res}$), equivalent N-path filter resonant tank ($C_{res}(K)$ and $L_{res}(K)$ are a function of $K$ to maintain a constant bandwidth), and shunt resistor ($R_{sh}$) to model the harmonic losses [25–28], and is shown in Fig. 2.7.

Unlike a traditional N-path filter, the in-band insertion loss of the T-line N-path filter is ideally independent of $C_{par}$ assuming the parasitic capacitance is absorbed into the synthetic transmission line. The limiting factors contributing to the in-band insertion loss are then the finite $Q$ of the transmission line inductors and harmonic losses $R_{sh}$. The simulated in-band gain of a T-line N-path filter for differing number of stages, $K$, is shown in Fig. 2.8, demonstrating that the in-band insertion loss and frequency offset are significantly improved. Furthermore, additional poles arise near the pass-band when $K > 1$, as described below.

The additional poles arise from examining a simplified PI section from Fig. 2.7 (shunt $L_{res}C_{res}$, series transmission line $L$, and shunt $L_{res}C_{res}$). The voltage gain transfer function of the section then has four complex poles and two corresponding natural
frequencies,

\[ \omega_0 = \frac{1}{\sqrt{C_{\text{res}} L_{\text{res}}}} = \omega_{LO}, \]  

(2.14)

and a new natural frequency

\[ \omega_n = \omega_{LO} \cdot \sqrt{1 + \frac{2}{L} \left( \frac{N |a_1|^2}{C_{bb} \omega_{LO}^2} \right)}. \]  

(2.15)

A comparison of a simulation of Fig. 2.8 (neglecting inductor finite Q and self-resonance) and T-line N-path filter is shown in Fig. 2.9. The lumped equivalent model simulation and calculation (2.16) matches the T-line N-path filter simulation well. The \( \omega_n \) approaches \( \omega_{LO} \) as \( \omega_{LO} \) increases (2.15), as illustrated in Fig. 2.9.

The voltage gain of the T-line N-path filter, using Fig. 2.7, neglecting the inductor losses and parasitics, is given by

\[ A_v(s) = \frac{4N^K |a_1|^2 K^{(2K+1)} R_s s^{2K+1}}{C_{bb} L^{(K+1)} s^{(2K+2)} + 4C_{bb} KL^K R_s s^{(2K+1)} + \ldots}. \]  

(2.16)
Figure 2.6: Transmission line N-path filter with $K$ N-path stages [3, 8].
Figure 2.7: T-line filter equivalent circuit with \( K \) N-path stages.
Figure 2.8: Simulated insertion loss improvement of T-Line N-path for differing values of K with comparison to original N-path (LO = 2 GHz, N = 8, $C_{bb} = 60$ pF, $R_s = 50$ Ω, $L = 5.2$ nH, $W = 400$ µm, $L_g = 65$ nm, device $NC_{par} \approx 2$ pF).
Figure 2.9: Comparison between lumped model and simulated T-Line N-path filter with \( K = 2 \) (\( N = 8 \), \( W/K = 200\mu m \), \( L_g = 65\text{nm} \), \( C/K = 30\text{pF} \) and \( L/2K = 1.3\text{nH} \)). PI model assumes \( K\text{Ron} = 3.6\ \Omega \), \( NC_{\text{par}}/K = 2\text{pF} \), and \( R_s = 50\ \Omega \).
2.3.2 Out-of-Band Rejection of T-Line N-path

The out-of-band gain can be derived assuming $K$ cascade “T” transmission line sections (where a “T” section is a series inductor $L/2K$, shunt out-of-band resistance $KR_{on}$, and series inductor $L/2K$) and is approximated at high frequencies by

$$s_{21\,out-of-band}(s) \approx \frac{8R_s K^{(2K+1)} R_{on}^K}{s^{K+1} L^{K+1}} \cdot \frac{1}{(1 + s^{-1} L^{-1} (2K^2 R_{on} + 4KR_s)(2K + 1))}.$$  

(2.17)

At high frequencies $s_{21\,out-of-band}(s) \approx 8R_s K^{(2K+1)} R_{on}^K / (s^{K+1} L^{K+1})$, which is superior to a traditional N-path filter, whose out-of-band gain is given by $s_{21\,out-of-band}(s) \approx 2R_{on}/R_s$. In Fig. 2.11, the out-of-band rejection improvement is illustrated by plotting the transfer function of the lumped model (Fig. 2.10) along with simulations of the T-line and traditional N-path filter showing good agreement between model and simulation.
Figure 2.10: Out-of-band rejection model for T-line N-path filter.
Figure 2.11: Simulated $s_{21}$ as a function of LO frequency of four-stage ($K = 4$) transmission line N-path filter and single-stage traditional N-path filter ($N = 8$, $W/L = 320\mu m/65nm$, $C/K = 30$ pF and $L/2K = 3$ nH) [3]. Out-of-band rejection calculation (2.17) assumes $KR_{on} = 6$ Ω, $L/K = 3$ nH, and $R_s = 50$ Ω [3].
2.3.3 Insertion Loss Limitations of Finite Inductor Q

It has been shown in [32] that the transfer function of multiple cascaded shunt N-path filters is equivalent to a single shunt N-path filter. This allows for the simplification of Fig. 2.12(a) to Fig. 2.12(b) for calculation of the in-band insertion loss and NF. The transmission line inductor finite Q is the main contribution to the in-band insertion loss and a simplified expression for the loss near $\omega_{LO}$ is

$$s_{21_{in-band}} \approx \frac{8 R_s R_{sh}}{(R_{ind} + 2 R_s)(R_{ind} + 2 R_s + 4 R_{sh})}, \quad (2.18)$$

where $R_{sh}$ is given by (2.5) with $R_a = \frac{1}{2} R_s + \frac{1}{2} R_{ind}$ and $R_{ind} = \frac{\omega_o L}{Q}$. The in-band insertion loss versus transmission line Q is shown in Fig. 2.13 demonstrating that a minimum inductor Q of 8 is needed for insertion loss improvement with the T-line technique.

2.3.4 Noise Analysis

The main contributions to the NF of the T-line N-path filter are the Q of the inductors and harmonic losses (modeled as $R_{sh}$ assuming $R_{sh} >> R_{on}$). From the simplified model of Fig. 2.12(b), the NF can be derived as

$$F \approx 1 + \frac{R_{ind}}{R_s} + \frac{(R_s + \frac{1}{2} R_{ind})^2}{R_s R_{sh}}, \quad (2.19)$$

where $R_{sh}$ is given by (2.5). The simulated and calculated T-line N-path filter NF versus Q is plotted in Fig. 2.14 showing good agreement.
Figure 2.12: (a) T-line N-path filter with K stages. (b) Simplified diagram for insertion loss and noise analysis.
Figure 2.13: Simulated and calculated (2.18) insertion loss of T-Line N-path versus transmission line inductor Q (LO = 500 MHz, N = 8, $C_{bb} = 60$ pF, $R_s = 50$ Ω, $L = 5.2$ nH, $W = 400$ µm, $L_g = 65$ nm, device $N C_{par} \approx 2$ pF).
Figure 2.14: Simulated NF of T-Line N-path with ideal clock (LO = 500 MHz, K = 4, N = 8, L = 6 nH) versus Q. Calculation (2.19) with $K R_{on} = 5 \Omega$. 
2.3.5 Effect of Inductor Coupling

Due to the proximity of the inductors to each other, there will be mutual coupling as shown in Fig. 2.15(a). This can be modeled by an induced inductance ($L_m$) in series with each N-path filter stage as shown in Fig. 2.15(b). The induced inductance resonates with the input capacitive response of the frequency translated baseband impedance and parasitic capacitance, creating a transmission zero. The zero is given by

$$\omega_z \approx \sqrt{\frac{L_m C_{bb} \omega_{LO}^2 + N |a_1|^2}{L_m (C_{bb} + C_{par} N^2 |a_1|^2)}},$$

(2.20)

using (2.2), (2.3), and including a series $L_m$. A simulation highlighting this effect is shown with simplified schematic diagram in Fig. 2.16 with an infinite port impedance (to neglect port impedance memory effects and harmonic impedance folding for simplicity) and is shown in Fig. 2.17. The calculation is performed by using (2.1) and adding $j\omega L_M$ to $Z_{in}$. As can be seen by the simulation, a transmission zero appears compared to the N-path filter without induced series inductance.
Figure 2.15: (a) T-line N-path filter with coupling between inductors. (b) T-line N-path filter with effective induced inductance.
Figure 2.16: Simplified model for simulation of zero with infinite port impedance.
Figure 2.17: Simulated N-path filter with and without series induced inductance ($f_{LO} = 1$ GHz and 2 GHz, $K = 1$, $N = 8$, $L_{M1} = 500$ pH, $C_{bb}/K = 20$ pF, $W = 80$ um, $L_g = 65$ nm, $KR_{on} = 6.1$ Ω).
2.4 Implementation and Measurement Results

A four stage ($K = 4$) transmission line N-path filter was implemented in a 65 nm bulk CMOS process with schematic diagram shown in Fig. 2.18 and die photograph in Fig. 2.19. A single-ended design was chosen to facilitate broadband tuning without requiring a balun. Moreover, a single-ended design will exhibit even and odd harmonic pass-bands [4]. An $N = 8$ N-path filter will reject $3^{rd}$ and $5^{th}$ order harmonic folding, but will exhibit $7^{th}$ harmonic folding [4].

2.4.1 Clock Generation

A divide-by-four divider with clock re-timing creates the non-overlapping 8-phase clock for an $N = 8$ N-path filter [9]. At the input of the clock generation circuitry, a buffered differential LO input operating at four times the fundamental drives a digital latch based ring divider to produce a 50% duty cycle 8-phase clock (Fig. 2.20). For single-ended designs, the common-mode noise of the clock generation circuitry will appear directly at the input port of the filter [33] potentially limiting noise performance. To alleviate the noise degradation due to the digital divider, clock re-timing techniques were employed as in Fig. 2.21 similar to [9]. The 8-phase non-overlapping clock is created by $\text{ANDing}$ the appropriate outputs of the clock re-timing circuitry as shown in Fig. 2.22. Following the digital logic clock generation circuitry are large buffers to drive the 1 mm distance to each N-path filter stage with further buffering located at each filter stage.
Figure 2.18: T-line N-path filter schematic/layout with digital logic divider. \( K = 4 \) stages, \( N = 8 \) phases, \( L/2K = 2nH \), and \( C_{bb}/K = 20 \) pF.
Figure 2.19: Chip micrograph (3mm x 1.4mm).
Figure 2.20: Ring divider for 8-phase 50% duty cycle clock.
Figure 2.21: Clock re-timing for divider noise reduction [9].
Figure 2.22: Non-overlapping clock generation for N = 8 phases.
2.4.2 Measured S-parameters

The measured S-parameters are shown in Figs. 2.23-2.24. As shown in Fig. 2.23, with the filter OFF, the synthetic transmission line has a cut-off frequency of 1.44 GHz slightly limiting the insertion loss at higher tuning frequencies. The out-of-band rejection is improved compared to traditional shunt N-path filters whose single stage rejection is typically limited to approximately 15 dB. The input impedance ($s_{11}$) is well matched across the entire tuning range (Fig. 2.24).

The measured 2\textsuperscript{nd}, 3\textsuperscript{rd}, and 4\textsuperscript{th} harmonic pass-band responses of the T-line filter at LO = 500 MHz are 5.2 dB, 11.4 dB, and 22.3 dB respectively below the fundamental similar to [8].

2.4.3 Measured In-band Frequency Offset

The improvement in the center-band peak $S_{21}$ frequency offset is illustrated in Fig. 2.25 by comparing the measured offset from the center LO to a simulated N-path filter with the same total device size ($W = 320 \mu m$, $C_{bb} = 80 \text{ pF}$, and added routing/layout $C_{par} = 1 \text{ pF}$). The measured offset is less than 1.5 MHz across the entire tuning range shifted to the right side of the LO.

2.4.4 Measured Linearity and Jammer Compression

The measured in-band linearity at LO = 1 GHz is shown in Fig. 2.26. For both the in-band IIP3 and in-band IIP2, the input two tone spacing was chosen to be approximately 50 kHz at a 100 kHz offset from $\omega_{LO}$. For the out-of-band linearity measurement, the input two tones were placed in the region of highest rejection. The out-of-band IIP3 was measured to be +25 dBm with two input tones at $F_1 = 1.136$ GHz and $F_2 = 1.27$ GHz producing the intermodulation term in-band at 1.002 GHz. The out-of-band IIP2 was measured separately to be +37 dBm with two input tones at $F_1 = 1.201$ GHz and $F_2 = 1.2015$ GHz producing the intermodulation term at baseband at 500 kHz which is up-converted by the 1 GHz LO to in-band at 1.0005 GHz. The measured in-band gain compression (Fig. 2.27) with an out-of-band jammer at a 250 MHz offset is $P_{1dB_{jam}} = +11 \text{ dBm}$. 
2.4.5 Measured Noise Performance

The in-band NF versus LO frequency is shown in Fig. 2.28 and the performance is limited by the cut-off frequency of the transmission line. The measured near in-band output noise power is shown in Fig. 2.29 illustrating the effect of the LO phase noise limiting the NF performance below an approximately 50 kHz offset. The NF versus out-of-band jammer power was measured at LO = 1 GHz with an out-of-band jammer at 250 MHz offset and is shown in Fig. 2.30. The jammed NF shows a NF less than +15 dB with a jammer power of over +10 dBm.

The measured LO leakage at LO = 1 GHz is better than -60 dBm and in-band image rejection is measured to be better than 67 dBC. The harmonic folding rejection was measured at LO = 500 MHz with largest contribution to folding occurring at the 7th harmonic due to the choice of N = 8 (Fig. 2.31).
Figure 2.23: Measured $S_{21}$ with $f_{LO} = 100$ MHz to 1.6 GHz and transmission line cut-off frequency $\approx 1.44$ GHz.
Figure 2.24: Measured $S_{11}$ with $f_{LO} = 100$ MHz to 1.6 GHz.
Figure 2.25: Measured in-band peak $S_{21}$ frequency offset of T-Line N-path filter compared to simulated offset without transmission line inductance.
Figure 2.26: Measured input in-band P1dB gain compression of +0.5 dBm, in-band IIP3 ≈ +29 dBm, and in-band IIP2 ≈ +70 dBm at 1 GHz.
Figure 2.27: Measured in-band gain compression at LO = 1 GHz of +11 dBm with jammer at 250 MHz offset.
Figure 2.28: Measured filter NF with tuning of $f_{LO} = 100$ MHz to 1.6 GHz.
Figure 2.29: Measured in-band noise output power at LO = 1 GHz (RBW = 20 Hz). Pout noise 1 dB increase at 65 kHz offset.
Figure 2.30: Measured NF versus out-of-band jammer power at a 250 MHz offset with LO = 1 GHz.
Figure 2.31: Measured harmonic folding rejection with LO fundamental at 500 MHz.
Table 2.1: State of the Art Comparison

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2.5 T-Line N-path Filter with Broadband LNA

A second version of the T-line N-path filter was fabricated in the same 65 nm CMOS process including a broadband resistive feedback LNA to demonstrate the improvement of out-of-band jammer compression that may be obtained. The schematic for the T-line N-path filter including the broadband LNA is shown in Fig. 2.32. The input impedance of the resistive feedback LNA is given by

\[ Z_{in} \approx \frac{R_L + R_f}{1 + g_m R_L}, \]  

(2.21)

where \( R_L = 50\Omega \), and \( R_f \) and \( g_m \) are chosen to provide \( Z_{in} \) to be \( 50\Omega \). The NF of the broadband LNA is given by

\[ F \approx 1 + \frac{R_s}{R_f} + \left( \frac{1}{g_m R_s} \right) \left( \frac{R_s + R_f}{R_s R_f} \right)^2. \]  

(2.22)

As shown by (2.22), the NF of the LNA may be improved by choosing a large \( g_m \) and an appropriate \( R_f \) to provide broadband impedance matching. This choice of LNA architecture is advantageous for broadband and low noise applications in which power consumption is not as much of a concern. The chip die photograph is shown in Fig. 2.33.

The measured S-parameters are shown in Figs. 2.34-2.35. The second version design was fabricated with transmission line inductance 10-to-15 percent less than the first version without LNA. Due to this choice, the \( \omega_n \) is more evident at lower frequencies compared to the first version design, demonstrating the dependance of \( \omega_n \) on transmission line inductance (2.15). The design is well matched across the full tuning range.

The measured in-band linearity and in-band compression is shown in Fig. 2.36. The third-order distortion is limited by the CMOS LNA (LNA Gain = 16.2 dB at 1 GHz, P1dB = -12.3 dBm, and IIP3 = +3 dBm). The measured LNA gain compression with an out-of-band jammer with the filter ON and OFF is shown in Fig. 2.37. A 19 dB improvement in P1dB compression is achieved with out-of-band jammer P1dB of +7 dBm.

A single-ended design demonstrates broadband tuning without the added loss of a balun, while sacrificing common-mode noise performance and even order responses.
[33]. The measured NF is approximately 5-10 dB across the band limited by the LNA NF (2-4 dB across the band due to the cut-off frequency), by the common-mode clock noise [33], and by inductor loss at higher frequencies. The power consumption is limited by the clock driving buffers, which are connected to the K N-path filters (total of 50-200 mW with the LNA approximately 20 mW).
Figure 2.32: T-line N-path filter schematic with resistive feedback LNA.
Figure 2.33: T-line N-path filter with LNA in 65 nm CMOS (3.5mm x 1.5mm).
Figure 2.34: Measured $s_{21}$ sweeping the clock frequency from 300 MHz to 1.6 GHz.
Figure 2.35: Measured $s_{11}$ sweeping the clock frequency from 300 MHz to 1.6 GHz.
Figure 2.36: Measured filter/LNA in-band gain compression and in-band IIP3 at 1 GHz and tone spacing of 500 KHz. IIP3 ≈ +4.9 dBm.
Figure 2.37: Measured filter/LNA gain compression at 1 GHz with out-of-band jammer at 230 MHz offset (maximum out-of-band rejection).
2.6 Conclusions

A transmission line N-path filter technique is analyzed that improves the high-frequency performance of the traditional N-path filter. Ideally, the T-line N-path filter technique removes the trade-off between out-of-band rejection and in-band insertion loss of the traditional N-path filter by absorbing device parasitic capacitance into a synthetic transmission line, improving in-band insertion loss. Moreover, the out-of-band rejection is further improved by low-pass filtering created by the transmission line inductance and switch ON resistance. The limitations are then placed on the quality of the transmission line inductance. A practical limitation on the number of stages is the power consumption needed to drive the high speed switching clock signals to each filter stage across the distance of the transmission line. Equations were derived detailing the in-band poles, out-of-band rejection, and NF that match simulation well. Measurements demonstrate that the proposed filter exhibits an out-of-band rejection of approximately 50 dB, and jammer power handling capability of +11 dBm in a 65 nm bulk CMOS process.

2.7 Acknowledgments

The text of this chapter, in part or in full, is a reprint of the material as it appears in published papers or as it has been submitted for publication in IEEE Microwave Wireless Components Letters (MWCL) and IEEE Transactions on Microwave Theory and Techniques (TMTT). The dissertation author was the primary researcher and the first author listed in these publications.
Chapter 3

Pseudo-random Clocking LO Leakage Suppression N-path Filter

3.1 Motivation for LO Leakage Suppression

Recently, interest has been focused on the N-path filter’s ability to create a fully integrated high Q RF tunable bandpass response [4]. The N-path bandpass filter translates a baseband lowpass impedance to a reference clock frequency creating a tunable band-select filter. However, this architecture suffers from spurious emissions at the input and output that are harmonically related to the clock frequency. These undesired harmonic emissions may desensitize the receiver, or they may desensitize other nearby receivers operating in the same band or in other bands, as shown in Fig. 3.1.

This chapter presents a modification to the traditional N-path filter, allowing for pseudo-random clocking. The result is a lowering of the LO leakage in-band and spreading of the leakage noise out-of-band. The architecture demonstrates LO leakage improvement at the fundamental and harmonics while maintaining performance in insertion loss, out-of-band rejection, linearity, and tuning range.
3.2 Shunt N-path Filter LO Leakage Mechanism

A shunt-switch architecture N-path filter with a lowpass capacitive baseband load is shown in Fig. 3.2(a). In general, the N-path filter translates the baseband impedance \( Z_{BB} = 1/(j\omega C) \) to the mixer switching frequency, creating a tunable bandpass filter. Due to parasitic capacitance mismatches, the differential LO will feedthrough to the input and output creating spurious emissions at the fundamental and its harmonics (Fig. 3.2(b)). Furthermore, with single-ended designs, common-mode noise will also appear at the output, often having an up-converted flicker noise component from the clock generation circuitry [32]. The clock leakage current through the capacitor and the corresponding output voltage leakage component is directly proportional to frequency related by

\[
V_{\text{out Leakage}} \propto R_s \cdot \Delta C \cdot \omega.
\]

(3.1)

The property of direct proportionality of the clock leakage current through the parasitic capacitance and frequency will be utilized in the following proposed pseudo-random clocking technique.
Figure 3.1: Wideband receiver approach implemented with an N-path filter and resulting LO leakage [4].
Figure 3.2: (a) Single-ended shunt architecture N-path filter. (b) Mechanism for clock feed-through due to switch mismatch.
3.3 Pseudorandom LO N-path Filter

To reduce the LO leakage, a two-stage switching scheme is employed as illustrated in Fig. 3.3 similar to [35]. The first mixer at the input of the filter is clocked by a multiplication of a baseband duo-binary pseudo-random bit sequence (PN) and the LO. The second series mixer is clocked by the same PN sequence. Since \((LO \cdot PN) \cdot PN = LO\), the original filter transfer function is preserved while significantly reducing the periodic LO leakage. The resulting LO leakage is composed of two components: a broadband component (mostly out-of-band) whose spectrum is \((PN \cdot LO)_{\text{leak}}\) and a tonal component composed of \((PN \cdot LO) \cdot PN_{\text{leak}}\). Assuming a broadband purely random PN sequence, the first LO leakage term is minimize as the LO spectrum power is broadened. Additionally, assuming a low frequency PN sequence minimizing \(PN_{\text{leak}}\), the second LO leakage tonal component is minimized. In this way, the total clock feed-through may be minimized. The circuit schematic of the pseudo-random N-path filter is shown in Fig. 3.4 with corresponding waveforms in Fig. 3.5.

The clock generation to produce the \(PN \cdot LO\) signal may be generated by additional digital logic as shown in Fig. 3.6.

Optimization of the PN sequence spectral properties may be performed to further lower the in-band LO leakage. In particular, digital high-pass filtering of the PN sequence will lower the near DC spectral power of the PN sequence creating a spectral null when up-converted to the LO frequency \((PN \cdot LO)\). Digital high-pass filtering is performed in a simple way by passing the random PN bit sequence through an iterative high-pass difference equation \((1 - Z^{-1})\) with limiting at each iteration. The simulated spectrum of a high-pass filtered PN sequence multiplied by an \(LO \cdot (PN \cdot LO)\) is shown in Fig. 3.7 and Fig. 3.8 demonstrating the spreading.
Figure 3.3: Simplified operation of the pseudo-random clocking N-path filter.
Figure 3.4: Two stage N-path architecture for a bandpass filter employing a pseudorandom clocking scheme.
Figure 3.5: Clock waveforms for pseudorandom clocking scheme.
Figure 3.6: Additional digital logic for creating the PN sequence multiplied by the LO.
Figure 3.7: Simulation of a 32 MHz 1 Mbit high-pass filtered PN sequence.
Figure 3.8: Multiplication of PN by a 1.024 GHz LO.
3.4 Measurement Results

A single-ended shunt architecture pseudo-random LO N-path filter was implemented with 65 nm CMOS technology. The fabricated die was wire-bonded for chip-on-board PCB hybrid using ribbon bonds. A two-stage transmission line N-path filter [3] approach was implemented to improve out-of-band rejection. The multiphase clock for an N = 8 phase N-path filter was created by a digital ring divider and digital logic for multiplication with an off-chip PN sequence generator. High-pass shaping of a 15 MHz PN sequence is performed to further improve the in-band noise floor (as in Fig. 3.7).

The measured S-parameters are shown in Fig. 3.11. As demonstrated by Fig. 3.11, the PN sequence slightly degrades the in-band insertion loss and out-of-band rejection due to additional switching losses. The frequency tuning range is limited by the packaging and bondwire inductance. Improved out-of-band rejection may be obtained by additional cascaded transmission line stages [3] or by using a series architecture - at the expense of insertion loss [32].

The measured in-band LO leakage improvement across the tuning range is shown in Fig. 3.12. The LO leakage spectrum at 1 GHz is shown in Fig. 3.13 demonstrating the high-pass shaping of the PN sequence spreading the leakage power out-of-band.

The measured in-band P1dB compression and IIP3 at LO = 1 GHz is shown in Fig. 3.14. The measured in-band gain compression due to an out-of-band jammer at a 200 MHz offset is shown in Fig. 3.14. A comparison summary of the state-of-the-art is shown in Table 3.1.
Figure 3.9: Chip layout schematic block diagram.
Figure 3.10: Micrograph in 65 nm CMOS (1.1mm x 1.1mm).
Figure 3.11: Measured S21 response of tuning LO from 100 MHz to 1.4 GHz.
Figure 3.12: Measured LO leakage versus frequency with and without PN sequence.
Figure 3.13: Measured in-band LO leakage at 1 GHz with and without PN sequence (RBW = 200 KHz, Span = 40 MHz).
Figure 3.14: The measured in-band gain compression is $P_{1dB} \approx +0$ dBm, and in-band $IIP3 \approx +22$ dBm at LO = 1 GHz. The measured in-band gain compression with a jammer at a 200 MHz offset is $P_{1dB_{jammed}} \approx +11$ dBm.
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### 3.5 Conclusion

A shunt architecture N-path filter with pseudo-random clocking is presented to improve the LO leakage in-band and at the LO harmonics. A 10 to 15 dB improvement in LO leakage was demonstrated across the tuning range with minimal degradation in other filter metrics. Further measurement and theoretical analysis is planned to be submitted to *IEEE Transactions on Circuits and Systems*.

### 3.6 Acknowledgments

The text of this chapter, in part or in full, is a reprint of the material as it appears in published papers or as it has been submitted for publication in *Silicon Monolithic Integrated Circuits in RF Systems (SiRF)*. The dissertation author was the primary researcher and the first author listed in these publications. The authors wish to acknowledge Dr. Vincent Leung for his contributions as co-author.
Chapter 4

A GaN HEMT N-path Filter

4.1 Motivation for GaN N-path Filter

Coexistence and multi-band coverage of current generation communication systems in a hostile jamming environment has become increasingly problematic with the growing number of users and spectral over-crowding. An extreme case, for example, would be a sensitive receiver being jammed by nearby radar in which device survivability is even in question. Moreover, current generation communication systems often employ multiple off-chip SAW filters and switches for frequency selectivity of each band; however, these filters are large, costly, and frequency fixed.

Recent N-path filters have been implemented in scaled CMOS improving device parasitic insertion loss and out-of-band rejection. However, due to the reduced device feature size, the switch gate voltage swing is relatively low, limited by the device gate-to-source break-down voltage, and limits the resulting jammer power handling capability to the +7 to +10 dBm range [3, 21, 34].

A GaN HEMT-based N-path filter should exhibit a much higher power handling capability. This chapter covers a discrete N-path filter implemented in GaN HEMT technology, which demonstrates superior break-down characteristics, high $F_t$, and low device $R_{ON}$. 
4.2 GaN N-path Filter Design

The design implements a hybrid GaN FET series-switch architecture N-path filter with a lowpass capacitive baseband load (Fig. 4.1), which demonstrates superior out-of-band rejection compared to the shunt-switch approach [3-4]. By contrast, this series-switch approach results in higher insertion loss due to device parasitics and series switch resistance [1-3]. In general, the N-path filter translates the baseband impedance \( Z_{BB} = \frac{1}{jC_{BB}} \) to the mixer switching frequency, creating a tunable bandpass filter with poles located at integer multiples of \( \omega_{LO} \) and 3 dB BW of approximately \( 2/(C_{bb}N_{Rs}) \), neglecting parasitic capacitance and bond-wire inductance [1].

The switching waveforms are shown in Fig. 4.2. An out-of-band jammer is down-converted by the switch to a baseband frequency and then filtered, with a bandwidth determined by the \((C_{BB}N_{Rs})\) time constant. The filtered baseband voltage is then up-converted creating a bandpass filter centered at \( \omega_{LO} \) at the filter’s output. As long as the down-converted voltage, \( V_{bb} \), and corresponding swing, \( V_{bb-swing} \), is much smaller than the gate driving voltage swing, \( V_{gswing} \), the switch turns on and off providing filtering with minimal distortion. However, if the jammer power increases such that \( V_{gswing} \) is not sufficient to properly switch the device, then the passive mixer will compress and distortion will occur. The power handling capability will be roughly proportional to \((V_{gswing} - V_{th})^2 / |Z_{BB} (\Delta \omega_j)|\), where \( V_{th} \) is the device turn-on and \( Z_{bb} (\Delta \omega_j) \) is the base-band impedance at the jammer offset. GaN technology offers high break-down devices that can withstand large gate-to-source swing allowing increased \( V_{gswing} \) and, correspondingly, larger out-of-band jammer power handling.
Figure 4.1: Single-ended series architecture N-path filter implemented with GaN switches.
Figure 4.2: Voltage waveforms of one branch of the N-path filter.
4.3 Measurement Results

The series architecture N-path filter was implemented with 0.4 $\mu m$ GaN HEMT Cree bare die wire-bonded for chip-on-board PCB hybrid. The device has an $R_{on}$ of 1.6 $\Omega$, $V_{gs}$ break-down voltage swing of 12 V, and power gain up to 6 GHz. An $N = 2$ design was chosen for proof-of-concept, and higher values of $N$ in the future will improve in-band image issues, harmonic folding, and insertion loss [4]. A Hittite optical modulator (HMC870LC5) and single-to-differential broadband balun is used to create a differential rail-to-rail LO with 3 Vpk-pk swing as shown in Fig. 4.4.

The measured $S_{21}$ response is shown in Fig. 4.5. The measured filter transfer function matches the expected series N-path filter transfer function with out-of-band rejection approaching 50 dB.

The frequency tuning range is limited by the driving amplifier and bondwire inductance, and it is expected that fully monolithic GaN versions will be capable of GHz frequency performance. The high insertion loss is limited by the clock overlap and the Fourier coefficient conversion of a two-phase N-path filter, which creates a minimum loss of 7.8 dB in the $N = 2$ case (loss proportional to $10\log(sinc^2(\pi/N))$) [4]). Higher values of $N$ will have improved in-band insertion loss at the expense of clock driving complexity. The NF is measured to be proportional to the insertion loss and may be improved by increasing the number of phases [4].

The measured in-band $P_{1dB}$, in-band $IIP3$, and out-of-band jammer tolerance is shown in Fig. 4.6. In Fig. 4.7, the increase of jammer tolerance versus $V_g$ swing is illustrated. A comparison summary of the state-of-the-art is given in Table 4.1.
Figure 4.3: (a) Two phase GaN N-path filter PCB. (b) Implementation with Cree bare die with wire-bonded chip-on-board attachment.
Figure 4.4: Testing setup for GaN N-path filter driven by optical modulator.
Figure 4.5: Measured $S_{21}$ response of tuning LO from 50 MHz to 300 MHz.
Figure 4.6: Measured in-band IP1dB of +10dBm, in-band IIP3 of +24.6 dBm, and out-of-band jammer (at 50 MHz offset) P1dB compression of +17 dBm.
Figure 4.7: Measured in-band IP1dB out-of-band jammer tolerance versus LO Vg.
Table 4.1: State of the Art Comparison

<table>
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<th>This Work</th>
<th>[21]</th>
<th>[34]</th>
<th>[36]</th>
</tr>
</thead>
<tbody>
<tr>
<td>Technology</td>
<td>GaN 400 nm</td>
<td>CMOS 65 nm</td>
<td>CMOS 65 nm</td>
<td>CMOS 65 nm</td>
</tr>
<tr>
<td>Frequency Range</td>
<td>50-300 MHz</td>
<td>0.4-1.2 GHz</td>
<td>0.1-1.2 GHz</td>
<td>0.1-1.6 GHz</td>
</tr>
<tr>
<td>OOB Rejection</td>
<td>30-50 dB</td>
<td>+55 dB</td>
<td>+59 dB</td>
<td>30-50 dB</td>
</tr>
<tr>
<td>In-band IIP3</td>
<td>+24.6 dBm</td>
<td>+9 dBm</td>
<td>-12 dBm</td>
<td>+29 dBm</td>
</tr>
<tr>
<td>Jammer IP1dB</td>
<td>+17 dB</td>
<td>&lt;+2 dBm</td>
<td>+7 dBm</td>
<td>+11 dBm</td>
</tr>
</tbody>
</table>

4.4 Conclusions

A GaN HEMT two phase series architecture N-path filter demonstrates a tunable bandpass filter with +17 dBm out-of-band jammer tolerance. This work highlights the future potential of designing highly robust and broadband tunable filters in GaN technology.

4.5 Acknowledgments

The text of this chapter, in part or in full, is a reprint of the material as it appears in published papers or as it has been submitted for publication in IEEE Radio Wireless Symposium (RWS). The dissertation author was the primary researcher and the first author listed in these publications.
Chapter 5

Application: A Signal Separation and Classification Receiver

5.1 Introduction

Spectrum over-crowding has become a major concern considering the vast number of communication bands (cellular, industrial, commercial, TV, etc.) that operate with little coordination. To help alleviate this issue, a Cognitive Radio (CR) receiver identifies unused spectrum for potential use for communication improving spectrum utilization. Two key components of identifying unused spectrum are signal separation and classification. Signal separation is needed if the CR receives signals (whether jammers or desired signals) in which the signal sources are separately located and may overlap in frequency. Additionally, classification is needed to determine whether there exists communication already within the band of interest. A simplified illustration of a MIMO receiver separating and classifying separately located signal sources overlapping in frequency is shown in Fig. 5.1. Such a CR receiver is often referred to a “spectrum aware receiver” for its ability to determine the contents of the frequency spectrum.

Cognitive radio systems are faced with the challenge of sensing a wide instantaneous bandwidth (up to 50 MHz) to cover multiple standards over a broad frequency range. Such a broad frequency span renders the receiver susceptible to out-of-band jammers. An ideal candidate for a broadband tunable front-end filter to help alleviate
the jammer susceptibility of the CR receiver is the N-path filter previously discussed. This chapter gives an overview of a signal separation and classification receiver (“the CLASIC receiver”) architecture that is a suitable application for the front-end N-path filter. Moreover, this chapter discusses the system testing and measurement results of a baseband channelizer for use in conjunction with a signal separation architecture for the CLASIC receiver.
Figure 5.1: Signal separation and classification using MIMO antenna architecture.
5.2 The CLASIC Receiver

One approach toward a signal classification receiver is shown in Fig. 5.2, where $S_1-S_n$ are separately located signal sources which may overlap in frequency, $f_o$ is the desired frequency band for classification, $n$ is the number of desired signals to be separated and the number of antennas each with a RF down-converter, and $A_1-A_n$ and $\phi_1-\phi_n$ is the amplitude and phase profile of each linear combination of signal sources received by each antenna that is a function of the transmission channel. The receiver utilizes a spatial antenna array to create the amplitude and phase profile matrix of each received signal as a function of the spatial channel properties and antenna spacing. An RF front-end with tunable band-select N-path filtering for each antenna is employed to select the signal band of interest and down-converts the signal to baseband by a quadrature RF mixer. Using the down-converted linearly combined signal source matrix, a MIMO core (signal separation block) separates each signal source by multiplying the received source matrix with an inverse linear complex transform of the channel transmission characteristics. The coefficients of the complex transform of the channel are learned from feedback control from DSP. After each signal source is separated, classification can be performed in DSP by a neural network classifier.

Fig. 5.3 illustrates a modification of Fig. 5.2 architecture to provide parallel channel classification of the desired band of interest. Baseband channelization following the quadrature down-converter has two main advantages: higher resolution of the classified signals (instead of classifying the full instantaneous BW, the full BW can be classified in smaller channels in parallel), and lower operating speed of the subsequent signal separation and DSP blocks.
Figure 5.2: Signal separation and classification block diagram operating at a signal channel at $f_o$. 
Figure 5.3: Signal separation and classification block diagram operating using a baseband channelizer for parallel channel signal separation and classification.
5.3 System Testing of a 16-to-1 Channelizer

A channelizer receives the down-converted I/Q quadrature spectrum (with 50 MHz bandwidth, in this case) from an RF front-end (one channelizer for each RF front-end). The channelizer then splits the complex baseband signal into smaller bandwidth complex channels each centered at DC to be fed to the signal separation block. For the channelization, several factors need to be considered: the separation scheme (number of stages) of down-conversion of each channel, linearity, and harmonic folding.

The proposed quarter-band separation scheme is illustrated in Fig. 5.4. The complex baseband signal with a bandwidth of $2f_c$ is divided into four consecutive segments in the frequency domain. In order to split the four segments into four DC-centered channels, quadrature up-conversion and down-conversion mixers are adopted to move the segment of interest to DC, and low-pass filters (LPF) with a cut-off frequency of $\frac{1}{4}f_c$ are used to reject the signals that are out-of-band. For segment 2 and segment 3, the local oscillator (LO) frequency of the up-conversion and down-conversion mixer is $\frac{1}{4}f_c$. While for segment 1 and segment 4, the LO frequency is $\frac{3}{4}f_c$. Additional mixing stages can be cascaded to further split each segment into more channels. Given the stage number $n$, the channelizer can generate $4^n$ consecutive channels in total.

The choice of the separation scheme and the number of stages allows a trade-off between LO harmonic folding frequencies needing to be appropriately filtered and the total number of output channels. For example, half-band separation (Fig. 5.5), i.e. each stage splitting the input into 2 segments, requires 4 stages to produce 16 output channels, while quarter-band separation (Fig. 5.4) requires fewer stages, leading to less power consumption, less additive noise, and less in-band fluctuation due to non-ideal frequency response in the LPFs. Compared to $\frac{1}{8}$-band separation, in which more LO frequency references ($\frac{1}{8}f_c$, $\frac{3}{8}f_c$, $\frac{5}{8}f_c$ and $\frac{7}{8}f_c$) are required and more LO harmonics appear in-band causing harmonic folding, quarter-band separation has a simpler LO generation and higher immunity to LO harmonic folding. More specifically, for quarter-band separation, only the 3rd-order harmonic folding response needs to be considered with adequate pre-channelizer filtering. The odd-order harmonic folding of quarter-band separation is illustrated in Fig. 5.6 showing that the $\frac{1}{4}f_c$ clock folds the 3rd and 5th harmonic while the $\frac{3}{4}f_c$ clock folds spectrum out-of-band (which should be appropriately
filtered by the RF front-end). Therefore, for quarter-band separation to minimize harmonic folding, a harmonic-reject mixer that alleviates $3^{rd}$ and $5^{th}$ harmonic folding only is needed.

A 16-to-1 channelizer splits the quadrature 50 MHz baseband signal into 16 consecutive channels centered at DC. The architecture of the channelizer is based on a 2-stage quarter-band separation structure with diagram shown in Fig. 5.7. The fundamental circuit building block of the channelizer, the SCU (Signal Conditioning Unit), translates a complex baseband input signal up (for an input that is on the left side of DC) and down (for an input that is on the right side of DC) together with low-pass filtering and is shown in Fig. 5.8. Depending on the clock LO frequency, SCUs are categorized into two types: SCUa’s LO reference is $\frac{1}{4}f_c$ (6.25 MHz for the 1st-stage and 1.5625 MHz for the 2nd-stage) while SCUb’s LO reference is $\frac{3}{4}f_c$ (18.75 MHz for the 1st-stage and 4.6875 MHz for the 2nd-stage). The first stage, comprising of one SCUa block and one SCUb block, splits the 50 MHz band into four 12.5 MHz-wide segments, while the second stage further splits each of the segments into four 3.125 MHz-wide channels, i.e. 16 channels in total. Further design specifications can be found in [37].
Figure 5.4: Illustration of quarter-band separation scheme.
Figure 5.5: Illustration of half-band separation scheme.
Figure 5.6: Illustration of quarter-band separation harmonic folding. (a) $\frac{1}{4}f_c$ harmonic clock folding (b) $\frac{3}{4}f_c$ harmonic clock folding.
Figure 5.7: Diagram of the channelizer with 16 channel outputs based on 2-stage, quarter-band separation scheme.
Figure 5.8: Diagram of signal conditioning unit (SCU).
5.4 Measurements of a BiCMOS 16-to-1 Baseband Channelizer

The prototype chip was fabricated in an IBM 0.18-um SiGe BiCMOS process and wire-bonded in a QFN package for PCB testing. The die micrograph is shown in Fig. 5.9(a) and the measured die size is 4.5mm x 3.7mm, including bonding pads. The measured power consumption is 71.5 mW from a 2.5 V power supply, excluding the output buffers for testing purposes. To test the channelizer, a PCB was fabricated with differential I/Q complex input and mux-selectable outputs (5.9(b)).

A baseband I/Q vector signal generator was used to generate a complex input signal and a multi-channel oscilloscope FFT was used to acquire the down-converted channel. The measured input to output gain transfer function of all 16 channels is shown in Fig. 5.10.

The third-order distortion measurement was performed by inputting a two-tone signal with 50 kHz spacing in the frequency region of channel 6 with a gain setting of 20 dB. The measured magnitude of the fundamental and the third order intermodulation tones at the output is shown in Fig. 5.12. The IMD3 was better than -40dBc at -20dBV output.

The 3rd-order harmonic folding of the first stage was measured by a two-tone test with one tone placed in-band in channel 6 and the second jammer tone placed at the third harmonic of the clock frequency and 14 dB higher than the in-band tone. The measured down-converted jammer tone was 32.6 dB lower than the in-band tone, giving the total rejection of 3rd-order harmonic folding to be better than 46 dBc, as shown in Fig. 5.13.
Figure 5.9: (a) A 16-to-1 channelizer in 180 nm BiCMOS (4.5 mm x 3.7 mm). (b) PCB test structure.
Figure 5.10: Channelizer gain transfer function of all 16 channels at 20 dB gain setting.
Figure 5.11: In-band distortion: (a) Third order distortion. (b) Harmonic folding.
Figure 5.12: Input Referred V1dB Compression = -27 dBV = -14 dBm (referred to 50 ohm). Input Referred Intermodulation Distortion Voltage = -19.1 dBV = -6.09 dBm (referred to 50 ohm).
Figure 5.13: Measured 3rd-order harmonic mixing. Input jammer tone is 14 dB higher than the input in-band tone.

5.5 Acknowledgments

The text of this chapter, in part or in full, is a reprint of the material as it appears in published papers or as it has been submitted for publication in IEEE Bipolar CMOS Technology Meeting (BCTM). The dissertation author was a co-author with research contribution from Dr. Hao Li, Chul Kim, Siddharth Joshi, and Prof. Gert Cauwenberghs.
Table 5.1: Summary of Channelizer Measured Results

<table>
<thead>
<tr>
<th>Process</th>
<th>0.18um BiCMOS</th>
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<tr>
<td>Channelizer Power</td>
<td>71.5 mW</td>
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<td>Harmonic Folding</td>
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<tr>
<td>3rd &gt; 46 dBc</td>
<td>1st stage</td>
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<tr>
<td>3rd &gt; 40 dBc</td>
<td>1st and 2nd stage</td>
</tr>
<tr>
<td>5th &gt; 52 dBc</td>
<td>1st and 2nd stage</td>
</tr>
<tr>
<td>Input P1dB (50Ω)</td>
<td>-14 dBm</td>
</tr>
<tr>
<td>(20 dB gain setting)</td>
<td></td>
</tr>
<tr>
<td>In-band IIP3 (50Ω)</td>
<td>-6 dBm</td>
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<tr>
<td>(20 dB gain setting)</td>
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</tr>
<tr>
<td>Output referred noise</td>
<td>123 nV/sqrt(Hz)</td>
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<tr>
<td>(0 dB gain setting)</td>
<td></td>
</tr>
<tr>
<td>Area</td>
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</table>
Chapter 6

Conclusions and Future Work

6.1 Conclusions

This dissertation focused on broadband tunable, fully integrated filters for out-of-band jammer rejection with intended applications such as cognitive radio, diversity receivers, and SAW filter replacement. Specifically, this dissertation focused on the N-path filter approach. While the N-path filter has many advantages in terms of full integration with the existing receiver and broadband tuning range, the approach still has limitations in terms of design trade-offs between insertion loss and out-of-band rejection, clock feed-through, and filter compression due to device scaling. This dissertation covered the innovations developed to address these issues: a transmission line N-path filter, a pseudo-random LO leakage suppression technique, and a jammer robust GaN N-path filter. Lastly, a cognitive radio signal classification system application of the N-path filter is reviewed.

In Chapter 2, a transmission line N-path filter has been introduced that ideally improves both the in-band insertion loss and out-of-band rejection of the traditional N-path filter. The T-line N-path filter absorbs the parasitic capacitance of the transistor switches into a synthetic transmission line broad-banding the in-band response. Moreover, the out-of-band rejection is improved by further low-pass filtering created by the transmission line inductance and switch resistance. An expression was derived for the out-of-band rejection and NF and was shown to match simulation. It has been shown that the T-line N-path filter introduces additional near in-band poles which was derived
for a $K = 2$ case. Two designs were fabricated in a 65 nm bulk CMOS process: a design with and without a broadband LNA. The stand-alone T-line N-path filter was measured from 0.1-to-1.6 GHz and achieved less than 5 dB insertion loss across the full range, 30 dB to 50 dB out-of-band rejection, in-band IIP3 of $+29$ dBm, and a $+11$ dBm P1dB out-of-band jammer tolerance. This work obtains higher order out-of-band rejection with higher P1dB compression than previously published higher order active N-path filter designs.

In Chapter 3, to mitigate the spurious clock feed-through of the traditional N-path filter, a pseudo-random (PN) clocking technique was introduced. The PN N-path filter maintains the same impedance translation and filtering properties of the traditional N-path filter at the expense of further clocking complexity and double switch resistance. A prototype was fabricated in a 65 nm bulk CMOS process. Measurements from 0.1-to-1.4 GHz demonstrate a 15 dB out-of-band rejection, in-band IIP3 of $+22$ dBm, out-of-band jammer tolerance of $+11$ dBm, and an LO leakage improve of 10 dB to 15 dB with magnitude ranging from -60 dBm to -80 dBm.

In Chapter 4, to improve the power handling of the N-path filter compared to a traditional N-path filter implemented in bulk CMOS, a first implementation of a GaN HEMT bandpass N-path filter was designed in a CREE 400 nm bare die technology bond-wired to a PCB. Measurements from 50 MHz to 300 MHz of a series N-path filter architecture demonstrate a P1dB of $+10$ dBm and an out-of-band jammer tolerance of $+17$ dBm beyond jammer power handling of the conventional CMOS N-path filter.

Lastly in Chapter 5, an application of a CMOS broad-band tunable N-path filter is discussed: a broadband tunable signal separation and classification receiver. The overall system architecture is described with measurement results from testing of a potential candidate for the baseband signal channelizer.

### 6.2 Future Work

The N-path filter has garnered interest recently due to the rapid improvement in process scaling of CMOS technology allowing operation at RF frequencies. This work has demonstrated the potential of high frequency operation of N-path filters using
transmission line techniques and methods to improve the clock feed-through; however, there still exists fundamental challenges for practical industry adoption of N-path filters as well as room for further investigation. A brief summary of potential investigations is given below.

- The clock generation of the N-path filter still remains one of the biggest challenges preventing the N-path filter from becoming adopted as a SAW filter replacement for industrial use. The specific limitation is reciprocal mixing of the out-of-band jammer and the phase noise of the clock generation circuitry folding the phase noise into the desired band. In classical receivers employing SAW filters, the phase noise specification is generally relaxed directly proportional to the out-of-band jammer attenuation that the SAW filter provides. However, in contrast, the jammer does not experience any attenuation proceeding the N-path filter leading to reciprocal mixing and in-band SNR degradation. In [38], the transfer function for reciprocal mixing of the N-path filter was derived.

- The T-line N-path filter technique shows promise at higher frequencies of operation. For example, the out-of-band rejection improves versus frequency due to the low-pass filtering effect. An interesting area of investigation would be pushing the limits of the frequency of operation of the N-path filter into 10’s of GHz using an aggressively scaled CMOS SOI process. Further advantages at higher frequency may be obtained since the N-path filter’s number of phases can be reduced to 4, simplifying the design and clock generation, as harmonic folding is no longer a concern as compared to lower frequency operation (the spacing between harmonics increases versus LO clock frequency).

- Further investigation into PN sequence optimization in terms of noise shaping may be considered for the PN-sequence N-path filter architecture.

- GaN N-path filtering for applications such as receiver high jammer withstand seems to be a promising prospect. However, further work is needed in terms of solving the challenges of high voltage clock generation.
References


[34] M. Darvishi, R. van der Zee, and B. Nauta, “A 0.1-to-1.2 GHz tunable 6th-order N-path channel-select filter with 0.6 dB passband ripple and +7 dBm blocker tolerance,” in IEEE International Solid-State Circuits Conference Digest of Technical Papers (ISSCC), Feb 2013, pp. 172–173.


