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Core-Shell Nanopillar Array Solar Cells using Cadmium Sulfide Coating on Indium Phosphide Nanopillars

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A thesis submitted in partial satisfaction
of the requirements for the degree Master of Science
in Electrical Engineering

by

Bor-An Clayton Tu

2013
ABSTRACT OF THE THESIS

Core-Shell Nanopillar Array Solar Cells
using Cadmium Sulfide Coating on Indium Phosphide Nanopillars

by

Bor-An Clayton Tu

Master of Science in Electrical Engineering
University of California, Los Angeles, 2013
Professor Diana L. Huffaker, Chair

This thesis presents a new strategy to fabricate nanostructured indium phosphide and cadmium sulfide photovoltaics. The cells are formed by chemical bath deposition (electroless deposition) of cadmium sulfide onto indium phosphide nanopillar arrays grown by selective-area metalorganic chemical vapor deposition. Characterizations through electrical and optical measurements show that the devices consisting of p-InP core and CdS shell have a conversion efficiency, open circuit voltage, short circuit current density and fill factor of 4.8%, 0.53 V, 15.8 mA/cm² and 0.57 respectively. A solution-based junction formation on nanopillars is developed and investigated in search of a quick and low-cost method to harvest solar energy.
This thesis of Bor-An Clayton Tu is approved.

Benjamin S. Williams

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Diana L. Huffaker, Committee Chair

University of California, Los Angeles

2013
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Since electrical engineers (me) know zilch about chemical formulae and reactions, I deeply thank Brion Bob (from the material science department) for working his magic with the chemical bath deposition of cadmium sulfide. Of course, he spent time explaining the ins and outs of the processes as I desperately jotted down as much as I could. Kudos once again!

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Chapter 1. Introduction and Background

1.1 Solar Energy

Among the different renewable energy sources, solar energy is one of the most abundant and can substitute or even replace fossil fuels. The sun puts out about $3.8 \times 10^{26}$ J of energy every second, equivalent to 90 billion hydrogen bombs exploding per second. While only one billionth of that power ($1.7 \times 10^{17}$ W) reaches Earth’s surface, one day of sunlight is enough to power the whole human race for more than half a century.

Besides being virtually unlimited, solar energy is environment-friendly. Today’s electricity generation and transportation rely heavily on burning fossil fuels which produces greenhouse gases (GHG) (Fig. 1). These gases trap heat from the earth’s surface that would normally radiate back out into space. It’s at a point now that the excessive amounts of GHGs are causing worldwide climate changes. In the US, 82% of energy is generated from fossil fuels [1]. With less than 1/30 of the world’s population, the US outputs 1/5 of all GHG emissions according to the U.S. Department of Energy. Worldwide GHG emission is also on the rise year after year (Fig. 2). Solar energy can help reduce GHG emission by providing clean energy conversions from sunlight, either actively such as photovoltaics and concentrated solar, or

![U.S. Greenhouse Gas Emissions in 2011](image1.png) ![Global Greenhouse Gas Emissions by Gas](image2.png)

Figure 1. Breakdown of U.S. (left) versus global (right) greenhouse gas emissions. Source: (left) Contribution of Working Group I to the Fourth Assessment Report of the Intergovernmental Panel on Climate Change, IPCC(2007), (right) [54]
passively such as water and air heating.

Solar power systems are modular and are readily scalable and versatile. Depending on required output, more panels can be linked together. This allows stand-alone solar power systems which are especially appropriate for remote, environmentally sensitive areas, such as national parks, cabins, and remote homes. On the other hand, large solar plants are also achievable and can supply energy to existing power grids. The current largest (in-operation) photovoltaic solar generation facility, the Agua Caliente Solar Project by First Solar, is located in Yuma County, Arizona, providing 247 MW of energy with plans to increase to 290 MW by 2014. With over 5 million modules, the solar plant covers over 5200 acres of land [2].

Despite all the benefits that solar power brings, it provides less than 0.1% of the electricity in the US (Fig. 3). The most dominant reasons for the low utilization is the manufacturing costs of solar cells and upfront installation fees that make consumers hesitant to buy in on solar energy. Fortunately, the dollar per Watt generated from solar has gone down in the past years (Fig. 4) since production of solar panels has increased dramatically. If more people

![Global Carbon Dioxide (CO2) emissions from fossil-fuels 1990-2008](image)

start adopting solar energy systems, prices will drop even more. A cleaner and more sustainable life-style should not be far off.

Figure 3. In the US, more than 80% of energy comes from fossil fuels (petroleum, coal, natural gas) and less than 0.1% of energy comes from solar. Source: U.S. Energy Information Administration, Annual Energy Review 2009, Table 1.3, Primary Energy Consumption by Energy Source, 1949-2009 (August 2010)

Figure 4. Adapted chart from [55] which compares prices of solar, crude oil, and natural gas generated electricity. Units are normalized to $/gigajoules for comparison.

1.2 Types of Solar Cells

Before delving into the exotic forms of solar cell technology, this section gives some history and evolution of solar cells. Since the discovery of the photovoltaic effect in the 19th
In the 20th century, solar cells have evolved and increasingly so in recent years. The quest to build cost-effective and highly efficient solar cells has been the driving force for researchers in the field. To date, the timeline for solar cells is typically split into three generations with overlaps in between.

**First Generation Solar Cells**

The first generation of solar cells is made from bulk silicon. They are currently the most efficient solar cells available for residential use and account for more than 80 percent of all the solar panels sold around the world. Generally silicon based solar cells are more efficient and longer lasting than non-silicon based cells. However, they are more at risk to lose some of their efficiency at higher temperatures than thin-film solar cells.

![Figure 5.](image_url) From left to right: Monocrystalline silicon solar cells, polycrystalline silicon solar cells, and amorphous silicon (thin-film) solar cells. Source: (left to right) Wikipedia Commons, Wikipedia Commons, NASA.gov

**Second Generation Solar Cells**

Second-generation solar cells which have been under intense development during the 1990s and early 2000s, are usually called thin-film solar cells because when compared to crystalline silicon based cells they are made from layers of semiconductor materials only a few micrometers thick. By using less material and less expensive manufacturing processes, the manufacturers are allowed to produce and sell panels at a much lower cost.
There are basically three types of solar cells that are considered in this category, amorphous silicon (some overlap with the cells mentioned previously), and two non-silicon platforms namely cadmium telluride (CdTe), and copper indium gallium diselenide (CIGS). Together they accounted for around 15% of the panels sold in 2010.

Third Generation Solar Cells

The third generation of solar cells is being made from variety of new materials besides silicon, including compound semiconductors [3], organic dyes [4][5][6], and polymers [7]. The goal is to improve on the solar cells already commercially available. Different structures are also part of the third generation solar cells such as using conventional printing press technologies to produce panels [8][9], tandem junctions [10–12], or nanowire [13], quantum dot integration [14], [15] to improve efficiencies. Currently, most of the work on third generation solar cells is being done in the laboratory or in R&D stages and for the most part is not commercially available.

Figure 6. Efficiency records of different types of solar cells [56]. It is worthy to note that emerging PV (third generation) have low efficiencies but have the most improvement over the past few years.
1.3 Nanotechnology and Solar Cells

Besides trying different materials, new structures have been explored for solar cell development. Third generation solar cells are of this nature as interesting ideas are drawn out daily. The solar cells presented in this work reside in this category where they will not only incorporate nanotechnology, but also use non-silicon based materials.

1.3.1 What is nanotechnology?

“There’s plenty of room at the bottom.” Famous lecture by physicist Richard Feynman explains to the public how “small” is the next “big” trend in the scientific world. In the year of 1959, he envisioned the endless possibilities of nanotechnology such as storing all printed books of mankind into a medium smaller than a dust particle. Half a century later, nanotechnology has indeed become a major player in the field of research and development. Nanotechnology is all technology but at the fraction-of-a-human-hair scale. From quantum dots to carbon nanotubes, from single electron transistors to biological sensors, from anti-bacterial socks to rain-repelling windshield coatings, nanotechnology has found itself integrated into a wide variety of products.

1.3.2 Why is it interesting and how is it useful?

Materials at the nanoscale often behave different than in bulk. For instance, gold at nanoscale can be semiconducting and aluminum can be magnetic. These “new” properties that only occur at miniscule sizes are what fascinate and excite engineers to explore nanotechnology.

‘Nano’ is a prefix meaning one billionth of or something very tiny. For something not even visible to the naked eye, how is it useful? For one, making something smaller means lesser use of material. It also means that the same amount of material can produce more final products. This often helps reduce the base cost of the individual product. For electronic devices, smaller
physical footprint also leads to lesser energy consumption and faster operating speeds. Additional features can be implemented without exceeding size or power specifications. For optics, with features on the scale of or smaller than the wavelength of light, nanotechnology can create all kinds of resonances, absorption and reflection reactions, and even ‘gaps’ where light is forbidden [16]. For biology, nanotechnology can help advance the cure of diseases by modifying medicine to accurately target infected cells but not the healthy ones. The list goes on.

In particular, nanopillars will be the main focus for this work. A nanopillar is a one-dimensional structure usually measuring a couple hundred of nanometers in length and a few tens of nanometers in width. Though the term is often used interchangeably with nanowires, a distinction is made here because of the uniform alignment and all-upright orientation. Nanopillars (and nanowires) have been used in electrical, optical, and even mechanical applications [17].

Why choose an array of core-shell nanopillars for solar cells? One of the advantages of using nanopillars over planar material is a higher surface to volume ratio. Taking a 1 cm$^3$ cube of silicon for instance, its volume is equivalent to 1x10$^{13}$ nanopillars with diameters of 150 nm and heights of 1300 nm. In terms of surface area however, the cube only has 6 cm$^2$ of surface area while the nanopillars have almost 1.5x10$^5$ cm$^2$! With the same amount of material, the nanopillar structures obviously provide tremendously more surface area. For solar cell applications, this means more surface to capture light. There is one condition though: the active region of the device must also exist over the whole area. This is where the core-shell junction comes into play. Instead of having an axial junction which would only create an active region at the cross-section of the pillar, the core-shell junction extends along the whole pillar. At the same time, the coaxial
arrangement yields orthogonalized pathways for light absorption and carrier collection (Fig. 7) leading to higher carrier extraction efficiencies. To enhance light absorption further, the nanopillars can be aligned in a periodic array formation which can induce light trapping effects [18][19] (Fig. 8).

**Figure 7.** Carrier generation and extraction from core-shell junction (left) versus axial junction (right). White arrows depict carrier generation direction and black arrows depict carrier collection direction. Dotted lines represent axis, \( r \) for radial and \( z \) for axial axis.

**Figure 8.** (a) Three-dimensional schematic of the complete structure used in the finite-difference time-domain simulations. To notice, the NP (nanopillar) is embedded in the BCB layer and capped by a conformal layer of ITO as transparent top electrode. (b) Unit cells of triangular, square, rectangular and parallelogram tiling patterns are investigated. (c) 2D contour plot of NP pitch \( P \) (500nm \( \leq P \leq 1,000 \text{nm} \)) and wavelength-dependent optical absorption. Red colour indicates high absorption and blue colour corresponds to low absorption. (d) Wavelength-dependent absorption as a function of different tiling patterns for a fixed 600-nm pitch (dashed cutline from Fig. c). Adapted from [19].
1.4 Semiconductors

Why has silicon become the mainstream material for solar cells? First of all, silicon is the second most abundant element around which is therefore economically attractive for mass production. Secondly, silicon is a well-studied and very commonly used semiconductor.

Semiconductors reside in the majority of today’s electronic devices. They hold a unique property of being conductive under certain conditions and insulating in others, thus the name. Conductivity is governed by the movement of free electrons inside a material. In most cases, those electrons are bound to atoms and can only flow freely in certain energy bands. The two critical bands are the valance band (the most outer bound electron band) and the conduction band (the lowest energy free flow electron band). In contrast to metals where the two bands overlap, semiconductors have an energy band gap where no electronic energy states exist. Unless a certain amount of energy is provided to the electrons to overcome this band gap, the semiconductor remains insulating. This is useful for making switches in digital components. How semiconductors can be used for solar applications will be further discussed.

1.4.1 PN Junctions

Dopants can be added to a semiconductor to increase the conductivity. Two types of dopants – acceptors and donors, allow for either more free holes or more free electrons in the semiconductor. The pn junction is the boundary formed when oppositely doped semiconductors are combined. A depletion region that has no free charges is then created as free carriers diffuse over the boundary and neutralize the opposite charges. At the same time, a built-in electric field in the depletion region will form and free charge will drift, hampering further diffusion. In
steady-state, the diffusion and drift of the free charges will balance out across the junction and a fixed depletion region size is obtained.

The behavior of the pn junction with regards to the potential barrier width produces an asymmetrical conducting two terminal device, more often known as the junction diode. Unlike the resistor which obeys the linear Ohmic law under bias, current through the diode shows an exponential I-V relationship. Using the I-V characteristics to quantify the diode will be discussed in the result sections.

1.4.2 Solar Cells

The semiconductor solar cell is a pn diode operating under light. As light shines on this junction, photovoltaic response causes carriers, both electrons and holes, to be generated. If the junction remains in open-circuit, the generated carriers within diffusion length and inside the depletion area recombine with the space charge which in turn reduces the depletion width. This change in depletion width makes up the open-circuit voltage ($V_{OC}$) of the solar cell. If the junction is placed within circuitry, a short-circuit current ($I_{SC}$) can be extracted.

To get a complete picture of the power conversion efficiency of solar cells, quantification of the generated current at each wavelength of the solar spectrum, or external quantum efficiency (EQE), is also of crucial importance. Poor external efficiency can be either a reflection of poor internal quantum efficiency (IQE) or can mean that large amounts of the light reaching the cell are unavailable for use because it is being reflected away by the cell or allowed to pass through it.

In an ideal solar cell, all carriers that are generated from photon absorption can be extracted. However, due to defects in the material and contact resistances, some carriers don’t contribute to the current. The percentage that does contribute is the IQE. In other words, the IQE
refers to the efficiency with which absorbed photons that can generate collectable carriers. For example, front surface passivation affects carriers generated near the surface, and since blue light is absorbed very close to the surface, high front surface recombination will affect the "blue" portion of the quantum efficiency. Similarly, green light is absorbed in the bulk of a solar cell and a low diffusion length will affect the collection probability from the solar cell bulk and reduce the quantum efficiency in the green portion of the spectrum. The final EQE of the cell depends on three major physical phenomena, which determine its overall photoconductivity: the optical absorption of light creating the free charge carriers, the electrical transport of these carriers that contribute to the current and the capture of the photo-generated excess carriers, leading to trapping or recombination.

Another figure of merit used to gauge a solar cell’s efficiency is the fill factor (FF). The fill factor is a ratio between the maximum output power of the solar cell and the product of the short-circuit current and the open-circuit voltage (Fig. 9).

![Figure 9](image)

**Figure 9.** The fill factor (FF) of a solar cell can be viewed as the ratio between the area under the blue box and the area under the green box. P_{max} is where the output power is maximized. The red curve is the I-V of a solar cell under light. Source: National Instruments [57]

The final power conversion efficiency (\( \eta \)) is then calculated as:

\[
\eta = \frac{V_{OC}(V) \times I_{SC}(A/cm^2) \times FF(\%)}{(\text{Incoming Intensity (W/cm}^2) \times \text{Area of Cell (m}^2))}
\]

Under one sun and AM1.5 conditions, the incoming intensity is taken as 1000 W/m^2.
1.5 Motivation

The motivation behind this work is to explore a unique method for creating a solar cell using semiconductor nanopillar arrays. While solar cell fabrication with nanopillars has been demonstrated and so has chemical bath coating for thin film or organic/inorganic hybrid solar cells, the combination of the two is still open for investigation. This work holds trial stages to gain some insight into solution-based processing. The main focuses in the following chapters are the fabrication techniques and performance examination of the solar cells.

Nanopillars open up the possibilities for light-weight and flexible photovoltaics. Using even less material than thin film panels, nanopillars are also attractive in costs. Though indium phosphide (InP) wafers are expensive compared to silicon, by using nanopillars there are ways to detach the pillars and re-use the substrates. This work also contributes as a pathfinder for nanopillar array solar cell development that can be later expanded to large area devices by means of deep UV lithography or nanoimprinting.

The chemical bath deposition which will be explained in detail later on, provides a simple and quick way to form pn junctions with the underlying doped nanopillars. The process does not require high vacuum systems, high temperatures, or any expensive equipment which are inevitable with most MOCVD or MBE growth of heterostructures. Besides the looser restrictions, this technique only involves solution-based procedures which allow large-area or roll-to-roll processing for mass production.

Taking the best of both sides, this study combines InP nanopillars and chemical bath deposition of cadmium sulfide (CdS) to examine how well they can generate power under light. It also lays down a foundation for future photovoltaic work that will use different material combinations and nanostructured designs.
Chapter 2. Solar Cell Fabrication

2.1 Structure

The solar cell structure used in this work is formed with arrays of core-shell heterostructure nanopillars on p-type InP substrate. The nanopillar core is p-doped InP and the shell is n-type CdS. Transparent conductive oxide (TCO) is placed over the tips of the shell (cathode) and metal contacts are deposited on the back side of the substrate which is connected to the core (anode). For planarization and insulation purposes, benzocyclobutene (BCB) is coated and etched back before the top contacts are deposited.

The CdS/InP combination is chosen because CdS is a direct wide bandgap (~2.43 eV) and intrinsically n-type material making both a window layer and a junction when deposited on top of the p-doped InP nanopillars. InP, which has an inherent bandgap around 1.34 eV, allows for good absorption of most of the solar spectra (Fig. 11, Fig. 12). Both CdS and InP have low surface recombination rates (compared to silicon or gallium arsenide) [20][21] which becomes a critical factor when the device structures have large surface-to-volume ratios, as do nanopillars. Last, it has been shown that the commonly used transparent contact, indium tin oxide (ITO), forms ohmic contact with CdS in high-efficient thin film solar cells [22][23].

Figure 10. Schematic shows the cross-section of the proposed structure for the solar cell device.
Figure 11. On the left is the top cross-section schematic of the core-shell nanopillar. On the right is the estimated bandstructure from point A to point B in the cross-section schematic. $E_c$, $E_F$, $E_v$ stand for the conduction band edge, the Fermi level, and the valence band edge respectively. Note: Band-offsets are not reflected here.

Figure 12. Chart shows common semiconductor compounds used for solar applications and their bandgap/lattice constant relations. The overlaying gray curve shows the solar spectrum (blackbody radiation) under AM1.5 conditions. The red box encloses the materials used in this work, CdS and InP. It can be seen that the combination covers most of the solar spectrum where irradiance is strongest. Source: SPIE Newsroom. DOI: 10.1117/2.1201104.003532
2.2 Nanopillar Growth

Nanostructured material can be obtained in various ways such as molecular beam epitaxy (MBE), colloidal dispersions, metalorganic chemical vapor deposition (MOCVD), etc. The InP nanopillars used here are grown by MOCVD. The basic principles behind MOCVD growth involve controlling gas flows, pressure and temperature. Gases with desired precursors are flown through a chamber over a heated substrate. The precursors pyrolyze and leave behind atoms that can bond to the substrate which leads to epitaxial growth. Such systems are suitable for large scale productions and are capable of utilizing multiple materials. However, with numerous adjustable parameters, controlling the MOCVD growth is a study within itself.

2.2.1 MOCVD – Catalyzed, VLS

The formation of nanowires in MOCVD reactors generally follows a vapor-liquid-solid (VLS) transition [24][25][26]. VLS was first proposed by Wagner and Ellis for silicon whiskers grown with a gold (Au) particle [24]. The liquid metal droplet attracts reaction species supplied from the surrounding vapor, and is readily supersaturated (overloaded) with reaction species. Highly anisotropic nanowire growth is caused by the precipitation of reaction species at the solid/liquid interface. Nanowire heterostructures can be grown in either the axial direction by alternating precursors or the radial direction (core–shell) by increasing growth temperature.

![Figure 13. Schmatic of VLS growth of silicon nanowires. (a) Thin film of gold on silicon substrate is heated up. (b) Gold nanoparticles form and attract vaporized silicon atoms. (c) As the gold particles become supersaturated from silicon atoms, nanowire growth forms at the substrate/particle interface.](image-url)
2.2.2 MOCVD – Self-Catalyzed, Selective Area Growth

In contrast to the often used metal-catalyzed growth mode, where metal nanoparticles are used to “seed” the growth, in this work, a self-catalyzed, selective-area growth mode is used to form the pillars. The following describes how this growth mode is achieved.

In this project, before growth, a thin oxide mask, roughly 20 nm, is electron beam (e-beam) evaporated onto a 2-inch p-type InP 111A substrate. ZEP520 e-beam resist is spin-coated on the substrate and nano-sized holes are then scribed into the resist using electron beam lithography (EBL). The hole patterning is designed using Tanner EDA L-edit software and the e-beam reads the template file to “write” the pattern into the resist. Unlike UV photolithography, no physical mask is required for EBL. High-resolution of 40~50 nm diameter hole sizes can be reproduced with ease. If satisfying results can be achieved in small samples (research stage), the plan is to port the recipe over to deep UV lithography or nanoimprint lithography for large scale production because though EBL brings the advantage of uniformity and high-precision, the method is fairly time consuming and costly for large area patterning. After developing the resist in ZED N-50, reactive ion etching (RIE) is performed to transfer the patterned holes into the oxide mask down to the substrate. The e-beam resist is then stripped off using a thorough cycle of wet and plasma etching. Finally, the substrate is either cleaved or diced and placed in the MOCVD chamber for pillar growth. As vapor precursors flow across the patterned substrate, vertical InP pillars grow out of the holes. To form p-type InP pillars, Zn dopants are incorporated during the growth. This forms the ‘core’ or the p side of the pn junction. Figure 14 shows a simple schematic of the whole process of selective area growth.
With the patterned substrate, vertical nanopillar growth in user-defined locations and sizes is achieved. Three samples are used for this project. Each sample is a 1 cm by 1 cm piece containing four devices. Each device pattern is a 500 µm by 500 µm array of holes with diameters of 60 nm and pitch of 600 nm. Actual pillar diameters varied within the range of 100 to 200 nm. Pillar heights turned out to have short ones in the 400 ~ 500 nm range, while longer ones were close to 3 µm. Figure 15(b) shows the InP nanopillars as grown. The different heights and morphologies of the pillars are still under investigation. In this project, the pillars are used as is.

**Figure 14.** Catalyst-free, selective area growth procedure. (a) A thin layer of oxide is deposited onto the substrate. (b) Patterning of the mask is done with e-beam lithography. (c) Pillar growth follow the patterning of the oxide and protrude vertically out of the holes.

2.3 Fabrication – Post-Growth

Back-end processing after the MOCVD growth which includes polymer spin-coating, defining contact pads with photolithography, metal and ITO depositions are all carried out in a
class 100 cleanroom. CdS coating is processed in a chemistry lab courtesy of Prof. Yang Yang’s group in the material science department.

2.3.1 Insulation Layer - BCB

To exclude effects from the substrate and to prevent shunting between top and bottom contacts, a layer of BCB is coated over the whole device. BCB is a polymer dielectric often used in microelectronics and photosensitive applications. It can be spin coated with controllable thicknesses and cured at temperatures above 150°C. Cured BCB has great chemical resistance and is suitable for making thin insulation layers.

Samples are first chemically cleaned with a cycle of acetone, methanol, and isopropanol rinsing then dehydration baked at 180°C for 5 minutes. To form stronger bonding between BCB and the sample, Dow Chemical Company AP3000 adhesion promoter is spin coated and heated before applying the BCB. Dow Chemical Company Cyclotene 3022-35 BCB is then spin coated at 3000 rpm for 45 seconds in an open-lid Headway spin-coater. Due to particle contamination being a big issue causing non-uniformity and low performing devices, the BCB is dispensed through a syringe/filter combination and disposed of after each run. BCB is first soft cured at 100°C for 1 minute (hotplate in air) and then hard cured at 250°C overnight in a Carbolite oven filled with N₂. The thickness of BCB is roughly 1.3 µm measured with a Nanospec reflectometer. This BCB layer not only planarizes the pillars but also acts as protection prior to the back metal deposition (Fig. 16).
2.3.2 Back Contacts

To make ohmic contact to the p-InP substrate, a short study with various metal stacks is performed. It has been known that forming ohmic contacts to p-InP is more difficult than to n-InP due to unavailability of metals with large enough work function. Various degrees of success have been shown [27–38] and are taken into consideration for this work. Limited by metal sources, only four combinations, Cr/Au, Ti/Au, Zn/Au, and Au/Zn/Au/Ni/Au, were tested with transmission line measurements (TLM). In the end, Au/Zn/Au/Ni/Au which gave the best results is evaporated onto the backside of each sample. The metal stack was deposited using a SLOAN 1800 with layer thicknesses of 300 Å / 100 Å / 1100 Å / 100 Å / 1000 Å. TLMs show $\sim10^{-4} \, \Omega \cdot \text{cm}^2$ series resistance after annealing at 380°C for two minutes.

2.3.3 Chemical Bath Deposition

To form the n-type shell around the pillars and complete the pn junction, chemical bath deposition (CBD) of CdS is used. Since the pillars are embedded in BCB, an etch-back in an Oxford 80+ RIE is performed to expose the pillars before CdS deposition. A 4:5 mixture of CF$_4$ and O$_2$ etches the BCB with an etch rate of roughly 50~60 Å/s. The recipe is run long enough to expose most of the pillars but leaves just enough behind to cover the substrate (Fig. 17).
Compared to growing heterostructures within the MOCVD chamber, a simpler and faster CBD method is elected. Though CBD of CdS has been studied since the 1960s and has been shown to be advantageous for large-area, low cost, and fast processing [39–43], it is more often used for window layers in thin film solar cells [44–47] and has not been used to form junctions on InP nanopillar array solar cells.

**Figure 17.** (a) Schematic of BCB etched back to expose pillar. (b) Tilted SEM of nanopillars extruding from

CBD is a solution-based method that allows controllable homogeneous precipitation of metal ions $M^{z+}$ (in this case $Cd^{2+}$) using sulfide ($S^{2-}$) or selenide ($Se^{2-}$) ions as precipitating agents. The typical reaction to form CdS is as follows [48]:

$$Cd(NH_3)_n^{2+} \rightarrow Cd^{2+} + nNH_3$$

(1)

$$SC(NH_2)_2 + 2OH^- \rightarrow S^{2-} + CN_2H_2 + 2H_2O$$

(2)

$$Cd^{2+} + S^{2-} \rightarrow CdS(s)$$

(3)

(1) Cadmium salt (cadmium acetate or CdAc is used here) is placed in ammoniacal medium ($NH_4AcO$ and $NH_3(H_2O)$) where $Cd^{2+}$ ions are released by dissociation of the corresponding ammino complexes. $n$ values can range from 1~6 depending on ammonia concentrations. (2) $S^{2-}$ ions are released by the alkaline hydrolysis of thiourea ($SC(NH_2)_2$). (3) Precipitation of CdS takes place once the concentrations of $Cd^{2+}$ and $S^{2-}$ ions exceed the solubility of CdS.
CdS tends to stick uniformly on InP but not as much on BCB. After dipping the samples in agitated and heated (200 rpm at 65°C) chemical bath solution for 25 minutes, CdS coats the exposed pillars as seen from SEM image Fig. 18(b). Samples are rinsed in DI water and N₂ blow dried. To ensure good bonding of CdS to InP, the samples are annealed on a hotplate at 120°C for 1 hour in ambient air. To check the thickness of CdS deposited, a glass slide was place in the chemical bath under same conditions and measured to be around 50 nm using a Dektak profilometer.

![Figure 18. (a) Schematic of CdS coated nanopillars. (b) Tilted SEM image of polycrystalline CdS on InP nanopillars.](image)

### 2.3.4 Transparent Top Contact – ITO

To make separate top contacts for each of the devices, photolithography is performed to pattern square pads (750 µm by 750 µm) slightly larger than the device areas. AZ5214E, a positive photoresist (PR), is spin-coated at 3000 rpm to give a 1.3~1.4 µm thick coating. After a 1 minute bake at 100°C (hotplate in air), UV photolithography is done using a Karl Suss MA6 mask aligner. Another bake at 110°C (hotplate in air) for 1 minute and flood exposure for 1 minute completes image reversal. The unique wall profile of the PR caused by image reversal (Fig. 20) promotes liftoff later down the process.
An ULVAC sputtering machine (JSP 8000) is used to deposit indium tin oxide (ITO). ITO is commonly used as transparent contacts for photovoltaics and shows over 80% transmission over the visible to near-infrared spectrum of the sunlight spectrum \[49\]. Glass slides were coated first to calibrate for thickness and sheet resistance. The final recipe used produced a thickness of 200 ~ 250 nm and a sheet resistance < 20 Ω/sq. measured with Dektak profilometer and four-point probe respectively. Finally, samples are rinsed and soaked in acetone overnight for liftoff. Conformal coating of the ITO on the pillars can be seen in Fig. 19(b).

**Figure 19.** (a) Schematic of ITO sputtered onto nanopillars to form top contacts. (b) Tilted SEM of ITO coated nanopillars.

**Image Reversal Process**

(a) Mask alignment and UV exposure. With AZ5214E positive resist, exposed resist becomes soluble. (b) An image reversal bake at 110C cross-links the exposed resist, the rest remains photoactive. (c) A flood exposure makes the resist which was not exposed in the first step soluble in developer. (d) Resist is developed in AZ400K 1:3 diluted for 25 seconds. (e) Metal deposition. (f) Lift-off in acetone and NMP.

**Figure 20.** (a) Mask alignment and UV exposure. With AZ5214E positive resist, exposed resist becomes soluble. (b) An image reversal bake at 110C cross-links the exposed resist, the rest remains photoactive. (c) A flood exposure makes the resist which was not exposed in the first step soluble in developer. (d) Resist is developed in AZ400K 1:3 diluted for 25 seconds. (e) Metal deposition. (f) Lift-off in acetone and NMP.
Chapter 3. Measurements

The finished devices go through a set of measurements including dark-light I-V and EQE measurements. The following sections describe the measurement setups and present the performance of the InP/CdS core-shell nanopillar array solar cells.

3.1 Current Measurement

Under dark, the solar cell is essentially a large area pn diode. Current (I-V) measurements taken without light input can provide some information on the quality of the diodes. The aim is to have low leakage (minimum dark current), good rectification (on-off ratio), and low series resistance (ohmic contacts). Once a working diode is confirmed under dark, a light source is added in. With illumination, photocurrent, open circuit voltages, and fill factors can be extracted from the I-V data.

3.1.1 Setup

The I-V setup (Fig. 21) includes a probe stage, a Keithley source meter, and a Newport white-light lamp. The conductive stage is positively biased and comes in contact with the bottom of the sample, while a single probe acts as ground that contacts the top ITO pads. The source meter is controlled by a Labview interface which sets voltage sweep parameters and records current readings. The white-light source simulates the AM1.5 solar spectrum and is calibrated to 1 sun. The probe is manually adjusted and positioned under an optical microscope.
3.1.2 Results

Figure 22(a) records the dark I-V characteristics of one of the solar cell devices. From the I-V under dark, the InP/CdS nanopillar arrays have dark current in the $1 \times 10^{-7}$ range at -1 V bias. By fitting the diode equation given as

$$I = I_0 (e^{\frac{qV}{nkT}} - 1)$$

where $I_0$ is the dark saturation current, $q$ as unit charge of an electron ($1.6 \times 10^{-19}$ C), $V$ as the bias voltage, $n$ as the ideality factor, $k$ the Boltzmann constant and $T$ as 300K, one can approximate the ideality factor. For small forward biases ($V = 50 \sim 100$ mV), the exponential term starts to dominate and the -1 term can be ignored. Rearranging the above equation with the simplification, the ideality factor can be extracted by evaluating:

$$\ln(I) = \frac{q}{nkT}V + \ln(I_0)$$

which is the natural log of the current against the voltage.
The ideality factor, $n$, gives some insight on how the carriers in the diode recombine. In most cases, the value should fall between 1 ~ 2 for pn diodes when Shockley-Read-Hall (SRH) recombination dominates. Here the $n$ values are calculated to be 2.2 ~ 2.4 which indicate multiple recombination mechanisms are taking place and causing diminished current in forward bias. Studies have shown that sulfur and cadmium vacancies lead to radiative recombination in polycrystalline thin film CdS [51], [52]. Since the CdS used in this project is polycrystalline, it is very likely the high ideality factor is due to carriers recombining in the shell. Post-deposition annealing and activation treatments can be used to annihilate vacancies and improve performance [52]. High series resistance calculated to be in the $10^3 \ \Omega$ realm may also be hindering the current as the interface between ITO and CdS was not optimized. Electron barriers between the ITO and CdS (band offsets) can be lowered by incorporating an extra layer such as ZnO or SnO$_2$ [53]. Other recombination sites such as surface states on nanopillars are also known to hamper current output [19].

Figure 22. I-V data plots from one of the nanopillar solar cell devices. (a) Dark I-V. To evaluate a diode’s performance, dark I-V characteristics are analyzed for leakage currents, ideality factors and series resistance. (b) Dark/light I-V comparison. It is to be noted that the current density (current normalized to device area) has been used here for efficiency calculation purposes.
Moving on to Figure 22(b), light/dark I-V measurements show $V_{OC}$, $J_{SC}$ and FF of 0.53 V, 15.80 mA/cm$^2$, and 0.57 respectively. Combining this information, the energy conversion efficiency, $\eta$, is 4.8%. Ideally the $V_{OC}$ would be the built-in potential of the junction. The built-in potential between abrupt junctions can be estimated with the following [50]

$$\varphi_{bi} = \frac{kT}{q} \ln \left( \frac{N_A N_D}{n_i^2} \right)$$

where $k$ is the Boltzmann constant, $T$ as the absolute temperature, $q$ as unit charge, $N_{A,D}$ as acceptor or donor carrier concentration, and $n_i$ as the intrinsic carrier concentration. However, in the case of the heterogeneous junction of CdS and InP, the smaller bandgap of InP would be the upper limit at 1.34 V. Assuming a Zn doping concentration of $N_A = 10^{17}$ cm$^{-3}$ (adopted from Hall measurements of planar bulk epitaxy of p-InP), the predicted $V_{OC}$ was calculated from

$$qV_{OC} = kT \ln \left( \frac{N_A}{n_i} \right) + \frac{E_{g,InP}}{2}$$

which is closer to 1.26 V. Intrinsic carrier concentration, $n_i$, for InP is taken as $1.45 \times 10^7$ cm$^{-3}$. Actual $V_{OC}$ is lower because photon collection and carrier generation are not at 100%. The next section will look further into the quantum efficiency of the cells. Dark current also governs the $V_{OC}$ and is mostly determined by the quality of the materials. At the moment, crystallinity of the InP pillars have not been confirmed. Judging from the non-uniform pillar shapes in Fig. 15(b), quality of the material has room to improve. Some comparisons with similar works including hybrid polymer/inorganic nanowire and homogeneous InP core-shell nanopillar solar cells are shown in Table 1.
3.2 External Quantum Efficiency Measurement

3.2.1 Setup

The EQE setup is identical to the I-V setup with the exception of a lock-in amplifier and a Newport monochromator with a built-in chopper and filters to break down white-light into single wavelengths. The light is then guided and focused onto the probe stage. Calibration of spot size and intensity is done on a known commercial silicon solar cell. Labview program is used to setup the wavelength scan range of the monochromator and retrieve current data points from the source meter.

![EQE setup configuration](image162x169to451x301.png)

**Table 1.** Comparisons with reported nanowire (nanopillar) solar cells that use CdS or InP.

<table>
<thead>
<tr>
<th></th>
<th>$V_{oc}$ (V)</th>
<th>$J_{sc}$ (mA/cm$^2$)</th>
<th>FF</th>
<th>$\eta$ (%)</th>
<th>ref.</th>
</tr>
</thead>
<tbody>
<tr>
<td>this work</td>
<td>0.53</td>
<td>15.8</td>
<td>0.57</td>
<td>4.8</td>
<td></td>
</tr>
<tr>
<td>ZnO/CdS core-shell nanowire (ensemble)</td>
<td>1.55</td>
<td>7.23</td>
<td>N/A</td>
<td>3.53</td>
<td>[58]</td>
</tr>
<tr>
<td>MEH-PPV/CdS hybrid nanowire (ensemble)</td>
<td>0.83</td>
<td>3.8*</td>
<td>N/A</td>
<td>1.62</td>
<td>[59]</td>
</tr>
<tr>
<td>CdS/Cu$_2$S core-shell nanowire (single)</td>
<td>0.61</td>
<td>10.96**</td>
<td>0.808</td>
<td>5.4</td>
<td>[60]</td>
</tr>
<tr>
<td>InP core-shell nanopillar (array)</td>
<td>0.674</td>
<td>11.1</td>
<td>0.585</td>
<td>4.23</td>
<td>[61]</td>
</tr>
</tbody>
</table>

* Estimated from figure.
** Calculated from reported $V_{oc}$, FF, and $\eta$.

**Figure 22.** EQE setup configuration.
3.2.2 Results

Figure 23 records the external quantum efficiency (EQE) scanning from 400 nm to 1000 nm. It shows a peak around 550 nm to 580 nm of 40% EQE that gradually decreases until it rolls off at the bandgap of InP. Low EQE could mean that not enough carriers are generated or too many are recombining before they can be extracted. The EQE goes hand in hand with the short-circuit current observed previously. To improve the EQE, anti-reflection coatings and surface treatment of the nanopillars should be considered.

Figure 23. EQE measurements of the nanopillar solar cell.
Chapter 4. Conclusion

In summary, a quick method to combine CdS and InP nanopillars to make solar cells has been demonstrated. The structure is in a core-shell configuration where the CdS shell acts as both the window layer and the junction. Zn doped InP nanopillars is the core and the main absorber material. The CdS/InP junction is formed by chemical bath deposition of CdS which provides a simpler alternative to MOCVD growth of heterostructures. Fabrication steps are repeatable and suitable for larger area nanopillar arrays if needed. Performance-wise the devices show efficiencies up to 4.80% and have $V_{OC}$, $J_{SC}$ of 0.53 V and 15.80 mA/cm$^2$ respectively.

Future work involves more investigation and modeling of the interfaces between the InP core, polycrystalline CdS, and ITO. Each interface is critical for improving the leakage current, short-circuit current and series resistance through the device. Doping concentrations in the InP nanopillars are also being examined through capacitance measurements. How wide the depletion layer is and where the junction is can affect the open-circuit voltage of the cells. In fabrication terms, incorporation of the nanopillars into flexible substrates is also in the works. By removing the rigid semiconductor substrate from the devices, measurements can pinpoint nanopillars and rule out parasitic effects from the substrate. The substrate can be cleaned and re-used. Re-growth of pillars on the detached substrate has shown positive preliminary results.

This work successfully introduces a new fabrication method for core-shell nanopillar array solar cells. It adds to the arsenal of emerging photovoltaics and will expand the utilization of solar energy.
References


