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Electron Transport through Chemically-Derived Nanostructures

by

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Electron Transport through Chemically-Derived Nanostructures

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Andrew Kean Leong Lim
Electrical devices that combine the functionality of lithographically patterned semiconductor circuits with the flexibility inherent in chemical systems present an opportunity to explore fundamental physical processes and simultaneously, to address more practical applications. This dissertation describes efforts to make such chemically-derived structures, by incorporating individual nanometre-sized molecules (C_{60} and semiconductor nanocrystals/nanorods) into a single electron transistor geometry. Electrical transport measurements are used to characterise these devices.

A significant barrier to building these devices is the difficulty in connecting electrodes from the external metre-sized world where measurements are made to a nanometre-sized object. One solution is to place the molecule in a junction formed by the electromigration-induced failure of a metal nanowire, a technique that produces electrically stable transistors in surprisingly high yields. Understanding the process of junction formation is not only of intrinsic interest, but it has also proven to be a highly reliable diagnostic tool to differentiate between successful devices and tunnel junctions not containing the sample molecule.
The fabrication of $C_{60}$-based single electron transistors was one of the first applications of this method. Extensive transport spectroscopy was performed on these devices by tuning parameters such as the transistor bias voltage, the applied electric and magnetic fields and the temperature. The electronic and vibrational degrees of freedom of the cluster appear to couple during electron transport and a model for this behaviour was proposed, based on molecular oscillations within a transistor junction. On several occasions, individual $C_{60}$ molecules were well connected to the junction electrodes, permitting observation of the Kondo effect in these devices.

The break-junction technique was also used to create single electron transistors based upon colloidal semiconductor nanocrystals, facilitating spectroscopy on a semiconductor material that is quantum confined in three dimensions. The techniques to produce these nanocrystals are chemically quite flexible and recent syntheses have produced elongated nanorods where confinement is lost in one direction (resulting in a one-dimensional quantum wire). Preliminary experiments on these objects exhibit an intriguing dependence on the applied magnetic field.
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Finally, to my parents and family, thank you for giving me opportunities to pursue my curiosity throughout the years. I am happy with the choices that I have made and the path that they have led me to follow. Hopefully the latest move will be as successful …

Andrew Lim
Berkeley, California
August 2000
Chapter 1

Introduction

1.1 Definitions and Motivations

Demand for high performance integrated circuits has forced the semiconductor industry to miniaturise their components aggressively with each new generation. Optical lithography, the most common technique for producing microelectronic devices, has advanced the minimum feature size from 1.5 microns in 1985 to 130 nm, the state of the art in 2000 [1]. Even smaller features are possible using electron beam writing (down to 20 nm) [2,3]. Simultaneously, synthetic chemists have been building larger chemical systems of greater complexity by mimicking processes that occur in nature (so-called “biomimetic” strategies). Self-assembly techniques are used to organise simple molecular units into stable three-dimensional structures up to 100 nm in size [4-6]. Examples include self-assembled monolayers [7-10], organometallic supramolecular complexes [5,11], templated crystals [12] and dendrimers [13-17]. At the convergence of these two approaches lie nanostructures, a term that loosely describes a structural motif that has been constructed from a set of nanometre-sized components (see Figure 1-1).

The scope of this definition is vast, ranging from devices fabricated a few at a time, such as photovoltaic cells based on nanocrystalline materials [18-20] to the largest of the massively parallel self-assembled structures described above. It includes biological structures such as DNA tiles [21,22] as well as entirely artificial ones (quantum wells and quantum dots grown by
molecular beam-epitaxy for example [23-25]). In this dissertation, we shall concentrate on a subset, namely systems where a small number of nanometre-sized chemical species have been incorporated into electrical circuits defined by lithographic patterning. To do this successfully is one of the major challenges in this field and therefore this is our first objective, to make “novel” chemically-derived nanostructures.

What is our motivation for studying these nanostructures? From a fundamental scientific perspective, they provide a platform to probe the physical properties of the molecule that has been inserted, often producing information complementary to previous efforts (compare studies of transport through semiconductor nanocrystals to measurements made using optical spectroscopy,
for instance [27,28]). In the process, the nanostructure as a whole may show characteristics that are desirable for certain applications. One of the best examples is the single electron transistor [29-31]. This device is essentially a three-terminal field effect transistor, in which electrons tunnel from one electrode onto a central island (which may consist of individual molecules) and off onto a second electrode. A third electrode (called a gate) can be used to turn the current flow on and off. The components of this object are shown in Figure 1-2.

Previous experiments on single electron transistors have shown that they can act as electrical switches [32-34]. Devices based on molecules offer an opportunity to tailor these switching characteristics, since the details of current flow will be determined by which molecule is chosen as the central island. When working properly, these transistors should be important components of nanometre-sized electrical circuits – not only are they small, but frequently they can be manipulated using techniques that are compatible with other elements in the system (they do not need high temperature processing, for instance, which is often required in semiconductor

Figure 1-2 Elements of a single electron transistor. Electrons tunnel from the source onto the molecule and off onto the drain electrode. The gate can be used to turn current flow on and off.
fabrication). We shall confine our discussion to single electron transistors based on individual molecular clusters. The second objective of this project, then, is the electrical characterisation of such devices using various forms of transport spectroscopy.

The electrical characteristics of the transistor will be strongly influenced by the small (nanometre) size of the central island (the cluster in this case) through which electrons must flow. A theory exists to describe transport in this regime, known as the Coulomb Blockade model and we shall summarise its main features in Section 1.2. Much experimental work on single electron transistors has already taken place (historically with metal quantum dots and GaAs/AlGaAs 2-Dimensional Electron Gas or 2DEG systems) and we make note of the most significant accomplishments in Section 1.3. This discussion will also give a perspective of our niche in this field. The chapter concludes with an outline of the remainder of this dissertation (Section 1.4), focusing on our efforts to make and then to measure single electron transistors based on three molecular systems, C$_{60}$ and semiconductor nanocrystals and nanorods.

1.2 Energy scales and transport in the Coulomb Blockade theory

In this section, we introduce a model for transport through single electron transistors, the Coulomb Blockade theory and extract several key energy scales that will help explain some of our experimental results. This description is not intended to be exhaustive and we refer the reader to other articles to provide a comprehensive review of recent theoretical and experimental advances [35-37].
Consider the situation depicted in Figure 1-2. A cluster with a fixed number of electrons \( n \), is isolated from the external environment by energy barriers between it and the source, drain and gate electrodes. Initially, the source and the drain are kept at the same potential and no additional electrons can tunnel onto the cluster. Tunnelling can be induced by appropriately changing the energy level of one of these electrodes, which leads to the addition or removal of one electron. The corresponding change in its Coulomb energy (known as the charging energy, \( U \)) can be expressed in terms of the capacitance \( C \) between the cluster and its environment. Using basic electrostatics, the change in the electrostatic potential required to add one electron to the cluster is then \( U = e^2/C \), where \( e \) is the fundamental electron charge.

We can obtain an estimate for the charging energy as follows [38]. Firstly, we carry out a calculation of the electrostatic energy of half of the system (one electrode) in this configuration. The cluster is represented as a spherical equipotential shell of radius \( r \) with all of its charge concentrated at a point at the centre, lying above an infinite plane at zero potential. The edge of the sphere and the plane are separated by a distance \( d \) and a material with dielectric constant \( \varepsilon \) occupies the region between them. The capacitance between the sphere and the plane is given by:

\[
C \sim \varepsilon \frac{r}{2d} \quad (1-1)
\]

Secondly, we choose to neglect the capacitance to the gate since it is usually at least an order of magnitude less than the capacitance to either the source or drain electrodes in our device geometries. We approximate the total capacitance of the cluster as twice the capacitance to one electrode and hence the charging energy is:

\[
U = \frac{e^2}{C} = \frac{0.6}{\varepsilon r} \left(1 + \frac{r}{2d}\right)^{-1} \text{ eV·nm} \quad (1-2)
\]
For a cluster 0.7 nm in diameter (C$_{60}$ for example), embedded in a medium of dielectric constant 1.5 and separated from each electrode by 0.15 nm (which corresponds well to the 1 nm electrode separation in our junctions), the charging energy is ~525 meV.

In the molecular systems we are studying, another energy scale of significance is the energy spacing between discrete quantum levels, denoted $\Delta E$. Addition of an electron, therefore, requires an energetic barrier of $(U + \Delta E)$ to be overcome. For CdSe nanocrystals 6 nm in diameter for example, $U \approx 50$ meV and $\Delta E \approx 20-50$ meV, depending on which energy level is being populated.

To observe single electron charging phenomena, we must ensure that the energy $(U + \Delta E)$ exceeds the ambient thermal energy, $k_B T$ (where $k_B$ is the Boltzmann constant and $T$ is the temperature). Figure 1-3 is a summary of several energy scales relevant to C$_{60}$ and to CdSe nanocrystals/nanorods. Immediately we can see that the charging energy and the quantum level spacing will be significant in C$_{60}$ even at room temperature, making it a candidate for a room-temperature single electron transistor. Other excitations (such as vibrational modes) require the use of lower temperatures to guarantee that they are not smeared out by thermal fluctuations (in practice, we measure at the lowest temperature attainable to achieve better resolution of spectral features and to minimise device noise). CdSe transistors should exhibit stable behaviour at 77 K and in the past, we have taken reliable spectra from these devices at this temperature.

An additional requirement must be met to observe single electron charging. The potential barriers in the system must be sufficiently opaque that the number of electrons on the cluster is fixed on the timescale of a tunnelling event. Otherwise, electrons would be able to flow through the equivalent of a narrow wire (an Ohmic contact) rather than tunnel through the potential barrier to the cluster. The transition between current flow in the Ohmic and tunnelling regimes occurs when
the resistance of the potential barrier \( R \) exceeds the resistance quantum, that is if:

\[
R >> \frac{\hbar}{e^2} \sim 25.8 \text{ k}\Omega
\]  \hspace{1cm} (1-3)

where \( \hbar \) is the Planck constant. In our transistors, this condition is consistently attained.

We are now ready to formulate a simple description of transport through the cluster, based on the energy considerations outlined to date. Consider the energy level diagram shown in Figure 1-4A. It depicts the electrochemical potential of a cluster (\( \mu_{\text{cluster}} \)) at particular source-drain and gate
Figure 1-4 Coulomb blockade in a single electron transistor. (A) A situation in which current flow is blocked. The electrochemical chemical of the cluster with \( n+1 \) electrons exceeds the electrochemical potential of both the source and drain electrodes. (B) In this case, a voltage \( V \) is applied, allowing an electron to tunnel from the source electrode onto the cluster (giving it \( n+1 \) electrons). The additional electron immediately tunnels off, returning the cluster to the \( n \) electron state. The process repeats and a macroscopic current flows. Adapted from Kouwenhoven et al. [36]
voltages. The states in the source and drain are filled up continuously to their Fermi levels (denoted by $\mu_{\text{source}}$ and $\mu_{\text{drain}}$) and an external potential $V$ is used to bias these two electrodes with respect to each other. The solid energy levels of the cluster represent filled states with $n$ electrons, while the dotted levels represent (currently unfilled) states with $n+1$ electrons. The difference in the electrochemical potential between these two states is given by $(U + \Delta E)$.

In the scenario shown in Figure 1-4A, a bias voltage is applied to the source and drain electrodes such that $eV = \mu_{\text{source}} - \mu_{\text{drain}}$. The cluster is stably occupied by $n$ electrons, since $\mu_{\text{source}}$ and $\mu_{\text{drain}}$ are both higher than the electrochemical potential of the $n$ electron state $\mu_{\text{cluster}}(n)$, which means no electrons can tunnel off, but lower than the electrochemical potential of the $n+1$ electron state $\mu_{\text{cluster}}(n+1)$ which means no electrons can tunnel on. Consequently, no current flows and we are in the Coulomb Blockade regime.

The condition for current to flow (which means an electron can either tunnel on or tunnel off to initiate conduction) is that there must be a level in the energy window between $\mu_{\text{source}}$ and $\mu_{\text{drain}}$. An example might be $\mu_{\text{source}} > \mu_{\text{cluster}}(n+1) > \mu_{\text{drain}}$. If this is the case, then an electron will tunnel onto the cluster (after that process, it has $n+1$ electrons). Since $\mu_{\text{cluster}}(n+1) > \mu_{\text{drain}}$, the excess electron will promptly tunnel off, leaving $n$ electrons on the cluster once more. The process will repeat itself endlessly, leading to macroscopic current flow (it is depicted in Figure 1-4B).

There are two main methods to shift the electrochemical potential of the cluster so that it lies within the energy window. The gate can used to generate an external electric field that changes $\mu_{\text{cluster}}$, without directly participating in current flow. If the gate voltage is swept in the positive direction, states with additional numbers of electrons will move consecutively into the source-
drain window (since positive voltages will tend to stabilise electrons on the cluster). As each one passes through, it will produce a peak in the conductance as the cluster fluctuates between \( n \) and \( n+1 \) electron states. These are known as *Coulomb oscillations* and a plot of conductance versus gate voltage will show a series of these at regular intervals. In between each oscillation, the number of electrons on the cluster is again stable and no current will flow.

In the second method, the bias voltage can be changed to access states with additional electrons. Starting from the situation shown in Figure 1-4A, the voltage can be increased until \( \mu_{\text{source}} = \mu_{\text{cluster}}(n+1) \), whereupon an electron can tunnel onto the cluster and current will flow. Note that the position of \( \mu_{\text{cluster}}(n+1) \) will also change in response to changes in the electric field when the bias voltage is changed. Raising the bias voltage further will produce no significant changes in the current level (at least in this simple model) until \( \mu_{\text{cluster}}(n+2) \) has been exceeded. At this point, a second conduction pathway opens and the current level increases yet again. A plot of the current as a function of the bias voltage should produce a series of current steps and hence the overall structure is known as a *Coulomb staircase*.

We have just described one simple scenario for conduction. A complication that often occurs is a situation where many energy levels of say the \( n+1 \) electron state lie within the energy window, with the constraint that the \( n+2 \) electron state is still not accessible, that is \( \mu_{\text{cluster}}(n+2) > \mu_{\text{source}} > \mu_{\text{cluster}}(n+1, \text{ ground and some excited states}) > \mu_{\text{drain}} \). Electrons can tunnel into any one of the \( n+1 \) electron states and this will manifest itself as peaks in the conductance as each excited level becomes accessible.
As it stands, our model, while primitive, is sufficient to explain most of the experimental features we have observed. We can now proceed to a historical review of the systems to which Coulomb blockade theory has been applied, before concluding with a description of our own efforts.

### 1.3 A brief history of the field

Experiments on single electron charging began in the 1960’s with studies of transport through granular thin films using metal-insulator-metal tunnel junctions. Examples include work by Giaever and Zeller [39] and Lambe and Jaklevic [40]. In 1975, Kulik and Shekhter proposed a theory to account for these experimental results and it forms the basis of much of our current understanding [41].

A limitation of this early work was the inability to isolate and measure individual grains to remove the effects of averaging. This objective was only met in the mid-1980’s with advances in fabrication technology. Fulton and Dolan made and measured Coulomb oscillations in aluminium tunnel junctions in 1987 (using thin film deposition techniques that are relevant to us even today) [42]. Studies of similar metal dots have explored superconductivity [43] and spin-polarised [44,45] transport in mesoscopic systems, using increasingly complex device geometries (such as suspended tunnel junctions [46,47]). These dots have been incorporated into innovative nanostructures such as electron turnstiles and pumps [48] and recently, an aluminium single electron transistor was mounted on an optical fibre and used as a scanned electrometer [49-51].

Simultaneously, research has been carried out on quantum confinement in semiconductor heterostructures (mostly using high mobility GaAs/AlGaAs 2DEG systems grown by molecular
beam epitaxy, in which electrons are confined to the interface between these two materials) [52,53]. Initial efforts employed dots that resemble pillars and they exhibited resonant tunnelling effects through quantum levels [54]. More recent experiments have fully depleted the dot of its electrons, establishing the existence of a shell structure akin to the hydrogenic orbitals in atoms [55,56].

Much work has also been undertaken on laterally confined heterostructures, in which lithographically patterned electrodes and selective etching are used to confine the 2DEG into a quantum dot [53]. Early results in these systems include the observation of quantum levels in these “artificial atoms” [57,58], the coupling of individual dots into “artificial molecules” [59-61] and the coupling of photons into the electron tunnelling process [62,63]. One recent result of note is the observation of the Kondo effect in a quantum dot (an experiment that is particularly relevant to us, see Chapter 4) [64-67].

In the latter half of the 1990’s, developments in electron beam lithography and scanned probe microscopy have opened up a new domain known as “molecular electronics” that attempts to combine nanometre-sized materials into molecular scale electronics or to tailor them as molecular materials for electronic applications (using rotaxanes as switches for instance) [68-70]. Theoretical interest in the field dates back to 1974 [71], but there were few successful experiments in the interim and that alone is a testament to the considerable practical difficulties that must be overcome to realise these devices.

One of the first experiments to measure transport through a few molecules involved two-terminal studies of conjugated aromatic systems, establishing diode-like behaviour in these devices [72]. Recent theoretical studies have shown that current amplification can be achieved with these
junctions, by adding a third (gate) electrode [72]. In the interim, bistable molecular rotaxanes have been incorporated into switches with very high on:off ratios even at room temperature [70]. Unfortunately, the switching process is irreversible at present, although there are indications that this problem has been overcome [73].

Transistors have been made from individual single-walled carbon nanotubes that display semiconducting behaviour [74]. Most importantly, they operate reliably at room temperature, an absolute requirement for any practical application. These devices exhibit abrupt current turn-on characteristics and rapid switching times (~100 MHz), both desirable features. Metallic nanotubes have been shown to be ballistic conductors over micron length scales, addressing the issue of nanometre-sized interconnects, which would be needed to shuttle electrons through these systems [75].

Research on chemically-derived single electron transistors began in Berkeley with attempts to incorporate metal (gold) and semiconductor (CdSe) nanocrystals into two-terminal tunnel junctions, tethering them in place with linker molecules [38,76]. Measurements at low temperature yielded Coulomb staircase behaviour and it was decided to add a gate electrode to complete the field effect transistor geometry. Subsequent experiments produced additional characteristics of single electron charging, including Coulomb oscillations as well data on the excited state spectrum of the nanocrystals [34,38]. Several groups have duplicated and extended these measurements to other nanocrystals such a silver, platinum and palladium [77-79].
1.4 To the rest of this dissertation

What is our niche in this field? Recall from Section 1.1 that the objectives for this project were two-fold: to make novel nanostructures constructed around individual molecules and to probe their electrical characteristics using transport spectroscopy. We have carried out research on single electron transistors based on C\textsubscript{60} as well as semiconductor nanocrystals and nanorods and these efforts are detailed in the remainder of this dissertation (as outlined below).

One of the major obstacles to successful experiments on these nanostructures is making the electrical connection between a nanometre-sized object and the outside world where measurements are performed. We choose to focus on one method for doing so – wiring the molecule using break-junction electrodes made by the failure of a metal nanowire (Chapter 2). This chapter also provides comments on microfabrication procedures and it should be used in conjunction with the detailed manufacturing instructions in Appendix A.

We return to complete the characterisation of break-junction formation in Chapter 3. The procedure generates gaps of ~1 nm routinely and we discuss the underlying physical process as well as practical issues such as device yield. It was found that considerable information about the electrical behaviour of the resulting transistor could be obtained by monitoring the conductance as the nanowire fails and we detail this correlation.

In Chapter 4, we open the discussion of specific chemical systems with an analysis of electrical transport through a C\textsubscript{60}-based single electron transistor. Results of note include evidence for a coupled electro-mechanical oscillation that occurs when electrons tunnel onto or off the C\textsubscript{60} cluster. We propose a model (colloquially dubbed vibraBall) to account for these observations.
Other devices showed characteristics indicative of the Kondo effect, which manifests itself as finite zero bias conductance due to spin-flip transport through the cluster.

Two systems that exist in the limit of strong quantum confinement are discussed in Chapter 5, namely semiconductor nanocrystals (zero-dimensional structures) and nanorods (1-dimensional objects). Both show characteristics of single electron charging in our device geometry and we describe efforts to probe their energy spectrum using a combination of applied electric and magnetic fields as well as the temperature dependence.

Finally, in Chapter 6, we conclude this dissertation with a summary of our experimental work and some thoughts on the directions for future research.
References and Notes


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Chapter 2

Single Electron Transistors: Device Fabrication

2.1 Introduction

Historically, nanometre-sized chemical systems have been studied extensively here at Berkeley. One group that has received much attention are colloidal metal and semiconductor nanocrystals between 2-10 nm in diameter [1,2]. Nanocrystals of this size were thought to have particularly interesting electron transport behaviour, leading to efforts to insert them into electrical circuits and then to probe the characteristics of the resulting device under different external conditions (temperature, applied electric and magnetic field and photo-excitation for example) [3,4].

A fundamental question in all experiments involving nanocrystals (and indeed other samples with the same size scale, such as C_60 and semiconductor nanorods) is how to connect individual or a few nanometre-sized objects to the metre-sized external world where measurements are made [5,6]. Traditional fabrication techniques used by the semiconductor industry are inadequate to meet this challenge and so they had to be adapted to meet our needs [7,8]. Quite generally, our design uses electron-beam lithography to define two very sharp, closely spaced electrical contacts (electrodes or leads) onto which the sample molecules are deposited. A voltage bias is applied between the electrodes and the resulting current flow measured.

Initial experiments examined gold and cadmium selenide nanocrystals. Remarkably, their electrical (voltage-current) characteristics showed behaviour reminiscent of the single electron
charging effects observed in GaAs devices (Chapter 1) [9]. Pursuing the analogy, we decided to add a third electrode, a gate, which can be used to apply an external electric field to the molecule and hence to shift its energy spectrum. This device is known as a single electron transistor (SET), as shown schematically in Figure 2-1. Here a molecule resides or is tethered between the source and drain electrodes, forming a tunnel junction through which electrons can flow. The whole junction lies on an insulating silicon dioxide layer that separates it from a highly doped silicon substrate that acts as the back gate.

The design and fabrication considerations necessary to produce the device are described step-by-step in this chapter. An outline of the actual procedure is presented in Figure 2-2. In the first two or three steps (gate, gate contact and metal1/metal2), layers of insulating material and metal interconnects are laid down on a silicon substrate. The process involves photolithographic patterning, which is carried out in parallel on the entire wafer. It is described in Section 2.2. In the
Growth of field oxide

Growth of gate oxide (gate layer)

Contacting the gate (gate contact layer)

Defining metal interconnects and bonding pads (metal1 and metal2 layers)

Defining active junction areas (e-beam layer)

Deposition of sample molecule

Packaging and wire-bonding

Figure 2-2 Major fabrication steps for a single electron transistor.
next step, the crucial active junction areas are fabricated. Here the device electrodes are generated using electron-beam lithography, a much slower process and only subsections of the wafer (individual die or small blocks of die) are processed at once.\textsuperscript{a} We use two junction designs. In the first, a small gap is left between the electrodes into which the sample molecule can be deposited (known as \textit{small-gap junctions} and described in Section 2.3). In the second, the electrodes are allowed to overlap intentionally, the sample molecule again deposited and the junction broken by passing a large current through it (known as electromigration-induced \textit{break-junctions} and described in Section 2.4) [10].

Finally, we address an important issue when making devices involving small molecules, namely how to characterise the exact topology of the junctions with respect to the sample molecules. An attempt was made to build a SET that could be viewed in a high-resolution transmission electron microscope (TEM). This is described in Section 2.5. The complete instructions to reproduce any of these devices can be found in Appendix A.

\textsuperscript{a} To clarify the terminology used here, individual SET’s with sample molecules deposited are referred to as \textit{devices}, comprising the source and drain electrodes (known together as the \textit{junction}), the sample molecule and the back gate. A \textit{die} consists of a fixed number of junctions wired in common. Multiple, electrically separate die are printed on the full \textit{wafer}. The wafer may be broken up into sub-units called \textit{blocks} for fabrication purposes.
2.2 Basic fabrication: insulating layers and interconnects

2.2 (i) Growth of the field oxide

The starting materials are 4-inch (100) silicon wafers, degenerately n-doped with arsenic to a room temperature resistivity between 0.001 – 0.005 $\Omega\text{cm}$ ($10^{19} – 10^{20}$ dopant atoms/cm$^3$). It is this substrate that serves as the back gate for the device. The high level of doping is required to ensure that the silicon conducts as a metal even at the low temperatures (down to 300 mK) routinely used in these measurements [11].

A uniform layer of silicon dioxide (1 $\mu$m) is first grown on top of the entire wafer (the field oxide). It serves primarily as an insulating barrier to prevent any conduction between the gate and the junction lying above once a voltage difference is applied between them. Additionally, it prevents accidental electrical shorting resulting from the final wire-bonding step shown in Figure 2-2 and this purpose determines the actual thickness of the layer. The oxide is grown by wet thermal oxidation of the silicon wafer at 1100 ºC for 3 hours in a steam environment in a CMOS clean, resistively-heated furnace tube. Cleanliness is an issue: ionic contamination (particularly Na$^+$) can severely diminish the dielectric properties of the oxide and any particulates will result in an uneven coverage of the substrate [12].

2.2 (ii) Growth of the gate oxide

In the active junction regions of the device, it is desirable to maximise the electrostatic (capacitive) coupling between the gate and the molecule above. This is achieved presently by
minimising the thickness of the oxide there. These areas are defined using photolithography and then holes are etched in the field oxide all the way back to the silicon substrate (using HF buffered oxide etch). A thin layer (30 nm) of silicon dioxide (the gate oxide) is then re-grown in these regions by dry thermal oxidation of silicon at 900 °C for 2 hours in an oxygen-only environment. The resulting silicon dioxide profile, with the thick field oxide and the thin gate oxide, is shown in Figure 2-3. A combination of low growth temperature and the oxygen-only environment produces a very high quality silicon dioxide layer with fewer defects and hence superior dielectric breakdown properties. Dry oxidation is too slow (and unnecessary) for growing thicker oxide layers (such as the field oxide) [15].

The current design layout, the set series, incorporates several improvements in gate oxide performance over its predecessors. It was observed through experiment that devices made using the older dklein layout exhibited significant leakage current between the back-gate and the junction above. In approximately one-third of the die, the resistance between the gate and the central ground bar was measured to be ~10 kΩ – 100 MΩ at 1.5 K with ≤30 V applied gate voltage, which is inadequate for our purposes. We sought to eliminate this problem and at the same time, to increase the capacitive coupling of the gate to the junction, which involved thinning the gate oxide from 70 nm (dklein series) to 30 nm (set series).

b A more profitable approach may be to use an insulating material with a higher dielectric constant than silicon dioxide (ε = 3.9). The semiconductor industry has identified several possibilities, including Ta₂O₅ (ε=25) and (Ba,Sr)TiO₃ (ε = 300). The former is probably a better near-term option: it is a more mature technology and it appears to be quite compatible with our current process design [13,14].
The most important change to the die layout was to confine the areas of thin oxide to the active junction regions only. This minimises conduction through any ionic defects, stress dislocations or pinholes present elsewhere in the silicon dioxide. Previously, 136 000 \( \mu \text{m}^2 \) of thin oxide lay between an electrode and the gate. The current design reduces that to 9 000 \( \mu \text{m}^2 \), a potential 15-fold improvement (the difference is apparent optically, compare Figure 2-4, panels A and B). Conduction between the ground bar and the gate was significantly reduced by preserving thicker field oxide over most of that area. Higher quality gate oxide was also grown across the wafer by dropping the growth temperature (from 950 °C used previously), by doubling the post-oxidation \( \text{N}_2 \) anneal time and by observing stricter cleanliness protocols [16]. The net result is a lower oxide failure rate (presently only 10-15% of die show measurable conduction between the gate and ground bar at 1.5 K) and an increased dielectric breakdown field (>4 MV/cm at present, up from 3 MV/cm previously).

**Figure 2-3** Silicon dioxide profile after the growth of the gate oxide. Holes are etched in the field oxide below the active device regions and dry thermal oxidation used to grow high quality gate oxide.
Figure 2-4 Basic die layout, showing features fabricated by photolithography. In both cases, source leads run horizontally and a central (drain) ground bar runs vertically. Junctions are formed where they intersect. (A) In the set design, the gate oxide (30 nm) is confined to the 6 junction regions (shown by the arrows), while the blue region everywhere else is field oxide. (B) In the klein design, the much larger dark grey rectangle running most of the length of the ground bar is thinner oxide (70 nm). The lighter grey region is the field oxide. The four square pads at the corners of the die are electrical contacts to the gate.
2.2 (iii) Contacting the gate (set series only)

At this stage, the back gate is buried under a layer of silicon dioxide. To contact it electrically, the oxide is stripped from the back-side of the wafer (again using HF buffered oxide etch) and platinum deposited immediately onto the bare silicon. The entire wafer is subsequently annealed using rapid thermal processing in an Ar atmosphere to ensure the formation of an ohmic contact. It is imperative that a native silicon dioxide layer does not form on the freshly-etched substrate as the oxide will block diffusion of the platinum atoms into the silicon and hence prevent formation of the desired low-resistivity platinum silicide [17,18]. Platinum was chosen as the gate contact material in spite of this drawback since it is fairly inert chemically, thus expanding the range of situations in which these die are useful. If this feature is not desired, aluminium may be substituted since it will reduce any native oxide to silicon, forming an ohmic contact far more easily.

2.2 (iv) Defining metal interconnects and bonding pads

Metal interconnect and bonding pads are now patterned on the front side of the wafer. In the current scheme, all the ground electrodes are tied together to a central bar (see Figure 2-4A). Source electrodes are contacted independently. The interconnects and bonding pads are patterned simultaneously (using photolithography) in a two-step lift-off process. During the metal1 step, thin layers of chromium (3.5 nm) and gold (40 nm) are evaporated onto the front-side of the wafer. The succeeding metal2 step involves adding metal, chromium (3.5 nm) and gold (250 nm), on the bonding pads so that they just cover the edge of the gate etch trench.

This two-level “thin-thick” metallisation process (shown schematically in Figure 2-5) was chosen primarily to ensure that the electrodes adequately covered two step edges (that is, abrupt changes in topography), namely the edge of the gate etch trench (a 1 μm step), which is spanned by the
metal1/metal2 interconnects and the foot of the metal1 interconnects, which are spanned by the e-beam electrodes (to be written in the next step). The maximum thickness of the e-beam electrodes is approximately 100 nm (for reasons discussed below). Metal1 must be thinner than this (40 nm) to ensure the e-beam layer seals over it. However, metal of this thickness is not only insufficient to bridge the edge of the gate etch pit but also difficult to wire-bonded reliably. The thicker metal2 layer (250 nm) is added to addresses these concerns [15].

![Diagram](image)

**Figure 2-5** “Thick-thin” interconnect profile. The metal interconnects (metal1) must remain intact over the 1 μm step between the field and gate oxides (they are reinforced with an additional metal layer, metal2), yet be thin enough such that the e-beam metallisation can cover them.

This problem can also be solved by using sputtering instead of evaporation to deposit the metal layers. Atoms arriving from the sputtering target are not strongly collimated and therefore high angle or vertical features (such as the edge of the gate etch pit) will be better covered. In the semiconductor industry, this particular problem is addressed by recessing the field oxide into the silicon wafer (fully or partially recessed LOCOS for example [15]). This results in a wafer surface where the tops of the field and gate oxides are co-planar with no abrupt step edges between them.
2.3  **Small-gap junctions: the original design**

2.3 (i)  **Defining active junction areas**

The critical device areas, where individual nanometre-sized molecules connect to the electrodes, are defined at this point (the *e-beam* layer in Figure 2-2). “Standard” techniques are limited to features spaced by 30-50 nm, which is insufficient for this task [19]. We use a fabrication scheme that combines electron-beam lithography on a two-layer resist and an angle (or “shadow”) evaporation for the metallisation step, to produce junctions separated by less than 5 nm [20-23].

Electron-beam resist is spun over the entire wafer, firstly a 300 nm layer of methyl methacrylate/methacrylic acid (MMA/MAA) copolymer and then a 125 nm layer of poly(methylmethacrylate) (PMMA) polymer of approximately 950 000 Dalton molecular weight. Upon electron exposure, the copolymer becomes much more soluble in a developer solution than the polymer, an effect that is amplified as the copolymer layer receives additional dosage from electrons scattered from the underlying substrate. By taking advantage of this effect, two chevrons (or lines) drawn in the resist pointing at each other can generate a PMMA bridge that is completely undercut in one direction (see Figure 2-6). Metal is evaporated into this pattern. For

![Figure 2-6 Bilayer resist undercut. (A) The electron beam inscribes two closely spaced chevrons in the bilayer resist. (B) After development, the P(MMA/MAA) layer is undercut, leaving a free-standing PMMA resist bridge.](image)
this process, a thin, a high molecular weight resist top layer is preferred since it suffers less from the “proximity effect”, meaning that the pattern as drawn is preserved with higher fidelity.

A small-gap junction is produced subsequently by evaporating metal at an angle through the PMMA “shadow mask” layer (see Figure 2-7). Two depositions of chromium (3.5 nm)/gold (10 nm) are performed at ±15º to the normal. This produces images of the PMMA pattern that are shifted by 110-130 nm on the substrate, thus allowing the gap between the chevrons to be narrowed. Remarkably, the electrodes meet *underneath* the resist bridge. This rather convoluted process is necessary since any gap directly drawn this close together in the resist would collapse when developed. Finally, a layer of metal is evaporated vertically downwards to ensure good overlap of this layer with the metal interconnects. Note that we use an electron-beam evaporator to provide a well collimated metal source and hence sharply defined electrodes.

The yield of sharp electrodes spaced by <5 nm (our stated aim) never exceeded 10% for any extended period. Junction separations ranged from 5 – 60 nm, with a median around 30 nm. The radius of curvature of the electrodes at their tip varied between 20 – 50 nm, with a median around 40 nm. Empirically, it was found that the setup of the converted scanning electron microscope (SEM) used for lithography (its focus and astigmatism in particular) and the resist condition (especially thickness and moisture content) most crucially determined the quality of the junction. It was problematical to control both parameters simultaneously within the fine tolerances required to make the process work over any period of time. This foreshadows one of the improvements we sought in subsequent generations of devices (see Section 2.4).
Figure 2-7 Formation of a small-gap junction using angle evaporation. (A) Successive evaporations of Cr and Au are done at ±15° to the normal, forming a gap less than 10 nm wide (the thin gold layers). A third evaporation (the thick gold layer) deposits more metal to ensure good connectivity with metal1 interconnects. (B) Scanning electron micrograph of a fabricated junction. The thin gold layers are light grey and the thick gold white in colour.
Routine characterisation of the junctions after fabrication was also difficult until the introduction of high-resolution, field-emission SEM’s. The image in Figure 2-7B was taken using such an instrument. Unfortunately, any junction imaged in the microscope was useless for subsequent deposition of sample molecules (probably due to carbon contamination deposited on the substrate by the electron beam), severely curtailing efforts to use junctions of known separation.

2.3 (ii) Deposition of nanocrystals

Once fabrication was complete, the die was prepared for deposition of the sample molecule. Typically, either gold or CdSe nanocrystals (typically 3-6 nm in diameter) were tethered to the electrodes using bifunctional 1,6-hexanedithiol linker molecules [24]. A single die was cleaned in oxygen plasma (80 W for 4 minutes) and then immediately immersed in a saturated solution of 1,6-hexanedithiol in isopropanol (typically for 24 hours, although equilibrium coverage should be achieved in 6 hours). Ideally, the linker molecules should form a uniform self-assembled monolayer on the electrodes, one thiol end group binding to the gold electrodes, leaving the other end free to bind with nanocrystals [25]. Practically though, there are many pathways to deactivate the thiol functionality, including oxidation, disulfide bond formation and the formation of a 6-membered ring with both ends terminated on an electrode.

After removal from the linker solution, the die is immersed in either a solution of charge stabilised gold nanocrystals in water or in a solution of CdSe nanocrystals in toluene. An image of a completed device is shown in Figure 2-8. The coverage of nanocrystals is normally very high (approaching 30% on the electrodes), which belies the claim of a single electron transistor with one molecule in place. However, electron transport occurs by tunnelling (a very distance dependent mechanism) and so it is probable that one nanocrystal dominates the observed transport behaviour.
The fraction of working SET’s, that is those showing single electron tunnelling behaviour and some dependence of their I-V characteristic on the applied gate voltage, was very small (approximately 1% of the junctions tested). Of those, most devices were quite unstable, showing device “switching” and noise, perhaps due to interaction with neighbouring nanocrystals. Efforts to improve this yield culminated in the far superior break-junction method for constructing SET’s.

2.4 Break-junctions: improving single electron transistor yields

2.4 (i) Fabricating break-junctions

Break-junction single electron transistors were stumbled upon during efforts to improve the yield of small-gap devices. In one instance, a die was produced with many electrodes accidentally
shorted together (serendipitous nanowires). It was discovered that the nanowires could be broken by passing a large current through them, consistently leaving electrode separated by approximately 1 nm. Upon breaking, clean metal surfaces are presented to the sample molecule, which allows more reliable electrical contacts to be made. We focus on fabricating break-junction devices here and defer a discussion of their characteristics (such as junction morphology and device yield) to Chapter 3.

Nanowires are produced in essentially the same way as the earlier small-gap junctions, albeit with the lithographic patterns drawn so that the electrodes are overlapped at their apex once the metal angle evaporation is performed (Figure 2-9). A typical overlap is between 5-40 nm. The nanowires are broken by ramping a voltage bias on the junction and allowing a large current to flow (usually 3-10 mA at an applied bias of 100-500 mV). Above a certain voltage threshold, the junction will break with fairly characteristic behaviour [26].

During initial experiments, sample molecules were then deposited on the broken junctions, either with or without linker molecules. It was found, however, that more stable SET’s were produced if

![Fabrication of a break-junction.](image)

**Figure 2-9** Fabrication of a break-junction. (A) Successive angle evaporations form a narrow gold nanowire (20-40 nm) at the apex of the electrodes. Useful break-junctions are produced if the thickness of the nanowire is <20 nm. (B) A scanning electron micrograph showing the (lighter) overlapped region at the centre of the (darker) thin gold areas.
the sample molecule was deposited on intact nanowires and the junction cooled to low
temperature (usually 1.5 K in a flowing helium atmosphere) before breaking. This is the in-situ
method used currently.

In an example examining C\textsubscript{60}, a die containing the nanowires is cleaned in oxygen plasma (80 W
for 4 minutes). Approximately 0.3 mL of a concentrated solution of C\textsubscript{60} in toluene (stored in
quartz glassware to prevent oligomer formation [27]) is immediately deposited dropwise onto the
die, allowing time for the solution to dry between drops. The C\textsubscript{60} surface coverage can be
changed by changing the number of drops added. After drying, the sample is ready to be mounted
in its carrier and inserted into the cryostat for breaking. This procedure is used to generate most of
the SET’s discussed in subsequent chapters.

When it became apparent that we had a reliable method to generate SET’s, it was realised that the
next bottleneck would be the production of the nanowires themselves. We sought alternatives that
would allow large-scale production of these nanometre-sized junctions, a capability that may
become a necessity for future applications.

2.4 (ii) Manufacturing SET’s en masse

In 1998, the prospect of high throughput fabrication of nanostructures became available at
Berkeley. The key component was the Nanowriter electron-beam lithography system, which
consists of a Leica EBL100 lithography system that has been significantly modified by the Centre
for X-ray Optics (Lawrence Berkeley National Laboratory) [28,29]. It offers very high resolution
(<5 nm spot size) at high beam currents (500 pA, 100 kV). In comparison, the JEOL JSM-6400
scanning electron microscope used previously only offered similar resolution at 5-10 pA, 20 kV.
Here we have an immediate order of magnitude reduction in the time taken to write the e-beam patterns (which scales linearly with the beam current), yet with no loss of pattern definition.

The Nanowriter has other advantages when writing large areas. It uses an interferometric stage positioning system allowing very accurate registration between the e-beam layer and the metal1 interconnects (better than 30 nm across a 4” wafer), as well as stable focus compensation across the same distance. Both of these features are crucial in ensuring good reproducibility when many junctions drawn. This eliminates one of the major process variables alluded to in Section 2.3 (i).

We have also added flexibility to earlier steps by using a reduction stepper instead of a contact printer for photolithography. The stepper allows rapid and inexpensive changes in mask design on a master copy of the device layout, rather than being forced to change individual copies on a contact mask. The fabrication procedure now makes full use of standard 4” wafer handling techniques (thin film growth, etching and resist processing for example), lessening operator involvement and hence speeding up the process and reducing the risk of breakage.

Taken together, these capabilities allow multiple die and even entire wafers (nanotube superchip devices for example) to be processed at once, dramatically speeding up fabrication. Figure 2-10 shows this most graphically. In the current generation, 36 junctions can be printed in one session on each of 208 die on a wafer in a 4-6 hour period. In previous generations, we were limited to 4 or 5 die each containing 42 junctions in the same time. A remarkable time and resource saving!
2.5 Membrane structures: viewing the device morphology

One of the major problems encountered in experiments on these single electron transistors is simply characterising the device once it has been made. Even now, the molecules being studied are too small to be observed, except in certain circumstances by high-resolution, field-emission scanning electron microscopy (with an in-lens or immersion detector) or tapping mode atomic force microscopy (AFM). This section describes an effort to do so prior to the advent of these techniques. We attempted to make an entire CdSe nanocrystal SET on a free-standing silicon nitride (SiN)$^d$ membrane and then to view the device with transmission electron microscopy (TEM). This project was not pursued past initial testing, but the fabrication technique has been used elsewhere (in making SET nanopores for example [30,31]) and remains of interest.

$^d$ The silicon nitride is non-stoichiometric. Hence the use of the generic SiN instead of Si$_3$N$_4$. 

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Figure 2-10 Massively parallel nanostructure fabrication. (A) A single junction produced by the Nanowriter, (B) which is only one of a 4" wafer full of devices
Fabrication of the free-standing SiN membrane is a two step process involving [32]

- growth of the low-stress SiN
- patterning and bulk micromachining of the substrate

Junctions were subsequently built on the membranes using techniques similar to those outlined previously (albeit taking care not to break the 30 nm substrate). After deposition of the sample molecule (usually nanocrystals that were tethered to the electrodes using dithiol linkers), the device was subject to analysis in the TEM. Unfortunately, no devices were both imaged and then probed electrically.

2.5 (i) **Growth of the low-stress silicon nitride**

The starting materials are 2-inch (100), prime grade, single sided polished silicon wafers, a choice dictated by requirements for the micro-machining step (see next section). A uniform layer of silicon-rich silicon nitride (15 – 200 nm thick) is grown on the entire wafer by low pressure, chemical vapour deposition (LPCVD) at 835 ºC and 140 mTorr in a resistively-heated furnace tube. The chemical precursors are dichlorosilane (silicon source) and ammonia (nitrogen source) in a 4:1 ratio by flow rate. This produces a film that is self-supporting once the silicon substrate is etched away (it has a measured tensile stress of approximately 800 MPa). Increasing the silicon content will reduce film stress (down to ~50 MPa for a film grown with a 6:1 dichlorosilane:ammonia ratio), but it also increases the number of pinhole defects. This film will serve as the membrane support for the device as well as the insulating layer between a gate electrode deposited on the back-side of the wafer and the junction on the front-side.

2.5 (ii) **Patterning and bulk micro-machining of the substrate**

The silicon substrate must be etched away where the devices lie to enable viewing in the TEM (the 200 keV electrons used can pass easily through 30 nm of SiN, but not 250 μm of silicon).
This is done in a process called *bulk micro-machining* [15,19]. Firstly, the SiN is patterned photolithographically and then etched in a plasma of SF₆/He, exposing the underlying Si surface. The silicon is removed in aqueous KOH solution at 80 °C using the SiN as an etch mask. KOH is an anisotropic etchant that will stop with high selectivity on Si (111) planes – the (100): (111) etch rate is approximately 400:1. Starting with a (100) orientation wafer results in inward tapering etch pits, extending though the wafer and only stopping at the SiN layer on the other side. Typically, we start with square etch masks and so the etch pits resemble square pyramids (Figure 2-11).

2.5 (iii) **Patterning and imaging a nanocrystal-based device**

Construction of device electrodes and metal interconnects on the SiN membrane front surface employs very similar photo- and e-beam lithography processing as the steps described above, with a few caveats. Firstly, during resist processing (spinning and developing) and lithography, it is imperative not to use the vacuum wafer handling tools since they will apply unequal pressure across the membrane and break it. Wafers should be handled manually and if necessary, held in

![Figure 2-11 Anisotropic etching of Si (100). Using a SiN mask (bottom side), the bulk of the silicon wafer is removed using aqueous KOH. This etchant stops high selectively on Si (111) crystal planes and on SiN. The result is a free standing SiN membrane.](image)
place by clamping at the edges. Secondly, the dosages for e-beam lithography over a membrane are much higher than those over a full substrate since secondary exposure of the resist arising from electrons scattering back off the substrate no longer occurs. Typically, doses up to 1500 $\mu$C/cm$^2$ for the finest features and 300 $\mu$C/cm$^2$ for the interconnects were used, up to 2-3 times higher than the values for a device with a full substrate.

Each die contains four separate areas with free-standing membranes. Junctions are patterned on each membrane and then nanocrystals deposited on the entire die. Handling individual die at this stage is quite difficult since they are only 2 mm square – the size is constrained by the dimensions of the TEM sample holder. Imaging is carried out in a conventional Topcon 002B LaB$_6$-filament microscope at the National Centre for Electron Microscopy, Lawrence Berkeley National Laboratory. A representative device is shown in Figure 2-12. The electrodes here are very sharp.

![Figure 2-12](image)

*Figure 2-12* CdSe nanocrystal device fabricated on a SiN membrane. In this transmission electron micrograph, the dark grey regions are the particularly sharp gold electrodes, the lighter grey dots are CdSe nanocrystals and the mottled amorphous background is the membrane itself. At high magnifications, it was possible to resolve CdSe wurtzite lattice fringes in individual nanocrystals. The scale bar is 50 nm.
(despite slightly overlapping each other), a generic observation in all these junctions. This is most probably due to the absence of the substrate to back-scatter electrons during lithography. Hence only well-collimated incident electrons expose the resist, leaving much shaper electrodes. Note the high contrast between the nanocrystals and the amorphous membrane.

During the test and imaging phase of this project, approximately 100 junctions were observed. Junction separations ranged from overlapping to 50 nm, with a median of 20 – 30 nm (similar to the small-gap junction results), while the radius of curvature at the apex of the electrodes was consistently 10 – 30 nm. Membranes between 30 – 50 nm thick proved to be somewhat robust throughout fabrication and imaging (indeed, a wafer full of free-standing 30 nm membranes was thrown at high speed off the spin-coater, landing about a 50 cm away with fewer than one-quarter of the membranes being lost!). Major losses occurred when separating single die from the larger blocks and while handling with tweezers (approaching 50% in several instances).

Finally, efforts were made to realise a fully functional SET by evaporating a layer of aluminium on the rear of the membrane to act as the back gate. The few devices tested showed shorted connections between the gate and the electrodes above, possibly due to pinholes known to exist in the SiN membrane. Further, the presence of the aluminium layer significantly decreases the contrast between the nanocrystal sample and the substrate background, making TEM analysis quite arduous. At the same time, routine access to high resolution SEM became available, allowing us to characterise conventional devices made with a full substrate (a much simpler proposition). Membrane-based devices were therefore not pursued.
2.6 Summary

We have considered one of the main questions when examining chemically-derived nanostructures, that is exactly how to wire them up. This chapter traced each step in the fabrication of single electron transistors based on individual molecules, starting with large-scale device features (dielectric layers and interconnects) and progressing to the critical junction regions where the electrodes actually contact the sample molecules. For the latter, two alternatives are outlined: break-junctions made by the electromigration-induced failure of metal nanowires (currently used in C\textsubscript{60}-based SET’s) and junctions drawn so that the electrodes are spaced by a small gap (used for nanocrystal-based SET studies and potentially useful for studying nanorods). We also describe a device optimised for sample analysis in the TEM. In the next chapter, the focus shifts to the formation and transport characteristics of break-junctions.
References and Notes


32. D. Lieberman, personal communication
Chapter 3

Characteristics of Break-junctions

3.1 Introduction

The overall goals of this project are to make electronic devices based on nanometre-sized molecules and to measure their transport properties in a simple circuit. Until recently, simply producing two-terminal devices with electrodes spaced closely enough that they can be bridged with individual molecules with some certainty has been difficult [1-4]. Break-junctions made by the electromigration-induced failure of metal nanowires offer a solution [5].

Each nanowire consists of two overlapping electrodes fabricated using electron-beam lithography and shadow evaporation (full details can be found in Chapter 2). Passing a large current can break the nanowire at its weakest point (in a process akin to electromigration [6]), reliably producing junctions with about 1 nm separation. This is precisely the size regime of the molecules we wish to examine. Nanowires are broken with sample molecules either absent (generating a tunnel junction) or present (often resulting in a single electron transistor or SET).

In this chapter, we describe the systematic behaviour of break-junctions, addressing issues such as device geometry, yield and most importantly, electrical characteristics. We begin with bare nanowires in which the mechanism of failure is not complicated by interactions with sample molecules. Much is known about electromigration as a physical process, but studies by the
semiconductor industry tend to be confined to much larger metal lines (upwards of 500 nm wide) that are made from different materials (copper or aluminium rather than gold) [7-10].

The second part of the chapter addresses junctions where sample molecules have been deposited, the candidates for SET’s. This analysis raises a key question. When the nanowire is broken, can we unequivocally identify those devices where the sample molecule occupies the gap between the electrodes, rather than a fragment left over from the nanowire? One answer can be found through transport studies of the device (as discussed in Chapters 4-5). Another piece of evidence lies in the electrical characteristics of the nanowire while it is breaking: tunnel junctions and single electron transistors show markedly different conductance behaviour as a function of applied voltage. We shall re-visit this question throughout the chapter.

### 3.2 Nanometre-sized tunnel junctions

#### 3.2 (i) Breaking bare nanowires: methods and results

The nanowires used in these break-junction studies and to make SET’s are fabricated with the electrodes overlapping by 5 – 40 nm, with a median around 30 nm. The apex of each electrode is usually quite sharp, with a radius of curvature between 20 – 40 nm. A representative junction is shown in Figure 3-1A. Current fabrication techniques permit nanowires of this quality to be produced very consistently, allowing much greater control over the formation of tunnel junctions and SET’s.

After initial preparation by cleaning in oxygen plasma, the nanowires are electrically connected in the four-terminal configuration shown in the inset to Figure 3-1. Two terminals are connected to a
Figure 3-1 Bare break-junctions measured at 1.5 K. (A) SEM image of a nanowire and (B) its 4-terminal, low bias I-V trace. (C) Breaking trace of a clean nanowire, showing a sudden, characteristic drop in the conductance. Just prior to that, a small decline in conductance is routinely observed (blue arrow). (D) SEM image of a broken junction showing a break in the thin gold part of the electrode (dark grey) near the thick gold section (white), resulting in (E) a stable tunnel junction. Inset: 4-terminal measurement configuration.
voltmeter (in actuality a voltage preamplifier) to measure the voltage drop across the junction, while the other two terminals are connected to the current source. In an ideal setup, this arrangement removes the contact resistance (the resistance arising from the interface between the electrodes and the sample molecule and from the wires leading up to the sample), consequently allowing more accurate measurement of the resistance of the junction alone. Figure 3-1B depicts a low-bias current-voltage (I-V) trace taken of the junction in Figure 3-1A at 1.5 K while using the 4-terminal configuration. The resistance value (30 Ω) is typical of the nanowires used in these experiments.

The applied voltage is now ramped steadily from zero at 30 mV/s. At low current levels, the conductance remains fairly constant (of the order of 10 mS) as seen in Figure 3-1C. Once the voltage drop across the junction approaches 500 mV (with about 5 mA of current flowing), there is a distinctive dip in the conductance (blue arrow), indicating the onset of electromigration at the weakest point in the nanowire. The atoms there will rearrange under the large local electric fields (>10 MV/cm) and ultimately, there will be a second sudden drop in the conductance below the conductance quantum (38.7 μS) as the nanowire finally breaks [11]. This behaviour is characteristic of junctions formed in the absence of sample molecules (contrast this with the breaking traces of C₆₀ SET’s in Section 3.3 where the conductance can fluctuate for an extended period).

A scanning electron micrograph (SEM) of a junction after nanowire failure is shown in Figure 3-1D*. The break apparently occurs in the thin gold region of the right electrode near the start of the

* It was not possible to image this junction in the SEM prior to breaking, since contamination caused by the electron beam (probably from polymerisation of organic residue) will dramatically affect the transport
thick gold (white area). The location of the actual gap between the electrodes varies from sample to sample, depending on the microscopic structure of the original nanowire. Figure 3-1E depicts an I-V trace from such a device. It shows an exponential increase in the current as a function of the bias voltage that was stable up to 200 mV in this case (in other instances, the junction was stable to voltages exceeding 1 V). There was also no dependence on the applied gate voltage. Cumulatively, such behaviour is typical of single tunnel junctions and it was found that most nanowires broken without sample molecules exhibit conductance characteristics similar to this example.

Experiments have been carried out on several hundred junctions from different fabrication runs, mostly at low temperature (1.5 K) in a flowing helium environment. Figure 3-2A shows the critical voltage (measured in a 4-terminal configuration) and the current at which a selection of junctions fails. There appears to be a voltage threshold of approximately 500 mV that must be exceeded before electromigration will occur, but little dependence on the current flowing through the wire (breaking currents vary from 3 – 15 mA). Naïvely, this suggests a process with an activation barrier, although the actual details are probably complicated by the presence of atomic defects and strain in the metal film. Electromigration will be discussed more fully in Section 3.2 (ii).

Irrespective of the mechanism of formation, break-junctions formed at liquid helium temperatures show tunnelling resistances ranging from hundreds of kΩ to over 100 GΩ, with a median around 10 GΩ (see Figure 3-2B). Previous measurements on tunnelling between two gold contacts properties of the nanowire. Specifically these contaminants produce non-linear I-V behaviour and conductance that depended on the applied gate voltage.
Figure 3-2 Systematic breaking behaviour of bare nanowires. (A) The critical current and voltage at which a selection of nanowires were broken. It suggests that the voltage drop across a junction must exceed 500 mV before it will fail. (B) Tunnelling resistances for the junctions after breaking. The median is of the order of 10 GΩ, representing a electrode gap of ~1 nm.

(which used either mechanically-controlled break-junctions or metal electrodeposition) suggest that all the resistance values in this range correspond to electrodes spaced by a few Å to over 1 nm, exactly the size range we require [12,13]. Contrast this with the success rate of small-gap junctions prepared by direct lithography, where the yield of electrodes separated by <5 nm never exceeded 10% [14]. On the other hand, nanowires broken at 77 K and at room temperature tend to form junctions showing much higher tunnelling resistances (sometimes over 200 GΩ, which is
the point where current leakage through the SiO$_2$ insulating layer starts to dominate conduction). This suggests that these electrodes are quite widely separated (well over 1 nm), making them particularly suitable for devices incorporating longer semiconductor nanorods. We have made a transistor using examples that are 20 nm long and the results are reported in Chapter 5.

3.2 (ii) Electromigration on the nanometre scale

In this section, we move from describing the formation of break-junctions to postulating a mechanism based on electromigration-induced failure of the nanowire. Electromigration strictly refers to the movement of atoms due to an electric field. It arises from the combined effects of the field on charged atomic nuclei (the *direct force*) and the momentum imparted to those nuclei by the current carrying electrons (the *electron wind*) [7,8]. These forces are illustrated in Figure 3-3. In our nanowires, initial experiments suggested that material (gold in this case) diffuses away from the negative electrode (the right contact in Figure 3-1D for example), implying that the electron wind is the dominant effect (if we assume that electrons are the charge carriers). This would be in good agreement with results from failure analysis in the semiconductor industry [9,10]. More exhaustive tests indicated that a competing effect in determining where the nanowire breaks may be the film stress in the electrode evaporated second (see Figure 2-9A) and the issue remains unresolved at the present.

As the electrical stress on the nanowire increases (with increasing bias voltage), it exhibits a series of small declines, interspersed with plateaux in the conductance before final junction failure (for instance, the region marked with a blue arrow in Figure 3-1C). This behaviour is observed for every device, although the exact pattern will vary. It most probably arises from changes in the microcrystalline structure of an electrode. Conduction is strongly determined by the transmission of electrons through the boundary between adjacent metal grains in these wires.
When the conductance drops, the grains have reorganised (changed in size or shifted relative to each other) into a less favourable configuration for electron transport, perhaps with the formation of material voids.

Arguably the most interesting observation during these studies is the ~500 mV lower bound on the voltage drop across the junction before it will break. This number is consistent across nanowires fabricated in different batches, suggesting that variables such as film stress and material impurities are not important issues. It is also independent of factors such as the power dissipated during the breaking process (~10 nW) and the current density (~$10^{13}$ A/m$^2$ at 1.5 K, considerably higher than the failure level for nanowires measured at room temperature [11]), which vary a great deal between junctions. Ultimately, it would be useful to measure the local voltage distribution within the nanowire, perhaps using an STM or a conducting AFM. One such

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**Figure 3-3** Forces at work during electromigration. The competing effects are the direct force of the applied field on the Au nuclei and the *electron wind* resulting from momentum transfer between the current carrying electrons and the metal atoms.
experiment has been carried out using contact mode AFM at room temperature with a doped diamond tip, but it lacks the spatial resolution to study our nanowires accurately [15].

### 3.3 Break-junction single electron transistors

The break-junctions described in the previous section are immediately useful for making SET’s based on nanocrystals or C₆₀ [16]. During the initial attempts, sample molecules were deposited onto electrodes that had been broken at low temperature and then the entire die cooled to 1.5 K for measurement. It was quickly realised that it was better to deposit the molecules and then break the nanowire in-situ at low temperature. In this way, metal surfaces free of external contamination are directly exposed to the sample molecule. Up to 60% of these junctions exhibited single electron tunnelling behaviour and some variation of their I-V characteristic on the applied gate voltage, compared with about 1% of the devices made using the small-gap junction method. The sample molecule coverage determines the success rate: higher concentrations resulted in more SET’s, but each device was comparatively usually more unstable (more frequent device “switching” and noise) as the molecule in the junction interacted with its immediate neighbours.

A trace of conductance as a function of the applied voltage, taken as the junction breaks, shows features that are unique to SET’s where a sample molecule has become lodged between the electrodes (see Figure 3-4A, which is an example using C₆₀ molecules). Starting at the point indicated by the magenta arrow, there is a significant “tail” in which the conductance drops slowly to zero through a series of plateaux. One explanation suggests that the molecule becomes involved with the electromigration of atoms in the electrode, each plateau representing a
metastable arrangement at that bias voltage. In other devices, the conductance is even known to increase quite dramatically (by up to an order of magnitude) after the nanowire first breaks.

The presence of the tail in the conductance trace is an excellent predictor for the successful creation of a SET (an I-V trace coming from the same device is shown in Figure 3-4B). In one instance, good devices were forecast with 100% accuracy from a set of 13 break-junctions. The shape of the conductance fluctuations in the tail is dependent on the particular sample molecule (nanorods, for instance, show fewer features in the tail compared with C₆₀). Finally, if a molecule has not fallen into the gap between the electrodes, the tail will not be present and the breaking trace will more closely resemble the plot for a clean nanowire, that is, the conductance will drop abruptly below the conductance quantum (compare for instance, the SET breaking trace in Figure 3-4A with the tunnel junction result in Figure 3-1C).
Analysis of the tail in junctions resulting in successful C₆₀ SET’s just prior to nanowire failure often reveals a staircase of conductance plateaux separated by the conductance quantum ($e^2/h$).

An example is shown in Figure 3-5. Normally, current flows through many transmission channels running between the shorted electrodes [17,18]. Atomic migration shuts down the channels one at a time, an effect that is most apparent when only a few remain open (near junction failure). This behaviour appears to be moderated by the C₆₀ molecules (although the exact mechanism is not clear at this stage), since it does not occur in their absence. In the end, only a single metal atom contact remains and once it is gone, the only pathway for the electron flow is by tunnelling though a cluster. Similar conductance plateaux have been observed during experiments on ballistic transport in mechanically controlled break-junctions [13,19,20] and in contacts formed by the momentary touching of macroscopic wires [21,22].

![Figure 3-5](image)

**Figure 3-5** Conductance quantisation during junction breaking. As the nanowire approaches failure, the conductance changes by steps of $e^2/h$, suggesting that electron transmission pathways are being closed one-by-one.
3.4 Summary

Break-junctions are a significant advance in the study of devices based on individual small molecules. This chapter discusses their advantages in producing higher yields of single electron transistors that tend to have more stable transport behaviour as well. Considerable information about what lies between the electrodes can be gained from an analysis of the junction conductance as it breaks, including evidence to differentiate between tunnel junctions and single electron transistors. Finally, a mechanism for junction formation is described as a result of electromigration-induced failure of the starting nanowire. In the next chapter, we shall use these devices to probe the electrical characteristics of the “smallest” switch made to date: the C$_{60}$ single electron transistor.
References and Notes


Chapter 4

C$_{60}$-based single electron transistors

4.1 Introduction

C$_{60}$ is an allotrope of carbon, together with diamond and graphite. Each molecule (or cluster) consists of 60 carbon atoms arranged at the vertices of a truncated icosahedron (see Figure 4-1), a shape resembling both a soccer ball and a geodesic dome (the latter was invented by the architect Buckminster Fuller [1,2], which lead to the common names “buckminsterfullerene”, “buckyball” or “fullerene” for C$_{60}$). Kroto and co-workers reported its discovery in 1985 during a series of mass spectrometry experiments on the products of the laser vaporisation of carbon rods [3,4]. More extensive investigations began only after methods were found for gram-scale synthesis (by resistively heating carbon rods in a helium atmosphere [5-7]) and purification (by solvent extraction and chromatography [8,9]). This material (now available commercially) is >99.9 % C$_{60}$, providing us with a suitable starting point for experiments on C$_{60}$-based single electron transistors (SET).

Figure 4-1 Structure of a C$_{60}$ molecule. 60 carbon atoms are arranged into a truncated icosahedron, with 20 hexagonal and 12 pentagonal faces. The whole molecule looks very much like soccer ball. This entire class of carbon clusters is known as fullerenes.
We begin this chapter by highlighting the properties of C\textsubscript{60} that are relevant to our efforts to make a SET and to carry out transport spectroscopy on the molecule. Our experiments are presented in the context of previous experimental probes of the electronic and vibrational structure of C\textsubscript{60} using a number of optical, electrochemical and transport methods and then we finish by describing our niche and aims in this field (Section 4.2).

Our experiments are carried out in a low-noise, cryogenic environment and this requires particular instrumentation. Details of the experimental setup are presented in the Section 4.3. This is followed by results from the simplest experiments, that is the SET working at low temperature (1.5 K) in the absence of an applied magnetic field. The data can be simply explained by using the standard model of single electron charging, which allows us to extract information about the intramolecular vibrational modes of C\textsubscript{60} (Section 4.4). There are significant features that are not accounted for by conventional analysis and we propose the vibraBall model to deal with them (Section 4.5). All of these measurements can be repeated at different temperatures and applied magnetic fields to gain further insight and we describe these efforts in Section 4.6.

In this series of experiments, three SET devices were found to behave quite differently from all the others. They more closely resemble GaAs SET’s tuned so that electron transport occurs in the Kondo regime. Section 4.7 presents our data and in particular, the dependence of transport on the applied magnetic field. Meanwhile, Section 4.8 introduces the Kondo effect (a model for its origin and its observable manifestations), as well as considering the fit between our results and these expectations.
4.2  C\textsubscript{60}: a ubiquitous molecule

4.2 (i)  Physical properties and electronic structure

The C\textsubscript{60} cluster consists of both hexagonal and pentagonal faces (see Figure 4-1). In spite of this, every carbon atom is identical by symmetry and this is consistent with the observation of only one peak in the NMR spectrum [10,11]. The C–C bond length is 1.46 Å on the edge between a hexagon and a pentagon (with greater single bond character) and 1.40 Å between two hexagons (with greater double bond character). The molecule has a diameter of approximately 7.1 Å [12], which dictates the electrodes separation we require to make a tunnelling contact for the SET.

This physical structure confers considerable chemical stability onto C\textsubscript{60}. Each carbon atom is \(sp^3\) hybridised to three nearest neighbours, leaving a single 2\(p\) orbital free for \(\pi\)-bonding (much like individual planes in the graphite structure). Ordinarily, the \(\pi\) electrons should be free to delocalise around the entire carbon backbone, producing a highly stable aromatic molecule. However, the pentagons in the structure only allow single bonds (since double bonds would introduce excessive ring strain), resulting in significant localisation of the \(\pi\) electron density in the hexagons [13,14]. Yet this effect only seems to reduce the stability of C\textsubscript{60} slightly, compared with the fully aromatic structure. The binding energy per carbon atom in C\textsubscript{60} is calculated to be <10% smaller than the value in graphite (7.4 eV), which is particularly stable [15,16]. Experimentally, the fullerenes form under extreme temperatures (>3000 K), which would destroy most other covalently bonded molecules [17]. This robustness is important for making SET’s since we pass relatively large currents through the molecule during transport measurements.

The deviation from a strictly delocalised \(\pi\) electron system should also confuse calculations of the C\textsubscript{60} electronic structure. Fortunately, it appears that the simplest model, Hückel molecular orbital
theory, can correctly predict the ordering of energy levels near the Fermi level, if not their energies [18]. The results of a Hückel calculation on the π electrons only are shown in Figure 4-2 (the σ bonds which arise from a combination of the $sp^2$ orbitals lie 3-6 eV below the Fermi level and do not contribute to electron transport through the cluster) [18]. Using Hund’s rule, electrons are assigned to energy levels within the manifold and the result is a zero spin ground state in

![Energy spectrum of C60 calculated by Hückel molecular orbital theory. Despite its simplicity, the theory produces the correct level structure near the Fermi level (the filled $h_u$ state and the empty $t_{1u}$ and $t_{1g}$ states). The wavefunction for the $t_{1u}$ state is also shown. Adapted from Haddon [18]](image-url)
which the \( h_u \) orbital (the highest occupied molecular orbital or HOMO) is completely filled. The next highest energy levels, the lowest unoccupied molecular orbitals (or LUMO) are the triply degenerate \( t_{1u} \) levels, which lie about 2 eV above the HOMO. A representation of a \( t_{1u} \) wavefunction is shown in the inset to Figure 4-2, with its odd parity under inversion and the three nodes arising from its \( L = 5 \) angular momentum state quite apparent. Overall, the Hückel picture can be used to identify which eigenstate \( C_{60} \) will exist in after the addition of an electron, but not the exact energy required to do this.

Finally, before going on to a review of previous experimental and theoretical work on \( C_{60} \), we present a summary of some of its pertinent physical properties (see Table 4-1).

**Table 4-1** Physical properties of \( C_{60} \). Adapted from Dresselhaus et al. [12]

<table>
<thead>
<tr>
<th>Property</th>
<th>( C_{60} ) value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Diameter</td>
<td>7.10 Å</td>
</tr>
<tr>
<td>C–C bond length</td>
<td>1.44 Å (1.46 Å pentagon, 1.40 hexagon)</td>
</tr>
<tr>
<td>Number of distinct sites</td>
<td>1 (I( _h ) symmetry)</td>
</tr>
<tr>
<td>Mass</td>
<td>( 1.2 \times 10^{-24} ) kg</td>
</tr>
<tr>
<td>Moment of inertia</td>
<td>( 1.0 \times 10^{-43} ) kg·m(^2)</td>
</tr>
<tr>
<td>Density</td>
<td>1.72 g/cm(^3)</td>
</tr>
<tr>
<td>Electron affinity</td>
<td>2.65 eV</td>
</tr>
<tr>
<td>First ionisation potential</td>
<td>7.58 eV</td>
</tr>
<tr>
<td>Work function</td>
<td>4.7 eV</td>
</tr>
<tr>
<td>Optical absorption edge</td>
<td>1.65 eV</td>
</tr>
<tr>
<td>Spin-orbit splitting</td>
<td>0.22 meV</td>
</tr>
<tr>
<td>Dielectric constant (static)</td>
<td>4.0 – 4.5</td>
</tr>
<tr>
<td>Thermal conductivity (300 K)</td>
<td>0.4 W/mK</td>
</tr>
<tr>
<td>Electrical conductivity (300 K)</td>
<td>1.7 nS/m</td>
</tr>
<tr>
<td>Phonon mean free path</td>
<td>50 Å</td>
</tr>
</tbody>
</table>
4.2(ii) Previous work on C\textsubscript{60}: a perspective

In the last 15 years, vast effort has been expended in fully characterising the C\textsubscript{60} molecule. We focus here on a few areas relevant to our experiments, namely the electronic and vibrational spectroscopy of C\textsubscript{60} and its anions as well as transport spectroscopy carried out on individual clusters by STM.

The electronic structure of C\textsubscript{60} can be studied most simply by ultraviolet (UV)-visible spectroscopy and photoluminescence [19,20]. Anions can be generated by doping with alkali (potassium, sodium and rubidium) or alkaline earth (barium and strontium) atoms [21,22]. Charge transfer readily occurs between the electrophilic C\textsubscript{60} and the metal donor, leading to all possible combinations of M\textsubscript{x}C\textsubscript{60} (x = 1-6). Electrochemistry (usually by cyclic voltammetry) can be used to study undoped C\textsubscript{60} molecules in solution phase [23]. Individual clusters acquire additional charge (from the negative electrode in a reduction sweep for example) at voltages that correspond to specific ionic states. This measurement should be comparable to our SET experiment. UV and x-ray photoemission spectroscopy can be used to study C\textsubscript{60} in the solid phase [24,25]. Photons are used to excite electrons from the cluster into the vacuum level and by measuring the kinetic energy of the exiting electrons, the density of states can be determined. In each of these cases though, the spectra are very broad with peak widths of the order of tens to hundreds of meV, making it difficult to observe vibrational excitations with high resolution.

Intra- and intermolecular vibrational studies on C\textsubscript{60} are carried out optically by infrared and Raman spectroscopy [26,27]. These techniques yield complimentary information due to differences in their selection rules and higher order spectroscopy can be used to access modes that are optically-inactive at first-order [28]. Of particular interest are the low-energy intramolecular vibrations and a pictorial representation of these modes is shown in Figure 4-3 [29]. Inelastic
neutron scattering and high resolution electron energy loss spectroscopy (HREELS, a technique where incident electrons are scattered inelastically off the sample and by measuring their final energy, the position of individual energy levels can be determined) are other options that are not subject to optical selection rules [30-32]. Their energy resolution is poorer, limiting their usefulness to optically inactive modes and studies of phonon dispersion relations. All of these techniques still operate on an ensemble of molecules. It is also possible to examine individual C$_{60}$ clusters, an approach taken in STM and in our SET experiments.

**Figure 4-3** Low energy vibrational normal modes of the C$_{60}$ molecule. The eight $H_g$ modes are Raman active and the four $F_u$ modes are infrared-active. Adapted from Schlüter et al. [29].
Scanning tunnelling microscopy is based on electron tunnelling between an atomically sharp metal tip and a conducting substrate [33,34]. If fullerene molecules are inserted in the gap between these two electrodes, the current transport characteristics are modified, generating information about the energy spectrum of C₆₀ itself (scanning tunnelling spectroscopy or STS) as well as the nature of the C₆₀-substrate interaction (this is somewhat analogous to the C₆₀-source/drain interface in our SET experiment) [35,36]. STM has been used to manipulate C₆₀ around the substrate, as well as to image individual carbon atoms in the cluster [37]. Recently, STS has been extended to low temperature inelastic electron tunnelling spectroscopy (IETS) on individual molecules [38-40]. Here each vibrational mode can be resolved and forthcoming results on C₆₀ should provide a direct comparison with our efforts [41].

4.2 (iii) Our niche in this field

From a spectroscopic point of view, our experiments on C₆₀-based SET’s described below have many of the same advantages as STM: measurement of individual molecules, high energy resolution and the absence of optical selection rules to restrict which energy levels are visible. Key differences include the presence of a back gate to apply an external electric field, which provides an additional parameter to assist deconvolution of the energy spectrum. Our device is compact and requires no moving parts, making it both simple to mount in a standard cryogenic measurement apparatus and easily adapted for optical studies and sample characterisation (SEM or AFM).

From a broader perspective, the small size of a C₆₀ cluster makes it an ideal candidate for a room temperature SET (an objective that has not been realised to date). If successful, it would be the first switch (or logic gate) based on an individual molecule to operate under ambient conditions.
an important milestone in efforts to make *useful* nanometre-scale electronics. Finally, we must not disregard the “coolness” factor (in the local parlance)!

4.3 Experimental setup

Before delving into our experimental observations, we briefly describe the apparatus and equipment setup used to make these measurements. The most common configuration is a 2-terminal DC current-voltage ($I$-$V$) probe at constant gate voltage ($V_g$), as depicted in Figure 4-4. A DC voltage is applied to the source and drain electrodes of the tunnel junction through a voltage divider. The divider (usually 100 kΩ: 1 kΩ or 10 kΩ: 1 kΩ) serves to increase the resolution of the voltage source (that is, finer voltage increments are possible) as well as limiting the voltage.

![Figure 4-4 2-terminal measurement configuration](image)

A bias voltage ($V$) is applied to the molecular tunnel junction through a voltage divider (formed by the resistors $R_1$ and $R_2$) and the current measured. The gate voltage, $V_g$, is applied through a low pass filter, formed by a resistor ($R_g$) and a capacitor ($C$).
range (useful in the event of operator error). The current flow through the device is measured with a current pre-amplifier (Ithaco 1211). An external electric field is applied via the back gate through a low pass filter (typically 100 MΩ: 1 pF, giving a 0.1 s rise time). In this setup, the digital-to-analogue ports (16-bit, 100 kSamples/s) on a multifunction I/O card (AT-MIO-16X, National Instruments) are used to apply both the source-drain and the gate voltages. The card is controlled through a standard Windows 95/98 (Microsoft) computer running a home-built measurement program (Mezurit, M.W. Bockrath) written in LabWindows/CVI (also National Instruments), which also serves to log and to display the data. The current level is read back from the current amplifier (as a voltage) by the analogue-to-digital ports (16-bit, 100 kSamples/s) on the same card.

We have found that this combination has an adequate noise baseline, especially if the data acquisition rate is maximised (by turning off the real-time data display, “Fast Mode” in Mezurit, thus increasing the sampling rate to >1 kSamples/s) while keeping a running average (30 points is normal). Care must be taken when operating Mezurit since its fully digital nature allows large (accidental) voltage excursions that will destroy the device. Voltage spikes will also occur when parameters are being changed in the program as our current LabWindows/Windows 95/98 environment does not individual tasks to be prioritised and to run independently of each other (LabWindows 5/Windows NT does have these capabilities, but other problems arise with its implementation that will not be discussed here).

Other experimental configurations can also be used, including 4-terminal DC measurements that are carried out with a voltage pre-amplifier (Stanford Research Systems SR560) placed in parallel with the junction. For AC measurements, a lock-in amplifier (Stanford Research Systems SR830) is used to generate and then to detect an additional AC voltage modulation (normally at 13-17 Hz,
at a peak-peak voltage of ~1 mV after passing through a 1 MΩ: 1kΩ voltage divider). This setup provides data on the differential conductance \((dI/dV)\) as a function of the applied voltage and it is particularly useful in removing DC background noise. We have not had success obtaining AC results for devices where the current level is much lower than 100 pA. Other experimental conditions that can be changed include the temperature (discussed below) and the applied magnetic field (varied between 0-12 T using a superconducting magnet).

Most \(C_{60}\)-based SET’s are made and measured at 1.5 K. Junctions broken at this temperature have the correct spacing to admit one cluster only. The ensuing device is more stable, exhibiting less electrical “switching” and noise. More importantly, the width of the observed energy levels scales directly with the temperature (due to thermal broadening of the electron Fermi distribution), making lower temperatures more desirable for high resolution spectroscopy. Much information about the device can also be obtained from the temperature dependence of its transport behaviour. To meet these requirements, we mount the sample inside a top loading variable temperature insert (or VTI, Oxford Instruments), which is itself mounted within a liquid helium dewar (also Oxford Instruments). The VTI can control the temperature from 1.5 K to 300 K, nominally in 0.1 K increments. It operates by immersing the sample in a stream of flowing helium vapour, which is kept at a preset temperature by balancing the evaporative cooling of liquid helium and the effects of a resistive heater. Use of a top loading insert (which is vacuum isolated from the surrounding helium bath) allows rapid sample exchange (2 hours cycle time) with minimal loss of cryogens.
4.4 Gate voltage dependence: results

4.4 (i) Experimental results

We begin a presentation of our results on C\textsubscript{60} with the simplest measurements: \(I-V\) and \(dI/dV-V\) traces at various gate voltages, taken at base temperature (1.5 K) with zero applied magnetic field. Figure 4-5A shows \(I-V\) curves taken from a SET in a 2-terminal DC measurement. In each trace, there is a region of strongly suppressed conductance at small bias voltages (a conductance gap), followed by a number of step-like features once a voltage threshold has been exceeded. The shape of these features is reproduced at different gate voltages, even though the (voltage) width of the conductance gap changes. The gap can also be reduced to zero, which occurs around \(V_g = 6.04\) V for this device. Figure 4-5B shows a plot of \(dI/dV\) versus \(V\) taken for the same device in an AC measurement at three of the five values of \(V_g\) shown in panel A. The step features have become peaks in the differential conductance and several are part of a multiplet on closer examination. Consider the trace at \(V_g = 6.9\) V for example. There are well-defined peaks at \(V = -27.7\) and 26.6 mV, which have associated “shoulders” at -32.8 and 24.7 mV respectively.

A number of individual traces can be pieced together to produce a two-dimensional diagram showing \(dI/dV\) as a function of both \(V\) and \(V_g\) (Figure 4-6 shows plots from 4 devices) [42]. The peaks in \(dI/dV\) have become lines in these diagrams, making it fairly simple to distinguish actual features from device noise and switching. The black triangular regions correspond to the conductance gap. It evolves linearly with gate voltage, even closing at certain points (defined to be where \(V_g = V_c\)). This behaviour is both quite general, having been observed in 13 different devices made in completely separate batches and also characteristic of a single electron charging (a more thorough discussion of this statement follows in the next section). Away from \(V_c\), the conductance gap continues to widen, the largest gap observed being >270 mV.
Figure 4-5 Response of a C₆₀ SET at different gate voltages. (A) I-V curves taken in a 2-terminal DC measurement at five gate voltages at 1.5 K. (B) $dI/dV-V$ curves taken in the corresponding AC measurement at three of those gate voltages. The upper two traces are offset by 15 nS and 30 nS respectively for clarity.
Figure 4-6: Two dimensional plots of $dI/dV$ vs $V$ and $V_g$. The black regions correspond to the conductance gap. The rest of the colour scale ranges from purple to pink to white (the white representing 30 nS in A, B and C and 5 nS in D). The white arrows mark the intersection of the $dI/dV$ lines with the conductance gap. The gate voltage axis in D is discontinuous as the device switched at $V_g = 1.15$ V.
The slope of the lines in $dI/dV$ provides information on the effectiveness of the gate in perturbing the energy spectrum of the cluster in the tunnel junction. It is encapsulated in the dimensionless parameter, $\alpha$, which is a ratio of the change in $V_g$: change in $V$. In panel D, $\alpha \sim 160$, while in two other devices, $\alpha < 10$ (8 for panel B and 5 for panel D), entirely consistent with device modifications (reducing the gate oxide thickness) that increased the capacitive coupling between the gate and the junction above. The device in panel A has the same oxide thickness as that in panel D, but its $\alpha$ value is only 14, perhaps suggesting a junction geometry in which the source-drain electrodes do not screen the electric field from the gate as effectively.

There are also several noteworthy features visible amongst the $dI/dV$ lines, especially those that do not directly border the conductance gap (indicated by the white arrows in Figure 4-6). Every device displays a low-energy line in the range of 3-7 meV (with a median of 5 meV), an observation that will be fully explained in Section 4.5. In panel A of the Figure, this line becomes a doublet, with a splitting of 1-2 meV (more apparent in the pair at positive bias voltages, but also present at negative voltages). To date, the cause of this behaviour is not known. In panel D, there is a series of $dI/dV$ lines all separated by about 5 meV (this is particularly visible at negative source-drain voltages). The maximum conductance of these devices is also quite different, approaching 30 nS in three devices but barely exceeding 5 nS in panel D. Since transport is governed by electron tunnelling onto the cluster, which is a strongly distance dependent process, there are probably two factors at work: the size of the gap between the source and the drain electrodes and the position of the C$_{60}$ molecule in that gap.

One question (often asked) about all of these results is: are we sure that it is an individual C$_{60}$ molecule in the tunnel gap and not “something else”? The evidence is circumstantial (since it is not possible to directly observe individual clusters in the device geometry), so we offer a proof by
elimination. The combination of non-linear, step-like $I-V$ behaviour and dependence on the applied gate voltage is only observed in devices where C$_{60}$ solution has been deposited. As summarised in Chapter 3, we have conducted a series of break-junction and transport experiments with clean nanowires and on no occasion were both these characteristics seen. This excludes artefacts arising from the nanowires themselves or from junction breaking. The size of the conductance gap always exceeds 150 meV, which translates to an object smaller than 2 nm in the junction. A possibility is a metal nanoparticle that has broken off one of the electrodes. However, the features in the transport spectra of completely separate devices are identical (the line at 5 meV is one example), an unlikely coincidence if metal particles are being formed during either fabrication or in the rather violent (and unpredictable) process of nanowire failure.

Another potential complication is conduction through more than one cluster. Multiple C$_{60}$ molecules conducting in parallel should show sets of $dI/dV$ lines that cross each other but have different slopes and are offset in bias voltage. Every set corresponds to transport through distinct molecules, which lie in slightly dissimilar electrostatic environments and hence conduct at different values of $V$ and $V_g$. Such devices should also be quite “switchy” as neighbouring clusters electrostatically gate transport through each other. This was observed in early SET’s where very high C$_{60}$ concentrations were used. Once the coverage was lowered, this effect essentially disappeared, apart from one recent anomaly. Clusters in series are a different matter, especially as it is known that C$_{60}$ will form small oligomers (dimers, trimers and tetramers) in solution despite careful handling [43]. Such devices should show suppressed conductance since the whole junction will only conduct when the energy levels of all the molecules are aligned. This behaviour is not apparent, although the option cannot always be categorically ruled out.
4.4 (ii) Fit to the Coulomb Blockade model

Many of the observations made in the previous section can be explained using the standard Coulomb blockade model (Chapter 1) [44,45]. The conductance gap stems from an energetic barrier to electron tunnelling from the electrodes onto the C\textsubscript{60} cluster that exceeds the average thermal energy of the environment. It is a combination of the charging energy required to add a single electron to the molecule ($U$) and the energy spacing between adjacent quantum levels in C\textsubscript{60} ($\Delta E$). To add an electron, the voltage bias must be increased so that it exceeds this barrier, after which current will start to flow. The reverse is true when an electron is removed.

The gate is used to apply an external electric field that shifts the entire energy spectrum of the C\textsubscript{60} molecule, bringing different quantum levels into resonance. As more positive gate voltages are applied, an additional electron may be stabilised on the cluster. The threshold is the point where the conductance gap disappears, that is at $V_c$. At $V_g < V_c$, the C\textsubscript{60} charge state with $n$ electrons ($C_{60}^{n-}$) is the ground state, while at $V_g > V_c$, the $n+1$ electron state ($C_{60}^{(n+1)-}$) is more stable. At $V_g = V_c$, both states have the same energy and the number of electrons on the cluster will alternate between $n$ and $n+1$. This results in electron flow through the device and hence a measurable current. Based on the HOMO-LUMO/band offsets for C\textsubscript{60} on gold determined by photoelectron spectroscopy, it is believed that $n$ is either zero or one when no gate voltage is applied [24].

Therefore, we are probably probing the $C_{60} \rightarrow C_{60}^{1-}$ or the $C_{60}^{1-} \rightarrow C_{60}^{2-}$ transition as the gate voltage traverses $V_c$ in the positive direction. The exact position of $V_c$, though, is determined by the electrochemical environment around the cluster, comprising the Fermi level of the source and drain electrodes (not necessarily just their work functions since there may be an applied bias voltage), the gate voltage and the charge distribution due to adjacent C\textsubscript{60} molecules and organic
contaminants. It explains why $V_c$ is not reproducible from device to device, a fact that is quite evident in Figure 4-6.

Gate voltage can also be swept to locate the largest value of the conductance gap, providing information on the charging energy of the cluster and from there, an upper bound for its size. In Figure 4-7, we depict the $dI/dV$ plot for a device with the largest charging energy seen to date (over 270 meV). Using Equation 1-2, with an electrode-C$_{60}$ separation of $d = 2$ Å and assuming

![Figure 4-7](image)

**Figure 4-7** Large conductance gap C$_{60}$ device. The conductance gap and hence the charging energy exceeds 270 mV, providing an upper bound on the size of the cluster. The zig-zag patterns at both positive and negative bias voltages result from the way the data was taken. As the gate voltage was swept in the positive direction, strips of fixed bias voltage range were taken and pieced together in real time. This ensures immediate recovery from device switches, which fortunately did not occur in this case.
the free-space dielectric constant $\varepsilon = 1$, gives a maximum diameter for the cluster of 1.8 nm. In comparison, one molecule of $C_{60}$ is 0.7 nm in diameter, providing a check that our measurement is reasonable. It was not possible to extend the bias voltage range to ascertain the actual charging energy since the device became very unstable when more than 270 mV was applied. This is visible as the noisy area in the right-hand corner of the $dI/dV$ plot. One other device actually showed a full “diamond”, in which the conductance gap opened from zero, reached a maximum and then closed again. The charging energy from this device was much smaller (~120 meV), making it difficult to identify this junction unequivocally as a single $C_{60}$ device.

The lines in the $dI/dV$ plots are a second, but equally important characteristic that we now discuss. In the Coulomb blockade model, they provide information on the excitation spectrum of a particular charge state of $C_{60}$, appearing when additional energy levels become available for transport. When $V_g < V_c$, increasing bias voltage produces a series of $dI/dV$ lines for the transition $(C_{60}^{n-} \text{ground state}) \rightarrow (C_{60}^{(n+1)-} \text{ground and excited states})$, that is the quantum levels of the $C_{60}^{(n+1)-}$ state are being probed. Conversely, if $V_g > V_c$, increasing bias voltage examines the transition $(C_{60}^{(n+1)-} \text{ground state}) \rightarrow (C_{60}^{n-} \text{ground and excited states})$ \text{– a probe of the quantum levels of the} $C_{60}^{n-}$ state. Referring back to Figure 4-6, it is the excited states that are marked with the white arrows. The energy of an excited state relative to its ground state is determined from the bias voltage at which the excited state line intercepts the conductance gap.

Armed with this interpretation, we can start to extract information about the quantum levels of $C_{60}$. The previous section identified a feature at 5 meV common to many devices. It is usually present on both sides of $V_c$, which suggests that it is an excitation of both the $n$ and $n+l$ electron states. In principle, any of the degrees of freedom of $C_{60}$ (electronic, vibrational and rotational)
can give rise to this excitation and we address them in turn. Transitions to low lying electronic states are an obvious possibility. What makes them unlikely is the presence of the 5 meV line in both charge states of C\textsubscript{60} as well as the regularly spaced series of $dI/dV$ lines (corresponding to a set of excited states equally spaced in energy) seen most clearly in Figure 4-6D. Past experimental studies have not had sufficient energy resolution to detect these levels, as discussed in Section 4.2 (ii). On the other hand, theoretical studies on the electronic structure of C\textsubscript{60} anions (C\textsubscript{1−} to C\textsubscript{6−}) using density functional theory show no evidence for identical low energy excitations in charge states differing by one electron or for a manifold of states lying 5 meV above the HOMO [46].

Rotational energy levels are quantised by $\hbar^2/2I$, where $I$ is the moment of inertia of C\textsubscript{60}. This corresponds to an energy scale of 0.3 μeV, four orders of magnitude smaller than the excitations observed here. Finally, we consider vibrational excitations coupled with electrons tunnelling on and off the cluster. Vibrational modes are relatively insensitive to the charge state of the molecule and so this hypothesis can simply explain the presence of the 5 meV lines in both C\textsubscript{60−} and C\textsubscript{(n+1)−}. The manifold of states would then arise from successive excitation of additional vibrational quanta.

To confirm the proposition, it would be helpful to identify which vibrational modes are being excited. Figure 4-3 summarised the known low energy intramolecular normal modes. The lowest energy excitation is the $H_g(1)$ mode, which occurs at 33 meV and corresponds to a C\textsubscript{60} deformation from a sphere to a prolate ellipsoid (as depicted in the inset to Figure 4-8) [26]. The main part of this Figure shows two-dimensional $dI/dV$ data taken from the same device as Figure 4-6A, but over an extended bias voltage range. A feature is quite evident at ~35 meV (indicated
with the red arrows), which is attributed to the $H_g(1)$ mode. Similar lines in the $dI/dV$ spectrum have been observed on three other occasions. This mode is not seen in every SET and possible explanations include processes in which an electron tunnels onto the cluster without exciting this vibration as well as difficulties in detecting the feature if the device is too noisy.

In any case, it appears that intramolecular vibrational modes are too high in energy to account for the 5 meV line. We postulate an alternative excitation that may do so in the next section.
4.5 vibraBall model

An alternative possibility to explain the 5 meV \( dI/dV \) feature is oscillations of the entire \( C_{60} \) molecule within the potential that holds it between the source and drain electrodes [42]. This scenario is illustrated in Figure 4-9, which shows one half of the actual system. An individual molecule of mass \( M \) is confined near the electrode by a van der Waals interaction (depicted in the right panel of the Figure). Near their equilibrium separation, we can approximate the potential by a harmonic oscillator with spring constant \( k \). The allowed energy levels are the normal ladder of states equally separated by the vibrational quantum \( hf \), where \( h \) is the Planck constant. The use of a single electrode in this argument is quite general since the presence of the second one will merely change the effective spring constant. This becomes the static situation prior to excitation.

**Figure 4-9** Van der Waals potential confining \( C_{60} \) between the electrodes. In equilibrium, individual molecules are held in a harmonic oscillator-like potential with spring constant \( k \). The allowed excitations form a series of energy levels separated by \( hf \).
When an electron tunnels onto the cluster, there is now an additional effect: the interaction between the C\textsubscript{60} anion and the image charge it induces in the metal electrode. The net force is attractive, shortening the C\textsubscript{60}–electrode equilibrium separation by a distance $\delta$ (we are “compressing the spring”, as depicted in Figure 4-10). More importantly, the cluster has been displaced from its previous position and being subject to a harmonic potential, it will oscillate until a new equilibrium is reached. This is the dynamic situation, which we call vibraBall. We note in passing that this situation is directly analogous to Franck-Condon transitions that are observed in molecular spectroscopy.

Combining this interpretation, the discussion in Section 4.4 (ii) and the 5 meV features observed in Figure 4-6, the $dI/dV$ lines at $V_g < V_c$ must then probe the ground and excited vibrational states of C\textsuperscript{60\textsuperscript{n-}} when an electron tunnels onto the cluster. Figure 4-6D shows an extensive manifold of such levels. For $V_g > V_c$, we are probing the excited vibrational states of C\textsuperscript{60\textsuperscript{n-}} when an electron

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**Figure 4-10** Attractive electrostatic interaction between the C\textsubscript{60} anion and its image charge. Adding an electron to the cluster decreases the distance between C\textsubscript{60} and the electrode by an equilibrium distance $\delta$ and sets a mechanical oscillation in motion.
The model is elegant and simple to describe, but does it bear any resemblance to reality? To the best of our knowledge, this vibrational mode has never been identified in previous experiments (although logically it should exist elsewhere). The van der Waals interaction between $C_{60}$ and a gold surface has been measured by STM and Auger electron spectroscopy to have a binding energy of $\sim 1$ eV and a equilibrium separation between the centre of a cluster and the surface of 6.2 Å [36,47,48]. If we assume that a Lennard-Jones potential is applicable here, we can use it to fit these parameters and then we approximate its form near its minimum with a harmonic oscillator potential. That potential has a force constant of $k \sim 70$ N/m. From the mass $M$ of a $C_{60}$ molecule (Table 4-1), a simple calculation yields a vibrational frequency of $f = (1/2\pi)\sqrt{k/M} \sim 1.2$ THz and a vibrational quantum of $hf = 5$ meV. This is in very good agreement with the 3-7 meV range seen experimentally for the $dI/dV$ line, suggesting that the vibraBall model encapsulates most of the essentials physics of the problem.

To put the analysis on a more solid foundation, we construct the Hamiltonian for relevant to this situation,

$$\hat{H} = \left( \frac{\hat{p}^2}{2M} + \frac{1}{2}M\omega^2 \hat{x}^2 \right) + (\epsilon_0 - e\mathcal{E}\hat{n})$$

where $\epsilon_0$ is the ground state electron energy level with $C_{60}$ uncharged, $e$ is the charge of the electron, $\mathcal{E}$ is the electric field between the $C_{60}$ anion and its image charge and $\hat{n}$ is the number operator indicating the number of additional electrons on the cluster. The second term above, therefore, is a measure of the energy of the electron, quantised by the harmonic potential and including electrostatic effects. The first term represents the energy of the carbon framework in the
cluster, where $\hat{p}^2/2M$ is the normal kinetic energy operator for the C$_{60}$ molecule and $\frac{1}{2}M\omega^2x^2$ is the term arising from the van der Waals interaction between the cluster and the electrodes.

There are two cases of interest. When $\hat{n} = 0$ (no additional electrons on the cluster), the Hamiltonian reduces to the harmonic oscillator form and the allowed energy levels $E_m$ are given by the usual form,

$$E_m = (m + \frac{1}{2})\hbar f$$

where $m$ indexes the energy levels and $f$ is the C$_{60}$ vibrational frequency.

If $\hat{n} = 1$ (a single additional electron), then the Hamiltonian corresponds to a displaced harmonic oscillator with energy levels given by,

$$E_m = (m + \frac{1}{2})\hbar f + \varepsilon_0 - \frac{1}{2}k\delta$$

where $\delta$ is the displacement of the cluster away from its uncharged position (introduced earlier).

Using the corresponding harmonic oscillator wavefunctions, we can obtain the root-mean squared displacement $x_m$ of C$_{60}$ in the $m$th-vibrational level as $x_m = (2m + 1)^{1/2}x_0$, where $x_0 = (\hbar f/k)^{1/2}$ ~3 pm is the zero point fluctuation. We can also try to estimate $\delta = F_e/k$ directly by calculating the force, $F_e$, between two charges separated by twice the C$_{60}$–electrode distance (which is 6.2 Å, from above). This crude approximation gives $\delta \sim 2$ pm, suggesting that any displacement is quite small relative to the gap between the cluster and electrodes.

We can also calculate the transition rate, $R_{fi}$, into various vibrational states. Starting with Fermi’s golden rule for this system,

$$R_{fi} = \left(\frac{2\pi}{\hbar}\right)|\langle f|V|i\rangle|^2\delta(E_f - E_i)$$

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where \( \langle f | V | i \rangle \) is the transition matrix element between the initial state of C_{60} and a final state where an electron has tunnelled on, generating additional vibrational quanta. The energy difference between these states is,

\[
E_f - E_i = \hbar \omega + \epsilon_0 - \frac{\gamma}{2} k \delta
\]

The matrix element \( \langle f | V | i \rangle \) is simply the overlap integral between the two corresponding harmonic oscillator wavefunctions representing the initial and final states, \( \psi_i(x) \) and \( \psi_f(x - \delta) \) respectively,

\[
\langle f | V | i \rangle \sim \left( \frac{\delta^2 / 2x_0}{n!} \right)^n \exp \left( -\frac{\delta^2}{2x_0} \right)
\]

We can then plot the relative transition rates into each vibrational level for the values of \( \delta \) and \( x_0 \) estimated in this system (see Figure 4-11). The most likely transition is into a final state with no vibrational quanta excited, which concurs with our observation that this \( dl/dV \) line is generally the most conducting. The \( m = 1, 2 \) and \( 3 \) states have appreciable transition probability, but higher vibrational levels do not play a large role. Again, this agrees with the experiment where one excited vibrational state is usually all that is seen. The exception is the device in panel D of Figure 4-6, which shows an extended excited state manifold. Additionally, the expected monotonic decrease in transition probability is also not observed in this junction (the \( dl/dV \) line intensity seems to vary in a rather random fashion). We speculate that this behaviour may have resulted from much stronger coupling to one electrode, which is indicated by the different slopes of the \( dl/dV \) lines in the Figure. Variations in peak intensity may also arise from coupling to other degrees of freedom such as vibrational modes perpendicular to the device surface.
The vibraBall model accounts for most of the hitherto unexplained features in the $dI/dV$ spectrum. Its success suggests that these vibrational motions should be observable in nanometre-sized systems when the object is (i) sufficiently small (and light) and (ii) tightly bound to the substrate. Both of these factors will ensure that the vibrational frequency is high enough to be resolved at temperatures of $\sim 1$ K. In the next section, we shall address the issue of the temperature more fully, considering its effect on transport through these devices.

**Figure 4-11** Transition probabilities into each final vibrational state. Using Fermi’s Golden Rule, a normalised probability distribution for the electron to excite certain vibrational states was calculated.
4.6 Temperature and applied magnetic field dependence: results

4.6 (i) Temperature dependence

Temperature is a parameter employed routinely in studying single electron transport, providing much information about the energy scales relevant in a system. We have only been able to make limited use of it since C$_{60}$ devices tend to be quite unstable if they are raised far above liquid helium temperatures. Unfortunately, this is the range in which the most interesting changes to the tunnelling spectrum are expected to occur. In this section, we report the best results amongst a group of devices that did survive to higher temperatures and then apply the normal Coulomb Blockade theory to explain the behaviour observed.

In the standard experimental protocol, the temperature and hence the thermal energy scale $k_BT$ (where $k_B$ is the Boltzmann constant) are fixed first. A source-drain bias voltage is chosen such that $eV < 4k_BT$, ensuring that we are in the “linear response” regime. The gate voltage is swept through the region where the conductance gap is almost zero. Peaks in the differential conductance (Coulomb oscillations) are observed only when $V_g = V_c$ (see Chapter 1 for a more detailed description).

Figure 4-12 depicts results from a Coulomb oscillation in a C$_{60}$ device measured at a range of temperatures. As the temperature increases, the conductance peaks in Panel A decrease in amplitude and increase in width (measured here as full width at half maximum). For clarity, not every temperature measured is shown. In Panel B, the trend in peak height is quite apparent. Interestingly, it stops decreasing after about 6 K, remaining at a constant value to as high a temperature as we can measure. The peak width (seen in Panel C) increases linearly with temperature (the slope is $~5\text{ mV/K}$), leading to thermal smearing of the peak.
Figure 4-12 Temperature dependence of Coulomb oscillations in a C\textsubscript{60} SET. (A) A Coulomb oscillation is measured at different temperatures. The abscissa for each peak maximum has been aligned as have the baselines for each oscillation. (B) The height of the peak decreases with increasing temperature until it reaches a plateau at 6 K. (C) The peak width increases monotonically as a function of temperature.
Using the Coulomb Blockade model, we begin by defining three temperature ranges that are relevant to our observations [49]:

- \( e^2/C < k_B T \), where charge quantisation is unimportant
- \( \Delta E < k_B T < e^2/C \), a classical dot, in which multiple quantum levels (that cannot be resolved from each other) participate in electron transport
- \( k_B T < \Delta E, e^2/C \), a quantum dot, where electrons tunnel into a few, well separated energy levels

Recall from previous discussions that \( U = e^2/C \) is the charging energy of the cluster and \( \Delta E \) the spacing between quantum levels. The conductance through a classical dot is known to be independent of temperature and equal to half of the value in the high temperature limit. The Coulomb oscillations should simply broaden with temperature until charge quantisation is lost. In contrast, the peak height in a quantum dot decreases linearly within increasing temperature.

Based on this interpretation, the device shown in Figure 4-12 appears to be a classical dot down to about 6 K (~0.5 meV) and then moves into the quantum regime at lower temperatures. We note that the energy scale for this transition is several orders of magnitude smaller than expected, based on the known energy spectrum of C_{60}. The discrepancy is unresolved at this stage, although it may be possible to check this hypothesis by using another feature of classical versus quantum dots. The peak height in a series of Coulomb oscillations is approximately uniform in a classical dot, but varies randomly in a quantum dot (as it depends on the coupling between a particular energy level and the source and drain electrodes). Several C_{60} SET’s have already shown multiple oscillations, although technical difficulties (such as the destruction of the device) have prevented the collection of reliable data.
4.6 (ii) Applied magnetic field dependence

In contrast to the rich if somewhat perplexing dependence on the sample temperature, most devices show no variation with the applied magnetic field. This is surprising since the $g$-factor of C$_{60}$ and its ions is non-zero ($g = 2.00221$ for C$_{60}^{n+}$ and $g = 2.00056$ for C$_{60}^{n-}$) as measured by electron paramagnetic resonance (or EPR) [50,51]. Applying a 10 T field should result in a peak splitting of ~2.3 meV, an energy resolution that is easily attainable in this experiment. Admittedly, most devices are sufficiently noisy that identifying peaks positions is difficult, but even in the quietest SET’s, no splitting was observed. There are exceptions to the last statement and one of them is the subject of the next section.

4.7 A special device

During the present series of experiments on C$_{60}$-based SET’s, one device (since joined by two others) exhibited transport characteristics radically different from the others (see Figure 4-6 for examples of the norm). Panel A of Figure 4-13 depicts a plot of the differential conductance as a function of the source-drain and gate voltages, taken at zero magnetic field in a 2-terminal AC measurement for this device. Several features stand out immediately. The $dI/dV$ lines bordering the conductance gap do not form the familiar cross pattern around the point where $V_g = V_c$. Instead the conductance gap appears to close only from the left side of the diagram. For $V_g > V_c$, a line at positive bias voltage continues upwards, but its counterpart at negative $V$ is missing.

Perhaps, the most interesting feature though, is the presence of a sharp conductance peak at zero bias voltage that does not change with gate voltage. Application of a magnetic field (in this case
Figure 4-13 Effect of magnetic field on a Kondo C_{60} SET. (A) Two-dimensional $dl/dV$ plot taken as a function of bias voltage and gate voltage at zero magnetic field and 1.5 K. Note the peak in the conductance at $V = 0$. (B) The corresponding plot taken with a 10 T applied field. This peak has now split symmetrically into two others.
10 T) causes the line to split (as shown in Figure 4-13B). It becomes a doublet, with peaks located at ±1.3 mV. The effect is more easily seen in the corresponding line traces taken at fixed gate voltages (Figure 4-14). Figure 4-14D show splitting of the distinct peak to the right of $V_g = V_c$ (Figure 4-14C) while a less intense feature to the left of this point (presented in Figure 4-14A) also splits in a magnetic field (Figure 4-14B). This is the key feature of this device and its explanation lies outside simple Coulomb Blockade theory (as we discuss below).

Other features are noteworthy. All the $dI/dV$ lines apart from the zero bias peak are very broad (up to 3-4 mV) in some cases – it is usually 1-2 mV for SET’s at this temperature. These lines do not split at high magnetic fields, suggesting that they correspond to features already observed in other devices (a reassuring check) and therefore, that the zero bias peak is probably caused by an effect that has thus far not been seen in $C_{60}$ devices. Of the two other SET’s that showed the zero bias peak, one was quite noisy and difficult to measure. The second was found during conscious attempts to make such devices. In this case, the nanowire was broken at a slightly higher temperature (4 K) after which the junction showed limited gate-dependent $I-V$ behaviour. The entire sample was then thermally cycled to room temperature overnight before being cooled back down to 1.5 K for measurement. The zero bias peak became apparent at this point. Despite this accomplishment, a reliable protocol to generate this type of device has not been found – successful targeted searches are currently as common as serendipitous finds.
The transport characteristics described in the previous section follow patterns seen in GaAs SET’s [52-55] and recently in carbon nanotube devices[56]. In these systems, the behaviour is attributed to the Kondo effect. This phenomenon arises where a magnetic impurity begins to interact strongly with a sea of conduction electrons, a transition that occurs once the temperature

\[ \text{Figure 4-14} \text{ Evolution of the Kondo peaks with magnetic field. (A) A line trace of the differential conductance vs the source-drain bias taken at a gate voltage to the left of } V_g = V_c \text{ for the device shown in Figure 4-13 (the actual gate voltage is indicated with the white dotted line), showing the zero bias peak. (B) The peak splits into two at 10 T. (C) On the right hand side of } V_g = V_c, \text{ there is a much more distinct zero bias peak (taken at } V_g = 5 \text{ V, the right hand end of the data shown in Figure 4-13). (D) At 10 T, the peak again becomes a doublet.} \]
is lowered below a threshold for the sample (known as the Kondo temperature, $T_K$). SET’s allow that magnetic impurity to be a single electron spin localised on a quantum dot or a molecule (such as $C_{60}$), which is then coupled to the Fermi seas of the source and drain electrodes [57,58].

We make use of the standard picture of transport through a SET to illustrate the origin of the Kondo effect. Consider the case depicted in Figure 4-15A. It shows the energy diagram for a quantum dot (we shall use “quantum dot” to refer also to $C_{60}$ molecules in this section) with one unpaired spin (that is, an odd number of electrons) that occupies the spin-degenerate energy level closest to the Fermi level (labelled $\varepsilon_0$). The dot lies between two electrodes (the source and drain) that are at the same electrochemical potential ($\mu_S = \mu_D$). Recall from Chapter 1 that electrons cannot tunnel onto the dot (at least in a first-order process) since the additional energy required to do so exceeds the Fermi energy of the electrodes. An electron cannot tunnel off either, since $\mu_S = \mu_D > \varepsilon_0$. Hence current flow should be blocked.

Higher order tunnelling processes, though, allow virtual states where the energy barrier is exceeded momentarily (one instance is illustrated in Figure 4-15B). Here the spin-up electron from the dot has tunnelled off to the drain electrode. Simultaneously, a spin-down electron tunnels on from the source electrode (a spin-up electron is not permitted due to the Pauli Principle). The final situation is depicted in Figure 4-15C, noting that the unpaired spin on the dot has been flipped (the electrons at the Fermi level of the electrodes lie within a vast Fermi sea, so their spin polarisation is not preserved). This process leads to an enhanced density of states at the electrochemical potential of the electrodes, $\mu_S = \mu_D = 0$ (zero bias). This is the cause of the zero bias line seen in Figure 4-13A and as a peak in Figure 4-14C. Where the line exists, it has no gate voltage dependence since the Kondo tunnelling process is not strongly dependent on the energy spectrum of the dot at particular $V_g$ [57,58].
Figure 4-15 Kondo effect for an odd or even number of spins. (A) A quantum dot lies between two electrodes that are at the same electrochemical potential. One spin-degenerate energy level is shown, filled with one or two electrons. The addition of electrons is blocked since $\mu_S, \mu_D < U$ (charging energy). (B), (C) In the odd spin case, higher order tunnelling events allow this energy barrier to be exceeded momentarily, permitting net electron flow coupled with a spin flip. (D) In a singlet state (even number of electrons, all paired) this channel is not accessible. (E) Kondo transport can occur if the ground state is a triplet, possibly seen in our C$_{60}$ SET’s.
Conversely, if there are an even number of electrons on the dot that are all paired (Figure 4-15D), the spin-flipping process cannot occur and therefore, we do not normally expect zero bias conduction. As additional electrons are added to the dot, therefore, every second state should exhibit a zero bias line and this is indeed observed with GaAs and nanotube devices.

In our case, only one transition between odd ↔ even electron number states is visible, since the C\textsubscript{60} charging energy is so large. Remarkably, a zero bias line can be seen on both sides of that transition. One possible explanation requires the charge state with an even number of electrons to exist as a spin triplet rather than a singlet (Figure 4-15E). The most likely candidate is C\textsubscript{60}\textsuperscript{2-}, which is likely to have a triplet ground state according to previous density functional calculations [46]. C\textsubscript{60} itself is improbable, since it is known to be a closed shell molecule with a HOMO-LUMO gap of ~2 eV[12]. In Section 4.4 (ii), it was noted that the clusters in our SET’s were either neutral or in the -1 charge state, ruling out C\textsubscript{60}\textsuperscript{4-} as a possibility. If we assume our assignment is correct, then the transition being observed is C\textsubscript{60}\textsuperscript{1-} → C\textsubscript{60}\textsuperscript{2-}. The zero bias line is then more intense in the C\textsubscript{60}\textsuperscript{2-} state since it allows two channels for Kondo spin flips rather than one. While it is internally consistent, this argument has yet to be confirmed in other samples and thus remains speculative at present.

Up to this point, we have been examining transport behaviour at zero source-drain bias, which is known as the equilibrium Kondo effect. Applying a finite bias gives rise to its non-equilibrium counterpart [58]. If a potential \( V \) is applied between the electrodes, then the Kondo peak will split into two smaller peaks, each pinned at the Fermi level of one electrode (Figure 4-16 shows the contrast between the density of states in the equilibrium, Panel A and non-equilibrium, Panel B, situations). The peaks are also smaller due dissipative processes (lifetime broadening) that occur
as the electron moves from higher to lower chemical potential. If a magnetic field is also applied, the spin-degeneracy of the HOMO ($\omega_0$ in Figure 4-15) will be lifted, generating two states Zeeman split by $\pm g\mu_B B$, where $g$ is the $g$-factor, $\mu_B$ is the Bohr magneton and $B$ is the magnetic field. This prediction has no adjustable parameters, so it is a particularly stringent test of the Kondo theory. For a 10 T field, we had previously estimated a splitting of ~2.3 mV. Comparing this with the device in Figure 4-13/4-14, we note highly satisfactory agreement, with two lines visible at ±1.3 mV. Most importantly, neither has any gate dependence, which is the behaviour expected of Kondo levels. In contrast, $dI/dV$ features arising from first order transport through Zeeman-split molecular energy levels will show variations with $V_g$. Therefore, although the data

Figure 4-16 Density of states (DOS) of the dot in the Kondo regime. (A) In the equilibrium case where $\mu_S = \mu_D$, the sharp peak in the DOS lies at zero bias. A broader, lower peak represents the energy level at $\omega_0$ (see Figure 4-15). (B) In the non-equilibrium case where $\mu_S \cdot \mu_D = eV$, the DOS is split into two peaks, pinned at the Fermi level of each electrode. Adapted from Wingreen et al. [58]
is limited at this stage, a Kondo analysis appears fully consistent with our experimental results for C\textsubscript{60}.

One glaring omission, though, is the absence of data on the temperature dependence of transport through these SET’s (primarily because the devices have usually stopped functioning before such scans could be taken). Below the Kondo temperature, the zero bias conductance of triplet states is expected to decrease with increasing temperature, reach a minimum and then increase again (in comparison, the conductance in singlet states should increase monotonically) [53]. This probably results from destruction of the spin correlation in the tunnelling process as temperature increases.

Recently, preliminary temperature dependence data was obtained for a C\textsubscript{70} rather than a C\textsubscript{60} device. The two dimensional \(dI/dV\) plot for this device showed an extended region with a zero bias peak that splits into a doublet with the correct separation in a magnetic field. No Coulomb oscillations were observed for the gate voltage values that were accessible and therefore the results in Figure 4-17 are shown as a function of the bias voltage. Quite encouragingly, the Kondo peak height does decrease with increasing temperature, although the results need to be confirmed and extended to the C\textsubscript{60} system to complete the analysis.
4.9 Summary

The C$_{60}$ single electron transistor has proven to be a most interesting chemically-derived nanostructure, one in which many aspects of mesoscopic physics are observable. Throughout this chapter, we have described transport experiments in which the applied electric and magnetic fields and the sample temperature were varied to carry out spectroscopy on the molecule. In the process, we found that electronic and mechanical degrees of freedom can be coupled, even at the nanometre scale and also with suitable thought, an appealing name can be coined to label them (the vibraBall mode)! A junction exhibiting unusual transport behaviour led to the identification of the Kondo effect in these devices and significant work continues in this direction. In the next chapter, we create single electron transistors around a chemically diverse system: semiconductor nanocrystals and nanorods.
References and Notes


41. P. L. McEuen & W. Ho, personal communication


Chapter 5

Nanocrystal-based single electron transistors

5.1 Introduction

Nanocrystals are solids between 1-20 nm in size that retain the crystal structure of the bulk material. Each cluster consists of a few thousand atoms at most [1,2]. A wide variety of substances can adopt this form, including metals [3-5], metal oxides [6-8] and inorganic semiconductors [9-11], created using techniques such as gas phase cluster growth [12,13], solid state synthesis [14,15] and solution phase chemistry [16,17]. We shall focus only on semiconductor nanocrystals belonging to the II-VI family that have been made by colloidal synthesis, specifically cadmium selenide (CdSe) and its derivatives [18,19]. Figure 5-1A shows a transmission electron micrograph of a 5 nm CdSe nanocrystal in which individual lattice planes

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**Figure 5-1** Structure of a colloidal CdSe nanocrystal. (A) Transmission electron micrograph of the nanocrystal, observed along it (001) direction. The white dots correspond to atomic lattice fringes. The scale bar is 5 nm long. (B) Schematic of the nanocrystal showing alternating planes of Cd (blue) and Se (red), as well as the organic capping groups on the surface. Image courtesy of A.V. Kadavanich.
are visible (as the white dots). Their perfect ordering confirms that the nanocrystal is one
crystalline domain, with no stacking faults or atom dislocations. Figure 5-1B depicts its room
temperature crystal structure (which is wurtzite) with alternating cadmium and selenium planes
along the (001) direction. The nanocrystal is slightly prolate in this direction, with an aspect ratio
of 1.2: 1 between the long and short axes [20]. The entire cluster is capped with organic ligands,
which prevent the nanocrystals from aggregating and also permit chemical manipulation. Such an
object can be integrated into a variety of nanostructures, including our target, a nanocrystal-based
single electron transistor (SET).

The first half of this chapter opens by describing the synthesis of CdSe nanocrystals. This is
followed by a summary of its physical and chemical properties, especially those that make a
nanocrystal an attractive candidate for electron transport studies. Various industrial and academic
researchers have already incorporated them into different devices and we review their efforts as
well as our place in the field (Section 5.2). Some of our experiments on SET’s containing
nanocrystals are described in Section 5.3, where the discussion is confined to devices made using
the break-junction technique (as outlined in Chapter 3).

Recent modifications to the synthesis technique have led to rod-like nanocrystals over 50 nm in
length (termed quite unsurprisingly nanorods). Section 5.4 reviews the information currently
available on their synthesis and physical properties. We have carried out 2-terminal transport
measurements on these nanorods and the preliminary results are presented in Section 5.5.
5.2 Nanocrystals: a flexible chemical system

5.2 (i) Synthetic techniques

Colloidal CdSe nanocrystals can be made by the rapid injection of inorganic precursors (dimethylcadmium and elemental selenium in this case) into a solution of hot surfactant (tri-\textit{n}-octylphosphine oxide or TOPO in the usual procedure) \cite{16,21}. Rapid nucleation ensues, followed by a period of nanocrystal growth where their size increases and their size distribution narrows \cite{22}. Additional injections can be used to make larger nanocrystals if desired. Presently, TOPO-capped CdSe nanocrystals can be synthesised between 1-15 nm in diameter, with a 4\% size variance in the best cases. Once the basic synthesis has been completed, different precursors can be used to add an epitaxial shell of a different material (making “core-shell” nanocrystals such as CdSe/CdS) \cite{23}. Alternatively, ligand exchange can be used to modify the functionality of the surfactant group, an important step in building SET’s.

5.2 (ii) Physical properties and electronic structure

Semiconductor nanocrystals of different sizes (but the same chemical composition) exhibit a most striking property: they absorb and emit light across a wide spectrum of colours (clearly seen in Figure 5-2). The luminescence is also continuously tunable with size. Larger CdSe nanocrystals, for example, emit in the red region, while smaller ones shift towards the blue end of the spectrum (luminescing yellow and green) \cite{18,24}.

\footnote{Changing the chemical composition of the nanocrystals can extend this range further. Emission in the infrared occurs in InAs \cite{11} (and InP \cite{24} to a lesser extent), while blue (ZnS and CdS \cite{25,26}) and ultraviolet (TiO\textsubscript{2} \cite{27}) nanocrystals are also possible.}
Both of these observations result from changes in the electronic density of states as a function of nanocrystal size. A semiconductor will enter the *quantum-confined* limit, once the size (the Bohr radius) of the electron-hole pair (known as an *exciton*) created upon photon excitation exceeds the length scale of the object [19,29]. If spatially confined in one dimension, it is known as a quantum well, in two as a quantum wire and in all three as a quantum dot. The degree of quantum confinement determines the density of states in the system. Quantum dots have a discrete set of energy levels, intermediate between strict molecular orbitals and the solid-state material, which shows a series of continuous valence and conduction bands. Specifically, the size of the semiconductor band gap increases continuously with decreasing particle size, explaining the trend observed in the optical absorption and luminescence experiments.

A simple explanation for these changes in the size of the band gap can be found by modelling the nanocrystal as a “particle-in-a-sphere” with the potential becoming infinite at the surface [30,31]. The solutions to this problem are energy levels quantised by:

![Figure 5-2](image-url)  
*Figure 5-2* Optical emission from CdSe nanocrystals of different sizes. Larger nanocrystals (~ 5 nm in diameter) luminesce in the red part of the spectrum, while smaller ones (~ 3 nm) emit green light. The luminescence is continuously tunable with size. Image courtesy of M.P. Bruchez.
where $m_{\text{eff}}$ can be approximated as the effective mass of the electron in CdSe and $\alpha_{nl}$ is a constant dependent on the angular momentum of the particular eigenstate. Most significantly, the spacing between energy levels and hence the nanocrystal band gap increase with decreasing size. This is, of course, a very crude approximation and more quantitative results require an approach such as the $k\cdot p$ perturbation method (an effective mass approximation that uses parameters fitted from experimental data) [32-34] or a pseudopotential method (using a superposition of screened electrostatic potentials) [35-37]. Both calculations yield reasonable results for the electronic structure, but a full description lies beyond the scope of this chapter. For now, we turn to the experimental studies on quantum dots.

Optical studies have contributed the bulk of the information known about the electronic properties of these zero-dimensional systems. Absorption and photoluminescence are the simplest experiments. Amongst other successes, they have been used to explain the long emission lifetime of CdSe nanocrystals and the Stokes shift of their band edge luminescence [38,39], as well as measuring the quantum yield of nanocrystal emission [23]. Femtosecond spectroscopy has been used to probe the dynamics of the exciton in both CdSe and InP [40,41] and the vibrational spectrum of CdSe has been investigated by resonance Raman spectroscopy [42].

A major problem that arises in ensemble studies of nanocrystals is inhomogenous line broadening due to particles of slightly different sizes. Previously, techniques such as hole burning and fluorescence line narrowing [43] were used to reduce the effective linewidth of spectral features. More recently, spectroscopy on individual nanocrystals has become possible, revealing effects such as an extended LO phonon series, luminescence intermittency as an electron is ionised from
the nanocrystal into the surrounding matrix and spectral diffusion of the emission spectrum (probably due to trapped charges on the surface of the nanocrystal) [44-46].

5.2 (iii) Transport studies and device applications

Nanocrystals have been inserted into a number of device applications, all of which exploit their ease of band gap engineering and chemical manipulation. They act as the light-harvesting element in photovoltaic cells [47]. Under “solar” illumination, exciton formation occurs in a layer of nanocrystals, after which the electron and hole separate and pass through a conducting polymer matrix to their respective electrodes. Different sized nanocrystals can trap photons of different wavelengths. The inverse process (that is, electron-hole recombination emitting a photon) creates a light emitting diode [48,49]. Here charge is injected from two sides of a bilayer sandwich consisting of a layer of conducting polymer and one of nanocrystals. Recombination occurs close to the interface (on the polymer side). Varying the nanocrystal size produces different coloured diodes. A third application is as a photonic band gap material for fibre-optic applications [50,51]. CdSe nanocrystals are assembled within a matrix of ordered silica beads and then sintered together. The result is a periodic structure with a band gap at infrared wavelengths.

In comparison, electrical transport measurements on nanocrystals for purely spectroscopic reasons are less common. One recent effort used scanning tunnelling microscopy (STM) to explore the excited state spectrum of individual colloidal InAs nanocrystals, reporting results that showed an electronic structure with closed shells [52,53]. They were able to use this data to understand complimentary optical studies (photoluminescence excitation) and vice versa, clearly demonstrating the benefits of a combined approach.
5.2 (iv) Our niche in this field

When carrying out tunnelling spectroscopy, the advantages that accrued to our \( \text{C}_6\text{O} \)-based SET’s are also relevant here: the ability to apply an external electric field using a back gate and a device geometry that simplifies cryogenic operations and sample characterisation. Additionally, the power to change the nanocrystal band gap without changing the chemistry required to insert it into a SET brings devices such as switches, with tunable turn-on thresholds, closer to realisation. Lastly, straightforward manipulation of the surface ligands presents an opportunity to incorporate nanocrystals into more complex chemically-derived nanostructures.

5.3 Single electron transport through nanocrystals

Research on SET’s based on CdSe nanocrystals has a long history at Berkeley. These efforts made use of a small-gap junction geometry and their results have already been published elsewhere. In this section, we shall focus solely on experiments carried out with nanocrystal break-junction devices, which were actually the pioneering studies done to establish the break-junction technique (in hindsight, it’s obvious that blowing up a metal nanowire should produce just the right-sized gap to fit a small molecule!). Hence the data is not as high quality as for \( \text{C}_6\text{O} \), but even these initial studies approach the best small-gap junction results.

CdSe nanocrystals, 3-6 nm in diameter and capped with TOPO were used in these experiments. They are chemically tethered to an intact gold nanowire using bifunctional linker molecules (1,6-hexanedithiol), one end of the molecule attaching to the electrode and the other end to the nanocrystal. This approach ensures very high coverage of nanocrystals on the nanowire (probably too high for stable electrical measurements as we shall see below). Full details of this procedure
and of the sample die are summarised in Chapter 2. The device is cooled to low temperature (1.5 K) and the nanowire broken \textit{in-situ}, leaving two electrodes with a nanocrystal in the gap between them (at least in successful attempts).

Similar experiments are performed on nanocrystal junctions as on C$_{60}$ SET’s, namely 2- and 4-terminal AC and DC measurements, taken as a function of source-drain and gate voltage in an external magnetic field and at different temperatures. Figure 5-3A shows a now familiar two-dimensional plot of $dI/dV$ as a function of $V$ and $V_g$ taken for a 3 nm CdSe nanocrystal sample (the size is determined from its absorption spectrum). The conductance gap (indicated by the blue regions) is successfully tuned to zero by changing the gate voltage and this occurs at $V_g = -4.80$ V. The charging energy for this device is approximately 47 meV. Using Equation (1-2), with an electrode-nanocrystal separation of $d = 6$ Å (half the length of the hexanedithiol chain) and assuming that $\varepsilon = 2$ (the dielectric constant of the TOPO capping on the nanocrystal [54]), gives a calculated cluster size of 2.5 nm. This agrees reassuringly well with the known sample size of 3 nm.

A number of $dI/dV$ lines are visible away from the edge of the conductance gap. Figure 5-3B is a line trace taken at fixed gate voltage for the same device shown in Panel A. The black arrows mark two lines visible at positive bias voltages that intercept the ground state line at 3 and 8 mV respectively, indicating the position of these two excited states in the nanocrystal energy spectrum. Indeed this SET and others like it have shown that CdSe has an extensive manifold of excited states. Their mapping has been limited by premature device destruction. It must be noted that none of these features corresponds to the vibraBall mode observed in C$_{60}$. An estimate for the mass of a thousand-atom CdSe nanocrystal shows that it is about 8000 times more massive than a
Figure 5-3 Differential conductance through SET's based on CdSe nanocrystals. (A) A two-dimensional plot of the conductance as a function of source-drain and gate voltages at 1.5 K and zero magnetic field. (B) A line trace through the top diagram taken at $V_g = -4.5$ V is shown here. The black arrows mark the position of excited states as discussed in the body of the text.
single C_{60} molecule, which translates into a vibrational quantum that is almost two orders of magnitude smaller (tens of μeV compared with meV). At 1.5 K (where this device was measured), we have insufficient energy resolution to observe these particular energy levels.

One problem that makes it difficult to obtain detailed spectra is the amount of noise and the “switchiness” inherent in these devices. The data shown in Figure 5-3 has come from one of the most stable SET’s made from colloidal semiconductor nanocrystals. Even so, noise rapidly becomes an issue once higher bias voltages are applied. Most devices also tend to switch quite frequently, which means that a complete \( \frac{dI}{dV} \) diagram often requires different datasets to be stitched together. A factor contributing to this behaviour is the complicated chemical (and hence electrical) environment surrounding the nanocrystal. The TOPO capping groups and the dithiol linkers provide alternative electron transport pathways that tend to become active at arbitrary values of \( V \) and \( V_g \). They compete with the main electron tunnelling process, leading to short-term fluctuations in the current level that appear as noise.

Additional difficulties arise from the close proximity of neighbouring nanocrystals when a linker molecule is used to tether them to the electrodes. Scanning electron micrographs demonstrate that the nanocrystals often form close packed islands. Adjacent nanocrystals will randomly gate transport through the nanocrystal carrying most of the current, causing unexpected shifts in the observed energy spectrum. Another scenario has multiple dots conducting in parallel. An example is depicted in Figure 5-4. The \( \frac{dI}{dV} \) spectrum consists of several overlapping series of “diamonds”, corresponding to different nanocrystals starting to conduct at slightly different values of \( V \) and \( V_g \). Each nanocrystal is coupled to the source, drain and gate electrodes slightly differently and this is reflected in different slopes in the \( \frac{dI}{dV} \) lines. The net result is a rather complex spectrum, which is both noisy and switchy.
What are potential solutions to these problems? The key issue is probably the excessively high coverage of nanocrystals. One answer may to deposit a more dilute solution of nanocrystals, which should ensure a more even coverage and help prevent aggregation. It may also be possible to eliminate the linker molecule altogether, since they seem to work too well in producing a close packed nanocrystal layer. Control experiments show that this technique works reasonably well with TOPO capped CdSe nanocrystals and of course, it has been quite successful with C₆₀. Excluding the linker has the additional advantage of reducing the chemical debris in the active junction region. It is probably less helpful to eliminate the capping groups on the nanocrystals themselves since part of their function is to supply electronic passivation (thus preventing surface trap states from being formed). There is evidence to suggest that this step would be unnecessary, given that stable transport behaviour has already been observed with capped colloidal nanocrystals by STM.
5.4 Extending the paradigm: nanorods

In the first part of this chapter, we alluded to the chemical flexibility inherent to colloidal nanocrystals. This flexibility has been exploited to produce nanostructures with different shapes and sizes in the CdSe system, including crystalline nanorods up to 100 nm in length [55]. Figure 5-5A shows transmission electron micrographs of examples that are about 20 nm in length and 3 nm in diameter (an aspect ratio of ~7:1 in this case, although examples 100 nm long and 4 nm in diameter have been synthesised) [56]. Panel B of the same Figure depicts a high resolution image of the same sample, showing that the nanorod consists of a single crystalline domain (the atomic lattice fringes extend regularly throughout the nanorod without interruption) [57].

Objects of this size and uniformity are examples of one-dimensional quantum wires, the system being quantum confined radially (since the extent of the nanorod in that direction is smaller than the Bohr radius of the exciton) and unbounded along its long axis (the c-axis, in the nomenclature used to describe its wurtzite crystal structure). This makes them interesting candidates for transport spectroscopy and we describe preliminary experiments in this direction in the next section. In the meantime, we conclude this discussion with a brief summary of the nanorod synthesis technique.

CdSe nanorods are synthesised using small modifications to the nucleation and growth technique outlined in Section 5.2 (i) for spherical nanocrystals. The basic procedure requires highly preferential crystal growth along the (001) direction (the long axis), a process that can be controlled by varying three parameters. The longest rods require TOPO to be replaced as the
surfactant by a mixture of TOPO and hexylphosphonic acid (8% mole ratio), an additive that enhances the growth of the (001) crystal face over all others; use of a moderate initial injection rate, to allow the nucleation while leaving sufficient monomer concentration for rapid crystal growth; and slow addition of monomer solution subsequently to sustain growth while suppressing additional nucleation. A thin epitaxial shell can be grown subsequently as in the nanocrystal case by adding other precursors (CdS and ZnS are the only shells attempted to date) [57]. After the basic synthesis was completed, the nanorods were prepared for incorporation into SET devices. Longer rods were much more difficult to manipulate chemically at this stage. In particular, they tend to precipitate from most solvents (apart from chloroform), yielding an intractable product. Occasionally, addition of a small amount of dodecylamine will allow the product to be resuspended and reused.

Figure 5-5 Transmission electron micrographs of CdSe nanorods. (A) Low resolution image of a field of nanorods. The scale bar is 100 nm. (B) High resolution image of the same sample, showing wurtzite (100) lattice fringes and confirming the crystallinity of the nanorods. The long axis is the (001) axis and the scale bar is 10 nm long. Adapted from Manna et al. [57].
5.5 Electrical transport through nanorods

Nanorods have one advantage that makes electrical transport experiments easier (compared with nanocrystals or C\textsubscript{60}): their length (typically $\geq$20 nm for the samples we have measured) allows electrical contacts to be attached much more simply. We have chosen to do so using break-junction electrodes. This technique allows the junction to be formed \textit{in-situ} at low temperature, exposing fresh metal surfaces to the nanorod, leading to better contact with the electrodes and hence a more stable tunnelling spectrum. Alternatively, for the longest samples (~100 nm), the nanorod may be deposited first and then metal electrodes fabricated on top of them, ensuring similar high quality contacts. This approach has been used successfully in nanotube devices.

Before presenting the results from our nanorod transport studies, we briefly describe the device and its fabrication process. CdSe nanorods (~20 nm long and 4 nm wide, see Figure 5-6A for a transmission electron micrograph of the sample) coated with a single layer of CdS, were stripped of their TOPO/hexylphosphinic acid capping groups by refluxing in pyridine under an argon atmosphere. A SET die with intact nanowires was cleaned with oxygen plasma and the nanorod solution immediately deposited upon it. The entire device was baked at 180 °C (flowing nitrogen, reduced pressure) to ensure removal of the weakly attached pyridine ligands (and hence good contact between the nanorod and the electrodes), while preventing sample oxidation (which occurs rapidly at elevated temperatures if any oxygen is present).

The nanowire was subsequently broken at 77 K, which tends to produce electrodes with a larger separation than those broken at 1.5 K. The bias voltage was ramped steadily at 30 mV/s until the junction failed (the conductance trace is shown in Figure 5-6B). Unlike C\textsubscript{60} SET’s, there appears
to be little evidence of step-like structure in the conductance centred around $e^2/h$ (the conductance quantum). The device was then cooled to 1.5 K for spectroscopic measurements.

A limited set of 2-terminal DC measurements was carried out on these nanorod devices, as a function of the applied magnetic field and the temperature. Figure 5-7A displays a plot of the differential conductance as a function of $V$ and $V_g$ at zero magnetic field. The conductance gap (blue regions in the diagram) can be tuned reversibly with gate voltage, although it never closes completely to zero. At positive bias voltages, the ground state $dI/dV$ lines intersect at $V = 0$ as expected (we shall call the gate voltage at this point $V_g = V_c$ for reference purposes only), but its counterpart at negative voltages consists of two different features, marked “a” and “c” in the Figure. In both cases, their lowest energy $dI/dV$ lines approach, but do not intersect at $V = 0$, which is an observation also been made in C_{60} devices, but it remains unexplained at this time.
Figure 5-7 Magnetic field dependence of a CdSe nanorod device. (A) Two-dimensional $dI/dV$ plot taken as a function of $V$ and $V_g$ in zero applied magnetic field at 1.5 K. Three noticeable features, marked “a”, “b” and “c” in the diagram are discussed more fully in the text. (B) They shift quite significantly when a 10 T field is applied to the device.
There is another interesting feature visible near $V_g < V_c$, namely a line of negative differential resistance (or NDR) that is labelled “b” in the Figure. A line trace taken at a fixed gate voltage within this region is shown in Figure 5-8. As the bias voltage is increased in the positive direction, the device behaves normally: conduction is zero due to Coulomb blockade until a sufficiently large voltage has been applied to access the nanorod charge state with one fewer electrons (indicated by the sharp $dI/dV$ peak). In the negative direction, the differential conductance becomes negative (which corresponds to a decrease in the current level as the applied voltage increases). The exact cause of NDR in this device is not known, although one intriguing explanation is conduction through dots in series. Referring back to the TEM of this sample in Figure 5-6A, we notice that nanorods in this sample may consist of multiple crystalline domains. If these conduct as multiple dots in series, then current will flow only if the energy levels of all the dots are aligned, a situation which will give rise to NDR.

**Figure 5-8** Negative differential resistance in a CdSe nanorod device. A line trace is depicted here, taken at fixed gate voltage for the device shown in Figure 5-7A (zero magnetic field, 1.5 K) near the feature marked “b”. The black arrow in this diagram indicates the region of negative differential resistance.
Our suggestion (not even a hypothesis at this stage) is supported by the observed charging energy of the nanorod, which is about 75 meV (from the maximum width of the conductance gap). This value is much larger than expected for a cylinder 20 nm long and 4 nm in diameter, which are the overall dimensions of the nanorods used in this experiment. Using the results calculated for a spherical nanocrystal in Section 5.3 (where a charging energy of 47 meV corresponded to an object size of 2.5 nm) as a guide only, we anticipate that the dot in the nanorod case is of this size too (and not ten times larger). This agrees reasonably well with the domain size seen in the TEM image.

To understand the transport behaviour we have just outlined more fully, we subjected the device to an external magnetic field. A $dI/dV$ diagram as a function of $V$ and $V_g$ for a 10 T field is shown in Figure 5-7B. The spectrum at positive bias is relatively unchanged, apart from a small bend in the ground state line at $V_g < V_c$. At negative voltages, though, the feature labelled “a” in the zero field plot has shifted to higher voltage. Data taken at other magnetic fields (1, 3, 4 and 5 T) shows that the apex of the feature appears at increasing voltages as the field increases. No explanation has been found for this phenomenon. Note that feature “c” does not appear to shift with magnetic field and based on that observation, we assign it as the other half of the closing conductance gap. The line of NDR is still there and there appears to be no Zeeman splitting of any of the spectral features. From the electron $g$-factor measured in bulk CdSe ($g = 0.68$), we would expect a 0.8 meV line splitting in a 10 T field, which should just be visible in this experiment.

We were also able to conduct temperature dependence experiments on this device. It appeared to be remarkably stable with respect to thermal cycling from base temperature up to ~50 K, the $dI/dV$ spectrum (and its field dependence) being unchanged once the sample was returned to 1.5 K. Characteristics of single electron charging (a conductance gap that could be tuned to zero
with gate voltage for example) were observed at 77 K, although the device was very unstable at this temperature. It even conducts at room temperature, with evidence of some gate voltage dependence. The absence of a crossing point at zero bias prevented us from observing the temperature dependence of a Coulomb oscillation. The device was measured at voltages outside the linear response regime for temperatures and it appears that the conductance increases monotonically with temperature, with no power law dependence observed.

5.6 Summary

We have demonstrated that devices can be made from semiconductor nanocrystals and nanorods using the break-junction technique, with relatively stable electrical characteristics and in good yield. Preliminary measurements on both these systems show quite interesting results. In the nanocrystal case, transport spectra comparable to the quality of C_{60} data should be obtainable once the interaction between neighbouring particles is eliminated (by reducing sample concentration). Such results should allow direct comparison with optical spectra. Nanorods show (unexplained) conductance that depends strongly on the applied magnetic field. It may arise partially from a fascinating possibility, individual crystalline domains conducting in series. Additional experiments are needed to characterise and explain these effects fully.
References and Notes


56. L. Manna, personal communication
Chapter 6

Conclusions

6.1 A retrospective

In Chapter 1, we put forward two objectives: to create innovative nanostructures centred upon chemical species and to probe their physical properties using electrical transport measurements. We were specifically interested in building single electron transistors based on individual nanometre-sized molecules ($C_{60}$ as well as semiconductor nanocrystals and nanorods). In this chapter, we consider how successful we were in fulfilling those goals.

One of the major hurdles inherent in building these structures is finding a way to connect electrodes from a few nanometre-sized objects to the external metre-sized world where the measurements are made, a span of nine orders of spatial magnitude. We described two methods to do so: break-junctions made by the electromigration-induced failure of metal nanowires and junctions drawn lithographically so that the electrodes are spaced by a small gap. The former was found to be more successful in yielding devices that not only conducted, but also showed stable electrical behaviour under test. For these reasons, break-junctions became the focus of our experimental work.

An understanding of the process of junction formation, through electromigration occurring on a nanometre scale, is of fundamental interest. It is also a highly reliable diagnostic tool to differentiate between successful single electron transistors and tunnel junctions not containing the sample molecule. Analysis of the junction conductance of $C_{60}$ devices as the nanowire was
broken showed quantum conductance plateaux that were particularly helpful in predicting the subsequent behaviour of the device.

$C_{60}$ became the major chemical system examined in this study. It satisfied the requirement for a novel nanostructure, since the charging energy of $C_{60}$ is sufficiently high that stable devices should be room temperature single electron transistors. This is a requirement for practical application on anything but an experimental scale. Our goals were far more modest: to probe the transport spectroscopy of a $C_{60}$-based device by tuning experimental parameters such as the transistor bias voltage, the applied electric and magnetic fields and the temperature. We found that electronic and vibrational degrees of freedom could be coupled even on the nanometre scale and postulated a molecular oscillation within a transistor junction dubbed the “vibraBall” to explain our observation. In a few devices, individual $C_{60}$ molecules were well coupled to their electrodes, moving those systems into the Kondo regime. Finite conduction at zero bias voltage becomes possible, as a result of correlated tunnelling between two electrons involving a series of virtual states.

We have also used the break-junction technique to create single electron transistors based upon colloidal semiconductor nanocrystals. These devices allowed us to probe a system that was quantum confined in all three dimensions and in several instances, we observed a complex spectrum of excited states. These nanocrystals are chemically quite flexible and recent syntheses have produced elongated nanorods that are no longer confined in one direction (that is, one-dimensional systems). We have begun preliminary transport studies on these devices too and they show an intriguing dependence on magnetic field.
6.2 Future directions

Where do we go from here? In the short term, previous success with break-junctions based on gold nanowires indicates one direction of inquiry. Nanowires can be made from aluminium, providing a superconducting density of states in the electrodes or from cobalt, allowing experiments with spin-polarised electrons. For any electrode material, the nanowire should break cleanly, leaving a nanometre-sized gap. Aluminium is a logical choice, since its electromigration behaviour is well known from studies in the semiconductor industry.

As for the choice of chemical system, it may be interesting to probe C\textsubscript{70} and its homologues to confirm the presence of the vibraBall mode seen in C\textsubscript{60}. Preliminary studies of C\textsubscript{70} have shown evidence for the Kondo effect in these devices and it would be noteworthy to confirm that such behaviour is quite general. It would also be appealing (and quite simple) to determine whether the stacking faults in semiconductor nanorods affect electron transport, a possibility alluded to in Chapter 5. From a wider perspective, semiconductor nanocrystals appear to have well understood chemical properties and they may be the best option when the electronic properties of a device need to be tuned without resorting to wholesale changes in the chemical processing (such applications have already been found in fluorescent labelling and photovoltaic devices).

In the longer term, single electron transistors may be incorporated into sensing elements. For this application, chemically-derived devices can designed using insights from biology (DNA templated molecular recognition, for example) and organic chemistry (targeted linkages using molecules that form self-assembled monolayers, for instance). An early step in this direction may incorporate carbon nanotube charge sensors to detect particular ions in an electrophoretic stream.
Appendix A

Details of single electron transistor device fabrication

Fabrication is carried out primarily in the UC Berkeley Microfabrication Laboratory in Cory Hall. We also make use of metal deposition systems (contact the Haller group) and the Nanowriter electron-beam lithography system (contact Erik Anderson) in Building 2 at LBL.

Two generations of single electron transistors have been produced during my time here, namely break-junctions and small-gap junctions. In both cases, the basic fabrication modules are:

- Growth of field oxide
- Growth of gate oxide (gate layer)
- Contact to the gate (gate contact layer)
- Definition of metal interconnects and bonding pads (metal1 and metal2 layers)
- Definition of active junction regions (e-beam layer)

We are currently using break-junction devices (set13 – set27 and succeeding die) from wafer n++Si06. They represent the newest design layout and should be used as the starting point for future modifications. Small-gap junctions were produced from wafers dkg (dkg01 – dkg32) and n++Si01 (set01 – set12). What follows are complete directions for device fabrication as well as the succeeding sample deposition (C_{60}, nanocrystals or nanorods) and packaging.
A.1 Fabrication of break-junctions

The starting materials are 4-inch (100), 500-550 μm thick, prime grade, single-sided polished silicon wafers, n-(arsenic) doped to a resistivity range between 0.001 – 0.005 Ωcm (Nova Electronic Materials, Richardson TX). The entire layout (apart from the Nanowriter run file) is stored in set.tdb, an L-Edit design file.

Growth of field oxide (tylan1/tylan2, CMOS clean atmospheric oxidation furnaces)

1. Pre-clean tylan1/tylan2 with trichloroethylene (TCA) using the stca1-4 program (TCA cleaning at 1100 °C, overnight).
2. In sink6, cycle the wafers through the standard pre-furnace cleaning module, that is immerse in Piranha (approximately 5:1 H₂SO₄: H₂O₂), 120 °C, 10 minutes; rinse with de-ionised (DI) water; strip surface oxide in 1:10 HF: water (VLSI grade); rinse with DI water to a resistivity setpoint of 16 MΩcm.
3. Grow approximately 1 μm of “wet” silicon dioxide at 1000 °C, 5 hours (tylan1/tylan2) in a steam atmosphere using the swetoxb program (the major steps are a 5 min “dry” pre-oxidation under O₂, the main oxidation under steam/O₂ and a 20 min N₂ post-oxidation anneal). Exact oxide thickness should be checked with film thickness measuring equipment (Nanometrics Nanospec AFT).

Patterning and growth of gate regions (gcaws2, GCA 6300B 10x wafer stepper & tylan5/tylan6, gate oxide CMOS atmospheric oxidation furnaces)

1. De-hydrate the wafers at 120 °C (convection oven), 20 min.
2. Prime the wafers with hexamethyldisilazane (HMDS) at 120 °C, 1 min (primeoven cycle 0).
3. Spin Shipley Microposit S1818 G-line photoresist onto the front side of the wafers using 340 rpm, 10 s spread and 6000 rpm, 30 s spin steps (svgcoat2, program 9). Bake at 90 °C, 8 min.

4. Determine the optimal exposure dose for the wafer stepper (for gcaws2, use the *expo square* program). Optimal settings were exposure 0.2 s, focus 260 (13/8/1999). Using the *gate* mask from the *set* mask series, flash the *11x13* exposure program onto the sample wafers in gcaws2.

5. Develop the wafers in Shipley Microposit Developer Concentrate: water (1:1) at room temperature, 50 s with gentle agitation. Rinse with water.

6. Hard bake the photoresist at 150 °C (oven), 1 hour.

7. Etch the gate regions back to the silicon substrate in 5:1 buffered oxide etch (etch rate ~100 nm/min, so approximately 12 minutes, err on the side of over-etching). Rinse with water.

8. Pre-clean tylan5/tylan6 with trichloroethylene (TCA) using the stca5-6 program (TCA cleaning at 1100 °C, overnight).

9. Strip the photoresist remaining on the wafers in PRS-3000 Positive Photoresist Stripper at 80 °C, 20 min (sink5). Rinse the wafers with water in spindryer3.

10. Cycle the wafers through the standard pre-furnace cleaning modules in sink8 and then sink6.

11. Grow approximately 30 nm of “dry” silicon dioxide at 900 °C, 100 min (tylan5/tylan6) in an O₂ only atmosphere using the *sgateox* program (the major steps are the main oxidation under O₂ and a 40 min N₂ post-oxidation anneal). Exact oxide thickness should be checked with the Nanospec.
Contacting the gate – back side contacts (Haller electron-beam evaporator & heatpulse1, rapid thermal processing), the standard approach & a simpler process

1. Spin Olin OiR 897-10i I-line photoresist onto the front side of the wafers at 1300 rpm, 30 s (svgcoat1/2, program 5). Bake at 90 °C, 60 s. Repeat the process. Hard bake at 150 °C, 1 hour.

2. Etch the back side of the wafers back to the silicon substrate in 10:1 buffered oxide etch (etch rate ~23 nm/min, approximately 3 min). Rinse with water.

3. Immediately transfer the wafer into the evaporator for platinum deposition (use the 4”-wafer holder in the Haller evaporator). Evaporate 150 nm of Pt at 0.1 nm/s for the first 20 nm and 0.5-1 nm/s for the remainder.

4. Strip front side protection resist with PRS-3000 at 80 °C, 20 min (sink5). Rinse the wafers with water in spindryer3.

5. Rapid thermal anneal in heatpulse1 under Ar ambient in two steps: at 375 °C, 60 s and then at 700 °C, 60 s. Purge the annealing chamber thoroughly before annealing (for 20 minutes) otherwise poor contacts are formed.

Contacting to the gate – front side contacts (gcaws2, Haller RF sputterer & heatpulse1), used in manufacturing nanotube “superchips”

1. De-hydrate the wafers at 120 °C (convection oven), 20 min.

2. Prime the wafers with HMDS at 120 °C, 1 minute (primeoven cycle 0).

3. Spin Shipley S1818 photoresist onto the front side of the wafers at 4000 rpm, 30 s (spinner1).
   Bake at 90 °C, 5 min.

4. Immerse in chlorobenzene, 5 min. Bake at 90 °C, 5 min.

5. Using the gatecontact mask from the set mask series, flash the 11x13 exposure program onto the sample wafers in gcaws2.
6. Develop in Shipley Microposit Developer Concentrate: water (1:1) at room temperature, 60 s with gentle agitation. Rinse with water and blow the wafers dry.

7. Hard bake the photoresist at 120 °C (oven), 1 hour.

8. Etch the gate regions back to the silicon substrate in 5:1 buffered oxide etch (etch rate ~100 nm/min, so approximately 12 minutes, err on the side of over-etching). Rinse with water.

9. In the Haller RF sputterer, sputter successively platinum (250 nm, 4 × 30 s depositions, spaced by 30 s substrate cooling periods) and tungsten (150 nm, 8 × 30 s depositions, spaced by 30 s substrate cooling periods) onto the front side of the wafer.

10. Lift off in acetone. Rinse with IPA.

11. Strip any remaining photoresist with PRS-3000 at 80 °C, 1 hour (sink5). Rinse the wafers with water in spindryer3.

12. Rapid thermal anneal in heatpulse1 under Ar ambient at 700 °C, 180 s. Purge the annealing chamber thoroughly before annealing (20 minutes) otherwise poor contacts are formed.

Definition of metal interconnects and bonding pads (v401, Veeco 401 thermal evaporator, gcaws2 & disco, Disco Automatic Dicing Saw)

1. In v401, evaporate successively chromium (3.5 nm, 0.1 nm/s) and gold (40 nm, 0.1 nm/s for the first 10 nm and then 0.5 nm/s for the remainder) onto the wafers.

2. Spin 10i photoresist onto the front side of the wafer at 4100 rpm, 30 s (svgcoat1/2, program 1). Bake at 90 °C, 1 min.

3. Using the metall mask from the set mask series, flash the 11x13 exposure program onto the sample wafers in gcaws2. Optimal settings were exposure 0.95 s, focus 250 (7/10/1999). Ensure symmetric alignment of the metall layer with the gate layer and close down the shutters in gcaws2 to prevent exposure of neighbouring die.
4. Develop the pattern using Olin OPD 4262 positive resist developer, 60 s (svgdev, recipe 1).

5. Hard bake at 120 °C (convection), 1 hour.

6. Etch the metal1 pattern using successively Transcene TFA gold etchant (Danvers, MA):
   water (1:1), room temperature, 20 s and Cyantek CR-7 chromium etchant (Fremont, CA),
   room temperature, 7 s. Rinse with water.

7. Strip all photoresist with PRS-3000 at 80 °C, 40 min (sink5). Rinse the wafers with water in
   spindryer3.

8. Spin S1818 photoresist onto the front side of the wafers using 340 rpm, 10 s spread and 6000
   rpm, 30 s spin steps (svgcoat2, program 9). Bake at 90 °C, 3 min.

9. Immerse in chlorobenzene, 5 min. Bake at 90 °C, 2 min.

10. Using the metal2 mask from the set mask series, flash the 11x13 exposure program onto the
    sample wafers in gcaws2. Optimal settings were exposure 0.24 s, focus 260 (13/10/1999).

11. Develop in Shipley Microposit Developer Concentrate: water (1:1) at room temperature, 70 s
    with gentle agitation. Rinse with water.

12. In v401, evaporate successively chromium (3.5 nm, 0.1 nm/s) and gold (200 nm, 0.1 nm/s for
    the first 10 nm and then 0.5-1 nm/s for the remainder) onto the wafers.

13. Liftoff in acetone. Rinse with IPA.

14. Spin 10i photoresist onto the front side of the wafer at 1300 rpm, 30 s (svgcoat1/2,
    program 5). Bake at 120 °C (convection), 5 min.

15. Dice the wafer (with 11 rows and 21 columns of die) into blocks that can be used in the
    Nanowriter using the disco dicing saw (diamond blade). The row pitch is 7.62 mm and the
    column pitch is 4.23 mm. Row offset is 1.81 mm and column offset is 0.27 mm. Typically we
    use blocks of 3 rows and 4 columns. Dicing speed should be 5 mm/s and the wafer is cut so
    that 175 μm remains (no dicing tape).
Definition of active junction regions (Nanowriter electron-beam lithography system & Haller electron-beam evaporator)

1. Strip the dicing protection resist from a 3 row/4 column block with PRS-3000 room temperature, 30 min. Rinse with acetone, IPA.

2. Dehydrate at 120 °C (convection), 10 min.

3. Spin MicroChem NANO MMA(8.5)MAA (9% in ethyl lactate) e-beam resist (Newton, MA) onto the front side of the block at 3500 rpm, 30 s (spinner1). Bake at 150 °C, 1 hour.

4. Spin MicroChem NANO 950KPMMA (3.5 % in anisole) e-beam resist on to the front side of the block at 6000 rpm, 30 s (spinner1). Bake at 150 °C, 1 hour.

5. To mount the block at the centre of a 4” wafer (thus enabling standard Nanowriter wafer handling techniques to be used), use the following steps. Remove 3 (expendable) pieces of silicon from the same wafer as the block. These will serve as references for the Nanowriter front side height alignment system. Spin Olin 825 35 G-line photoresist onto a blank wafer at 2200 rpm, 30s. Rapidly, position (by hand) the block at the centre of the wafer (wafer flat to the right) and the 3 reference pieces at the positions of the sapphire balls in the height alignment system. Bake at 120 °C, 3 min.

6. Using the set Nanowriter run file, expose all 12 die in the block (accelerating voltage 100 kV, dose 3500 μC/cm², beam current 500 pA). To produce overlapping junctions, junction separations in the CAD file were typically 220 – 260 nm.

7. Develop in 4-methyl-2-pentanone (MIBK): IPA (30:70), 30 s with agitation and MIBK: IPA (20:80), 15 s.

8. Load the block onto the centreline of the angle evaporation stage (equipped with ±15° stops) for the Haller e-beam evaporator. Evaporate successively at +15° Cr (3.5 nm, 0.1 nm/s) and Au (10 nm, 0.1 nm/s), at -15° Cr (3.5 nm, 0.1 nm/s) and Au (10 nm, 0.1 nm/s) and
horizontally Cr (3.5 nm, 0.1 nm/s) and Au (0.1 nm/s for the first 10 nm and then 0.5-1 nm/s for the remainder).

9. Liftoff in acetone. Rinse with IPA.

10. Spin 10i photoresist onto the front side of the block at 1300 rpm, 30 s (spinner 1). Bake at 90 °C, 3 min.

11. Dice the block into individual die in the disco using the row and column parameters in step 5 of this module. This time it will be necessary to use dicing tape.

12. Strip the dicing protection resist from the block with PRS-3000 room temperature, 30 min.
    Rinse with acetone, IPA.

Depositing C₆₀ (a typical protocol) – the procedure for nanocrystal or nanorod devices without bifunctional linker molecules is similar

1. Mix C₆₀ (Southern Chemical Group, 99.5 % purity, 21 mg) with toluene (Fisher, analytical grade, 6 mL) in quartz tubes. Ultrasonicate the solution in the VWR 75D ultrasonic bath (power 7, 10 min).

2. Centrifuge the solution at approximately 1000 rpm (1000 g in this case), 15 min. Remove 1 mL of the supernatant and dilute with 6 mL of toluene, again in quartz glassware. Keep the solution wrapped in aluminium foil.

3. Rinse a die (made above) with acetone, IPA.

4. Pre-clean technics-c with O₂ plasma (300 W, 20 min). Place the die onto a glass slide in the chamber, which should then be purged well. O₂ plasma clean at 80 W, 4 min (these parameters are close to the upper limit for junction survival).

5. Immediately drop 1 drop of the diluted C₆₀ solution onto the die. Allow it to dry slightly before wicking and then blowing the solution off. Repeat as many times as necessary (15 drops yields a good density of working devices).
Mounting the device (westbond, West Bond 7400B ultrasonic wedge bonder)

1. Mount the die in a 16-lead side braze pin packages (currently CSB01644, Spectrum Semiconductor Materials, San Jose CA) using a small amount of silver paint. Bake at 120 °C, 10 min.

2. Wire bond using the westbond, taking grounding precautions to prevent electrostatic discharge from destroying the device. Typically we bond the gate first, all signal pins and then the two pins connecting the ground bar. It may be difficult to bond to the pads on the die itself due to C₆₀ buildup. If so, increasing the ultrasonic power (up to 450 arbitrary units) may help.

3. Once the device is bonded, it is stable for up to a week if kept under aluminium foil in an anti-static foam box.

A.2 Fabrication of small-gap junctions

The starting materials are 4-inch (100), 500-550 μm thick, test grade, single-sided polished silicon wafers, n-doped to a resistivity range between 0.001 – 0.008 Ωcm (PCA). The patterns for photolithography are stored in maskf.kic (an xkic3 design file) and individual e-beam patterns are stored as dkgXX.rf6 or setXX.rf6 (NPGS run files) and xxxyyy.dc2 (DesignCAD 2D ASCII design files).

Growth of field oxide (tylan1/tylan2)

1. Pre-clean tylan1/tylan2 with trichloroethylene (TCA) using the stca1-4 program (TCA cleaning at 1100 °C, overnight).

2. In sink6, cycle the wafers through the standard pre-furnace cleaning module.
3. Grow approximately 1 μm of “wet” silicon dioxide at 1100 °C, 3 hours (tylan1/tylan2) in a steam atmosphere using the *swetoxb* program. Exact oxide thickness should be checked with the Nanospec.

Patterning and growth of gate regions (quintel, Quintel Q-2001CT Contact Printer & tylan5/tylan6)

1. De-hydrate the wafers at 120 °C (convection oven), 20 min.
2. Prime the wafers with HMDS at 120 °C, 1 minute (primeoven cycle 0).
3. Spin Shipley S1818 photoresist onto the front side of the wafers at 6000 rpm, 30 s (spinner1).
   Bake at 90 °C, 5 min.
4. Using the *cm* mask from the *dklein* mask series, flash the pattern onto the sample wafers in the quintel. The optimal setting was a 6 s exposure.
5. Develop in Shipley Microposit Developer Concentrate: water (1:1) at room temperature, 60 s with gentle agitation. Rinse with water and blow the wafers dry.
6. Hard bake the photoresist at 120 °C (convection), 1 hour.
7. Etch the gate regions back to the silicon substrate in 5:1 buffered oxide etch (approximately 12 minutes, err on the side of over-etching). Rinse with water.
8. Pre-clean tylan5/tylan6 with trichloroethylene (TCA) using the stca5-6 program (TCA cleaning at 1200 °C, overnight).
9. Strip the photoresist remaining on the wafers in PRS-3000 at 80 °C, 20 min (sink5). Rinse the wafers with water in spindryer3.
10. Cycle the wafer through the pre-furnace cleaning modules in sink8 and then in sink6.
11. Grow approximately 70 nm of “dry” silicon dioxide at 950 °C, 120 min (tylan5/tylan6) in an O₂ only atmosphere using the sgateox program. Exact oxide thickness should be checked with the Nanospec.

Contacting the gate (quintel, v401, & tylan14, Al annealing furnace)

1. De-hydrate the wafers at 120 °C (convection oven), 20 min.
2. Prime the wafers with HMDS at 120 °C, 1 minute (primeoven cycle 0).
3. Spin Shipley S1818 photoresist onto the front side of the wafers at 6000 rpm, 30 s (spinner1).
   Bake at 90 °C, 5 min.
4. Immerse in chlorobenzene, 5 min. Bake at 90 °C, 5 min.
5. Using the gate mask from the dklein mask series, flash the gate regions onto the sample wafers in the quintel. The optimal setting was a 6 s exposure.
6. Develop in Shipley Microposit Developer Concentrate: water (1:1) at room temperature, 60 s with gentle agitation. Rinse with water and blow the wafers dry.
7. Hard bake the photoresist at 120 °C (convection), 1 hour.
8. Etch the gate regions back to the silicon substrate in 5:1 buffered oxide etch (approximately 12 minutes, err on the side of over-etching). Rinse with water.

9. In v401, evaporate aluminium (200 nm, 0.1 nm/s for the first 10 nm and then 0.5-1 nm/s for the remainder) onto the wafers.
10. Liftoff in acetone. Rinse with IPA.
11. Strip any remaining photoresist with PRS-3000 at 80 °C, 40 min (sink5). Rinse the wafers with water in spindyer3.
12. Anneal at 400 °C, 25 min (tylan14) under a H₂/N₂ (4%) reducing atmosphere using the vsint400 program (the major step is an anneal done at the programmed temperature).
Definition of metal interconnects and bonding pads (quintel & v401)

1. Repeat steps 2-6 of Contacting the gate using the \textit{cp} mask from the \textit{dklein} set in the quintel.

2. In v401, evaporate successively chromium (3.5 nm, 0.1 nm/s) and gold (40 nm, 0.1 nm/s for the first 10 nm and then 0.5 nm/s for the remainder) onto the wafers.

3. Liftoff in acetone. Rinse with IPA. If any metal remains, remove it using gentle ultrasonication.

4. Repeat steps 1-3 in this section using the \textit{cc} mask from the \textit{dklein} set. This time evaporate chromium (3.5 nm) and gold (250 nm).

5. Liftoff in acetone. Rinse with IPA.

Definition of active junction regions (jeol107, JSM-6400/NPGS electron-beam lithography system & Haller electron-beam evaporator)

1. Spin MicroChem NANO MMA(8.5)MAA (9 \% in 2-ethoxyethanol) e-beam resist (Newton, MA) onto the front side of the entire wafer at 3000 rpm, 30 s (spinner1). Bake at 150 °C, 1 hour.

2. Spin MicroChem NANO 950KPMMA (2 \% in chlorobenzene) e-beam resist on to the front side of the entire wafer at 6000 rpm, 30 s (spinner1). Bake at 150 °C, 1 hour.

3. Using a diamond scribe, score and break-off single die to be written in the jeol107. Use only those pieces where the resist appears uniform.

4. Using the \textit{dkgXX} or \textit{setXX} NPGS run file, expose each die in the jeol107 (accelerating voltage 20 kV, dose 600 \(\mu\)C/cm\(^2\) for the finest features or 150 \(\mu\)C/cm\(^2\) for the interconnects, beam current 5 pA). To produce small-gap junctions, separations in the CAD file were typically 220 – 260 nm.

5. Develop in MIBK: IPA (30:70), 30 s with agitation and MIBK: IPA (20:80), 15 s.
6. Load the block onto the centreline of the angle evaporation stage (equipped with ±15° stops) for the Haller e-beam evaporator. Evaporate successively at +15° Cr (3.5 nm, 0.1 nm/s) and Au (10 nm, 0.1 nm/s), at -15° Cr (3.5 nm, 0.1 nm/s) and Au (10 nm, 0.1 nm/s) and horizontally Cr (3.5 nm, 0.1 nm/s) and Au (0.1 nm/s for the first 10 nm and then 0.5-1 nm/s for the remainder).
7. Liftoff in acetone. Rinse with IPA.

Depositing CdSe nanocrystals using a linker molecule (a sample process)
1. Mix 1,6-hexanedithiol (Fluka, >97% purity, 0.38 mL) with IPA (Fisher, electronic grade, 10 mL). Transfer to a container that will retain the solvent for 24 hours.
2. Rinse a die (made above) with acetone, IPA.
3. Pre-clean technics-c with O₂ plasma (300 W, 20 min). Place the die onto a glass slide in the chamber, which should then be purged well. O₂ plasma clean at 80 W, 4.
4. Immediately place the die in the hexanedithiol solution, close the container and stir. After 24 hours, remove the die and rinse it well with IPA.
5. Mix dry CdSe nanocrystals capped with trioctylphosphine oxide (TOPO) with enough toluene (Fisher, analytical grade) to give a UV optical density of ~1 at the first exciton peak when measured through a cell with a 1 cm path length. Filter through a 0.22 μm PTFE filter.
6. Immerse the die in this solution and stir for 24 hours. Remove the die and rinse well with toluene.
A.3 Fabrication of SiN membrane devices

Fabrication of free-standing silicon nitride (SiN) membranes proceeds in two major steps:

- Growth of low-stress nitride
- Patterning and bulk micro-machining of the substrate

followed by the creation of device features by:

- Definition of metal interconnects (metal1 and metal2 layers)
- Definition of active junction regions (e-beam layer)

These structures were used as substrates onto which nanocrystals were deposited and then the entire device viewed in a TEM (tem01 – tem016n). Below are directions for fabrication only.

The starting materials are 2-inch (100), p-doped, prime grade, single-sided polished silicon wafers. The patterns for photolithography are stored in measTEM2.kic (an xkic3 design file) and individual e-beam patterns are stored as temXXnYY.rf6 (NPGS run files) and xxxyyy.dc2 (DesignCAD 2D ASCII design files).

Growth of low-stress nitride (tylan18, low-pressure chemical vapour deposition furnace)

1. In sink6, cycle the wafers through the standard pre-furnace cleaning module.
2. Grow between 15 – 200 nm of low stress nitride (tylan18) using the bslowd program (dichlorosilane: ammonia ratio 4:1 ratio by flow rate). The actual deposition rate is slightly faster at the beginning of a run, but typically settles to about 3.5-4 nm/min after about 20 nm has been laid down. As with all LPCVD tubes, the deposition rate is higher further away from the gas source. Exact nitride thickness should be checked with the Nanospec or more accurately, with an ellipsometer.
Patterning and bulk micro-machining of the substrate (quintel, technics-c)

1. De-hydrate the wafers at 120 °C (convection oven), 20 min.

2. Prime the wafers with HMDS at 120 °C, 1 minute (primeoven cycle 0).

3. Spin Shipley S1818 photoresist onto the front side of the wafers at 4500 rpm, 30 s (spinner1).
   Bake at 90 °C (hotplate), 2 min.

4. Spin Shipley S1818 photoresist onto the back side of the wafers at 4500 rpm, 30 s (spinner1).
   Bake at 90 °C (hotplate), 5 min.

5. Using the etch mask from the meastem_2 mask series, flash the gate regions onto the sample wafers in the quintel. The optimal setting was a 7 s exposure.

6. Develop in Shipley Microposit Developer Concentrate: water (1:1) at room temperature, 60 s with gentle agitation. Rinse with water and blow the wafers dry.

7. Hard bake the photoresist at 120 °C (convection), 1 hour.

8. Repair any scratches carefully on the front and the rear with S1818 applied with a paintbrush.
   Bake at 120 °C (convection), 10 min.

9. Pre-clean technics-c with O₂ plasma (300 W, 20 min). Etch the nitride back to the silicon substrate using SF₆/He plasma (75 W, etch rate is ~50 nm/min)

10. Strip any remaining photoresist with PRS-3000 at 80 °C, 20 min (sink5). Rinse the wafers with water in spindryer3.

11. Load the wafer vertically into a Teflon cassette and etch away the silicon substrate in KOH: water (1:2 w/v) at 80 °C with constant gentle stirring. The etch rate is approximately 50-60 μm/hour, although the end point is more easily detected by actually observing the wafer (free-standing nitride membranes are light blue in colour). Periodically turn the wafer to ensure uniform etch rates up and down the wafer. Rinse with water parallel to the wafer surface.

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Definition of metal interconnects (quintel & Haller e-beam evaporator)

1. De-hydrate the wafers at 120 °C (convection oven), 20 min.

2. Spin Shipley S1818 photoresist onto the front side of the wafers at 6000 rpm, 30 s (spinner1).
   Use a chuck that holds the wafer by its edges (that is, not a vacuum chuck). Specifically, avoid using the resist coater or developer tracks or the wafer stepper automatic wafer handler as the membranes will break during the various transfer processes. Bake at 90 °C, 5 min.

3. Immerse in chlorobenzene, 5 min. Bake at 90 °C, 5 min.

4. Using the au1 mask from the meastem_2 mask series, flash the gate regions onto the sample wafers in the quintel. The optimal setting was a 7 s exposure. Use dicing tape to hold the wafer in position on the quintel sample chuck rather than the vacuum system.

5. Develop in Shipley Microposit Developer Concentrate: water (1:1) at room temperature, 60 s with careful agitation. Rinse the wafers with water and blow them dry without applying any “unequal” force across the membranes.

6. In the Haller e-beam evaporator, evaporate successively chromium (7.5 nm, 0.1 nm/s) and gold (40 nm, 0.1 nm/s for the first 10 nm and then 0.5 nm/s for the remainder) onto the wafers.

7. Liftoff in acetone. Rinse with IPA.

8. Repeat steps 1-3 in this section using the au2 mask from the meastem_2 set. This time evaporate chromium (3.5 nm) and gold (250 nm). Evaporate the gold layer slowly as excessively rapid deposition will produced stressed metal films that may buckle the underlying membrane.

9. Liftoff in acetone. Rinse with IPA.
Definition of active junction regions (jeol107 & Haller electron-beam evaporator)

1. Spin MicroChem NANO MMA(8.5)MAA (9 % in 2-ethoxyethanol) e-beam resist (Newton, MA) onto the front side of the entire wafer at 3000 rpm, 30 s (spinner1). Bake at 150 °C, 1 hour.

2. Spin MicroChem NANO 950KPMMA (2 % in chlorobenzene) e-beam resist on to the front side of the entire wafer at 6000 rpm, 30 s (spinner1). Bake at 150 °C, 1 hour.

3. Using the score marks etched into the silicon, carefully break-off strips to be written in the jeol107. This step has the highest attrition rate for the membranes as it is quite difficult to remove individual sections from the rest of the wafer.

4. Using the temXXnYY NPGS run files, expose each die in the jeol107 (accelerating voltage 20 kV, beam current 5 pA). Note that when performing e-beam lithography over a membrane, the absence of the substrate means that a considerably higher dose is required for full exposure (for a given pattern/accelerating voltage). Thus doses up to 1500 μC/cm² for the finest features and 300 μC/cm² for the interconnects were often used. It is also difficult to focus precisely on the substrate unless focus marks are already in place (either scratched on or features made by photolithography).

5. Develop in MIBK: IPA (30:70), 30 s with agitation and MIBK: IPA (20:80), 15 s.

6. Load the strip onto the centreline of the angle evaporation stage (equipped with ±15° stops) for the Haller e-beam evaporator. Evaporate successively at +15° Cr (3.5 nm, 0.1 nm/s) and Au (10 nm, 0.1 nm/s), at -15° Cr (3.5 nm, 0.1 nm/s) and Au (10 nm, 0.1 nm/s) and horizontally Cr (3.5 nm, 0.1 nm/s) and Au (0.1 nm/s for the first 10 nm and then 0.5-1 nm/s for the remainder).

7. Liftoff in acetone. Rinse with IPA.

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