Title
Fluxless Bonding Processes Using Silver-Indium System for High Temperature Electronics and Silver Flip-Chip Interconnect Technology

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Publication Date
2015

Peer reviewed|Thesis/dissertation
DEDICATION

To

my dear family

Whose affections, unconditional love and encouragement
make it possible for me to complete this work,

I love you.
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ACKNOWLEDGMENTS

Over the past four years I have received support and encouragement from a great number of individuals. I am deeply indebted to my advisor, Professor Chin. C. Lee, for his fundamental role in my doctoral work. Prof. Lee provided me with every bit of guidance, assistance, and expertise that I needed during my study. In addition, I would also like to thank him for his nominations for numerous fellowships and the generous financial support from his research grants. Without his guidance and persistent help my Ph.D. program and this dissertation would not have been possible.

Besides my advisor, I would like to thank the rest of my committee members: Professor G. P. Li, Professor James Earthman, and Professor Mark Bachman, for their encouragement, insightful comments, and hard questions on my research. I also want to thank Professor Farghalli A. Mohamed for his support on my experiment and II-VI Foundation for their financial support granted, during my Ph.D. study.

My colleagues, Dr. Chu-Hsuan Sha, Dr. Wen-Pei Lin, Shou-Jen Hsu, Yi-Ling Chen, and Dr. Ming-Je Sung, have all extended their support in a very special way, and I gained a lot from them, through their personal and scholarly interactions, their suggestions at various points of my research program. I also want to thank all of the INRF staffs for their assistance.

My time at UC Irvine was made enjoyable in large part due to the many friends that became a part of my life. I would like to thank my roommate, Paula Hao, for all the great times that we have shared. They were always supporting me and encouraging me with their best wishes.
Lastly, I cannot finish without thanking my family. I warmly thank and appreciate my parents for their material and spiritual support in all aspects of my life. I also would like to thank my brother, sister and brother-in-law, for they have provided assistance in numerous ways. I want to express my gratitude and deepest appreciation to my older sister, Yuan-Hsuan Wu, for her great patience, teaching and suggesting in my Ph.D. life. Without her, I would not be here to complete my Ph.D. program. In my heart, my family always occupies an important part. This dissertation would not have been possible without their love, support, and encouragement I received from my parents, my family.
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• Journal Paper


• Conference Proceedings and Presentations


ABSTRACT OF THE DISSERTATION

Fluxless Bonding Processes Using Silver-Indium System for High Temperature Electronics and Silver Flip-Chip Interconnect Technology

By

Yuan-Yun Wu

Doctor of Philosophy in Engineering
University of California, Irvine, 2015
Professor Chin C. Lee, Chair

In this dissertation, fluxless silver (Ag)-indium (In) binary system bonding and Ag solid-state bonding are used between different bonded pairs which have large thermal expansion coefficient (CTE) mismatch and flip-chip interconnect bonding application. In contrast to the conventional soldering process, fluxless bonding technique eliminates contamination and reliability problems caused by flux to fabricate high quality joints. Due to large CTE mismatch, high quality joints are important to manage the shear strain which develops in the bonded objects. Besides, the resulting Ag and Ag-In joints have relative high melting and operating temperature which can be utilized in high temperature packages. There are two section are reported. In the first section, the reactions of Ag-In binary system are presented. In the second section, the high melting temperature, thermal and electrical conductivity joint materials bonding by either Ag-In binary system bonding or solid-state bonding processes for different bonded pairs and flip-chip application are designed, developed, and reported.
Our group have studied Ag-In system for several years and developed the bonding processes successfully. However, the detailed reactions of Ag and In were seldom studied. To design a proper bonding structure, it is necessary to understand the reaction between Ag and In. The systematic experiments were performed to investigate these reactions. A 40 µm Ag layer was electroplated on copper (Cu) substrates, followed by indium layers of 1, 3, 5, 10, and 15 µm, respectively. The samples were annealed at 180 °C in 0.1 torr vacuum. For samples with In thickness less than 5 µm, the joint compositions are Ag$_2$In only (1 µm) or AgIn$_2$, Ag$_2$In, and Ag solid solution (Ag) after annealing. No indium is identified. For 10 and 15 µm thick In samples, In covers almost over the entire sample surface after annealing. Later, an Ag layer was annealed at 450 °C for 3 hours to grow Ag grains, followed by plating 10 µm In and annealing at 180 °C. By annealing Ag before plating In, more In is kept in the structure during annealing at 180 °C. Based on above results, for those designs with In thinner than 5 µm, the Ag layer needs to be annealed, prior to In plating in order to make a successful bonding.

In this section, we further studied the Ag-In bonding and solid-state bonding for different bonded pairs and flip-chip application. For the silicon (Si) and aluminum (Al) pair, Al has been used as the material for interconnect pads on the ICs. However, its high CTE ($23 \times 10^{-6}/°C$) and non-solderable property limit its applications in electronic products. To overcome these problems, a fluxless Ag-In bonding was developed. Al was deposited Cr/Cu layer on the surface by E-beam evaporator to make it solderable. 15 µm of Ag and 8 µm of In were sequentially plated on the Al substrates and 15 µm of Ag was on Si chips with Cr/Au coating layer. The bonding was performed at 180 °C in 0.1 torr vacuum. The joint consists of Ag/(Ag)/Ag$_2$In/(Ag)/Ag. The joint can achieve a solidus temperature of beyond 600 °C. From shear test results, the shear strengths far exceed the requirement in MIL-STD-883H. Al is not
considered as a favorable substrate material because it is not solderable and has a high CTE. The new method presented in this thesis seems to have surmounted these two challenges.

Since Ag\textsubscript{2}In is weak inside the joint in Ag-In system, an annealed process was used to convert the joints into Ag solid solution (Ag) to increase the joint strength and ductility. Two copper (Cu) substrates were bonded at 180 °C without flux. Bonding samples were annealed at 200 °C for 1,000 hours (first design) and at 250 °C for 350 hours (second design), respectively. Scanning electron microscope with energy dispersive X-ray (EDX) analysis results indicate that the joint of the first design is an alloy of mostly (Ag) with micron-size Ag\textsubscript{2}In and (ζ) regions, and that of second design has converted to a single (Ag) phase. Shear test results show that the breaking forces far exceed the requirement in MIL-STD-883H. The joint solidus temperatures are 600 °C and 800 °C for the first and second designs, respectively. The research results have shown that high-strength and high temperature joints can be manufactured using fluxless low temperature processes with the Ag-In system and are valuable in developing high temperature package.

For real applications, a serious concern is the long-term reliability of the joints under thermal stress caused by CTE mismatch between the chip and the package. Thereby, the reliability of Ag-In joints in thermal cycling (TC) environment is assessed. Si chips and Cu substrates were bonded at 180 °C without flux, and then annealed at 250 °C to convert the joint into an alloy of intermetallic grains and (Ag). Si-Cu pair is chosen because of the large CTE mismatch. Two TC tests were performed. 10 samples were examined from -40 °C to 85 °C for 100 cycles first and -40 °C to 200 °C for 5,000 cycles later. Seven of ten samples survived beyond 5,000 cycles. Based upon these results, the Ag-In joints not only have high melting temperature but also can survive harsh TC environment.
To further investigate other alternative bonding method, the solid-state atomic bonding technique is introduced. High quality joints are crucial to bonding materials with CTE mismatch since shear stress develops in the bonded pair. Since stress concentrated at the voids in these joint, the breakage probability could increase. In addition, intermetallic compound (IMC) formation between the solder and under bump metallurgy (UBM) is essential for interconnect joint formation in the conventional soldering process. However, the interface between the IMC and solder is shown to be the weakest interface that tends to break first during thermal cycling and drop tests. Thus, we developed a solid-state bonding process along with ductile joint materials that no molten phase was included. Thus, the IMC and its related issues are eliminated.

In the first bonding experiment, 10 µm Ag layer with cavities were produced on the Si chips with Cr/Au coating layer and then bonded to the Cu substrates at 300 °C with 1,000 psi (6.9 MPa) static pressure in vacuum. Due to cavities, the bonding pressure can be reduced to 600 psi (4.1 MPa). No underfill or flux is needed. From cross-section SEM images, Ag joints are well bonded between Si chips and Cu substrates. The shear test results show that bonding strengths pass the MIL-STD-883H, except one sample. It eliminates a concern from the bonding strength for practical applications.

Due to the miniaturization of large-scale-integration of circuits on Si chip technology, the joint size and the pitch of the flip-chip joints have to be scaled down. As the joint shrinks, reliability issues and manufacturing difficulties emerge. One of these difficulties is elevated shear strain due to the increase of the intermetallic compound (IMC) layer ratio. Therefore, we demonstrated the Ag flip-chip interconnect process using solid-state bonding at 250 °C with a static pressure 800 psi in vacuum. Each Si chip has an array of 50 × 50 × 13 Ag flip-chip joints with 20 µm in pitch and 10 µm joint in diameter on Si chip. No flux or underfill is needed. The
cross-section SEM image shows that the Ag flip-chip joints were well bonded to the Cu substrate without cracks. Despite a large CTE mismatch between Si and Cu, no joint breakage is observed. The ductile Ag joint well manage the stress induced by significant CTE mismatch. The melting temperature of joints is 962 °C. Thus, high operating temperature device such as 200-450 °C becomes possible. To further evaluate this, a pull-off-test was performed. The breaking force was 1.5 times larger than the MIL-STD-883H criterion. There are several advantages to this solid-state Ag flip-chip bonding technology: high electrical and thermal conductivities, no IMCs and their related issues, a complete lack of flux, high ductility for managing CTE mismatch between chips and packages, high operating temperature, and possibility for a high aspect ratio of the interconnect.

To figure out the stress-strain of Ag and (Ag) at room temperature and elevated temperature, a typical ingot with 9.5 mm in diameter and 60 mm in length was fabricated. The main ingots were machined into ASTM tensile test samples by EDM. The stress-strain curves of Ag were measured at room temperature, at 221 °C (T_h = 0.4), and at 350 °C (T_h = 0.5), respectively, where T_h is the homologous temperature. For Ag ingot, at room temperature, the yield strength (YS) ranges from 51 to 106 MPa and ultimate tensile strength (UTS) is from 138 to 208 MPa which are comparable with the published data but the elongation (0.27 - 0.49) is about twice of the published value. At higher temperatures, the YS and UTS decrease but elongation varies little. Silver solid solution with 20 at. % In ((Ag)-In20) samples were also measured at room temperature, at 156 °C (T_h = 0.4), and at 265 °C (T_h = 0.5), respectively. (Ag)-In20 test samples have better results than pure Ag test sample. The YS is 14 MPa which is smaller than pure Ag test sample but UTS (308 MPa) and elongation (0.73) are 1.5 times of pure Ag sample.
Chapter 1

Introduction

1.1 High Temperature Electronics

High temperature electronics (HTEs) have been used in many applications recently, such as under the hood for exhaust gas sensors, oil and gas exploration and production (down hole temperatures to 325 °C) combustion engines in automobile and in exposed areas of an aircraft (150 °C to 350 °C). Even HTEs are used for space exploration (the surface of Venus is 485 °C) [1-4]. Besides, recent advances in semiconductor technology have greatly increased the operating temperature of semiconductor devices which high temperature device chips built on SiC and GaN-based semiconductors have demonstrated operating temperatures higher than 350 °C. For example, the operating temperature of SiC power devices can be 465 °C or higher [5-8].

Due to these existing needs, demand of HTEs is growing quickly. Therefore, before introducing the packaging of high temperature electronics, we have to have a clear definition of high temperature electronics in general. Fig. 1.1 portrays a simple device. It shows where junction, case, and ambient temperatures are. The question is that what temperature determines the device is in high temperature. The simplest choice is case or ambient temperature because these temperatures can be measured and specified. Consequently, high temperature electronics may be defined as those devices and/or subsystems that operate at elevated temperatures above 200 °C [9]. The advantage of HTEs is not only used in high temperature environment but to reduce the space and materials of cooling system. In other words, the overall cost will be reduced
too. However, here comes a challenge: a method to assembly theses chips and devices on packages where die-attachment can survive in high temperature environment.

![Diagram of junction temperature Tj, ambient temperature Ta, and case temperature Tc.]

Figure 1.1 A simple device structure.

### 1.2 Die-Attachments in Electronic Packaging

Table 1.1 displays the popular die-attach materials in electronic packaging and their melting and operating temperatures which are calculated by homologous temperature of 80% [10]. Based on section 1.1, the high temperature devices are operated and used in relative high temperature environments which are over 200 °C in general. From the table 1.1, silver filled epoxies, lead-tin eutectic solder, lead free solder and Au-tin eutectic solder have operating temperature just over 170 °C. Even in the case of high lead lead-tin solder, the operating temperature is only 185 °C. Other two Au-based solders can have relative high operating temperatures; nevertheless, the cost is high due to high percentage of Au. In fact, these device chips cannot be put to high temperature use unless high temperature die-attach materials are available, except sintered nano-silver pastes [11-15]. In the sintering process, high pressure such as 5 MPa or higher is required to consolidate the sintered Ag and reduce pores [16-17]. Research
is being pursued to reduce the sintering pressure and temperature needed. Therefore, we want to find out alternative materials which have a high melting and operating temperature.

**Table 1.1** The popular die attachment materials with melting and operating temperatures.

<table>
<thead>
<tr>
<th>Die-attach material</th>
<th>Melting temperature °C</th>
<th>* Operating temperature °C</th>
</tr>
</thead>
<tbody>
<tr>
<td>Silver filled epoxies</td>
<td>**100</td>
<td>75?</td>
</tr>
<tr>
<td>Lead-tin eutectic solder Sn63Pb37</td>
<td>183</td>
<td>92</td>
</tr>
<tr>
<td>Lead free solder Sn96.5Ag3Cu0.5</td>
<td>217</td>
<td>119</td>
</tr>
<tr>
<td>Au-tin eutectic solder Au80Sn20</td>
<td>280</td>
<td>170</td>
</tr>
<tr>
<td>High lead lead-tin solder</td>
<td>300</td>
<td>185</td>
</tr>
<tr>
<td>Au88Ge12</td>
<td>356</td>
<td>230</td>
</tr>
<tr>
<td>Au97Si3</td>
<td>363</td>
<td>236</td>
</tr>
<tr>
<td>Sintered nano-silver pastes</td>
<td>961</td>
<td>715</td>
</tr>
</tbody>
</table>

* **80% homologues temperature**  
  ** Softening temperature

**1.3 Challenges of High Temperature Die-Attachments**

In conventional thinking, for high temperature die-attach materials, if the melting temperature is 700 °C, the process temperature should be higher than 700 °C in order to form molten phase. This process temperature will damage nearly all electronics devices. Hence, the high temperature die-attachments need to work in low temperature process. Another concern of high temperature die-attachments is the coefficient of thermal expansion (CTE) between chips and substrates, for examples, Si chips and Cu substrates. This pair creates large CTE mismatch and results in shear strain during cooling process. A suitable die-attachment needs to survive under different chip and substrate pairs.
To surmount these challenges, we looked into high temperature die-attachments which have high melting temperature and can be bonded in low temperature and bonding pressure, i.e. silver (Ag) and indium (In). One problem of Ag-In binary system is that In gets oxidized easily. It requires using flux to remove the oxide formed during the bonding process to achieve good quality joints. However, flux residue may seriously affect the reliability and performance of the surface mount during bonding process [18]. Ultimately, a fluxless bonding process is required.

1.4 The Fluxless Techniques

Typically, in soldering/bonding process, the solder/ die-attach materials melt and chemical react with the substrates forming intermetallic compound (IMC) layer to achieve the joints. However, solder/ die-attachments and substrate metals have a native oxide layer on the surface. These oxide layer usually have high melting temperature, for example, the melting temperatures of SnO, SnO$_2$ and In$_2$O$_3$ are 1,080 °C, 1,630 °C and 1,910 °C, respectively. These temperatures are much higher than soldering/bonding temperature. The oxide layer blocks the interaction between the molten phase of materials and substrates and inhibits the formation of joints. Hence, a flux process is applied to remove the oxide layer. The flux composed of resin acids mainly can react with the metal oxides, such as CuO and SnO, and convert oxide layer into salts and water. However, during fluxing process, residues are accompanied, resulting in voids and uneven joint thickness. The performance of the device degrades due to these defects [19-20]. Thus, the fluxless process becomes very important in the electronic packaging process.

There are many methods to achieve fluxless bonding. The first one is using acid vapor, acetic or formic acid to reduce metal oxide [21-23]. This method is similar to the conventional soldering process, except that vapor chemicals rather than liquid chemicals are used.
However, the acid vapor is corrosive to devices. Another method is treating the solder by fluorine (F) in order to convert SnO or SnO₂ into tin oxyfluoride which can be dissolved in molten solder, where no flux is necessary.

Other than these methods, our group has developed a fluxless technique by providing an oxidation-free environment from the solder manufacture to joint formation [24-26]. The oxidation is prevented during entire bonding process. There are four requirements to prevent the oxidation.

1. Solder/ die-attach materials should be fabricated in an oxidation-free environment, such as deposition or electroplating in a vacuum. 2. There should be a thin capping layer on the solder/ die-attach materials to protect the inner solder/ die-attach materials from oxidation. 3. This thin capping layer should be able to dissolve and become one part of joints. 4. To inhibit oxidation, the bonding process should be performed in a vacuum, an inert gas environment, or H₂ environment. Our oxidation free fluxless soldering technique was first invented and reported in 1995 [27], and the idea has been applied to develop various fluxless processes based on Sn-Au, Sn-Cu, Sn-Bi, Sn-In, In-Au, In-Cu, In-Ag binary systems and In-Pb-Au ternary system [25-31].

The purpose of this dissertation is to produce IMC free joint between semiconductor die and common used substrate. We first work on Ag-In binary system. The advantage of Ag-In binary system is that the processing temperature can be as low as 180 °C. After the bonding, the joint consists of Ag₂In and Ag solid solution (Ag). The IMC containing joints can be converted to Ag-rich solid solution single phase joints after proper annealing. The shear test and reliability test are provided to examine the strength of Ag-In joints with different compositions. We later develop solid state bonding technique using pure Ag. The bonding can be achieved at 250 to 300 °C with a static pressure 600 psi (4.1 MPa) to 1,000 psi (6.9 MPa). The dissertation outline is
presented in next section.

1.5 Dissertation Outline

In this dissertation both Ag-In binary system bonding and solid state atomic bonding techniques are employed to meet different bonding pairs. The material depositions, materials fabrication process, bonding furnace setup, bonding process flow, and characterization analysis are reported in Chapter 2. In order to understand the reaction of Ag-In binary system during bonding process, the chemical reaction of Ag-In binary system at 180 °C which is bonding temperature is studied to identify the materials and provide the guideline of the thickness of Ag and In in bonding application. In Chapter 4, a Ag-In fluxless bonding process was developed to bond Si chips to aluminum (Al) substrates at 180 °C for high temperature applications. The bonding temperature is 80 °C below the typically reflow temperature of tin-based lead-free solders. The joint between Si and aluminum consists of five regions: Ag, (Ag), Ag$_2$In, (Ag), and Ag. (Ag) is Ag solid solution. This joint is complete, uniform, and has a solidus temperature higher than 600 °C. The success of this bonding process development proves Ag-In joint can manage large CTE mismatch between Si chip and Al substrate even there is IMC (Ag$_2$In) inside the joint.

In order to understand the strength of Ag-In joints, annealing process is applied to examine the bonding samples at 200 °C for 1,000 hours and 250 °C for 350 hours, respectively. After annealing, shear test is provided to get real strength data. All test samples pass the MIL-STD-883 H. Even the breaking force is higher than 200 kg, in fact the joint didn’t break during test. In addition, to find out the reliability of Ag-In joints whose joint compositions are an alloy of small intermetallic grains and (Ag), thermal cycling (TC) test is assessed. Two TC tests were
performed. First one is between -40 °C to 85 °C for 100 cycles. Another one is between -40 °C to 200 °C for 5,000 cycles. Seven of ten samples pass the TC test. That means Ag-In joints not only have high melting temperature but also survive harsh environment. The detail experimental design and results are reported in Chapter 5 and 6.

In Chapter 7, pattern Ag joint with 100 µm diameter cavities is made between Si chips and Cu substrates using solid state bonding at 300 °C with different bonding pressure. Neither flux nor underfill is involved. Due to cavities, the bonding pressure can be reduced from 1,000 psi (6.9 MPa) to 600 psi (4.1 MPa). Cross section SEM images of joints show that the pattern Ag joints were bonded to the Cu substrate without gaps or breakage. The shear test result shows that all samples pass the MIL-STD 883H, except one sample which was not well bonded.

In Chapter 8, we further demonstrated 10 µm Ag flip-chip interconnect joints between Si chips and Cu substrates using solid state atomic bonding at 250 °C with a static pressure of 800 psi (5.5 MPa) for 5 minutes in 0.1 torr vacuum. In experiments, an array of 50 × 50 × 13 Ag columns that had 10 µm diameter, 20 µm pitch and 10 µm height was fabricated in one chip region of Si wafers that were first metalized with Cr/Au. The corresponding load for each column was 0.044 gm. Cross section SEM images of one row of joints show that the Ag flip-chip joints were bonded to the Cu substrate without gaps or breakage. Despite significant coefficient of thermal expansion (CTE) mismatch between Si and Cu, the Si chips did not break from Cu. There are several advantages compared to the popular Sn based Pb-free flip-chip technology. They are high thermal conductivities, elimination of IMCs and its related issues, no flux issue, high ductility for managing CTE mismatch between chips and packages, high operation temperature, and the possibility for high aspect ratio interconnect.
Our group has developed several Ag-In fluxless bonding techniques; however, further experiments must be conducted to describe the mechanical properties in stress vs. strain. Nevertheless, as described in Chapter 9, we developed the growing process of pure silver and Ag solid solution ingots and performed tensile testing to examine the stress vs. strain at room temperature and elevated temperatures. The bulk of the ingots were machined to the ASTM tensile test (TT) samples using electrical discharge machining (EDM). The TT samples were tested at three temperatures: room temperature, $T_h = 0.4$ and $T_h = 0.5$, respectively, with a strain rate of $10^{-4}$ mm/s. Based on the tensile test results, the (Ag) has higher ultimate tensile strength and elongation than pure Ag. It is about 1.5 times of pure Ag sample.

In Chapter 10, a summary is given to conclude the critical findings in this dissertation.
Reference Chapter 1


Chapter 2

Experimental Setup and Techniques

2.1 Thin Film Deposition

In all experiments, there are two different deposition processes which are used to structure the multilayer metal films on different chips and substrates. First one is vacuum metal evaporation and the other one is electroplating. There are both advantages and disadvantage for these two methods. The vacuum metal evaporation provides excellent uniformity, cleanness and precise thickness control of films. On the other hand, it is costly and has lower deposition rate. For electroplating technique, it has higher deposition rate, is less expensive and can be done in the atmosphere. In the following sections, the vacuum metal evaporation and electroplating processes are presented.

2.1.1 Electron Beam Vacuum Evaporation

Electron beam (E-beam) vacuum evaporation is one of physical vapor deposition (PVD). In general, E-beam vacuum evaporation processes are commonly used in semiconductor industry to grow metallic films. In this deposition method, a target anode is bombarded with an electron beam given off by a charged tungsten filament under high vacuum environment. The electron beam provides energy for the target, and causes atoms from the target to transform into a gaseous phase. In high vacuum environment, these gaseous particles can travel directly to the object to be plated without colliding with the background gas. These atoms then deposit on the object and vacuum chamber to form a metallic film. The equipment used in this research for E-beam
vacuum deposition is the Temescal CHA-600S/CV-8 thermal evaporator which is a four-pocket e-beam evaporator. This system is equipped with a mechanical pump and a cryo pump that can evacuate the chamber down to $2 \times 10^{-6}$ torr range in two hours. This system allows deposition of up to four different materials in one vacuum cycle. The thickness crystal monitor is assembled inside the chamber and the metal deposition thickness is measured in real-time.

### 2.1.2 Electroplating

Electroplating is a process of thin film deposition on a conductive substrate in an electrolytic bath composed of a solution of the salt of the plating metal. The oxidation and reduction reaction are involved in electroplating process to complete thin film deposition. The oxidation reaction provides the source of the metallic ions; the reduction reaction is the plating of the metal on the desired object. The electroplating is driven by external DC power. The metal target is connected to the anode side which is the positive post of DC power, and it is required to supply the ions removed from solution. The plating object must be connected to the negative post of the DC power. This will cause the object to gain a negative charge and attracts the positive metal ions from the solution. Reduction will occur on the surface of the cathode side. Therefore, a thin film is plated on the object. In this thesis, several materials were deposited by electroplating process, such as Ag and In. In the process, the plating current, power voltage, temperature, PH level of plating solution, and the deposition rate are all monitored and controlled in order to create uniform thin films.

### 2.2 Material Fabrication
In this thesis, the fabrication of the Si Ag joints/flip-chip interconnects includes wafer cleaning, metallization, photolithography and electroplating processes, which is illustrated in Fig. 2.1.

2.2.1 Wafer Cleaning and Metallization

**Figure 2.1** A fabrication process flow of Si joints/flip-chip interconnects using photolithography, electroplating and bonding process.
Si wafers are chemically cleaned by RCA-1 cleaner, which is composed of ammonium hydroxide (NH$_4$OH) and hydrogen peroxide (H$_2$O$_2$), at 70 ± 5 ºC in order to remove any organic residue, ionic, films and metallic impurities from the Si surface. During the cleaning process, RCA-1 oxidizes the Si and leaves a thin oxide layer on the surface of the wafer, which should be removed if a pure Si surface is desired [1]. Si wafers are later soaked in diluted hydrogen fluoride (2 % HF) to remove this oxidation layer, revealing pure Si surface so that the metallization process could be performed. Prior to metallization, Si wafers undergo a dehydration process at 120 ºC. The Si metallization layers, Cr followed by Au, are deposited in E-beam vacuum evaporator under 7×10$^{-7}$ torr. The metallization layer, Cr, is the adhesion layer and the following Au layer protects Cr from oxidation and also serves as seed layer for electroplating.

2.2.2 Photolithography Process

After the wafer cleaning and metallization processes, wafers are then patterned using photolithography process. Two different types of joints are created; one is Ag layer with 100µm cavities and the other is flip-chip interconnects in 10µm diameter. All patterns are generated by positive photoresist, AZ P4620®. In general, for a positive photoresist, it is exposed with a uniform ultraviolet (UV) light to change the chemical structure of the photoresist so that it becomes more soluble in the developer. Therefore, after UV exposure, the exposed photoresist is washed away by the developer and the pattern is revealed. In our experiments, AZ P4620® are spun on 2” Si wafers followed by performing soft baking (pre-baking), which is applied to remove some of the photoresist solvent and densify the photoresist. Then, the pattern is defined after going through UV exposure with mask, the developing process, and hard baking. Hard
baking is used to drive off the remaining solvent from the photoresist and improve adhesion of the photoresist to the wafer surface. Photoresist becomes more durable for future electroplating. After hard baking process, O\textsubscript{2} plasma cleaning is applied to remove the photoresist residue on the Si surface.

2.2.3 Metal Deposition

After the O\textsubscript{2} plasma cleaning process, the joints/flip-chip interconnect materials, Ag and Ag-In are deposited utilizing electroplating process. Ag and In are electroplated at room temperature. The Ag plating bath is a mild alkaline plating solution at pH of 10.5 containing potassium hydroxide (KOH) and silver oxide (Ag\textsubscript{2}O). The In plating solution is indium sulfaminate bath at pH 1 to 3.5. During these electroplating processes, the plating current, power voltage, temperature, pH level of plating solution, and the deposition rate are all monitored in order to create uniform thin films.

Later, the photoresists are removed by the corresponding strippers, leaving Ag layer with cavities or flip-chip interconnects array on the Si wafers. During the photoresist removal process, the photoresist strippers chemically change the photoresists so that it can be removed easily from the substrate. Lastly, the Si chip with joints/flip-chip interconnects are bonded to the substrate using a fluxless Ag-In bonding or solid-state bonding process, respectively. In what follows, we reported the vacuum furnace and bonding setup.

2.3 Vacuum Furnace and Bonding Setup

Fig. 2.2 depicts the illustration of vacuum furnace built in house [2]. In this dissertation, all of bonding processes are done in this vacuum furnace. The vacuum furnace consists of a
quartz cylinder, two stainless steel plates, a heating platform, and a ceramic post. The quartz cylinder, having an inner diameter of 130 mm and a height of 200 mm, is sandwiched between two steel plates to construct a vacuum chamber. The interference between the cylinder and steel plate is sealed by an O-ring. It is easy to observe the sample during the reflow process because of the transparency of the quartz. The graphite platform, having a size of $75 \times 75 \times 10 \text{ mm}^3$, is drilled with many holes to allow the heating wire (Nickel-Chromium alloy) to go through the body of the platform. In Fig. 2.3, the wire is electrically insulated from the graphite using ceramic tubes and beads. Graphite was chosen as the material of the platform because it has been experimentally proven that it absorbs 97% of radiation and is a nearly perfect emitter of radiation [3]. Therefore, the platform will absorb a large amount of heat given off by the wires. It is also easy to machine and can withstand a very high temperature. The temperature is monitored by two type-K thermocouples (Chromel+ Alumel-) at two locations, the top surface of the sample and sidewall of the platform. Inside the vacuum furnace, a graphite platform is supported by a ceramic poster standing at the center of the base stainless steel plate.
In order to achieve thermal isolation from the upper and base plates, a ceramic poster having relatively low thermal conductivity is utilized to support the platform. The ceramic beads have the same function for heating wire. Once the chamber is in vacuum environment, heat is transferred to the upper and base plates from the platform through radiation. Because the plates are constructed of stainless steel, they are able to reflect and scatter radiation. The plates will not absorb much heat radiation and keep cooled to low temperature through natural convection by ambient air. It is designed so that the platform is well thermally isolated from the chamber enclosure that included the cylinder wall and two steel plates. This is a unique feature of the furnace design. It allows for the platform to be heated to high temperatures while the temperature of the rest of the chamber remains relatively low. It is very important to allow the chamber to be sealed in vacuum using O-ring. The upper plate is mounted with an ultra-torr connector to take
and hold the small K-type thermocouple probe for measuring the sample temperature. The base plate contains four ports with National Pipe Thread (NPT). Two of these are occupied by feedthroughs. One feedthrough is for a pair of copper wires to pass into the chamber to connect to the two ends of the heating wire. The other feedthrough is for thermocouple wires. Other two ports are used for the vacuum gauge and connecting to a mechanical pump. In this design, the chamber is allowed to pump down to 50 millitorrs and the maximum temperature of the platform is allowed to reach up to 450 ºC.

For the bonding process in the vacuum chamber, the samples electroplated with solder layers are mounted in a graphite fixture and applied with a static pressure to ensure intimate contact. The assembly is then placed on the graphite platform. Once the vacuum furnace is
pumped down and kept at 50 to 100 millitorrs to suppress oxidation during reflow/bonding, the temperature controller is turned on to heat up the platform. The reflow or bonding process is carried out at wide ranges of temperatures and dwell times for different bonding systems. After reaching the peak temperature, the heater is turned off and the assembly is allowed to cool down naturally to room temperature in a vacuum environment. Comparing to bonding in air, the amount of oxygen available to oxidize the molten solder was reduced by a factor of 15,200 in 50 millitorrs of vacuum.

2.4 Characterization Techniques

2.4.1 Scanning Electron Microscope/ Energy Dispersive X-ray Spectroscopy

The scanning electron microscope (SEM) uses a focused beam of high-energy electrons to generate a variety of signals at the surface of solid specimens. The signals that derive from the interactions between electrons and atoms that make up the sample include secondary electrons (SE), backscattered electrons (BSE), diffracted backscattered electrons (EBSD), characteristic X-rays, visible light (cathodoluminescence–CL), specimen current, and transmitted electrons. They reveal information about the sample including external topography (texture), chemical composition, crystalline structure and orientation of materials making up the sample. Fig. 2.4 displays the interaction volume and all of the signals produced by the interaction between electron beam and specimens [4]. Secondary electrons and backscattered electrons are commonly used for imaging samples. Secondary electrons are most valuable for showing high-resolution morphologies and topographies on samples. Due to the very narrow electron beam, SEM micrographs have a large depth of field, yielding a three-dimensional surface image of a specimen. Backscattered electrons are most valuable for illustrating contrasts in composition in
multiphase samples. For instance, a stronger BSE intensity is detected if a larger number of backscattered electrons reaching to a BSE detector. Larger atoms, with a greater Z-number, have a higher probability of producing elastic collisions due to their larger cross-sectional area. Thus, elements with a greater atomic number (Z) show brighter images than smaller atomic number in BSE images. The SE and BSE detectors are installed in the SEM to capture the images.

Figure 2.4 The interaction volume and all of the signals produced by the interaction between the electron beam and specimen.

X-ray generation is produced by inelastic collisions of the incident electrons with electrons in discrete orbitals (shells) of atoms in the sample. When the excited electrons return to the low energy states, it generates X-rays with fixed wavelength. An energy-dispersive detector is used to separate the characteristic x-rays of different elements into an energy spectrum. In addition, an EDX software system is used to analyze the energy spectrum for determining the specific elements in the specimen. Energy dispersive X-ray spectroscopy can be used to find the
chemical composition of materials in a small area (~10^6 mm^2), and can create element composition maps over this area. The spot size, defined as the diameter of the electron beam, depends on the density and atomic number of the interested elements and accelerating voltage. Typically, the higher accelerating voltage, the smaller is spot size. The smaller spot size image is sharper but also grainier in appearance due to the lower signal to noise ratios associated with a lower beam current. The larger spot size results in a less sharp but smoother image in appearance [5]. Moreover, the image has high resolution in high accelerating voltage, but the surface structure is unclear. On the other hand, in low accelerating voltage, the image is low resolution but clear surface structure [6].

2.4.2 X-Ray Diffraction

X-Ray Diffraction (XRD) is a laboratory-based technique commonly used for identification of the crystalline phases present in materials and the structural properties, such as lattice parameters, strain, average grain size, epitaxy, phase composition, preferred orientation, order-disorder transformation, thermal expansion, crystallinity, and crystal defect, of multilayer films. X-ray diffraction peaks are produced by constructive interference of a monochromatic beam of x-rays scattered at specific angles from each lattice plane in a sample. X-rays are generated in an cathode ray tube, in which a target material, such as Cu, Fe, Mo, or Cr, is excited using an electron beam, causing inner shell electrons to be ejected and replaced by electrons from higher energy outer orbitals. This interaction produces X-rays that are characteristic of the target material, which are then filtered and concentrated into a monochromatic incident beam of X-rays that is focused on the sample. The anode is a water-cooled block of Cu containing desired target metal. Diffraction occurs only when Bragg’s Law, nλ = 2dsinθ, is satisfied condition for
constructive interference from the interactions between the incident X-ray and lattice planes with spacing d, where \( \lambda \) is the wavelength of electromagnetic radiation, d is the lattice spacing in the crystalline sample, and \( \theta \) is the diffraction angle. The atoms should be arranged in a periodic array in a crystal and thus can diffract light. The diffraction peak intensities are determined by the arrangement of atoms in the entire crystal. These diffracted X-rays are then detected, processed and counted. Therefore, the x-ray diffraction pattern is the fingerprint of periodic atomic arrangements of a sample. By scanning the sample through a range of 20 angles, all possible diffraction directions of the lattice can be attained. In this study, it was applied to different materials and their results are presented as a plot of diffraction intensity corresponding to diffraction angles (20 degree). Finally, to obtain these results, Rigaku SmartLab XRD is used for X-ray diffraction analysis.

2.4.3 Dektak 3 Surface Profilometer

The Dektak 3 Surface Profilometer is an instrument to measure the vertical profile of samples (step height), thin film thickness, and other topographical features, such as film roughness or wafer bowing. Fig. 2.5 shows the Dektak 3 Surface Profilometer used in the experiments.
A diamond stylus is moved vertically into contact with the sample and then moved laterally across the sample for a specified distance and specified contact force. The instrument can measure small surface variations in vertical stylus displacement as a function of position. It can measure small vertical features ranging in height from 100 Å to 650,000 Å (6.5 µm) with a vertical resolution of ~ 5 Å on a 5” diameter sample stage. The height position of the diamond stylus generates an analog signal which is converted into a digital signal stored, analyzed and displayed [7]. The radius of diamond stylus is 12.5 µm, and the horizontal resolution is controlled by the scan speed and scan length. There is a horizontal broadening factor which is a function of stylus radius and of step height. This broadening factor is added to the horizontal dimensions of the steps. The stylus tracking force is factory-set to 50 milligrams.
Reference Chapter 2


Chapter 3

A Study of Chemical Reactions of Silver and Indium at 180 °C

3.1 Introduction

At present, popular solders used in electronic industries are tin-based lead-free solders [1]. An example is tin-3.5 % silver (Sn-3.5Ag) alloy that melts at 221 °C [2]. Typical reflow temperature of lead-free solders is 260 °C. There are many industrial applications where lower bonding temperature is needed. Our group has looked into the silver-indium (Ag-In) binary system which has a eutectic temperature of 144 °C [3]. In this system, only the indium-rich alloys, i.e., with low Ag composition, have been adapted in production by electronic industries. Ag-rich alloys, i.e., with high Ag composition, had seldom been attempted for bonding applications. Over the past many years, several fluxless bonding processes have been developed for which the resulting joints are Ag-rich alloys having solidus temperature higher than 695 °C [4-8]. A typical bonding temperature is 180 °C, above the horizontal isotherm of 166 °C. Since Ag and In react to form AgIn$_2$ compound even at room temperature [9-11], the chemical reactions during bonding at 180 °C are not well understood.

In this research, we investigated these chemical reactions and intermetallic compound (IMC) formation with systematic experiments. Since all our bonding processes based on Ag-In system were performed at 180 °C, the reactions were investigated at this temperature. Understanding of these reactions would greatly help the design of better bonding processes. In what follows, experimental design and procedures are first presented. Experimental results are reported. A summary is then given.
3.2 Experimental Design and Procedures

To help explain the experimental design and procedures, we briefly review the Ag-In phase diagram, as showed in Fig. 3.1 [3]. There are two solid solution phases, (Ag) and (In). The (Ag) phase can take up to 20 at. % indium. The solidus temperature ranges from 962 °C for pure Ag to 695 °C for (Ag) with 20 at. % In. The (In) phase has less than 1 at. % of Ag. A eutectic reaction occurs at 144 °C with 96.8 at. % In. Below the 144 °C solidus line, the alloy with In composition above 66.7 at. % is a mixture of AgIn$_2$ IMC and (In). As the temperature increases above 144 °C, the alloy converts to a mixture of molten phase (L) and AgIn$_2$ grains until temperature reaches to 166 °C. At 166 °C, the AgIn$_2$ begins to decompose into (L) and Ag$_2$In, also designated as γ phase, until 205 °C. Above 205 °C, the alloy with In composition ranging from 46 to 92.2 at. % converts to a mixture of (L) phase with ζ grains. At 205 °C, ζ phase decomposes into Ag$_2$In and (L) due to metatectic reaction.

Figure 3.1 Silver-Indium (Ag-In) binary phase diagram [3].
Copper (Cu) substrates of 10 mm × 12 mm in size are chosen as the platform of this study. They are cut from a 0.8 mm thick Cu sheet having 99.99% purity with a one side mirror finish. The Cu substrates are cleaned thoroughly by rinsing with acetone and deionized water to remove contaminations. The backside is painted with lacquer to prevent Ag and In deposition. Ag and In are electroplated sequentially on the Cu substrates. Fig. 3.2 depicts the cross section design of the sample. The Ag layer plated is thick enough so that the reaction between Ag and In never involves the Cu substrate. The Ag plating solution is a cyanide-free, mildly alkaline at pH 10.5. The In plating solution is sulfamate indium bath at pH 1 to 3.5. The bath temperature is room temperature. The current density is 13 mA/cm$^2$ for Ag plating and 21.5 mA/cm$^2$ for In plating. The current, voltage, temperature, and time are monitored closely during the plating processes. After plating, the sample is rinsed by deionized water and the lacquer on the backside of the Cu substrate is removed.

![Plating Diagram](image)

**Figure 3.2** Cross section of Cu/Ag/In structure to study chemical reactions of Ag and In at typical bonding temperature of 180 °C. The Ag layer is thick enough so that In does not have a chance to react with the Cu substrate.

For all samples, the thickness of Ag layer is fixed at 40 µm. The In thicknesses chosen for this study are 1, 3, 5, 10 and 15 µm, respectively. The thickness of In is measured and calibrated by α-step surface profiler. After plating, the sample is loaded in a vacuum oven that is pumped to 0.1 torr vacuum to suppress In oxidation during annealing process [12]. After the heater is turned on, it takes about 3 minutes to reach 180 °C. The sample is heated to 180 °C with
a dwell time of 5 minutes. The temperature is measured by a miniature thermocouple contacting the sample. After the heater is shut off, the assembly cools naturally in 50 millitorrs vacuum. It takes 90 minutes to cool down to room temperature. Indium thickness variation only causes the variation of molten phase (L) available to fill up the bonding interface gap. It will be reported in the next section. Chemical compositions and microstructures of the samples are analyzed using scanning electron microscopy (SEM) with energy dispersive X-ray (EDX) on the surface and on the cross section. The surface is also scanned by X-ray diffraction (XRD) to identify the chemical compounds.

3.3  Experimental Results and Analyses

3.3.1  Silver Layer Without Annealing

We began with Cu/Ag/In sample where the In layer is 1 µm. Fig. 3.3 shows SEM image on the surface of the sample after annealing at 180 °C. EDX analysis data give composition of 66 at. % Ag and 34 at. % In. Based on the Ag-In phase diagram in Fig. 3.1, this composition is Ag$_2$In IMC. To confirm this result, XRD was applied and the result is displayed in Fig. 3.4. All XRD peaks detected, (330), (600), (633), and (741) are associated with Ag$_2$In. These results indicate that the entire 1µm thick of In reacted with Ag to form Ag$_2$In after annealing. Fig. 3.5 exhibits a cross section SEM image of the sample, where EDX analysis detects two distinct regions. The first region shows composition of 66~68 at. % Ag and 32~34 at. % In, which is Ag$_2$In, consistent with EDX data taken on the surface of the sample. The region below is the solid solution phase, (Ag), with 97 at. % Ag and 3 at. % In. Based on EDX data, the (Ag) phase extends to 15 µm in depth. This observation shows that a small portion of In has diffused into the Ag layer to form (Ag), even at the annealing conditions of 180 °C for 5 minutes.
Figure 3.3 SEM image on the surface of a sample Cu/Ag/In(1 μm) after annealing at 180 ºC for 5 minutes: (a) low magnification and (b) high magnification. EDX analysis detects only Ag$_2$In.

Figure 3.4 XRD plot on the surface of sample Cu/Ag/In(1 μm) shown in Fig. 3.3, only Ag$_2$In is detected.
For the next experiment, the In layer in the Cu/Ag/In structure was increased to 3 μm. After annealing, Fig. 3.6 shows SEM image on the surface of the sample. SEM/EDX analysis detects only AgIn$_2$. To identify other reactions, SEM/EDX analysis on the cross section was employed. Fig. 3.7 displays the cross section SEM image. The SEM/EDX analysis detects three distinct regions. The first region is AgIn$_2$. The next region has composition of 70 at. % Ag and 30 at. % In, which is judged to be Ag$_2$In. Here, scallop structure was observed. The third region is (Ag). The formation of scallop IMC structure is due to the dissolution of Ag into the In-rich molten phase (In) [13], as illustrated in Fig. 3.8. Fig. 3.8(a) shows the as-plated sample where AgIn$_2$ layer is already formed when In atoms are plated over Ag layer, even at room temperature [9]. To confirm the compounds identified by EDX, XRD was applied on the surface of the sample. Fig. 3.9 displays the XRD result. The four dominating peaks associated with AgIn$_2$ are (211), (112), (202), and (213). A few peaks associated with Ag$_2$In are also picked up, i.e., (330), (550) and (633). The XRD data are consistent with SEM/EDX results. Since EDX picks up only AgIn$_2$ on the surface of the sample, it seems that XRD peaks of Ag$_2$In would have come from X-ray penetrating through the top AgIn$_2$ layer and getting diffracted by the Ag$_2$In layer.
Figure 3.6 SEM image on the surface of a sample Cu/Ag/In(3 μm) after annealing at 180 °C for 5 minutes: (a) low magnification and (b) high magnification. EDX detects only AgIn$_2$.

Figure 3.7 Cross section SEM image of sample Cu/Ag/In(3 μm) shown in Fig. 3.6. Three phases: AgIn$_2$, Ag$_2$In and (Ag) are detected.
Figure 3.8 Chemical reaction mechanisms during annealing process: (a) room temperature, (b) at or above 166 °C, (c) cooling down to room temperature.
The third experiment was then performed. The In layer thickness was increased to 5 µm. Fig. 3.10 is SEM image on the surface of the sample. SEM/EDX analysis on the surface of the sample detects only AgIn$_2$. Fig. 3.11 exhibits SEM image on the cross section of the sample. Three distinct regions are observed, AgIn$_2$, Ag$_2$In and (Ag). XRD data on the surface of the sample are provided in Fig. 3.12. The four dominating AgIn$_2$ peaks are (211), (112), (202), and (402). The Ag$_2$In peaks, (330), (550) and (633), are weaker than those observed in the sample with 3 µm. This is caused by thicker upper AgIn$_2$ layer which the X-ray has to penetrate through to get to Ag$_2$In. The results on this sample indicate that the entire 5 µm In layer was all consumed during the annealing process.
Figure 3.10 SEM image on the surface of a sample Cu/Ag/In(5 μm) after annealing at 180 °C for 5 minutes: (a) low magnification and (b) high magnification. EDX detects only AgIn₂.

Figure 3.11 Cross section SEM image of sample Cu/Ag/In(5 μm) shown in Fig. 3.10. Three phases: AgIn₂, Ag₂In and (Ag) are detected.
Figure 3.12 XRD plot on the surface of sample Cu/Ag/In(5 μm) shown in Fig. 3.10, exhibiting almost entirely AgIn$_2$ phase.

To determine how much In the reactions can consume during the annealing process, the fourth experiment was carried out where the In layer was increased to 10 μm. Fig. 3.13 shows SEM image on the surface of the sample. SEM/EDX analysis detects two different regions that intertwine, marked “A” and “B”. Region A is pure In and region B is AgIn$_2$. The ratio of pure In region to AgIn$_2$ region as determined by EDX is 1.2 to 1. SEM image on the cross section of the sample is provided as Fig. 3.14. Since pure In is very soft and ductile, it does not stay as the upper layer of the cross section after dicing and polishing. Accordingly, SEM/EDX analysis on the cross section detects only three distinct regions: AgIn$_2$, Ag$_2$In and (Ag). It does not detect pure In. To confirm indium existence on the sample surface, XRD was employed and the result is given in Fig. 3.15. A strong In peak at (101) is seen, together with In peaks at (110), (112),
(211), and (202). Other peaks are associated AgIn₂. No peaks associated Ag₂In are found because the X-ray cannot penetrate through the In and AgIn₂ layers to get to Ag₂In. The XRD and EDX results on the surface of the sample are consistent. That is, the 10 µm In layer was not consumed completely during the annealing process. As In thickness increases, Ag atoms need to diffuse through thicker AgIn₂ that was already formed to meet In atoms.

![SEM image on the surface of a sample Cu/Ag/In(10 µm) after annealing at 180ºC for 5 minutes: (a) low magnification and (b) high magnification. EDX analysis shows two regions intertwined, marked “A” and “B”. Region A is pure In and region B is AgIn₂. XRD data in Fig. 3.15 detect mostly In.](image)

**Figure 3.13** SEM image on the surface of a sample Cu/Ag/In(10 µm) after annealing at 180ºC for 5 minutes: (a) low magnification and (b) high magnification. EDX analysis shows two regions intertwined, marked “A” and “B”. Region A is pure In and region B is AgIn₂. XRD data in Fig. 3.15 detect mostly In.
Figure 3.14 Cross section SEM image of sample Cu/Ag/In(10 μm) shown in Fig. 3.13. Three phases: AgIn$_2$, Ag$_2$In and (Ag) are detected. The topmost layer should have been pure In, which did not stay on the cross section because of dicing and polishing processes.

![Figure 3.14 Cross section SEM image of sample Cu/Ag/In(10 μm) shown in Fig. 3.13. Three phases: AgIn$_2$, Ag$_2$In and (Ag) are detected. The topmost layer should have been pure In, which did not stay on the cross section because of dicing and polishing processes.](image)

Figure 3.15 XRD plot on the surface of sample Cu/Ag/In(10 μm) shown in Fig. 3.13, exhibiting mostly pure In.

![Figure 3.15 XRD plot on the surface of sample Cu/Ag/In(10 μm) shown in Fig. 3.13, exhibiting mostly pure In.](image)

The fifth experiment performed is for the sample with In layer increasing to 15 μm. Fig. 3.16 exhibits SEM image on the surface of the sample. The SEM/EDX analysis indicates that region marked “C” is pure In and region “D” is AgIn$_2$. The ratio of pure In region to AgIn$_2$ region is about 7 to 1. The cross-section SEM image, Fig. 3.17, shows three distinct regions: AgIn$_2$, Ag$_2$In and (Ag). It, however, does not show pure In. The reason is the same as that of
sample with 10 μm indium presented above. The XRD data on the surface of the sample are presented in Fig. 3.18. It is seen that the In (101) peak is stronger than that obtained from the sample with 10 μm In layer. This means that there is more pure In on the sample with 15 μm In layer than the sample having 10 μm In layer.

**Figure 3.16** SEM image on the surface of a sample Cu/Ag/In(15 μm) after annealing at 180 °C for 5 minutes: (a) low magnification and (b) high magnification. EDX analysis indicates two regions marked “C” and “D”. Region C is pure In and region D is AgIn₂.

**Figure 3.17** Cross section SEM image of sample Cu/Ag/In(15 μm) shown in Fig. 3.16. Three phases: AgIn₂, Ag₂In and (Ag) are detected. The topmost layer should have been pure In, which did not stay on the cross section because of dicing and polishing processes.
Figure 3.18 XRD plot on the surface of sample Cu/Ag/In(15 μm) shown in Fig. 3.16, exhibiting mostly pure In.

Based on the analysis data and discussions above, chemical reactions during the annealing process are proposed as follows [14],

\[ \text{Ag} + 2\text{In} \rightarrow \text{AgIn}_2 \]  \hspace{1cm} (1)

\[ 2\text{AgIn}_2 \rightarrow \text{Ag}_2\text{In} + 3\text{In(L)} \]  \hspace{1cm} (2)

\[ 2\text{Ag} + \text{In(L)} \rightarrow \text{Ag}_2\text{In} \]  \hspace{1cm} (3)

\[ \text{Ag} + 2\text{In(L)} \rightarrow \text{AgIn}_2 \]  \hspace{1cm} (4)
Eqs. 1 and 2 express the reactions below 166 °C and at 166 °C, respectively. Eq. 3 is the reaction of the molten phase with Ag to form Ag\textsubscript{2}In on the interface of AgIn\textsubscript{2} and Ag. Eq. 4 describes the reaction of Ag atoms with In atoms on the interface of In (L) and Ag\textsubscript{2}In to form AgIn\textsubscript{2}. According to Eq. 3, Ag reacts with indium in (L) to form Ag\textsubscript{2}In which has a melting temperature of 695 °C. Thus, during the bonding process at 180 °C, less and less (L) is available. Eventually, the entire (L) is consumed and the joint solidifies at the bonding temperature. Accordingly, it is critical to for the bonding structure design to provide enough (L) phase to flow and fill up the gap on the bonding interface caused by uneven surfaces. Even with the best effort to produce flat and smooth surfaces, gaps of a few microns are inevitable. Based on the results obtained so far, the thickness of In layer on the samples should be between 5 and 10 μm. In layer of 15 μm is also acceptable provided that the bonding time is increased beyond 5 minutes.

### 3.3.2 Silver Layer With Annealing

From the discussion above, In layer needs to be at least 5 μm in order to provide enough molten phase, (In), during the bonding process. If 5 μm In is consumed entirely to form only Ag\textsubscript{2}In, the resulting Ag\textsubscript{2}In thickness will be 10.7 μm. This may be too thick for many applications. The question is: how can we slow down the reaction between indium in (L) and Ag so that the (L) phase can stay longer on the bonding interface? Our observation on previous bonding experiments seems to indicate that the Ag\textsubscript{2}In growth rate depends on the Ag grain size [5]. To confirm this observation, we conducted the sixth experiment. The sample is the same as the one with 10 μm In layer thickness except that it was annealed at 450 °C for 3 hours before plating 10 μm In. Our previous experimental data have shown that Ag grains grow rapidly by annealing at high temperature; Ag grains grow from 26 nm to 3-5 μm [15]. For the sixth
experiment, after annealing the Ag layer on the sample at 450 °C, In was plated over the Ag. The sample was annealed at 180 °C for 5 minutes. A SEM image on the surface of the sample is shown in Fig. 3.19. The SEM/EDX analysis detects both pure In region marked “E” and AgIn$_2$ region marked “F”. The ratio of pure In region to AgIn$_2$ region is about 14 to 1. Fig. 3.20 displays cross section SEM images of the sample.

![Figure 3.19](image)

**(a) 2000×**

**(b) 10000×**

**Figure 3.19** SEM image on the surface of sample Cu/Ag/In(10 μm) after annealing at 180 °C for 5 minutes: (a) low magnification and (b) high magnification. EDX analysis shows pure In region marked “E” and AgIn$_2$ region marked “F”. For this sample, the Ag layer was annealed at 450 °C for 3 hours before plating the In layer. The similar sample but without Ag annealing is shown Fig. 3.13.
Figure 3.20 Cross section SEM image of sample Cu/Ag/In(10 μm) with Ag layer annealed at 450 ºC for 3 hours before plating the In layer. The cross section SEM image of a similar sample but without Ag annealing is exhibited in Fig. 3.14.

Based on chemical equations (3) and (4) and Ag₂In and AgIn₂ thicknesses observed, we calculated how much In was consumed in these two samples. The IMC thickness is the average thickness over the entire cross section of the samples. For the sample with Ag annealing, 1.5 μm In was consumed to form Ag₂In and 5 μm In was consumed to from AgIn₂. For the sample without Ag annealing, 2.8 μm In is consumed to form Ag₂In and 8.5 μm In was consumed to form AgIn₂. The detailed calculation procedure is presented in Table 3.1. The total In plated was 10 μm in either sample. For the sample with Ag annealing, not all In atoms react with Ag atoms. Pure In layer was not shown on the cross section SEM, Fig. 3.20, because the soft In layer got damaged easily during dicing and polishing processes. On the surface of the sample, the ratio of In region to AgIn₂ region is 14, as mentioned in the last paragraph. For the sample without Ag annealing, the ratio of In region to AgIn₂ region is 1.2. These results support our idea of increasing Ag grain size to slow down the reaction of In in (L) with Ag and thus decrease Ag₂In growth rate. In theory, microstructure with larger Ag grains has fewer grain boundaries for In atoms to diffuse into [5,16].
Table 3.1 Calculation of In thickness consumed in 2 versions of sample with 10 μm In: without Ag annealing and with Ag annealing at 450 °C for 3 hours.

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Sample without Ag annealing</th>
<th>Sample with Ag annealing</th>
</tr>
</thead>
<tbody>
<tr>
<td>Density of In (g/cm³)</td>
<td>7.31</td>
<td></td>
</tr>
<tr>
<td>Density of AgIn₂ (g/cm³)</td>
<td>8.43 [3]</td>
<td></td>
</tr>
<tr>
<td>Density of Ag₃In (g/cm³)</td>
<td>9.78 [3]</td>
<td></td>
</tr>
<tr>
<td>Atomic weight of In (g/mol)</td>
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<td></td>
</tr>
<tr>
<td>Atomic weight of AgIn₂ (g/mol)</td>
<td>338</td>
<td></td>
</tr>
<tr>
<td>Atomic weight of Ag₃In (g/mol)</td>
<td>331</td>
<td></td>
</tr>
<tr>
<td>Sample area (cm²)</td>
<td>1.36</td>
<td>1.43</td>
</tr>
<tr>
<td>Measured AgIn thickness (μm)</td>
<td>11</td>
<td>6.3</td>
</tr>
<tr>
<td>Measured Ag₃In thickness (μm)</td>
<td>6.0</td>
<td>3.0</td>
</tr>
<tr>
<td>Mole of AgIn₂</td>
<td>3.74x10⁻⁵</td>
<td>2.25x10⁻⁵</td>
</tr>
<tr>
<td>Mole of Ag₃In</td>
<td>2.41x10⁻⁵</td>
<td>1.27x10⁻⁵</td>
</tr>
<tr>
<td>Mole of indium in AgIn₂</td>
<td>2x3.74x10⁻⁵</td>
<td>2x2.25x10⁻⁵</td>
</tr>
<tr>
<td>Mole of indium in Ag₃In</td>
<td>2.41x10⁻⁵</td>
<td>1.27x10⁻⁵</td>
</tr>
<tr>
<td>Indium thickness in AgIn₂ (μm)</td>
<td>8.5</td>
<td>5.0</td>
</tr>
<tr>
<td>Indium thickness in Ag₃In (μm)</td>
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<td>1.5</td>
</tr>
<tr>
<td>Total indium thickness (μm)</td>
<td>11.3</td>
<td>6.5</td>
</tr>
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3.4 Summary

In this research, chemical reactions of Ag and In at 180 °C were investigated. 180 °C was chosen because it is a typical bonding temperature of Ag-In multilayer bonding structures. The samples are Cu substrates plated with 40μm Ag layer followed by In layer of thicknesses of 1, 3, 5, 10 and 15 μm, respectively. They were annealed at 180 °C for 5 minutes. The sample surfaces were examined by SEM/EDX and XRD. Cross sections of samples were evaluated by SEM/EDX. Table 3.2 summarizes the phases detected of all samples after annealing: In, AgIn₂, Ag₃In, and (Ag). Based on these results, in designing bonding structures, In thickness should be 5 μm or more to supply adequate molten phase (L) to fill up the gap on the bonding interface. For designs with In thinner than 5 μm, the Ag layer can be annealed at high temperature, such as 450 °C for 3 hours, before adding In layer. This annealing process increases the Ag grain size.
significantly and reduces the density of grain boundaries. It thus slows down the reaction rate of (L) and Ag in forming Ag₂In. Consequently, more molten phase (L) is kept in the bonding structure to fill up the gap on the bonding interface. The results of this investigation provide information on phases that can be expected in bonding experiments and offer valuable guideline in designing Ag and In layer structures for various bonding applications.

**Table 3.2** Compositions of Cu/Ag(40 µm)/In samples with different In thickness after annealing at 180 °C for 5 minutes. The Ag layer of the sample with * was annealed at 450 °C for 3 hours before plating In layer. In/AgIn₂ is the ratio of In to AgIn₂ regions measured on the surface of the samples.

<table>
<thead>
<tr>
<th>In thickness (µm)</th>
<th>In</th>
<th>AgIn₂</th>
<th>In/AgIn₂</th>
<th>Ag₂In</th>
<th>(Ag)/Ag</th>
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<tr>
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<td>x</td>
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<tr>
<td>15</td>
<td>x</td>
<td>x</td>
<td>7</td>
<td>x</td>
<td>x</td>
</tr>
</tbody>
</table>
Reference Chapter 3


Chapter 4

Bonding Silicon Chips to Aluminum Substrates Using Ag-In System Without Flux

4.1 Introduction

Among metals, aluminum (Al) has the unique advantages of lightweight, corrosion resistance and low cost. It weighs only 30% of copper (Cu) and 35% of iron (Fe). It costs only 25% of Cu by weight, $1,914/ton for Al versus $7,760.5/ton for Cu [1]. By volume, it costs only 7.5% of Cu. It has high electrical and thermal conductivities. It is easy to machine, cast, forge, shear, and roll. Thus, Al and its alloys have had enormous applications ranging from wrapping foils, beer cans, scuba tanks, car engines, airplanes, and electronic packaging. For examples, Al-Si composite baseplates are wrapped with Al skin for attaching high power devices [2]. For decades, Al has also been used as the material for interconnect pads on integrated circuits [3]. To make these Al pads solderable, a zincation process is used before Ni can be plated [3]. It is clear that while Al has had some electronic packaging applications, its application scope is quite limited. Fundamentally, there are two challenges which prevent Al from further expanding its applications in electronic products. The first is its high coefficient of thermal expansion (CTE) of \(23 \times 10^{-6}/^\circ \text{C}\), significantly higher than \(17 \times 10^{-6}/^\circ \text{C}\) of Cu. The second issue is that Al is not solderable; it does not bond to solders such as lead-free tin-based solder or lead-tin (Pb-Sn) solder without the zincation process followed by Ni plating. In this research, we set out to find techniques to surmount two challenges indicated above. Our first task is to make Al solderable without the zincation process. Then, we need to develop bonding techniques to manage the CTE...
mismatch. For demonstration, we chose to bond silicon (Si) chips to Al substrates. Si was selected because the Si-Al pair represents the bonding structure that has the largest CTE mismatch among all possible pairs between semiconductors and metals, i.e., $2.7 \times 10^{-6} /^{\circ}\text{C}$ of Si versus $23 \times 10^{-6} /^{\circ}\text{C}$ of Al. Numerous experiments have been performed. Our incessant persistence seems to pay off. We recently reported initial success in fluxless Sn bonding of Si chips to Al substrates [4], demonstrating the expanding application potential of Al substrates in electronic products, in particular in microwave and power modules.

In this project, we further expanded the application potential of Al in electronics. We explored the Ag-rich portion of the Ag-In system as the medium to bond Si chips to Al substrates. This system was chosen because high temperature Ag-In joints can be manufactured at low bonding temperature of 180 ºC. The bonding results are very encouraging. The joints are quite strong as measured by shear test data. In what follows, experimental design and procedures are presented. Experimental results are reported. A summary is then given.

4.2 Experiment Design and Procedures

Al substrates of 25 mm × 20 mm in size are chosen as the platform of this study. They are cut from a 1.75 mm thick Al sheet having 99 % purity. To prepare the Al substrates for bonding experiments, they are rinsed with acetone and deionized water to remove contaminations and dehydrated by baking at 120 ºC for 30 minutes. To make the Al substrates solderable, 100 nm of Cr and 200 nm of Cu are deposited on the substrates in a high vacuum E-beam evaporator in one vacuum cycle ($1 \times 10^{-5}$). Here, Cr is the adhesion layer and Cu prevents Cr from oxidation. The Cr/Cu composite also acts as the seed layer for the electroplating processes to follow. There are several choices of metals that can be electroplated such as gold.
(Au), Ag, Cu, and nickel (Ni). In this project, 15 µm of Ag and 8 µm of In are sequentially plated on the Al substrates. Only 10 mm × 12 mm area of the front surface of the substrates is plated. All other regions not plated, including the backside and edge faces, are coated with lacquer. The Ag plating solution is a cyanide-free, mildly alkaline at pH 10.5. The In plating solution is sulfamate indium bath at pH 1 to 3.5. The bath temperature is room temperature. The current density is 13 mA/cm² for Ag plating and 21.5 mA/cm² for In plating. A thin Ag capping layer is plated over the In layer to suppress In oxidation. The current, voltage, temperature, and time are monitored closely during the plating processes. After plating, the samples are rinsed with deionized water and the lacquer is removed. To make Si chips, 2-inch Si wafers are deposited with 30 nm of Cr, followed by 100 nm of Au using E-beam deposition in one vacuum cycle, 1×10⁻⁵ torr. The Si wafers are diced into 5 mm × 5 mm chips. The Cr layer is the adhesive layer and the Au layer prevents Cr oxidation. The Cr/Au dual layers function as a seed layer for electroplating 15 µm of Ag. The Al substrates and Si chips are ready for fluxless bonding experiments. Fig. 4.1 depicts the structure design of the sample.

![Figure 4.1 Bonding structure design of Si/Cr/Au/Ag and Al/Cr/Cu/Ag/In/Ag.](image)

To perform fluxless bonding, the Si chip is placed over the Al substrate and held by a fixture with 200 psi static pressure to ensure intimate contact [5]. The assembly is mounted on
the graphite platform in a vacuum furnace that is pumped to 100 millitorrs vacuum to suppress In oxidation during bonding. The platform is heated and the sample temperature is monitored by a miniature thermal couple. The bonding temperature is set at 180 °C with a dwell time of 5 minutes. The heater is shut off and the assembly cools naturally in 100 millitorrs vacuum. It takes about 90 minutes to cool to room temperature. No flux is used.

To evaluate the quality of the joints, scanning electron microscope with energy dispersive X-ray analysis (SEM/EDX) is employed to determine the chemical compositions, possible intermetallic, and microstructures of the samples. Six samples go through shear test to evaluate their shear strength and fracture modes. Two joint thicknesses are selected to access the ability of the design structure to deal with the large CTE mismatch.

### 4.3 Experimental Results and Discussion

Two designs were implemented, one with thick joint and the other having thinner joint. For the first design, Si chips with Cr/Au were plated with 15 µm Ag. Al substrates were plated with 15 µm Ag, followed by 8 µm In and thin capping Ag layer. Here, relatively thick Ag layers are selected to deal with the large CTE mismatch between Si and Al. The Si chip and Al substrate were held together with static pressure in a vacuum furnace. The sample was heated to 180 °C with a dwell time of 5 minutes and cooled naturally. The reactions during bonding are briefly presented below. When In is plated over Ag, some In reacts with Ag to form AgIn$_2$ compound even at room temperature [6-8]. According to Ag-In phase diagram as showed in Fig. 4.2, during the bonding process, as the temperature moves towards 180 °C, In layer melts at 156 °C and AgIn$_2$ decomposes into Ag$_2$In and (In) at 166 °C, where (In) is the indium-rich molten phase [9]. In other words, the (In) phase is derived from both the In layer and AgIn$_2$ compound.
The (In) phase wets the Ag layer on the Si chip and reacts with it to form AgIn$_2$. When this happens, bonding is essentially achieved. The (In) phase continues to react with Ag on the Si chip and Ag on the aluminum substrate to form AgIn$_2$ until the entire (In) phase is consumed during reflow process; at this time, Ag$_2$In begins to grow since AgIn$_2$ decomposes into Ag$_2$In and (In), and there are plenty of Ag atoms ready to react with (In). The joint solidifies even at the 180 °C bonding temperature because Ag$_2$In does not melt until 600 °C at least [9].

![Figure 4.2 Silver-Indium (Ag-In) binary phase diagram [9].](image)

Fig. 4.2 Silver-Indium (Ag-In) binary phase diagram [9].

Fig. 4.3 exhibits the cross section optical microscopy (OM) image of a sample. It clearly shows that the sample is well bonded, without visible voids. A cross section SEM image is displayed in Fig. 4.4. On the SEM images, there appear to be some voids of sub-micron in sizes. They might have been polishing compound particles embedded during the polishing process, but we have no way to tell exactly what they are. Fig. 4.5 shows the SEM image with 5 locations marked “a” to “e” where EDX analysis was performed. The results are presented in Table 4.1.
From the chip to the Al substrate, five distinct regions are clearly observed, staking as Ag/(Ag)/Ag$_2$In/(Ag)/Ag, nearly symmetrical. The Ag$_2$In layer has grown to 12 µm, pure Ag regions are 3µm, and solid solution (Ag) regions are 10 µm. The joint thickness is 40 µm.

**Figure 4.3** The cross section optical microscopy image of a bonded sample.

**Figure 4.4** Cross section SEM image of the sample shown in Fig. 4.3.
Figure 4.5 SEM image with locations marked “a” to “e” where EDX analysis was performed and the results are given in Table 4.1.

Table 4.1 EDX data on the cross section of sample shown in Fig. 4.5.

<table>
<thead>
<tr>
<th>Layer on Fig. 4.5</th>
<th>Composition (at. %)</th>
<th>Corresponding Phase</th>
</tr>
</thead>
<tbody>
<tr>
<td>a</td>
<td>Ag: 98-100, In: 0-2</td>
<td>Ag</td>
</tr>
<tr>
<td>b</td>
<td>Ag: 92-97, In: 3-8</td>
<td>(Ag)</td>
</tr>
<tr>
<td>c</td>
<td>Ag: 65-68, In: 32-35</td>
<td>Ag₃In</td>
</tr>
<tr>
<td>d</td>
<td>Ag: 95-97, In: 2-5</td>
<td>(Ag)</td>
</tr>
<tr>
<td>e</td>
<td>Ag: 98-100, In: 0-2</td>
<td>Ag</td>
</tr>
</tbody>
</table>

Despite the large CTE mismatch between Si and Al, the joints or Si chips did not break. This indicates that the Cr/Au adhesion composite on Si bonds well to Si on one site and to Ag on
another. The Cr/Cu adhesion composite on Al substrate also bonds well to Al substrate on one side and to Ag on another. A commonly used indicator for evaluating possible breakage caused by CTE mismatch is the maximum shear strain without stress. It is the strain calculated assuming that both bonded objects are free to contract during cooling down. It is the maximum possible shear strain on the resulting joint and is given by [10],

\[ \gamma = (\alpha_1 - \alpha_2)(T_2 - T_1)\frac{L}{2h} \]  

(1)

where \( \alpha_1 \) and \( \alpha_2 \) are the CTE of Si and Al, respectively, \( T_2 \) is the joint solidifying temperature, \( T_1 \) is the room temperature, \( L \) is diagonal length of Si ship, and \( h \) is the joint thickness. For this sample, the maximum shear strain without stress is calculated to be 0.29. This is a relatively large value compared to typical solder joints [11]. However, the samples did not break. We thus reduced the joint thickness in our second design.

For the second design, the joint thickness was reduced. The Ag layer on Si side was reduced to 4 µm and that on Al side to 8 µm. Indium layer decreased by 5 µm. The bonding conditions were that same as the first design. Several samples were made. Fig. 4.6 shows the cross section OM image of a sample and Fig. 4.7 is the SEM image. The joint is 16 µm thick. The compositions are Ag/(Ag)/Ag\(_2\)In/(Ag)/Ag as identified by EDX analysis. No visible voids are observed. The samples did not break either. This surprised us because we expected the samples to break due to large CTE mismatch. The maximum shear strain without stress calculated using Eq. 1 is 0.7, which is much higher than those seen in typical solder joints [11]. This result indicates that the bonding structure is inherently strong. To find out how strong it is, shear test was conducted.
Figure 4.6 Cross section optical microscopy image of a sample with thinner joint.

Figure 4.7 Cross section SEM image of the sample shown in Fig. 4.6.

Six samples of the first design were fabricated for shear test. During the test, the sample was mounted on the stage. A tool wedge pushed on one 5 mm-wide edge of the Si chip of the sample at a constant speed of 350 µm/s. Table 4.2 presents the breaking force and fracture
modes. The breaking force ranges from 16.7 kg to 93.7 kg. Two fracture modes were observed: chip breakage and joint fracture. According to military standards MIL-STD-883H method 2019.8, a force higher than 5 kg is considered passing the die shear test. Thus, all six samples far exceed the strength requirement specified in MIL-STD-883H. The force versus displacement curves are plotted in Fig. 4.8. For samples 1, 3, 4 and 5, the Si chip chipped away first. The force recorded is the force at which Si chip broke. Major portion of the Si chip remained bonded to the Al substrate. The tool wedge did not have a sharp edge to grip on and thus glided over the Si chip. Fig. 4.9 shows sample 5 after the shear test. It is clear that the fracture forces recorded for samples 1, 3, 4, and 5 are not the real breakage force of the joint. In fact, the joint never broke. For the samples 2 and 6, when the displacement reached 550 and 625 µm, respectively, the joint fractured and the Si chip was sheared off. The fracture forces of the joint are 93.7 and 75.2 kg, respectively, corresponding to 36.8 MPa and 29.5 MPa. The thickness of the Ag-In joint is 40 µm. It is not possible for the joint to deform with a shear displacement of 550 µm before fracture. Thus, the majority of the displacement is probably caused by the shear tester not by the samples. The company that performed the shear test did confirm that the displacement data are not accurate and should not be used for scientific analysis [12].

Table 4.2 Breakage forces and fracture modes of six samples during shear test.

<table>
<thead>
<tr>
<th></th>
<th>Breaking force (kg)</th>
<th>Bonding area (mm × mm)</th>
<th>Shear Strength (MPa)</th>
<th>fracture mode</th>
<th>Note</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>34.5</td>
<td>5.0 × 5.0</td>
<td>13.5</td>
<td>Si</td>
<td>die broke</td>
</tr>
<tr>
<td>2</td>
<td>93.7</td>
<td>5.0 × 5.0</td>
<td>36.8</td>
<td>Ag-In joint</td>
<td>Die removed</td>
</tr>
<tr>
<td>3</td>
<td>39.8</td>
<td>5.0 × 5.0</td>
<td>15.6</td>
<td>Si</td>
<td>die broke</td>
</tr>
<tr>
<td>4</td>
<td>16.7</td>
<td>5.0 × 5.0</td>
<td>6.6</td>
<td>Si</td>
<td>die broke</td>
</tr>
<tr>
<td>5</td>
<td>41.9</td>
<td>5.0 × 5.0</td>
<td>16.4</td>
<td>Si</td>
<td>die broke</td>
</tr>
<tr>
<td>6</td>
<td>75.2</td>
<td>5.0 × 5.0</td>
<td>29.5</td>
<td>Ag-In joint</td>
<td>Die removed</td>
</tr>
</tbody>
</table>

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Figure 4.8 Force versus displacement curves of six samples during shear test. The breakage force of each sample is indicated. The fracture modes are presented in Table 4.2.

Figure 4.9 Sample 5 after the Si chip was chipped off during the shear test. The breakage force is 41.9 kg at which the Si chip broke. Majority of the Si chip is still well bonded to the Al substrate.

For samples that fractured in the joint, it is of great interest to find out the fracture interface. Fig. 4.10 is the SEM image of the fracture surface of sample no. 2 on the Al substrate.
side. EDX analysis provides a composition for Ag$_2$In. Fig. 4.11 displays XRD distribution. It is seen that all XRD peaks detected are associated with Ag$_2$In. Scherrer formula in the XRD method was applied to estimate the Ag$_2$In grain size [13],

$$L = \frac{0.9\lambda}{B_{1/2}\cos\theta_B} \quad (2)$$

where $L$ is interpreted as a volume averaged crystallite dimension perpendicular to the reflecting planes, $\lambda$ is the X-ray wavelength, $\theta_B$ is the Bragg angle, and $B_{1/2}$ is the full-width-half-max (FWHM) of the peak after correcting for broadening caused by the diffractometer. $B_{1/2}$ is approximated by

$$B_{1/2}^2 = B_{obs}^2 - B_m^2 \quad (3)$$

where $B_{obs}$ is the measured peak width and $B_m$ is the breadth due to machine. The Ag$_2$In grain size obtained is 160 nm. Based on study above, the complete sample structure of Si/Cr/Au/Ag/(Ag)/Ag$_2$In/(Ag)/Ag/Cu/Cr/Al fractures within the Ag$_2$In region.
**Figure 4.10** SEM image of the fracture surface of sample no. 2 after the shear test. EDX detects only Ag$_2$In.

![EDX Spectrum](image)

**Figure 4.11** XRD plot on the fracture surface of sample no. 2 shown in Fig. 4.10. Only Ag$_2$In is detected.

### 4.4 Summary

In this research, Si chips were bonded to Al substrates using Ag-In system without flux. The bonding was conducted at a low temperature of 180 °C. The joints are composed of Ag/(Ag)/Ag$_2$In/(Ag)/Ag where (Ag) is a solid solution phase. As a result, the joint will achieve a solidus temperature of 600 °C at least, based on the Ag-In phase diagram. The shear strength of six samples was tested. Results of all six samples far exceed the requirement in MIL-STD-883H standards. Four samples broke within Si chip and the Ag-In joint never had a chance to be pushed by the tool wedge to fracture. The other 2 samples fractured along the Ag-In joint. The
shear strength of the joint is 36.8 MPa and 29.5 MPa, respectively. Fracture incurs within the Ag$_2$In region.

Acknowledgements

The authors thank II-VI Foundation for the financial support and encouragement on this research.
Reference Chapter 4


[12] Nordson DAGE, Fremont, California.

Chapter 5

The Strength of High Temperature Ag-In Joints Made between Copper by Fluxless Low Temperature Processes

5.1 Introduction

In electronic industries, popular die-attach materials are silver-epoxy, lead-free tin-based solders, and gold-tin (Au-Sn) eutectic [1-3]. Among them, the Au-Sn eutectic has the highest operating temperature of 172 °C, which is usually taken at homologous temperature of 0.8. In the advance and market demand of high temperature electronics, high temperature device chips built on SiC and GaN-based semiconductors have demonstrated operating temperatures higher than 350 °C. For example, the operating temperature of SiC power devices can go up to 465 °C [4-7]. To assemble these chips on packages, high temperature die-attachment materials are required. Based upon our literature search, the only thing available is sintered nano-silver paste [8-12]. This new bonding method is gaining ground in applications. In the sintering process, high pressure such as 5 MPa or higher is required to consolidate the sintered Ag and reduce pores. Research is being pursued to reduce the sintering pressure and temperature needed.

To produce high temperature joints at low process temperature, we have studied various binary systems and turned to the silver-indium (Ag-In) binary to design and develop the processes required [13]. For demonstration, we recently bonded 5 mm × 5 mm Si chips to aluminum substrates using fluxless Ag-In design [14]. The bonding was performed at a low temperature of 180 °C. The resulting joint consists of Ag/(Ag)/Ag$_2$In/(Ag)/Ag, where (Ag) is the
solid solution. The solidus temperature of the joint is limited by the solidus temperature of Ag$_2$In, which is 600 °C. Of the six samples sheared during shear test, only 2 broke in the joint and the breaking force is 75 and 94 kg, respectively. The breakage incurred in the Ag$_2$In compound layer and the fracture mode is brittle. The other four broke within Si chips and the actual strength of the joint could not be determined.

Since the Ag$_2$In compound breaks in brittle mode, in this research, we investigated the possibility of converting the Ag$_2$In compound layer into (Ag) after the joint is made. Post-bonding annealing step is added to convert Ag$_2$In into (Ag) by continuous reaction with nearby (Ag) and Ag regions. The joint structure of Ag/(Ag)/Ag$_2$In/(Ag)/Ag is expected to turn into Ag/(Ag)/Ag after the conversion. As a result, the joint solidus temperature will increase from 600 °C to at least 795 °C [13]. Instead of bonding Si chips to Cu substrates, Cu chips are bonded to Cu substrates to ensure that the sample breaks in the joint during shear test. Some preliminary results were recently presented in a conference [15]. In the paper, we report more complete and conclusive analysis and results. In what follows, experimental design and procedures are presented. Experimental results are reported. A summary is then given.

5.2 Experimental Design and Procedures

Fig. 5.1 depicts the bonding structure design. Cu was chosen to bond to Cu so that the Ag-In joint would break during shear test. For convenience in distinction, the upper Cu is called Cu chip and the bottom one is called Cu substrate. The 12 mm × 12 mm Cu substrates are cut from a 0.8 mm thick Cu sheet having 99.99 % purity with mirror finish on one side. The Cu substrates are cleaned thoroughly by rinsing with acetone and deionized water to remove contaminations. Ag and In are electroplated sequentially on the Cu substrates. The backside of Cu substrates is
painted with lacquer to prevent Ag and In deposition. The Ag plating solution is a cyanide-free, mildly alkaline at pH 10.5. The In plating solution is a sulfamate indium bath at pH of 1 to 3.5. The bath temperature is room temperature for both plating solutions. The current density is 13 mA/cm\(^2\) for Ag plating and 21.5 mA/cm\(^2\) for In plating. After plating In layer on the 15 µm Ag layer, a 0.1 µm thin Ag capping layer is plated over the In layer to suppress In oxidation. The current, voltage, temperature, and time are monitored closely during the plating processes. After plating, the sample is rinsed by deionized water and the lacquer on the backside of the Cu substrate is removed by acetone. The 10 mm × 11 mm Cu chips follow the same cleaning process and are electroplated with a 15 µm Ag layer. The Cu chips and substrates are ready for fluxless bonding experiments. There are two designs, with indium thickness of 5 and 8 µm, respectively. Relatively thick Ag layer of 15 µm is chosen so that the In does not have a chance to reach Cu and react with Cu.

![Diagram](image)

**Figure 5.1** Bonding structure design of Cu/Ag and Cu/Ag/In/Ag, not to scale. First design: indium thickness = 8 µm, second design: indium thickness = 5 µm.

In the fluxless bonding process, the Cu chip is placed over the Cu substrate and held by a fixture with 200 psi static pressure to ensure intimate contact with a silicone buffer [16]. The assembly is mounted on the graphite platform in a vacuum furnace that is pumped to 0.1 torr to
suppress In oxidation during bonding. The platform is heated and the sample temperature is
monitored by a miniature thermal couple. The bonding temperature is set at 180 °C with a dwell
time of 6 to 8 minutes. The heater is then shut off and the assembly cools naturally in 50
millitorrs vacuum. It takes about 90 minutes to cool to room temperature. No flux is used. After
bonding, we annealed the samples at 200 °C for 300, 500 and 1,000 hours, respectively to
convert the Ag₂In region of the joint to (Ag). 200 °C was chosen because it is more compatible
with the surviving temperature of most devices. The samples are then cut in cross section to see
the quality and compositions of the joints.

To evaluate the quality of the joints, scanning electron microscope with energy dispersive
X-ray analysis (SEM/EDX) is employed to determine the chemical compositions, possible
intermetallic structure, and microstructures of the samples. Six samples were put through shear
tests to evaluate their breaking forces and fracture modes.

5.3 Experimental Results and Discussion

5.3.1 Convert the Joints to Silver Solid Solution (Ag)

Two designs were implemented, with In layer thickness of 5 and 8 µm, respectively,
shown in Fig. 5.1. We started with In layer thickness of 8 µm, which is thus designated as the
first design. When In is plated over Ag, it reacts with Ag to form AgIn₂ compound even at room
temperature [17-19]. According to the Ag-In phase diagram in Fig. 5.2, as temperature increases
towards 180 °C, the In layer melts at 156 °C and AgIn₂ decomposes into Ag₂In and (In) at 166
°C, where (In) is the indium-rich molten phase [13]. The (In) phase wets and reacts with the Ag
layer on the Cu chip to form Ag₂In. When this happens, bonding is essentially achieved. The (In)
phase continues to react with both Ag layers to form more Ag$_2$In until the entire (In) phase is consumed. At this moment, the joint solidifies even at the 180 °C bonding temperature because Ag$_2$In does not melt until temperature reaches 600 °C [13].

**Figure 5.2** Silver-Indium (Ag-In) binary phase diagram.

Fig. 5.3(a) displays the cross section optical microscopy (OM) image of a typical bonded sample before annealing at 200 °C. It clearly shows that the sample is well bonded without visible voids. The reddish region is the Ag$_2$In layer of the joint. A cross section back-scattered SEM image is exhibited in Fig. 5.3(b). The lighter gray region is the Ag$_2$In layer, as confirmed by EDX. This Ag$_2$In region matches that in the OM image. Fig. 5.3(b) also provides the EDX analysis with 7 locations marked “1” to “7”. The results are presented in Table 5.1. Three phases are clearly observed: Ag, (Ag) and Ag$_2$In. Here, the Ag$_2$In layer is 15µm in thickness. It is interesting to note that (ζ) phase, where “Ag$_3$In” is on its Ag-rich boundary is not detected even though it is presented in the phase diagram, Fig. 5.2.
Figure 5.3 Cross section optical microscopy image and backscattered SEM image of sample bonded at 180 °C. (a) Un-annealed, (b) EDX data of layers marked “1” to “7” and the results are given in Table 5.1.

Table 5.1 EDX data on cross section of the sample of first design shown in Fig. 5.3(b).

<table>
<thead>
<tr>
<th>Layer on Fig. 5.3(b)</th>
<th>Composition (at. %)</th>
<th>Corresponding Phase</th>
</tr>
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<tbody>
<tr>
<td>1</td>
<td>Ag: 100, In: 0.00</td>
<td>Ag</td>
</tr>
<tr>
<td>2</td>
<td>Ag: 99.62, In: 0.38</td>
<td>(Ag)</td>
</tr>
<tr>
<td>3</td>
<td>Ag: 65.99, In: 34.01</td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>Ag: 67.27, In: 32.73</td>
<td>Ag&lt;sub&gt;2&lt;/sub&gt;In</td>
</tr>
<tr>
<td>5</td>
<td>Ag: 68.47, In: 31.53</td>
<td></td>
</tr>
<tr>
<td>6</td>
<td>Ag: 86.08, In: 13.92</td>
<td></td>
</tr>
<tr>
<td>7</td>
<td>Ag: 98.48, In: 1.52</td>
<td>(Ag)</td>
</tr>
</tbody>
</table>

To convert the Ag<sub>2</sub>In region in the joint to (Ag), more samples were produced using the same bonding conditions. These samples were followed by annealing in an oven at 200 °C for 300 hours. Fig. 5.4(a) exhibits the cross section OM image of a sample taken from the batch. Slight reddish zone still shows up, indicating that Ag<sub>2</sub>In is still in the joint. Fig. 5.4(b) shows the
SEM image of the joint with 7 locations marked where EDX data are presented in Table 5.2. Only three phases, (Ag), (ζ), and Ag₂In, were identified. Pure Ag was not there anymore. Locations 2 and 5 are thought to be (ζ) based on the composition and the phase diagram. To achieve complete conversion of Ag₂In into (Ag), the remaining samples were annealed at 200 °C for additional 200 hours for a total annealing time of 500 hours. Fig. 5.4(c) exhibits the cross section OM image of a sample. The slight reddish Ag₂In zone is still in the joint. Fig. 5.4(d) displays the cross section SEM image. EDX analysis indicates that the joint consists of only (Ag) with possible small patches of (ζ). The remaining samples were annealed at 200 °C for additional 500 hours for a total annealing time of 1,000 hours. Fig. 5.4(e) shows the cross section OM image of a sample. The slightly reddish Ag₂In region is still in the joint. Fig. 5.4(f) displays the cross section SEM image with locations marked for EDX analysis and results presented in Table 5.3. Small patches of Ag₂In and (ζ) are detected in the joint. According to the Ag-In phase diagram, the solidus temperature of the joint is 600 °C which is limited by the Ag₂In phase. After this severe annealing at 200 °C for 1,000 hours, the samples are still strongly bonded. Shear test results will be reported shortly. Samples bonded with other materials except sintered silver are likely to have failed after this annealing condition [11].
Figure 5.4 Cross section optical microscopy images and backscattered SEM images of first-design samples bonded at 180 °C. (a) After annealing at 200 °C for 300 hours, (b) EDX data of layers shown in (a) marked “1” to “7” and the results are given in Table 5.2, (c) After annealing at 200 °C for 500 hours, (d) Cross section backscattered SEM image of the sample shown in (c), (e) After annealing at 200 °C for 1,000 hours, (f) EDX data of layers shown in (e) marked “1” to “7” and the results are given in Table 5.3.
Table 5.2 EDX data on cross section of the sample of first design shown in Fig. 5.4(b).

<table>
<thead>
<tr>
<th>Layer on Fig. 5.4(b)</th>
<th>Composition (at. %)</th>
<th>Corresponding Phase</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Ag: 91.55, In: 9.45</td>
<td>(Ag)</td>
</tr>
<tr>
<td>2</td>
<td>Ag: 74.05, In: 25.95</td>
<td>(ζ)</td>
</tr>
<tr>
<td>3</td>
<td>Ag: 70.69, In: 29.31</td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>Ag: 66.10, In: 33.90</td>
<td>Ag₂In</td>
</tr>
<tr>
<td>5</td>
<td>Ag: 76.36, In: 23.64</td>
<td>(ζ)</td>
</tr>
<tr>
<td>6</td>
<td>Ag: 84.74, In: 15.26</td>
<td></td>
</tr>
<tr>
<td>7</td>
<td>Ag: 90.39, In: 9.61</td>
<td>(Ag)</td>
</tr>
</tbody>
</table>

Table 5.3 EDX data on cross section of the sample of first design shown in Fig. 5.4(f).

<table>
<thead>
<tr>
<th>Layer on Fig. 5.4(f)</th>
<th>Composition (at. %)</th>
<th>Corresponding Phase</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Ag: 90.81, In: 9.19</td>
<td>(Ag)</td>
</tr>
<tr>
<td>2</td>
<td>Ag: 83.63, In: 16.37</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>Ag: 81.22, In: 18.78</td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>Ag: 76.78, In: 23.22</td>
<td>(ζ)</td>
</tr>
<tr>
<td>5</td>
<td>Ag: 70.88, In: 29.12</td>
<td>Ag₂In</td>
</tr>
<tr>
<td>6</td>
<td>Ag: 86.15, In: 13.85</td>
<td></td>
</tr>
<tr>
<td>7</td>
<td>Ag: 94.86, In: 5.14</td>
<td>(Ag)</td>
</tr>
</tbody>
</table>

To convert the Ag₂In region of the joint to (Ag) completely, the second design was initiated and implemented, as indicated in Fig. 5.1. The In thickness is reduced from 8 µm to 5 µm and the Ag thickness has no change. Thinner indium layer results in thinner Ag₂In. This
increases the silver composition gradient from silver layers towards Ag$_2$In region and thus enhances the diffusion rate. The annealing condition was raised from 200 °C to 250 °C to shorten the annealing time. Bonded samples were annealed at several annealing times and studied to examine complete conversion of Ag$_2$In into (Ag). Fig. 5.5(a) shows the cross section OM image of a sample after annealing at 250 °C for 350 hours. The joint is still bonded well between the Cu chip and Cu substrate. The reddish zone associated with Ag$_2$In is gone, suggesting complete Ag$_2$In to (Ag) conversion. Fig. 5.5(b) exhibits the cross section SEM image of the sample where high quality joint is clearly observed. Fig. 5.5(b) also performed the EDX analysis with 10 locations marked “1” to “10”. These results are presented in Table 5.4. All locations measured exhibit the composition of (Ag). The annealing process has successfully converted the Ag$_2$In region of the joint into (Ag). As the result, the joint has only one phase, i.e., (Ag). The Ag composition in (Ag) is higher than 94 at. %. According to the Ag-In phase diagram, the solidus temperature of this (Ag) is 900 °C. It is worth mentioning that samples bonded with other die-attach materials except sintered silver could not have survived this annealing process [11].
Figure 5.5 Cross section optical microscopy image and backscattered SEM image of second-design sample bonded at 180 °C. (a) After annealing at 250 °C for 350 hours, (b) EDX data of layers marked “1” to “10” and the results are given in Table 5.4.

Table 5.4 EDX data on cross section of the sample of second design shown in Fig. 5.5(b).

<table>
<thead>
<tr>
<th>Layer on Fig. 5.5(b)</th>
<th>Composition (at. %)</th>
<th>Corresponding Phase</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Ag: 96.38, In: 3.62</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>Ag: 96.09, In: 3.91</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>Ag: 95.69, In: 4.31</td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>Ag: 94.78, In: 5.22</td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>Ag: 94.18, In: 5.82</td>
<td></td>
</tr>
<tr>
<td>6</td>
<td>Ag: 94.53, In: 5.47</td>
<td>(Ag)</td>
</tr>
<tr>
<td>7</td>
<td>Ag: 95.70, In: 4.30</td>
<td></td>
</tr>
<tr>
<td>8</td>
<td>Ag: 94.60, In: 5.40</td>
<td></td>
</tr>
<tr>
<td>9</td>
<td>Ag: 96.43, In: 3.57</td>
<td></td>
</tr>
<tr>
<td>10</td>
<td>Ag: 97.21, In: 2.79</td>
<td></td>
</tr>
</tbody>
</table>

5.3.2 Shear Test Results

The shear test experiment is now presented. Six samples from the first design, i.e. 8 μm In, annealed at 200 °C for 1,000 hours and seven samples from the second design, i.e. 5 μm In, annealed for 350 hours at 250 °C were fabricated for shear testing. For the first-design samples, the sample was mounted on the stage. A tool wedge pushed 10 mm-wide edge of the Cu chip of the sample at a constant speed of 350 μm/s [20]. Fig. 5.6 lists the breaking force and fracture mode. The breaking force ranges from 178 to 200 kg. Two samples did not break at a force of 200 kg which is the maximum force available from the shear tester. According to military standards MIL-STD-883H method 2019.8, a breaking force higher than 5 kg passes the die shear test. Thus, all six samples far exceed the requirement specified in MIL-STD-883H. Fig. 5.7(a)
displays the SEM image of the fracture surface after shear test. The fracture appears to be a mixture of brittle and ductile modes. Quantitative fracture evaluation is underway by tensile test of bulk samples.

![Shear test results](image)

**Figure 5.6** The bar chart and table illustrate the breaking forces of the 6 samples of the first design annealed at 200 °C for 1,000 hours and 7 samples of the second design annealed at 250 °C for 350 hours. The shear tester could not break samples no. 2 and no.3 of first design.
Figure 5.7 SEM image of the fracture surface of samples after the shear test. (a) First-design sample: EDX detects Ag$_2$In, (ζ) and (Ag). (b) Second-design sample: EDX detects only the solid solution phase (Ag).

For the second design, the samples were sent to Tianjin University [21] in China for shear test because the tester over there can better handle the shape of our samples. Fig. 5.6 presents the testing results. The breaking force ranges from 61 to 165 kg. The breaking force of all samples far exceeds the requirement specified in MIL-STD-883H. Fig. 5.7(b) shows the SEM image of the fracture surface. The fracture also appears to be a mixture of brittle and ductile modes. Quantitative fracture evaluation is also underway using tensile test.

It is worth pointing out that the breaking force of the first-design samples is significantly higher than that of the second-design samples (Fig. 5.6). The joint of the first-design sample consists of mostly (Ag) phase with small regions of (ζ) and Ag$_2$In compound. Thus, the joint is an alloy of three phases. The joint of the second-design samples consists of only the (Ag) phase. The breaking force data seem to suggest that an alloy joint is stronger than a single (Ag) phase joint. This is a preliminary assessment. Further investigation is required to confirm it.
5.4 Summary

Advances in semiconductor technology have demonstrated device chips that achieve operation temperature as high as 465 °C [4-7]. To put these chips into operations, they have to be bonded to a substrate or package and wired. The resulting joint must have high enough solidus temperature. Among all common die-attach materials, only sintered nano-silver and Au-Sn alloys with Au composition higher than 85 wt. % can meet this aim.

In this research, we looked into the Ag-In system and developed fluxless low temperature processes to produce high strength and high temperature joints between two Cu substrates. After bonding at 180 °C, the samples were annealed at 200-250 °C to alter the compositions and microstructures to increase the solidus temperature, the strength, and ductility. Two designs were experimented with. For the first design, the samples were annealed at 200 °C for 1,000 hours. The joint solidus temperature is at least 600 °C. Of the six samples sheared, the breaking force ranges from 178 to 200 kg. The shear tester could not break two of the six samples. These results far exceed the 5 kg requirement in military standards MIL-STD-883H method 2019.8. The fracture incurs inside the joint. The joint structure is an alloy of mostly (Ag) solid solution embedded with micron-size (ζ) and Ag$_2$In regions. For the second design, the samples were annealed at 250 °C for 350 hours. Seven samples were sheared and the breaking force ranges from 61 to 165 kg which far exceeds the requirement in military standards. Fracture also incurs inside the joint. The joint consists of only (Ag) phase with Ag composition higher than 94 wt. %. The solidus temperature is 900 °C. For either design, the samples break in a mix of brittle and ductile modes or ductile mode only.
The research results have shown that high strength and high temperature joints can be manufactured using fluxless low-temperature processes with the Ag-In system. Compared to the Au-rich Au-Sn alloy bonding technique that results in Au composition between 90 to 95 wt. %, this method is much more affordable because the price of Au is 60 times of Ag. Compared to sintered nano-silver technique, this method is less expensive because the manufacturing cost of nano-silver paste is very high, about 5× of Ag cost. One gram of nano-silver paste in production quantity costs 5× of the market value of Ag. Accordingly, the technology reported here should be valuable in developing high temperature packages.

Acknowledgements

The authors greatly appreciated the support and encouragement from II-VI Foundation. They also thank Professors Guo-Quan Lu and Xu Chen, Drs. Gang Chen and Yunhui Mei, and their students Yunjiao Cao and Dan Han of Tianjin Key Laboratory of Advanced Technology and School of Material Science and Engineering, Tianjin University, China, for performing the shear test of the second-design samples.
Reference Chapter 5


[21] Tianjin Key Laboratory of Advanced Technology and School of Material Science and Engineering, Tianjin University, China.
Chapter 6

Thermal Cycling Reliability Study of Ag-In Joints between Si Chips and Cu Substrates Made by Fluxless Processes

6.1 Introduction

For a semiconductor chip to function, it is bonded to and wired to a package. The material that bonds the chip to the package is called the die-attach material. The most commonly used die-attach materials are silver epoxies and solders [1-2]. Of these materials, the maximum operating temperature is constrained to 165 °C of 90Pb10Sn solder [3]. Here, the maximum operating temperature is set at a homologous temperature (\(T_h\)) of 0.8 [4]. Recent advances in semiconductor technology have greatly increased the operating temperature of semiconductor devices. For example, operating temperature of SiC chips as high as 465 °C has been demonstrated [5]. These device chips cannot be put to high temperature use unless high temperature die-attach materials are available. So far, our extensive literature search has identified the sintered nano-silver paste as the only thing available [6-10]. This technology reduces the silver paste to pure silver by sintering processes. During bonding and sintering, high temperature, 225 to 300 °C, and high pressure, 5 to 20 MPa are required [11-12]. Another consideration is that nano-silver pastes are costly, ranging from 5× to 10× of the cost of silver.

We have recently developed fluxless processes to produce high temperature and high strength Ag-In joints at 180 °C bonding temperature [13]. The joint solidus temperature is higher than 600 °C. Subsequent annealing steps improve the joint ductility and increase the solidus
temperature beyond 800 °C [14]. For real applications, a serious concern is the long term reliability of the joints under thermal stress caused by mismatch of thermal expansion coefficient (CTE) between the chip and the package. In this research, we focused on the reliability study using thermal cycling method. We fabricated samples of Si chips bonded to Cu substrates using the Ag-In system, annealed the samples, evaluated the joint composition and microstructure, and performed thermal cycling test between -40 to 200 °C for 5,000 cycles to ensure long term reliability. In what follows, experimental design and procedures are presented. Experimental results are reported. A summary is then given.

6.2 Experimental Design and Procedures

In this study, Si chips and Cu substrates are chosen to form the bonding pair because of the large CTE mismatch, i.e., $2.7 \times 10^{-6}/°C$ of Si versus $17 \times 10^{-6}/°C$ of Cu. Cu is also a popular substrate and lead-frame material. Large CTE mismatch is needed to really test the reliability of bonded samples under thermal cycling conditions. Fig. 6.1 depicts the bonding structure design. The 10 mm × 12 mm Cu substrates are cut from a 0.8 mm thick Cu sheet having 99.9 % purity with mirror finish on one side. The Cu substrates are cleaned thoroughly by rinsing with acetone and deionized water to remove contaminations. Ag and In are electroplated sequentially on the Cu substrates. The backside of Cu substrates is painted with lacquer to prevent Ag and In deposition. The Ag plating solution is a cyanide-free, mildly alkaline at pH 10.5. The In plating solution is a sulfamate indium bath at pH of 1 to 3.5. The bath temperature is room temperature for both plating solutions. The current density is 13 mA/cm$^2$ for Ag plating and 22 mA/cm$^2$ for In plating. The current, voltage, temperature, and time are monitored closely during the plating processes. After plating In layer on the 15 µm Ag layer, a 0.1 µm thin Ag capping layer is plated.
over the In layer to suppress In oxidation. After plating, the sample is rinsed by deionized water and the lacquer on the backside of the Cu substrate is removed by acetone. To make Si chips, 2-inch Si wafers are deposited with 30 nm of Cr, followed by 100 nm of Au using E-beam deposition in one vacuum cycle, 1×10^{-5} torr. The Si wafers are diced into 5 mm × 5 mm chips. The Cr layer is the adhesive layer and the Au layer prevents Cr oxidation. The Cr/Au dual layers function as a seed layer for electroplating 15 µm of Ag. The Cu substrates and Si chips are ready for fluxless bonding experiments.

In the fluxless bonding process, the Si chip is placed over the Cu substrate and held by a fixture with 200 psi (1.37 MPa) static pressure to ensure intimate contact. A silicone buffer is placed over the Si chip to avoid damaging Si chip. The assembly is mounted on the graphite platform in a vacuum furnace that is pumped to 0.1 torr to suppress In oxidation during bonding [15]. The platform is heated and the sample temperature is monitored by a miniature thermal couple. The bonding temperature is set at 180 °C with a dwell time of 7 to 9 minutes. The heater is then shut off and the assembly cools naturally in 50 millitorrs vacuum. It takes about 90 minutes to cool to room temperature. No flux is used. After bonding, samples are annealed at 250 °C for 190 hours in a typical convection oven to convert the Ag₂In region of the joint to an alloy of Ag₂In, (ζ) and (Ag) to strengthen the joint, where (ζ) is “Ag₃In” on its Ag-rich boundary. This condition is adapted based on prior annealing experience [14]. The samples are cut in cross section to see the quality and compositions of the joints. It is worth pointing out that in production environment, a large number of devices can be annealed at the same time. The annealing step will not add much to the production cost.
To evaluate the quality of the joints, scanning electron microscope with energy dispersive X-ray analysis (SEM/EDX) is employed to examine the chemical compositions, intermetallics, and microstructures of the samples. Ten samples are produced for thermal cycling test to evaluate the reliability.

### 6.3 Experimental Results and Discussion

Si chips coated with Cr/Au were plated with 15 µm Ag. Cu substrates were plated with 15 µm Ag, followed by 8µm In and thin capping Ag layer. Here, relatively thick Ag layers were selected to deal with the large CTE mismatch between Si and Cu. Fig. 6.2 exhibits the cross section optical microscopy (OM) image of a typical sample after bonding at 180 °C. Our previous study has shown that this type of joints consists of Ag/(Ag)/Ag\textsubscript{2}In/(Ag)/Ag structure. The distinct reddish middle region is Ag\textsubscript{2}In compound. During shear test, the joints broke in the Ag\textsubscript{2}In region and the fracture is brittle mode [13]. Post-annealing step was thus developed to strengthen the joint and change the fracture from brittle mode to a mixed mode [14].
Figure 6.2 Cross section optical microscopy image of a sample bonded at 180 °C. The joint consists of Ag/(Ag)/Ag$_2$In/(Ag)/Ag. The distinct reddish middle region is Ag$_2$In.

In present investigation, annealing condition of 250 °C for 200 hours was first designed. The resulting joint microstructure contains almost entirely the solid solution phase, (Ag). The annealing time was thus reduced to 190 hours to keep small amount of Ag$_2$In and ($\zeta$) in the joint. Fig. 6.3(a) displays a cross section optical image of a representative sample after annealing. It is observed that the Ag$_2$In layer shown in Fig. 6.2 has converted to a thin alloy region of Ag$_2$In, ($\zeta$) and (Ag). Fig. 6.3(b) exhibits a backscattered SEM image with 5 EDX locations marked. The EDX data are presented in Table 6.1. Three phases, (Ag), ($\zeta$) and Ag$_2$In are identified. The joint becomes an alloy of Ag$_2$In, ($\zeta$) and (Ag). Our previous shear test results have shown that an alloy joint like this is stronger than a joint consisting of a distinct Ag$_2$In layer. It is also stronger than a joint consists of entirely the solid solution phase (Ag) [14].
Figure 6.3 (a) Cross section optical microscopy image of a typical sample after annealing at 250 °C for 190 hours, (b) back-scattered SEM image where EDX data were obtained at locations marked “1” to “5” and provided in Table 6.1.

**Table 6.1** EDX data on cross section of the sample in Fig. 6.3(b).

<table>
<thead>
<tr>
<th></th>
<th>Ag at. %</th>
<th>In at. %</th>
<th>Corresponding phase</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>86.1</td>
<td>13.9</td>
<td>(Ag)</td>
</tr>
<tr>
<td>2</td>
<td>76.1</td>
<td>23.9</td>
<td>(ζ)</td>
</tr>
<tr>
<td>3</td>
<td>66.1</td>
<td>33.9</td>
<td>Ag₂In</td>
</tr>
<tr>
<td>4</td>
<td>86.9</td>
<td>13.1</td>
<td>(Ag)</td>
</tr>
<tr>
<td>5</td>
<td>87.3</td>
<td>12.7</td>
<td>(Ag)</td>
</tr>
</tbody>
</table>

Despite the large CTE mismatch between Si and Cu, the joint did not break after cooling down to room temperature during the bonding process. This indicates that the Cr/Au adhesion layer on Si bonds well to the Si chip on one side and to Ag on another side. A commonly used
indicator for evaluating the severity of CTE mismatch is the maximum shear strain without stress. It is the strain calculated assuming that both bonded objects are free to contract during cooling down. It is the maximum possible shear strain on the resulting joint and is given by [16],

\[ \gamma = (\alpha_1 - \alpha_2)(T_2 - T_1)L/2h \]  (1)

where \( \alpha_1 \) and \( \alpha_2 \) are the CTE of Cu and Si, respectively, \( T_2 = 180 \, ^\circ C \) is the joint solidifying temperature, \( T_1 \) is the room temperature, \( L \) is diagonal length of Si chip, and \( h \) is the joint thickness. For this design, the maximum shear strain without stress is calculated to be 0.21. This is relatively large compared to that of typical solder joints [17].

Ten samples were fabricated and annealed at 250 °C for 190 hours for thermal cycling test. Two thermal cycling (TC) profiles were used. The first TC profile is -40 to +85 °C with a cycle time of 170 minutes. The second TC profile is -40 to +200 °C with a cycle time of 26 minutes. It was performed at the University of Idaho due to its faster cycling time. The TC machine has dual chambers. The samples are moved up and down between a low temperature chamber set at -40 °C and a high temperature chamber set at 200 °C. The dwell time at each chamber is 10 minutes. This design greatly cuts down the temperature ramp-up time and cooling time. The first and second TC profile is shown in Fig. 6.4. In this study, the samples went through 100 cycles using the first TC profile in our laboratory to make sure that nothing broke. They were shipped to University of Idaho for 5,000 cycles using the second TC profile.
Figure 6.4 (a) The first thermal cycling (TC) profile: between -40 and 85 °C, (b) The second thermal cycling (TC) profile: between -40 and 200 °C.

Fig. 6.5, which is figure 2019-4 of MIL-STD-883H method 2019.8 [18], exhibits the criteria on minimum breaking force versus die area. Our die area is 5 mm × 5 mm, larger than 64 × 10^4 in². Thus, the minimum breaking forces required are 2.5 kg at 1×, 3.125 kg at 1.25×, and 5 kg at 2×, respectively. If separation occurs with a force between the 1× and 1.25× curves and with less than 50 percent of the die to substrate contained attach-medium coverage, it constitutes a failure. If separation occurs with a force between the 1× and 2× curves and with less than 10% of the die to substrate contained attach-medium coverage, it also constitutes a failure. If separation occurs with a force above the 2× curve, the sample passes the die shear strength test regardless of the percentage of die to substrate contained attach-medium coverage. To be conservative, we chose 5 kg as the criterion. It is worth mentioning that our research group started referring to Fig. 6.5 in 1989 [19]; at the time the MIL-STD-883 was at version C. Fig. 6.5 has not changed since then. Based on the purpose of MIL-STD-883H presented, the die shear strength test specifies the conditions obtainable in the laboratory and at the device level which give test results equivalent to the actual military and space operations in the field, and obtains
reproducibility of the test results.

![Graph showing die shear strength criteria]

**Figure 6.5** Die shear strength criteria: minimum force versus die-attach area (Figure 2019-4 of MIL-STD-883H).

During the 100 cycles using the first TC profile, samples was checked at every 10 cycles by pushing the Si chip with 5 kg force. Fig. 6.6 shows all ten samples; they all survived. During the 5,000 cycles using the second TC profile, samples were also checked regularly. Seven of ten samples survived 5,000 cycles with no breakage at all. Three samples failed at 850\(^{th}\), 2,600\(^{th}\) and 3,000\(^{th}\) cycles, respectively. Fig. 6.7 exhibits the fracture surface of samples broke at 850\(^{th}\) and 2,600\(^{th}\) cycles, respectively. The fracture mode of both samples is a mixture of ductile and brittle
modes. EDX analysis picks up the compositions of Ag$_2$In, (ζ) and (Ag). Fig. 6.8 shows the XRD data of both samples. All peaks are associated with Ag$_2$In, (ζ) and (Ag). The XRD results agree with EDX data well.

**Figure 6.6** Ten samples after 100 cycles of first thermal cycling (TC) test which is between -40 and +85 °C. All samples survived.

**Figure 6.7** SEM images of the fracture surface of samples that broke at (a) 850$^{th}$ cycle and (b) 2,600$^{th}$ cycle of thermal cycling test between -40 and 200 °C.
Figure 6.8 XRD plots on the fracture surface of two samples shown in Fig. 6.7. All peaks are associated with $\text{Ag}_2\text{In}$, ($\zeta$) and (Ag).

Fig. 6.9 presents the backscattered SEM image of one of the seven samples that survived
the second TC test for 5,000 cycles. Compared with samples prior to thermal cycling test, only some sub-micron voids were induced by the thermal cycling test. The Si/joint interface and joint/Cu interface are still in perfect shape, showing no sign of cracks or degradation. This observation again illustrates that the adhesion Cr/Au dual-layer can bond to Si on one side and bond to Ag on the other side.

![Cross section backscattered SEM image of a sample after surviving thermal cycling test between -40 to + 200 °C for 5,000 cycles.](image)

**Figure 6.9** Cross section backscattered SEM image of a sample after surviving thermal cycling test between -40 to + 200 °C for 5,000 cycles.

To assess our thermal cycling (TC) results versus what were reported by others, we searched for publications that use sintered nano-silver paste, which can provide comparable operating temperature range. We found only two publications that report thermal cycling results of samples bonded with sintered silver. Based on the data reported, we compiled Table 6.2 that includes important parameters for a comparison. One parameter often ignored in comparing thermal cycling test results is the indicator that shows how severe the CTE mismatch is between the chip and the substrate. The most commonly adapted indicator seems to be the maximum
shear strain on the joint at stress-free state, $\gamma$, as expressed in Eq. 1. This indicator is included in Table 6.2. Another way to find the severity of CTE mismatch is to use finite element analysis to compute stress distribution in the bonded structure. But this alone is a challenge task because the stress-strain curves of the joint materials at different temperatures are not available.

**Table 6.2** Thermal cycling test results of die-attach studies using sintered nano-Ag paste and Ag-In system.

<table>
<thead>
<tr>
<th>Chip material/size (mm²)</th>
<th>Substrate material</th>
<th>Joint material/ thickness(μm)</th>
<th>Bonding pressure (MPa)</th>
<th>Bonding temperature (°C)</th>
<th>Bonding time (second)</th>
<th>Thermal cycling profile (°C)</th>
<th>No. of cycles to failure</th>
<th>Maximum shear strain without stress</th>
<th>Ref.</th>
</tr>
</thead>
<tbody>
<tr>
<td>Si/ 7.8×7.8</td>
<td>Cu</td>
<td>Nano-Ag paste/37.5</td>
<td>5</td>
<td>275</td>
<td>5</td>
<td>a. 245 b. 99</td>
<td>0.46</td>
<td></td>
<td>[11]</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>5</td>
<td>225</td>
<td>60</td>
<td>a. 351 b. 87</td>
<td>0.37</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>5</td>
<td>300</td>
<td>60</td>
<td>a. 984 b. 646</td>
<td>0.51</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>5</td>
<td>275</td>
<td>60</td>
<td>a. 790 b. 105</td>
<td>0.46</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>10</td>
<td>275</td>
<td>60</td>
<td>a. 716 b. 448</td>
<td>0.46</td>
<td></td>
<td></td>
</tr>
<tr>
<td>SiC/ 1.71×1.38</td>
<td>Al₂O₃ DBC with Ag coated</td>
<td>Nano-Ag paste/25</td>
<td>No extra pressure</td>
<td>300</td>
<td>2,400</td>
<td>50–250³</td>
<td>4,000</td>
<td>0.028</td>
<td>[20]</td>
</tr>
<tr>
<td></td>
<td>AlN DBC with Ag coated</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0.0012</td>
<td></td>
</tr>
<tr>
<td>Si/ 5×5</td>
<td>Cu</td>
<td>Electroplated Ag-In/38</td>
<td>1.4</td>
<td>180¹</td>
<td>300–480</td>
<td>-40–200⁴</td>
<td>exceeding 5,000</td>
<td>0.21</td>
<td>This work</td>
</tr>
</tbody>
</table>

¹ After bonding, the samples are annealed at 250 °C for 190 hours.
² Failure criterion and failure probability: delamination more than 20% of the initial contact area and 63%.
³ Failure criterion: 50% drop in average bonding strength.
⁴ Failure criterion and failure probability: breakage at 5 kg force and 30%.
⁵ Values calculated using Eq. 1, where $T_1$ is room temperature and $T_2$ is the sintering (bonding) temperature.
The number of cycles to failure, $N_f$, is specified at a failure probability of $1 - 1/e = 0.63$ by the first group [11]. Among all different sintering and thermal cycling conditions reported by the first group [11], the highest $N_f$ achieved is 984, as shown in Table 6.2. The sample geometry results in high $\gamma$ values (Eq. 1) because of large CTE mismatch, large chip size, and relatively thin joint. The number of cycles to failure reported by the second group is 4,000 cycles [20]. The failure probability at 4,000 cycles was not mentioned. The sample geometry results in very small $\gamma$ value due to small CTE mismatch and small chip size. For our design, the $\gamma$ value is 0.21, a typical value of lead-free solder joints. Seven of ten samples survived beyond 5,000 cycles. The thermal cycling test stopped at 5,000 cycles because we believed that 5,000 cycles are good enough. Three samples broke at 850th, 2,600th and 3,000th cycles, respectively. The early failure was probably caused by imperfections and defects in the joints.

6.4 Summary

Our previous work has demonstrated that Ag-In joints in the alloy structure of micron-size intermetallic compound grains embedded in solid solution phase (Ag) can achieve not only high shear strength but also high solidus temperature beyond 800 °C [14]. The question raised by many is: “Can these Ag-In alloy joints survive harsh thermal cycling (TC) environment?” This research was performed in response to this question. The samples were fabricated by fluxless bonding between Si chips and Cu substrates at 180 °C and 200 psi pressure. The resulting joint structure is $\text{Ag}/(\text{Ag})/\text{Ag}_2\text{In}/(\text{Ag})/\text{Ag}$, where (Ag) is the solid solution phase. The samples were annealed at 250 °C for 190 hours to enhance joint ductility and strength. The joint structure turned into an alloy of (Ag) with small ($\zeta$) and Ag$_2$In grains. Please note that in production design, the effects of the annealing process at 250 °C for 8 days should be considered, including
increase in manufacturing time and the reliability of the IC chips and interconnect. Initial screening TC test from -40 to +85 °C for 100 cycles was conducted. All ten samples survived. They were then subjected to a second TC test from -40 to +200 °C for 5,000 cycles. The test stopped at 5,000 cycles because we believed that 5,000 cycles are adequate. Seven of the ten samples survived after 5,000 cycles. This TC test result shows that the Ag-In alloy joints possess three basic characteristics that high temperature electronics has been looking for: (a) high solidus temperature - beyond 800 °C, (b) high strength - 178 kg minimum breaking force on 10 mm × 11 mm Cu chip, and (c) high thermal cycling life - 5,000 cycles between -40 to +200 °C.

Acknowledgements

The authors greatly appreciated the support and encouragement from II-VI Foundation.
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and Measurement Conference, Nürnberg Exhibition Centre, Germany, May 2013, pp. 242-247.


Chapter 7

Solid State Bonding of Silicon Chips to Patterning Silver Joints on Copper Substrates

7.1 Introduction

Due to the size of electronic devices becoming smaller; the heat transfer surface area is also decreasing. They generate high heat flux and result in larger temperature rises [1]. Therefore, for electronic packaging, a high temperature die attachment material is needed. A common die attachment material is lead free solder [2]; however, the eutectic temperature of lead free solder is only 221 °C [3]. Even though the Au-Sn eutectic solder that is used in high power laser and microwave device, the eutectic temperature is 280 °C. Only sintered nano-silver paste can survive in high temperature environment [4-5]. Nevertheless, the cost and long sintering time are concerned for sintered nano-silver paste [6]. Besides, in electronic devices, copper (Cu) electrodes or Cu substrates have been extensively used to mount on Si chips. Cu is chosen due to its unique properties of high-electrical and thermal conductivities to provide a thermal path and electrical path for devices [7]. The challenge of using Cu is its high CTE of $16.7 \times 10^{-6}/°C$, much higher than that of all metals, ranging from $2.7 \times 10^{-6}/°C$ for Si to $7 \times 10^{-6}/°C$ for gallium arsenide (GaAs). It has been a challenge to solder large semiconductor chips to Cu substrates.

Our group has successfully demonstrated solid-state bonding by using 50 µm Ag as bonding medium between Cu chips and substrates [8], where solder and flux were unnecessary. Ag is chosen as the bonding material because it has the highest electrical conductivity (63 ×
10^6/m·Ω) and highest thermal conductivity (429 W/m·K) among all metals. In this research, a new structural design in the Ag bonding layer is reported to reduce the bonding pressure in the solid-state bonding process. The structures bonded with the Ag solid-state process are expected to sustain high operating temperatures, constrained only by the 780 °C eutectic temperature of the Ag-Cu binary system. In what follows, bonding mechanism, experiment designs and procedures are first presented. Experimental results are reported and discussed, followed by summary.

7.2 Bonding Mechanism

Our fundamental concept of solid-state bonding refers to the situation when the spacing between A atoms and B atoms is brought within atomic distance so that they share electrons. As a result, bonding between material A and material B will occur. The ability of material A and material B to share outer electrons depends on their electronic configurations. The theory was seldom investigated and is beyond the scope of this paper. In this paper, the ability for Ag atoms and Cu atoms to share outer electrons is determined by experimental bonding results. Interdiffusion of materials A and B does not affect the bonding ability as far as the A atoms and B atoms continue to share electrons after interdiffusion. According to the solid-state quantum bonding theory [9], the distance between two atoms needed for sharing electron is 1 nm or less. Therefore, the bonding materials need to be deformed easily in order to achieve atomic contact between bonding objects.

7.3 Experimental Design and Procedures

In experiments, the solid-state bonding process of the Cu-Ag interface is performed at
300 °C with 1,000, 800 and 600 psi of applied pressure. The 300 °C bonding temperature makes the Ag layer deform more easily to conform to the Cu surface profile. Fig. 7.1 illustrates the process flow of photolithography and solid state bonding of Ag joint with cavities from Si chips to Cu substrates. The 10 mm × 12 mm Cu substrates are cut from a 0.8 mm thick Cu sheet having 99.9 % purity with mirror finish on one side. The Cu substrates are cleaned thoroughly by slightly polishing with 0.5 µm diamond suspension and rinsing with acetone and deionized water right before bonding to remove contaminations and oxides. To make Si chips, 2-inch Si wafers are deposited with 30 nm Cr and 100 nm Au thin films by E-beam evaporation in one high vacuum cycle, at 1×10⁻⁵ torr. The Cr serves as the adhesion layer and Au is the seed layer for electroplating. AZ P4620®, photoresist (PR) of 10 µm in thickness is coated uniformly on Si wafer with spin conditions 2000 rpm for 40 seconds. Using photolithographic process, array of 25 × 25 columns with 100 µm in diameter and 200 µm in pitch is produced on the Si wafer. After photolithographic process, the thickness of photoresist is measured by Dektak 3 Profilometer. The Si wafers are diced into 6 mm × 6 mm chips for electroplating and solid state bonding experiments.
Figure 7.1 Fabrication process flow of photolithography and solid state bonding for Ag joints with 100 μm cavities of Si chip bonded to Cu substrate.

Ag layer of 10 μm in thickness is electroplated on the Si chip with 100 μm diameter columns. The Ag plating bath is a cyanide-free, mild alkaline plating solution at pH of 10.5 containing 5-8 % potassium hydroxide (KOH) and 2-3 % silver oxide. The Ag plating is conducted with current density 13 mA/cm² at room temperature. The current, voltage, temperature, and time are monitored closely during the plating processes. The photoresist is removed by acetone at room temperature. Si wafers are ultrasonically cleaned in isopropyl alcohol (IPA) bath. The Cu substrates and Si chips are ready for bonding experiments.

To achieve solid-state bonding, the Si chip with Ag patterned layer is placed over the Cu substrate. They are held together by a fixture with static pressure of 1000 psi (6.9 MPa) to ensure intimate contact. The assembly is loaded on a graphite stage in a vacuum oven, which is then pumped to 0.1 torr [10]. The graphite stage is heated to 300 °C for 5 minutes. The heater is
then shut off and the assembly cools naturally in 50 millitorrs vacuum. It takes about 90 minutes to cool to room temperature. The purpose of vacuum environment is to suppress Cu oxidation. Several samples are cut in cross section along one complete row of Ag with cavities and polished. Scanning electron microscopy (SEM) and optical microscopy (OM) are used to study the morphologies and quality of the surface. Shear test is performed to measure the strength of Ag joints and evaluate the fracture modes.

7.4 Experimental Results and Discussion

Using photolithographic process, PR columns were fabricated on silicon chips. Ag was electroplated on the Si chip with PR columns and the photoresist was stripped. For each Si chip, an array of 25 × 25 cavities with diameter of 100 µm and pitch of 200 µm was obtained. Fig. 7.2(a) shows the OM image of photoresist columns with about 100 µm diameter on the Si chip after photolithographic process. The pitch of photoresist column is 200 µm shown in Fig. 7.2(b). A plated Ag with cavities sample was cut in cross section to display the cavity profile and the thickness of Ag layer shown in Fig. 7.3. The SEM image exhibits that the thickness of Ag layer is well controlled in range 10 to 11 µm. The cavity profile shows the larger diameter in the bottom, which helps the deformation of Ag layer during bonding process. The Si chip with patterned Ag layer was flipped over and bonded to Cu substrate by solid-state bonding at 300 °C for 5 minutes with 1,000 psi pressure in 0.1 torr vacuum. Neither underfill nor flux was used.
Figure 7.2 Optical microscopy images of photoresist columns having about 100 µm in diameter and 200 µm in pitch on Si chip: (a) 1000×, and (b) 200×.

Figure 7.3 Secondary electron images of cavity profile and thickness of Ag layer: (a) 650×, and (b) 2500×.

The samples were cut along one complete row, polished and examined under optical microscope and SEM. Fig. 7.4 displays the cross section OM images of a typical bonding sample. The sample is well bonded between Si chip and Cu substrate despite the significant mismatch in coefficient of thermal expansion (CTE) between Si and Cu. It also shows that the
Cu filled into cavities completely. In Fig. 7.5, the secondary electron (SE) SEM images exhibit that the bonding interface is sharp without voids or gaps. In order to provide more room for Ag flowing and avoid the Cu filling into cavities, the bonding pressure is reduced to 800 psi (5.5 MPa).

**Figure 7.4** Cross section OM images of bonding sample with 1,000 psi bonding pressure: (a) 500×, and (b) 1000×.

![Cross section OM images of bonding sample with 1,000 psi bonding pressure](image)

**Figure 7.5** Cross section SE SEM images of bonding sample shown in Fig. 7.4: (a) 500×, and (b) 5000×.

![Cross section SE SEM images of bonding sample](image)
Fig. 7.6 displays the cross section OM and SE SEM images of bonding result. It is clearly that cavities still filled by Cu completely. From SE SEM image in Fig 7.6(c), it shows that they are still bonded successfully with bonding pressure 800 psi. The bonding pressure was decreased continuously down to 600 psi (4.1 MPa). Fig. 7.7 is cross section OM and BSE SEM images of a typical bonding sample. From Fig. 7.7(a), it is obviously that cavities are empty without Cu. In SE SEM image, the Ag joints are well bonded between Si chip and Cu substrate without visible voids or gaps.
Despite the large CTE mismatch between Si and Cu, the joints or Si chips did not break and the bonding pressure decreases from 1,000 psi to 600 psi. This indicates that the Cr/Au adhesion composite on Si bonds well to Si on one site and to Ag on the other. A commonly used
indicator for evaluating possible breakage caused by CTE mismatch is the maximum shear strain without stress. It is related to the strain calculated assuming that both bonded objects are free to contract during cooling down. It is the maximum possible shear strain on the resulting joint and is given by [11],

$$\gamma = (\alpha_1 - \alpha_2)(T_2 - T_1)L/2h$$  \hspace{1cm} (1)$$

where $\alpha_1$ and $\alpha_2$ are the CTE of Si and Cu, respectively, $T_2$ is the joint solidifying temperature, $T_1$ is the room temperature, $L$ is diagonal length of Si chip, and $h$ is the joint thickness. For this sample, the maximum shear strain without stress is calculated to be 1.24. This is a relatively large value compared to typical solder joints [12]. Moreover, the samples did not break. To find out how strong it is, shear test was conducted.

Six bonding samples with bonding conditions 600 psi bonding pressure at 300 °C are fabricated for shear test. During the test, the sample was mounted on the stage. A tool wedge pushed on one 5 mm-wide edge of the Si chip of the sample at a constant speed of 350 µm/s. Fig. 7.8 presents the shear test results of six samples with sample pictures. There are two fracture modes. One is Si chip breakage, another one is joint fracture. For sample No. 1 and 2, the Si chips broke first, so the breaking forces are not real breaking forces. It indicates that the Ag joints are stronger than Si. For other four samples, Si chips were removed. The breaking forces are 3, 13, 14, and 26 kg, respectively. According to military standards MIL-STD-883H method 2019.8, a force higher than 5 kg is considered passing the die shear test. All samples pass the requirement specified in MIL-STD-883H standard (5 kg) except No. 3 sample. To find out the reason of weak breaking force, the test samples of No. 3 and No. 6 are examined which has lowest and highest breaking forces.
Figure 7.8 Force versus sample No. bar chart of six samples during shear test. The breakage force of each sample is indicated.

Fig. 7.9 presents the OM and SE SEM fracture surface of sample No. 3 on Cu and Si side. From OM image on Cu side, the fracture occurs inside Ag joint. It shows that the Ag joint is bonded well on Cu substrate. In Fig. 7.9(b), the Ag traces decrease from right to left hand side on the Cu substrate. It indicates that the bonded area is not uniform for sample No. 3. From Fig. 7.9(d), the diameter of cavity shrinks to 75 μm. This presents that some Ag deformed and flowed into the cavities. For sample No. 6, Fig. 7.10(a) and (b) exhibit that the Ag traces are more uniform than sample No. 3 and the fracture is inside Ag joint. Fig 7.10(d) shows the diameter of cavity, and also shrinks to 76 μm during bonding process.
Figure 7.9 OM and SE SEM images of fracture surface of sample No. 3 after shear test: (a) OM image on Cu side, (b) SE SEM image on Cu side, (c) low magnification SE SEM image on Si side, and (d) higher magnification SE SEM image on Si side.
Figure 7.10 OM and SE SEM images of fracture surface of sample No.6 after shear test: (a) OM image on Cu side, (b) SE SEM image on Cu side, (c) low magnification SE SEM image on Si side, and (d) higher magnification SE SEM image on Si side.

For both test samples, these traces are the Ag that remained bonded on the Cu chip after shear test. On these traces, the breakage occurs inside the Ag joint rather than on the Cu/Ag bonding interface. The percentage of Ag traces on the entire area was estimated using image processing software. It is about 7.5 % for sample No. 3 and 6.2 % for sample No. 6. Even though the percentage of bonding area of No. 3 sample is larger than No. 6 sample. However, No. 6 sample has larger breaking force based on the shear test result. It may due to uniform bonding of sample No. 6 that the bonding strengthened. This also indicates that only less 8 % of the entire bonding
interface is strongly bonded. If the entire interface is all bonded strongly, the shear strength and breaking force could be increased. The percentage of bonding area of sample No. 3 and No. 6 are shown in Fig. 7.11.

![Fig. 7.11 The Ag traces on the Cu substrate: (a) sample No. 3, and (b) sample No. 6. The percentage of bonded area is 7.5 % and 6.2 %, respectively.](image)

7.5 Summary

In this research, Ag joints with cavities were produced on the Si chips with Cr/Au coating layer and then bonded to the Cu substrates. The bonding process is a solid-state bonding performed at 300 °C with 1,000 psi (6.9 MPa) static pressure for 5 minutes in 0.1 torr vacuum. Due to cavities, the bonding pressure can be reduced to 600 psi (4.1 MPa). No molten phase and flux are involved. For this case, the advantage is extremely low processing temperatures, 300 °C and the low bonding pressure, 600 psi (4.1 MPa). The intention to fabricate Ag joints with cavities is creating room for materials to flow, reducing the flow distance, and increasing the bonding area. According to cross-section images, Ag joints are well bonded between Si chips and Cu substrates. The shear test results show that Ag joints are strongly bonded and pass the military standard MIL-STD-883H, except one sample. It eliminates a concern from the bonding
strength for practical applications. The bonding structure is expected to sustain high operating temperatures as the eutectic temperature of the Cu-Ag binary system is 780 °C. Compared to current die-attachment methods, this novel bonding process can be applied to high temperature electronic devices.

Acknowledgements

The authors thank II-VI Foundation for the financial support and encouragement on this research.
Reference Chapter 7


Chapter 8

10 μm Silver Flip-Chip Joints Made by 250 ºC Solid-State Bonding Process

8.1 Introduction

Due to the miniaturization of large-scale-integration of circuits on Si chip technology [1-3], Si chip technology is approaching the limit of Moore’s law. According to Moore’s law, the transistor doubles every two years, be more specific, the transistor what doubles every two years. For example you can say, “the technology of the transistor changes every two years.” For a chip of the same area, the number of transistors increases, as does the I/O pin count. The number of flip-chip joints per area increases too. This indicates that the joint size and the pitch of the flip-chip joints have to be scaled down. In today’s flip-chip technology, the diameter of joint is about 100 μm. According to the International Technology Road Map for Semiconductors (ITRS), by 2016, the interconnect pitch for consumer and mobile products is projected to be 150 and 100 μm, respectively, [4]. The corresponding flip-chip joint diameters will be 75 and 50 μm. Because of the join shrinkage, the shear strain will increase, which presents a challenge for engineers. For solder based flip-chip joints, during the soldering process, the joints go through a molten state, which limits the aspect ratio of height to diameter. As the size of the chip shrinks, the diameter and the height of the solder joints are also reduced. However, the intermetallic compound (IMC) layer thickness of the solder joint does not scale down with the solder joint. Since the IMC does not deform much compared to the solder, the shear strain of solder section increases [5]. This situation gets worse during aging as the IMC grows thicker.
As a solution to this problem, our group utilized an Ag flip-chip technology using solid-state bonding. In this process, no IMC is involved. This is in contrast to nearly all soldering processes used in electronic industries, where IMC formation is essential for achieving bonding between solder and contact pads [6]. The interface between the IMC and solder is shown to be a weak interface that tends to break first during thermal cycling and drop tests [7-8]. We have successfully demonstrated a 40 μm Ag flip-chip by solid-state bonding [9]. In this process, Ag interconnect joints are made between Si chips and Cu substrates at 250 °C without using any solder or flux. Cu is chosen because Cu electrodes or contact pads have been extensively used in Si electronic packages. Cu has a large CTE mismatch with Si, \((16.7 \times 10^{-6}/°C \text{ versus } 2.7 \times 10^{-6}/°C)\), making bonding of Si to Cu a great challenge. Ag is chosen as the bonding material because it has the highest electrical conductivity \((63 \times 10^6/m\cdot\Omega)\) and highest thermal conductivity \((429 \text{ W/m·K})\) among all metals.

In what follows, we first report the experiment design and procedures. Experimental results are then presented and discussed, followed by a short summary.

### 8.2 Experiment Design and Procedure

In experiments, the solid-state bonding process of the Cu/Ag flip-chip interconnect is performed at 250 °C with 800 psi (5.5 MPa) of applied pressure. The 250 °C bonding temperature makes the Ag columns deform more easily to conform to the Cu surface profile. Fig. 8.1 illustrates the process flow of Si chips with a 10 μm Ag flip-chip interconnect bonding to Cu substrates by photolithography and solid-state bonding process. To make Si chips, 2-inch Si wafers are deposited with 30 nm Cr and 100 nm Au thin films by E-beam evaporation in one high vacuum cycle \((1\times10^{-5}\ \text{torr})\). The Cr is the adhesion layer and Au protects Cr from oxidation.
as well as serving as a seed layer for electroplating. AZ P4620®, photoresist (PR) of 10 μm in thickness is coated uniformly on a Si wafer with spin conditions 2,000 rpm for 40 seconds. Using a photolithographic process, 50 × 50 cavities of 10 μm in diameter and 20 μm in pitch were produced on one square. A Total of 13 squares are on a Si chip. An O₂ plasma cleaning process was applied to remove photoresist residue on the bottom of the cavities. After photolithographic process, the thickness of photoresist is measured by Dektak 3 Profilometer.

![Diagram](image)

**Figure 8.1** The process flow of Si chips with 10 μm Ag flip-chip interconnects bond to Cu substrate: (a) Si metallization, and photoresist coating, (b) soft baking and ultraviolet light exposure, (c) developing and hard baking, (d) Ag plating, (e) photoresist removal, (f) solid-state bonding.

Ag of 10 μm thickness was electroplated in the cavities. The Ag plating bath is a cyanide-free, mild alkaline plating solution at pH of 10.5 containing 5-8 % potassium hydroxide (KOH) and 2-3 % silver oxide. The Ag plating is conducted with current density 13 mA/cm² at room temperature. The current, voltage, temperature, and time are monitored closely during the plating
processes. After Ag plating, the photoresist was removed by acetone. Si wafers are ultrasonically cleaned in isopropyl alcohol (IPA) bath. The wafers are diced into 6 mm × 6 mm chips for the bonding experiment. The 10 mm × 12 mm Cu substrates are cut from a 0.8 mm thick Cu sheet having 99.9% purity with mirror finish on one side. The Cu substrates are cleaned thoroughly by slightly polishing with 0.5 μm diamond suspension and rinsing with acetone and deionized water right before bonding to remove contaminations and oxides. The Si chips and Cu substrates are then ready for bonding experiments.

To achieve solid-state bonding, the Si chip with Ag columns is placed over the Cu substrate. They are held together by a fixture with pressure of 800 psi (5.5 MPa). The assembly is loaded on a graphite stage in a vacuum oven, which is then pumped to 0.1 torr [10]. The graphite stage is heated to 250 °C for 5 minutes. The heater is then shut off and the assembly cools naturally in 50 millitorrs vacuum. No underfill and no flux are used. The purpose of a vacuum environment is to suppress Cu oxidation. Several samples are cut in a cross section along one complete row of Ag joints and polished. Scanning electron microscopy (SEM), energy-dispersive X-ray spectroscopy (EDX) and Optical microscopy (OM) are then used to study the morphologies and quality of the surface.

8.3 Experimental Results and Discussion

Following the procedures mentioned above, 50 × 50 cavities 10 μm in diameter and 20 μm in depth were fabricated in photoresist on Si chips coated with thin Cr and Au layers. Ag 10 μm in thickness was plated in the cavities. After Ag plating, the photoresist was removed by acetone, resulting in a Si chip with 50 × 50 Ag columns on one square. Fig. 8.2 shows the optical image and secondary electron (SE) images at 45° angle of the Ag (10 μm) columns with diameter
of 10 µm and pitch of 20 µm on Si/Cr/Au chip at (a) OM image 1000×; SE images: (b) 100x, (c) 2,000x, and (d) 5,000x. It is observed that the Ag columns are well produced. The roughness of top surfaces of the columns is less than 0.5 µm, and the sidewalls of columns are well defined. The Si chip with Ag columns was flipped over and bonded to Cu substrate by solid-state bonding at 250 °C for 5 minutes with 800 psi (5.5 MPa) pressure in 0.1 torr vacuum. The corresponding force is only 0.044 gm per column. Neither underfill nor flux was used.

**Figure 8.2** Optical image (OM) and secondary electron images at 45° of array of Ag (10 µm) columns having 10 µm in diameter and 20 µm in pitch on Si chip with Cr and Au layers at: (a) OM image 1,000×, (b) 100x, (c) 2,000x, and (d) 5,000x.
The bonded samples were then cut and polished to expose a row of Ag columns for SEM cross section observation. Fig. 8.3 shows cross-section backscattered electron (BSE) and SE images of 10 µm Ag flip-chip joints made between Si/Cr(30 nm)/Au(100 nm) and a Cu substrate. Fig. 8.3(a) is a low magnification image showing five columns in a row, (b) and (c) are high magnification images showing one joint. It is seen that the height of Ag interconnect is compressed by 10 %. Due to its ductility, the Cu substrate is also compressed down to 2 µm. These deformations occurred during bonding at 250 °C when the materials are more ductile. The ductility of Ag and Cu facilitate the intimate contact of Ag and Cu atoms at the interface during bonding process. Fig. 8.3(c) displays the bonding interface which shows that the Ag interconnect is well bonded to Cu without cracks. Some voids are shown inside the bonding interface due to uneven surface of Ag column. EDX quantitative analysis was applied at 4 locations near the bonding interface as exhibited in Fig. 8.4. Table 8.1 shows the EDX data. At locations 2 and 3 which are inside the Ag joint, Cu is detected. At locations 4 and 5 which are inside the Cu substrate, no Ag is detected. This implies that during the bonding process, Cu atoms diffused into Ag but Ag atoms did not diffuse into Cu. This is likely caused by small Ag grain size which facilitates grain boundary diffusion even at 250 °C.

On the bonding interface, both the surface of Ag column and the surface of the Cu substrate deformed to achieve atomic contact so that Ag atoms and Cu atoms share their conduction electrons. This is the fundamental requirement for solid-state atomic bonding. When the spacing between A atoms and B atoms is brought within atomic distance so that they can share electrons, bonding between material A and material B will occur. The ability of material A and material B to share electrons depends on their electronic configurations. In this project, the ability for Ag atoms and Cu atoms to share electrons is determined by experimental bonding.
results. Interdiffusion does not decrease the bonding ability as long as A atoms and B atoms share electrons after the interdiffusion [11].

Figure 8.3 Cross-section SE and BSE images of 10 µm Ag flip-chip joints made between Si chip with Cr (30 nm) and Au (100 nm) and Cu substrate by solid-state bonding at 250 °C with static pressure of 800 psi (0.044 gm per column): (a) low magnification image, and (b) and (c) high magnification image showing one joint.
Stress management of a Si flip-chip interconnect is necessary to prevent joint or chip fracture. The bonded structures have to sustain stresses induced by CTE mismatch between the Si chip and Cu substrate. A commonly used indicator for evaluating the survival of a bonded structure is the maximum stress-free shear strain. It is the strain calculated assuming that both bonded objects are free to contract during cooling down period. It is the maximum possible shear strain on the resulting joint and is given by [12],

\[ \gamma = (\alpha_1 - \alpha_2)(T_2 - T_1)L/2h \]  

(1)

where \( \alpha_1 \) and \( \alpha_2 \) are the CTE of Si and Cu, respectively, \( T_2 \) is the bonding temperature, \( T_1 \) is the room temperature, \( L \) is the diagonal of the bonded area, and \( h \) is the bonding layer thickness. The

**Figure 8.4** Cross-section BSE image at EDX analysis location.

**Table 8.1** EDX data at the five locations indicated in Fig. 8.4.

<table>
<thead>
<tr>
<th></th>
<th>Cu (at. %)</th>
<th>Ag (at. %)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0</td>
<td>100.0</td>
</tr>
<tr>
<td>2</td>
<td>4.0</td>
<td>96.0</td>
</tr>
<tr>
<td>3</td>
<td>11.6</td>
<td>88.4</td>
</tr>
<tr>
<td>4</td>
<td>100.0</td>
<td>0</td>
</tr>
<tr>
<td>5</td>
<td>100.0</td>
<td>0</td>
</tr>
</tbody>
</table>
CTE of Si and Cu is $2.7 \times 10^{-6}/^\circ\text{C}$ and $16.7 \times 10^{-6}/^\circ\text{C}$, respectively, and the bonding temperature is 250 °C. From Fig. 8.3(b) the thickness of Ag joint is 9.8 µm. The maximum stress-free shear strain is calculated to be 1.36. Despite the large CTE mismatch between Si and Cu, and the significant shear strain, the joints or Si chips did not break. To find out how strong it is, a pull test is conducted to examine the bonding strength.

A Pull test portrayed in Fig. 8.5 was performed on bonded samples. The test sample is mounted on the optical table and the force direction is vertical to test sample. Results of two samples, A and B, are reported in Table 8.2, including breaking force and fracture modes. There are two fracture modes: mode I is breakage near the Au-Ag interface, and mode II is breakage near the Ag-Cu interface. For both samples, the Si chips were pulled away completely. For clarity, a sketch was prepared to illustrate these fracture modes (Fig. 8.6). The breaking forces are 3.4 and 3.2 kg, which convert to 12.9 and 15.1 MPa, respectively. According to MIL-STD-883H method 2031.1, any flip-chip pull which results in separation under an applied stress less than 500 kg/in$^2$ × average solder bump area (in$^2$) × number of solder bumps shall constitute a failure. This translates to 1.98 and 1.67 kg of fracture force for our samples. The breaking force of our samples is almost 1.5 times of the military requirement.
Table 8.2 Breaking forces, strengths, applied stresses and fracture modes of two samples.

<table>
<thead>
<tr>
<th></th>
<th>Breaking force kg (columns)</th>
<th>Breaking strength MPa (psi)</th>
<th>Applied stress kg/in² (Failure criteria)</th>
<th>Fracture Modes on Cu side</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>3.4 (32500)</td>
<td>12.9 (1871)</td>
<td>846 (500)</td>
<td>Mode I: breakage near the Cr/Au–Ag interface</td>
</tr>
<tr>
<td>B</td>
<td>3.2 (27500)</td>
<td>15.1 (2190)</td>
<td>964 (500)</td>
<td>Mode II: breakage near the Ag–Cu interface</td>
</tr>
</tbody>
</table>
To evaluate the fracture modes, the samples were examined by SEM and EDX analysis. Fig. 8.7 shows the top view of OM and SE SEM images of fracture surface of sample A. Fig. 8.7(a) and (b) are OM images on Si and Cu side, respectively. Fig. 8.7(c) and (d) present SE SEM images of the fractures on the Si side and the Cu side. Fig. 8.7(c) shows three Ag columns remaining on a Si chip and one circular mark. It presents the mixed fracture modes for sample A. Based on the EDX, the breakage interface nears Au of the Cr/Au layer and the Ag column, designated as mode I. This is the electroplating interface when the Ag columns were plated on the Si chip coated with Cr/Au. The breakage interface between the Ag column and the Cu substrate is designated as mode II, which also happens to be the bonding interface. Sample B has the same fracture modes as sample A. Fig. 8.8 exhibits the 45° view SE SEM images on Cu side of sample A after pull test. Of interest to observe is that the columns are tilted in right and left edge. It is seen that the joint was deformed due to CTE mismatch between Si chip and Cu substrate. When temperature decreased from the bonding temperature to room temperature, the
Cu substrate shrank more than Si chip. Therefore, the ductile Ag joints deformed.

**Figure 8.7** OM and SE SEM images of sample A of Si chip bonded to Cu substrate using flip-chip Ag joints after pull test: (a) and (b) 1000×, (c) SE SEM images on Cu side, and (d) SE SEM images on Si side; fracture modes are breakage between electroplating interface of Cr/Ag and Ag column and solid-state bonding interface of Ag column and Cu substrate.
Figure 8.8 SE SEM images of 45° view of sample A after pull test: (a) left edge, (b) center position, and (c) right edge. The Ag columns are tilted in left and right edge.

8.4 Summary

In this research, we demonstrated 10 μm Ag flip-chip interconnect joints between Si chips and Cu substrates by solid state atomic bonding. After photolithography, an array of 50 × 50 × 13 cavities 10 μm in diameter, 20 μm pitch and 10 μm depth were fabricated on one chip region of the photoresist coated on Si wafers that were first metalized with 30 nm Cr and 100 nm Au. A 10 um layer of Ag was electroplated into the cavities. After stripping the photoresist, 50
× 50 × 13 Ag columns were obtained on each chip region. The Si wafers were diced into 6 mm × 6 mm chips. The chips were bonded to Cu substrates, which are emulated as Cu electrodes or pads on package substrate. The bonding condition of solid state bonding is 250 °C with a static pressure of 800 psi (5.5 MPa) for 5 minutes in a 0.1 torr vacuum. The corresponding load for each column was only 0.044 gm. Cross section SEM images of one row of joints show that the Ag flip-chip joints were bonded to the Cu substrate without breakage. In high magnification images, it was clearly observed that Ag joints deformed to match the surface profile of the Cu substrate to achieve intimate contact. Despite a significant CTE mismatch between Si and Cu, the Si chips did not break. The pull test results show Ag joints are bonded to Cu substrate well and pass the MIL-STD-883H method 2031.1. The breaking forces are 3.4 and 3.2 kg, which correspond to breaking strengths of 12.9 and 15.1 MPa, respectively.

In this flip-chip interconnect process the bonding force can be reduced to 0.044gm per joint. No cracking or damage was observed on the Si chips after bonding. During the bonding process, no molten phase incurs. Neither flux nor undefill is used. All reliability issues associated with IMC and IMC growth in the solder-based flip-chip interconnect technology do not exist in the Ag flip-chip process reported. The only limitation of this flip-chip interconnect process is the size of Ag joints by the photolithographic processes.

Acknowledgements

The authors thank II-VI Foundation for the financial support and encouragement on this research and the lab mate Wen P. Lin to support the experiment.
Reference Chapter 8


Chapter 9

The Growth of Pure Silver and Silver-Indium Ingots and Their Stress-Strain Characterization at Room and Elevated Temperatures

9.1 Introduction

Silver (Ag) has been known since ancient times and was separated from lead (Pb) as early as 4,000 BC using surface mining [1]. In history, Ag has been used for ornaments, jewelry, utensils, and currency in the form of coins and bullion in many civilizations and monetary systems. In industries, Ag is used in electrical contacts, conductors, and mirror coatings. In electronics, Ag has been used to produce bond pads on copper (Cu) leadframes or substrates, coating on Cu wires, contacts on solar panels, and Ag epoxies. In electronic applications, Ag has superior physical properties; it has the highest electrical conductivity and thermal conductivity among all metals. Ag is also very ductile and malleable.

To apply the superior physical properties of Ag to electronic packaging, we chose Ag as the bonding medium to attach Si chips to Cu substrates using solid-state bonding process [2]. The bonding process was performed at 250 °C with 1,000 psi of applied pressure which is an order of magnitude smaller than conventional thermocompression processes. The Ag solid-state bonding process was applied to flip-chip interconnects between Si chips and Cu substrates with a pitch of 500 µm and joint diameter of 250 µm [3]. Recently, the flip-chip joint size was shrunk down to 10 µm [4]. In these bonded structures, stresses develop due to mismatch of coefficient of thermal expansion (CTE) between the chip and the substrate. Before setting the bonding
experiment, it is necessary to know the stress vs. strain curves of Ag at room and elevated temperatures in order to estimate the stresses. We carried out an extensive literature search and could only find a few curves at room temperatures [5-7]. The data found deviates a great deal from each other. No curves were found at elevated temperatures.

Accordingly, we set out to measure the stress vs. strain curves of Ag at room and elevated temperatures. In addition, the stress vs. strain of silver solid solution with 20 at. % In (\((Ag)-In20\)) is also measured to gain mechanical properties of resulting joint of silver-indium system. To obtain consistent Ag and (Ag) qualities, we decided to grow our own Ag and (Ag) ingots and produce tensile test samples. In what follow, experimental design and procedures are presented. Experimental results are reported and discussed, followed by summary.

9.2 Experimental Design and Procedures

The ingot growth process reported in the literature [8] was studied and evaluated. American Society for Testing and Materials (ASTM) tensile test sample geometries were examined [9] and a specific Ag tensile test sample was chosen, as shown in Fig. 9.1. Based on this sample geometry, ingot size of 9.5 mm in diameter by 60 mm in length was selected. To grow this ingot size, quartz tube of inner diameter of 10 mm and outer diameter of 12 mm was used. For Ag ingot, 99.99 % purity Ag shots with 3-5 mm diameter were loaded into a quartz tube with one end closed. The open end of the tube is pumped by a vacuum pump and sealed by a hydrogen torch to form a capsule. This procedure decreases the Ag and In oxidation and voids during the growth process. The capsules were loaded to a furnace set at 1,020 °C and kept there for 30 minutes to melt the Ag shots. Agitation of the capsules was applied to help release air bubbles trapped in the molten Ag. Afterwards, the capsules were cooled inside the furnace with a
prescribed profile from 1,020 °C to room temperature. Subsequently, the Ag ingots were removed from the furnace. Small discs were cut for X-ray diffraction (XRD) and energy dispersive X-ray spectroscopic (EDX) analyses. The same process was used to fabricate the (Ag)-In20 ingot. 99.99 % purity Ag with 3-5 mm diameter and 99.99 % indium (In) shots with 4-6 mm diameter are used. Before loading In shots, In shots need to be etched to remove oxide layer on the surface by HCl. Fig. 9.2 shows the In shot before and after etching process by HCl. When temperature increases to 157 °C, In shots melt first and In starts to reacts with Ag until temperature decreases to 800 °C. The bulk of the ingots were machined to the ASTM tensile test (TT) samples using electrical discharge machining (EDM). In Fig. 9.1, A is gauge length, B is length of grip section, C is width of grip section, W is width of gauge, L is overall length and T is thickness. Each TT sample was then polished and annealed at $T_h = 0.4$ for 30 minutes to reduce internal stresses, where $T_h$ is the homologous temperature and $T_h = 0.4$ corresponds to real temperature of 221 °C.

<table>
<thead>
<tr>
<th></th>
<th>W</th>
<th>T</th>
<th>L</th>
<th>A</th>
<th>B</th>
<th>C</th>
</tr>
</thead>
<tbody>
<tr>
<td>mm</td>
<td>2</td>
<td>1.1</td>
<td>33.33</td>
<td>10.67</td>
<td>10</td>
<td>3.33</td>
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<td>0.0433</td>
<td>1.3120</td>
<td>0.4200</td>
<td>0.3937</td>
<td>0.1311</td>
</tr>
</tbody>
</table>

**Figure 9.1** The geometry of ASTM tensile test specimen, not in scale.
Figure 9.2 The In shots after being etched by HCl etchant to remove oxide on the surface: (a) before etching, (a) after etching.

The TT sample was mounted on an Instron model 5500R tensile test machine to measure the stress vs. strain curve. The load-elongation data were registered by a computer. The TT samples were tested at three temperatures: room temperature, $T_h = 0.4$ and $T_h = 0.5$, respectively, with a strain rate of $10^{-4}$ mm/s. For testing at elevated temperatures, the sample was heated in a furnace with temperature measured by a chromel-alumel thermocouple held at a distance of 0.5 cm between sample gauge surface and the thermocouple. This thermocouple was calibrated to within ± 2 K of the recorded temperature. Before testing, the sample was kept at the preset temperature for 20 minutes for achieve temperature uniformity. To evaluate the quality of the ingots, scanning electron microscope (SEM) and optical microscope (OM) are employed to examine the compositions and microstructures of the samples.

9.3 Experimental Results and Discussion

9.3.1 Characterization of Ag and Ag-In Ingots
For Ag ingot, Fig. 9.3 displays the XRD peaks of a disc sample cut from a typical Ag ingot. There are five peaks and the major grain orientation is (111). From the X-ray diffraction angle of a specific plane, the lattice constant was calculated. The calculated values for (111), (200), (220), (311) and (222) are 4.09, 4.08, 4.09, 4.08 and 4.09 Å, respectively. These values are within +0.09/-0.15 % of the published datum based on the international center for diffraction data (card no. 00-004-078), indicating that all diffraction peaks come from the same Ag FCC lattice [10].

![XRD plot on a disc sample cut from a typical Ag ingot.](image)

**Figure 9.3** XRD plot on a disc sample cut from a typical Ag ingot.

To explore the microstructural grains, a polished rectangular sample was etched with NH₄OH and H₂O₂ etchant at room temperature. Fig. 9.4 exhibits the optical microscopy (OM) image and SEM image. The black spots in the OM image show the voids at grain boundaries. It is observed that the grain size ranges from 200 to 950 µm. In [5], grain size ranges from 1 to 64 µm. In that report, commercial purity silver (99.9 %) was obtained from Handy and Harman. It
was treated severely cold worked and annealed in air at temperatures from 100 to 900 °C for 0.5 hour to recrystallize the grain structure.

**Figure 9.4** The surface of an ingot sample after being etched by NH$_4$OH and H$_2$O$_2$ etchant to explore the microstructure (a) optical microscope image, (b) SEM image.

For (Ag)-In$_{20}$ ingots, XRD result also show that the (111) is major peak of the test sample, as shown in Fig.9.5. The same etchant was used to find out the microstructural grains of (Ag)-In$_{20}$. It is intersecting that the sample surface didn’t be etched. Fig. 9.6 shows the sample after etching at 60, 180 and 480 seconds at room temperature. No significant etched mark was observed. Later, other sample was etched with same etchant at 50 °C for 60, 180 seconds and 35 minutes. Only slight etched mark was found on the 35 minutes sample surface. The etching results were shown in Fig. 9.7. Based upon etching results, it seems like (Ag)-In$_{20}$ has better corrosion resistance than pure Ag.
**Figure 9.5** XRD plot on a disc sample cut from a typical (Ag)-In20 ingot.

**Figure 9.6** The surface of an (Ag)-In20 ingot sample after being etched by NH₄OH and H₂O₂ etchant at different time: 60, 180 and 480 seconds.
Figure 9.7 The surface of an (Ag)-In20 ingot sample after being etched by NH₄OH and H₂O₂ etchant at 50 °C, (a) after 60, 180 and 480 seconds, and (b) OM image of 35 minutes etched sample.

9.3.2 Tensile Test Results

Fig. 9.8 displays the true stress-strain curve of a typical Ag sample tested at room temperature. For this sample, the yield strength (YS) is 64 MPa, the ultimate tensile strength (UTS) is 166 MPa and the elongation is 0.49. Many more samples were tested and the results are presented in Table 9.1. Of the samples tested at room temperature so far, the YS ranges from 51 to 106 MPa, UTS ranges from 138 to 201 MPa, and the elongation is from 0.27 to 0.49. The YS and UTS results are comparable to published data but the elongation results are almost twice of published values [5-6, 11]. This indicates that the Ag ingots that we grew are significantly more ductile. Fig. 9.9 are two representative SEM images of a typical sample tested at room temperature, showing slip bands and dimples, respectively, on the fracture surface. These are indications that the sample fractured in ductile mode.

Figure 9.8 The true stress-strain curve of a typical sample tested at room temperature.
Several TT samples were then tested at 221 °C ($T_h = 0.4$) and 350 °C ($T_h = 0.5$), respectively. Fig. 9.10 exhibits the true stress-strain curves of two typical Ag samples. Tested results of all samples are included in Table 9.1. At 221 °C, the YS ranges from 51 to 87 MPa, UTS is from 72 to 124 MPa, and elongation ranges from 0.17 to 0.37. At 350 °C, the YS ranges from 26 to 41 MPa, UTS is from 46 to 64 MPa, and elongation is from 0.15 to 0.39. It is seen that, at higher temperatures, the Ag samples yield more easily and become significantly weaker. These samples, however, did not become more ductile as we initially expected. Fig. 9.11 displays three samples after tensile test at three different temperatures. Based on above measurement, the data show large deviations. It may due to the voids at grain boundaries of test samples to affect the result of tensile test.
Figure 9.10 The true stress-strain curves of Ag sample tested at (a) 221 °C ($T_h = 0.4$), and (b) 350 °C ($T_h = 0.5$).

Table 9.1 Tensile test results of silver samples tested at different temperatures.

<table>
<thead>
<tr>
<th>Temperature (°C)</th>
<th>True yield strength (MPa)</th>
<th>True tensile strength (MPa)</th>
<th>Elongation</th>
</tr>
</thead>
<tbody>
<tr>
<td>Room temperature</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>96</td>
<td>201</td>
<td>0.27</td>
</tr>
<tr>
<td></td>
<td>72</td>
<td>155</td>
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</tr>
<tr>
<td></td>
<td>64</td>
<td>166</td>
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</tr>
<tr>
<td></td>
<td>65</td>
<td>141</td>
<td>0.30</td>
</tr>
<tr>
<td></td>
<td>106</td>
<td>138</td>
<td>0.32</td>
</tr>
<tr>
<td></td>
<td>51</td>
<td>161</td>
<td>0.39</td>
</tr>
<tr>
<td>221 ($T_h = 0.4$)</td>
<td>87</td>
<td>124</td>
<td>0.22</td>
</tr>
<tr>
<td></td>
<td>62</td>
<td>72</td>
<td>0.29</td>
</tr>
<tr>
<td></td>
<td>51</td>
<td>92</td>
<td>0.36</td>
</tr>
<tr>
<td></td>
<td>61</td>
<td>79</td>
<td>0.17</td>
</tr>
<tr>
<td></td>
<td>71</td>
<td>98</td>
<td>0.24</td>
</tr>
<tr>
<td></td>
<td>59</td>
<td>116</td>
<td>0.37</td>
</tr>
<tr>
<td>350 ($T_h = 0.5$)</td>
<td>41</td>
<td>50</td>
<td>0.15</td>
</tr>
<tr>
<td></td>
<td>41</td>
<td>64</td>
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</tr>
<tr>
<td></td>
<td>26</td>
<td>46</td>
<td>0.35</td>
</tr>
</tbody>
</table>
Figure 9.11 The samples after tensile tests at: (a) room temperature, (b) 221 °C ($T_h = 0.4$), and (c) 350 °C ($T_h = 0.5$).

Fig.9.12 shows the true stress-strain curve of a typical (Ag)-In20 sample tested at room temperature. For this sample, the YS is 14 MPa, the UTS is 307 MPa and the elongation is 0.73. To compare with pure Ag tensile test result, the YS is much smaller, UTS and elongation are almost 1.5 times larger. The aforementioned indicates that (Ag)-In20 deforms more easily and is much stronger than pure Ag. From elevated temperature test data, the YS is 52 MPa and UTS is 282 MPa at 156 °C ($T_h = 0.4$) and YS is 43 MPa and UTS is 83 MPa at 265 °C ($T_h = 0.5$). The elongations are 0.57 and 0.17, respectively. Fig. 9.13 displays the true stress-strain curves of two samples tested at elevated temperature. Many more samples were tested and tested results of all samples of (Ag)-In20 are included in Table 9.2.
Figure 9.12 The true stress-strain curve of a typical (Ag)-In20 sample tested at room temperature.

Figure 9.13 The true stress-strain curves of (Ag)-In20 sample tested at (a) 156 °C ($T_h = 0.4$), and (b) 265 °C ($T_h = 0.5$).
Table 9.2 Tensile test results of (Ag)-In20 samples tested at different temperatures.

<table>
<thead>
<tr>
<th>Temperature (°C)</th>
<th>True yield strength (MPa)</th>
<th>True tensile strength (MPa)</th>
<th>Elongation</th>
</tr>
</thead>
<tbody>
<tr>
<td>Room temperature</td>
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<td>233</td>
<td>0.57</td>
</tr>
<tr>
<td></td>
<td>14</td>
<td>307</td>
<td>0.73</td>
</tr>
<tr>
<td>156 (T_h : 0.4)</td>
<td>41</td>
<td>220</td>
<td>0.50</td>
</tr>
<tr>
<td></td>
<td>52</td>
<td>282</td>
<td>0.57</td>
</tr>
<tr>
<td>265 (T_h : 0.5)</td>
<td>43</td>
<td>83</td>
<td>0.17</td>
</tr>
<tr>
<td></td>
<td>54</td>
<td>93</td>
<td>0.16</td>
</tr>
</tbody>
</table>

The stress-strain curves at three different temperatures show that the transition from elastic strain to plastic strain is sharper at lower temperature. During tensile test, dislocation mobility is the principal factor of brittleness in ductile materials. In elastic strain regime, atoms in the metallic crystal lattice move according to Hooke’s law. Once the stress applied goes beyond the elastic strain, plastic deformation begins where the bonds between atoms break and realigned. At a higher temperature, the atoms gain more energy from the environment, which helps the atoms break and reconnect more early. Accordingly, the transition from elastic to plastic strain is less distinct at a higher temperature. During plastic deformation at a high temperature, not only do dislocations move on the slip system, grain boundary sliding also occurs [12], which creates voids at the boundaries and decreases the strength of samples. Hence, the sample is weaker at higher at a higher temperature.

9.4 Summary

In this research, we first developed the processes of Ag ingots in quartz capsules. A typical ingot is 9.5 mm in diameter and 60 mm in length. A sample of disk shape was cut from
each ingot for SEM/EDX and XRD evaluations. The main ingots were machined into ASTM tensile test samples by EDM. Many Ag tensile test samples were tested at room temperature, 221 °C (T_h = 0.4), and 350 °C (T_h = 0.5), respectively, to obtain the stress-strain curves. The results were presented in Table 9.1. At room temperature, the YS and UTS are similar to reported values, but the elongation is about twice of reported value. At a higher temperature, the YS and UTS decrease but the elongation changes little. An etching process reveals the Ag grains and the size ranges from 200 to 950 µm. For (Ag)-In20 test sample, the YS is smaller than pure Ag test sample but UTS and elongation are 1.5 times of pure Ag sample. All results were presented in Table 9.2. In addition, to compare with pure Ag, (Ag)-In20 has relative high corrosion resistance. We hope that our work to understand the microstructure and stress-strain behavior of Ag and (Ag)-In20 is valuable to the electronic community and the industry as a whole.

Acknowledgements

The authors greatly appreciated the support and encouragement from II-VI Foundation. They also thank Professor Mohammed for generously letting us use the tensile test equipment in his laboratory.
Reference Chapter 9


Chapter 10

The Summary and Conclusion

In this dissertation, the reaction of Ag-In binary system was studied and its bonding applications were developed between thermal expansion mismatch materials. Solid-state bonding was used in flip-chip interconnect bonding applications. Besides, the mechanical properties of Ag-In system and pure Ag at elevated temperature were discussed. In order to produce high quality joints, ductile and high conductivity bonding media, such as Ag, and Ag-In, and proper metallization layers were utilized. The details of all the experimental results and evaluations are reported in previous chapters. Finally, the short summary and conclusion of all these results will be given in the next paragraphs.

10.1 Ag-In Reactions Summary

In electronic industries, popular die attachment material is lead free solder, such as Sn-3.5 Ag. The reflow temperature of lead free solder is typically 260 °C, a temperature needed in various industrial applications. To achieve this, our group has looked into Ag-In binary system. This system not only utilizes low process temperature, but also works under high operating temperature at joint. The silver-indium system has become important in electronic packaging applications. The In-3.5 % Ag eutectic alloy has been used for laser diode attachment since 1980. The Ag-rich alloys were less studied but have received significant attention recently for producing high temperature joints at low bonding temperature. In multilayer Ag-rich bonding structure design, typical bonding temperature is 180 °C and the process can be made entirely
fluxless. The solidus temperature of joints fabricated is higher than 695 °C. Despite success in several bonding processes, the chemical reactions of Ag and In at 180 °C were least investigated.

In this study, we performed systematic experiments to investigate these reactions. In experimental design, copper (Cu) substrates were electroplated with 40 µm Ag layer, followed by indium layers of 1, 3, 5, 10, and 15 µm, respectively. Thick Ag layer was chosen to prevent In from reacting with the Cu substrate. The samples were annealed at 180 °C in 0.1 torr vacuum for 5 minutes to emulate the bonding conditions. The microstructure and composition on the surface of the samples were evaluated using scanning electron microscopy (SEM) with energy dispersive X-ray spectroscopy (EDX) as well as X-ray diffraction. They were then cut in cross section, polished, and examined by SEM/EDX. The results show that, for samples with 1 µm thick In, the In layer converts to Ag$_2$In entirely after annealing. For samples with In thickness of 3 and 5 µm, AgIn$_2$, Ag$_2$In, and solid solution (Ag) all form after annealing. No indium was identified. For samples having 10 and 15 µm thick In, In covers almost over the entire sample surface after annealing. The effect of annealing Ag layer was investigated. After Ag plating, samples were annealed at 450 °C for 3 hours to grow Ag grains. This was followed by plating 10 µm In and annealing at 180 °C. The result shows that, by annealing Ag before plating In, more In is kept in the structure during annealing at 180 °C. In theory, this effect is caused by larger Ag grains and thus fewer grain boundaries resulting from annealing the Ag layer. Based on above results, for those designs with In thinner than 5 µm, the Ag layer needs to be annealed, such as 450 °C for 3 hours, prior to In plating in order to make a successful bonding. Other than scientific values, the results of this investigation are useful in designing better bonding structures.

10.2 Ag-In Joints Summary
A fluxless bonding process was developed between silicon chips and aluminum substrates using Ag-In binary system. Results indicate that the Ag-In system can manage the large mismatch between the coefficient of thermal expansion (CTE) of Si chips ($2.7 \times 10^{-6}/°C$) and Al substrates ($23 \times 10^{-6}/°C$). The bonding structures are Si/Cr/Au/Ag and Al/Cr/Cu/Ag/In/Ag. Cross-section SEM images exhibit nearly perfect joints between the Si chips and Al substrates. Energy dispersive X-ray analysis shows that the joint consists of Ag/(Ag)/Ag$_2$In/(Ag)/Ag, where (Ag) is a solid solution phase. Based on Ag-In phase diagram, the joint can achieve a solidus temperature of 600 °C at least, even though the bonding is performed at 180 °C. Six samples are shear tested. The shear strengths obtained far exceed the requirement specified in MIL-STD-883H standards. Among four tested samples, Si chips broke first. The breaking forces are not real breaking forces for joint. Other two tested samples, the joint fractured. The breaking forces are 93.7 and 75.2 kg, respectively. Corresponding to breaking strength are 36.8 and 29.5 MPa. Al is not considered as a favorable substrate material because it is not solderable and has a high CTE. The new method presented in this thesis seems to have surmounted these two challenges.

In order to increase the Ag-In binary system bonding strength, the annealed process is used to convert the joints into Ag solid solution (Ag). Two copper (Cu) substrates were bonded using silver (Ag) and indium (In) at 180 °C and annealed at 200-250 °C to convert the joints into the solid solution (Ag) for enhanced strength and ductility. Cu-Cu pair was chosen so that the samples break in the joint during shear test. The upper Cu was electroplated with 15 µm Ag layer. The lower Cu was plated with 15 µm Ag layer, followed by In and 0.1 µm Ag to inhibit indium oxidation. Two designs were implemented, using 8 µm and 5 µm In, respectively. The Cu substrates were bonded at 180 °C in 0.1 torr vacuum without flux. Afterwards, samples were
annealed at 200 °C for 1,000 hours (first design) and at 250 °C for 350 hours (second design), respectively. Scanning electron microscope with energy dispersive X-ray analysis (SEM and EDX) results indicate that the joint of the first design is an alloy of mostly (Ag) with micron-size Ag$_2$In and ($\zeta$) regions, and that of second design has converted to a single (Ag) phase. Shear test results show that the samples are very strong. For our first design, the breaking force ranges from 178 kg to 200 kg. The shear tester could not break two of the six samples. In our second design, the breaking force ranges from 61 to 165 kg. These results far exceed the 5 kg requirement in military standards MIL-STD-883H method 2019.8. Fracture incurs inside the joint and is a mix of brittle and ductile modes or only ductile mode. The joint solidus temperatures are 600 °C and 800 °C for the first and second designs, respectively. The research results have shown that high-strength and high temperature joints can be manufactured using fluxless low temperature processes with the Ag-In system and are valuable in developing high temperature packages.

We have recently developed fluxless processes to produce high temperature and high-strength Ag-In joints at 180 °C bonding temperature. The joint solidus temperature is higher than 600 °C. Subsequent annealing steps improve the joint ductility and increase the solidus temperature beyond 800 °C. For real applications, a serious concern is the long-term reliability of the joints under thermal stress caused by mismatch of thermal expansion coefficient (CTE) between the chip and the package. Therefore, the reliability of Ag-In joints in thermal cycling (TC) environment is assessed. Si chips and Cu substrates were bonded using silver (Ag) and indium (In) multilayer structure without applying any flux. After bonding, the samples were annealed in air at 250 °C for 190 hours to convert the joint into an alloy of small intermetallic grains and solid solution (Ag). The resulting joint has a solidus temperature higher than 800 °C. Si-Cu pair was chosen because of the large coefficient of thermal expansion mismatch, i.e., 2.7 ×
10⁻⁶/°C of Si versus 16.7 × 10⁻⁶/°C of Cu. Two TC tests were performed. All 10 samples passed 100 cycles of initial TC test between -40 °C and 85 °C. They were then subjected to 5,000 cycles of TC test between -40 °C and 200 °C. Seven of ten samples survived beyond 5,000 cycles. Three samples broke at 850th, 2,600th, and 3,000th cycles, respectively. The early failure was probably caused by imperfections and defects in the joints. Based upon these results, it seems that our Ag-In joints compare favorably with sintered silver joints. The Ag-In joints not only have high melting temperature but also can survive harsh TC environment.

10.3 Patterning Ag Joints Summary

Due to the miniaturization of electronic devices; the heat transfer surface is also reduced. It creates high heat flux and results in larger temperature rises. A high melting temperature die attachment is needed to be used in these electronic devices. Besides, copper (Cu) electrodes or Cu substrates have been extensively used to mount on Si chips in electronic industries. The challenge of Si-Cu structure is their CTE mismatch. Cu is 16.7 × 10⁻⁶/°C, much higher than that of all semiconductors, ranging from 2.7 × 10⁻⁶/°C for Si to 7 × 10⁻⁶/°C for gallium arsenide (GaAs). To accomplish this, pure Ag joints used as a bonding medium between Cu substrates. Ag is chosen as the bonding material because it has the highest electrical conductivity (63 × 10⁶/m·Ω) and highest thermal conductivity (429 W/m·K) among all metals.

In this research, a new structural design in the Ag bonding layer is reported to reduce the bonding pressure in the solid-state bonding process. 10 µm Ag layer with cavities were produced on the Si chips with Cr/Au coating layer and then bonded to the Cu substrates at 300 °C with 1,000 psi (6.9 MPa) static pressure for 5 minutes in 0.1 torr vacuum. Due to cavities, the bonding pressure can be decreased to 600 psi (4.1 MPa). No underfill and flux are needed. During
bonding process, no molten phase is involved. For this case, the advantage is extremely low processing temperatures and the low bonding pressure. The intention to fabricate Ag joints with cavities is creating room for materials to flow, reducing the flow distance, and increasing the bonding area. According to cross-section images, Ag joints are well bonded between Si chips and Cu substrates. The shear test results show Ag joints are strongly bonded and pass the military standard MIL-STD-883H, except one sample. It eliminates a concern from the bonding strength for practical applications. The bonding structure is expected to sustain high operating temperatures as the eutectic temperature of the Cu-Ag binary system is 780 °C. This novel bonding process can be applied to high temperature electronic devices.

10.4 Flip Chip Joints Summary

In the scaled down trend on the gate length of CMOS transistors, the flip-chip joints have to shrink to cope with the increasing number of I/O pins per unit area. According to the International Technology Road Map for Semiconductors (ITRS), the pitches of flip-chip joints for low-end consumer and mobile products by 2016 are projected to be 150 and 100 μm, respectively. The corresponding joint diameters are 75 and 50 μm, respectively. Presently, almost all flip-chip joints are made of Sn-based Pb-free solders composed of Sn with a small percentage of Ag and/or Cu. As the solder joint shrinks, reliability issues and manufacturing difficulties emerge. One of these difficulties is elevated shear strain due to the increase of the intermetallic compound (IMC) layer ratio. Upon analyzing and understanding these problems, we looked into alternative material systems. In this thesis, Ag joint material and solid-state bonding to Cu substrate were studied with small pitch flip-chip designs. The Cu substrate is emulated as Cu electrodes or contact pads on the package substrate. The flip-chip
interconnect discussed in the following paragraphs were all produced on Si, which were first metalized with 30 nm of Cr and 100 nm of Au, by photolithography and electroplating processes.

We demonstrated that the Ag flip-chip interconnect process by using solid-state bonding at 250 °C. More specifically, the Si wafers were diced into 6 mm × 6 mm chips. Each Si chip has an array of 50 × 50 Ag flip-chip joints with 20 μm pitch and 10μm joint diameter on one square, total 13 squares on one Si chip. These Si chips were bonded to the Cu substrate at 250 °C with a static pressure 800 psi for 5 minutes in 0.1 torr vacuum. No flux or underfill is needed. Also no molten phase was involved. During bonding, the corresponding load for each column was set to only 0.044 gm. These cross section scanning electron microscope (SEM) images show that the entire row of Ag flip-chip joints exposed on the cross section were well bonded to the Cu substrate without cracks. In high magnification images, it was clearly observed that the Ag surface deformed to match with the surface profile of the Cu substrate to achieve an intimate contact. Despite a large mismatch in the CTE between Si and Cu, no joint breakage was observed. The ductile Ag joint well manage the stress induced by significant CTE mismatch between Si and Cu. Also, for the structure, the joint height is approximately 9.5 μm. The whole joint layer has a melting temperature at 962 °C. The operating temperature is 715 °C, which is calculated by homologues temperature of 80 %. Thus, high operating temperature device such as 200-450 °C is possible. To further evaluate this, a pull test was performed and fracture modes were analyzed. From the pull test, the breaking forces and breaking strengths obtained were 3.4 and 3.2 kg, and 12.9 and 15.1 MPa, respectively. The measured breaking force was 1.5 times larger than the MIL-STD-883E criterion of the pull- off test.
Our fundamental theory of solid-state bonding is that when the spacing between Ag atoms and Cu atoms is brought within an atomic distance so that they share electrons, bonding between Ag and Cu will occur. In our study, during the solid state bonding process, temperature and pressure were applied, and the bonding was done in a 0.1 torr vacuum. All of these conditions provide the chance for intimate contact between the two bonding materials, Cu and Ag. Also, the diffusion process may also occur in the bonding mechanism, although it is not required to achieve bonding.

Compared to the Sn-based Pb-free solder, there are several advantages to this solid-state Ag flip-chip bonding technology: high electrical and thermal conductivities, no IMCs and their related issues, a complete lack of flux, high ductility for managing CTE mismatch between chips and packages, high operation temperature, and possibility for a high aspect ratio of the interconnect.

10.5 Ag and Ag-In Ingots Summary

After conducting a thorough literature search, it was found that stress-strain curves of silver (Ag) are only available at room temperature. Of those published, the curves do not seem to relate to each other. In this research, we first developed the processes of Ag ingots in quartz capsules. A typical ingot is 9.5 mm in diameter and 60 mm in length. The main ingots were machined into ASTM tensile test samples by EDM. We measured the stress-strain curves of Ag at room temperature, at 221 °C (T_h = 0.4), and at 350 °C (T_h = 0.5), respectively, where T_h is the homologous temperature. Silver solid solution with 20 at. % In ((Ag)-In20) samples were also measured at room temperature, at 156 °C (T_h = 0.4), and at 265 °C (T_h = 0.5), respectively. To obtain consistent sample quality, we grew our own ingots and produced tensile test samples.
according to ASTM standards. Many samples from several growth runs were tested. For Ag ingot, at room temperature, the yield strength (YS) ranges from 51 to 106 MPa and ultimate tensile strength (UTS) is from 138 to 208 MPa which are comparable with the published data but the elongation (0.27 - 0.49) is about twice of the published value. At a higher temperature, the yield strength and ultimate tensile strength decrease but elongation varies little. Silver solid solution ((Ag)-In20) test samples have better results than pure Ag test sample. The YS is 14 MPa which is smaller than pure Ag test sample but UTS (308 MPa) and elongation (0.73) are 1.5 of pure Ag sample. Fracture surfaces and modes were examined and can be used to indicate that the sample is in ductile mode at room temperature. X-ray diffraction (XRD) was used to identify the preferred grain orientations. It shows that Ag and (Ag)-In20 have a major orientation on the (111) plane.

In this dissertation, these high electrical conductive interconnections along with the two fluxless bonding technologies, Ag-In binary system bonding and solid-state bonding provide new and alternative connection methods in electronic packaging industry. The joints formed by these bonding technologies have potentially high electrical and thermal conductivities, high ductility, high aspect ratio, and high operation temperature, which are valuable in particularly small size flip-chip applications and high temperature devices for long term operations.