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A 23:1 Bandwidth Ratio Quasi-lumped Component Balun on a Multilayer Organic Substrate

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Abstract: In this paper, we present the design and development of a novel ultra-wideband coupled line balun on a multilayer Liquid Crystal Polymer (LCP) substrate. The balun is designed using a quarter wavelength (λ/4) asymmetric broadside coupled line. The defected ground structure (DGS) and a lumped phase compensation circuit are developed to achieve wide bandwidth performance for the balun. The balun has a measured bandwidth ratio of 23:1, from 80 MHz to 1860 MHz. Within the operating bandwidth, the experimental results demonstrate that the balun achieves an input return loss of better than 10 dB, an insertion loss of better than 1 dB, an amplitude imbalance of better than ±0.4 dB and a phase imbalance of better than ±10 degrees. The size of the balun is 40.64 mm x 40.64 mm or 0.22 λg x 0.22 λg, where λg is the guided-wavelength at the center frequency of 970 MHz.

1. Introduction

In radio frequency (RF) and microwave circuits, a balun is a component which converts a single-ended signal to differential signals and vice versa. Thus, broadband baluns are extremely useful in many designs of balanced components. For examples, it is used in the design of a wideband quasi-yagi antenna [1]. Broadband baluns can also be utilized as power combiners to design wide bandwidth push-pull amplifiers [2, 3, 4], balanced mixers [5, 6, 7] and filters [8]. A Marchand balun [9] is one of the most common topologies for achieving wide bandwidth. Many wideband Marchand baluns have been reported in [10]-[18]. These baluns are based on two sections of λ/4 coupled transmission lines. Therefore, their size will be large at low frequencies. When the frequency moves away from the quarter wavelength, the bandwidth of the baluns depends mostly on the characteristic impedance of the two coupled line sections [19]. It is difficult to maintain high even-mode impedance over the bandwidth ratio of 10 to 1. Therefore, planar Marchand baluns typically have a bandwidth ratio of less than 10 to 1 [10-18]. The balun in [20] has a wide bandwidth from 1 MHz to 3 GHz, but it is designed using three ferrite cores that result in a large and bulky component. Coplanar waveguide (CPW) baluns [21,22] typically have a bandwidth ratio larger than 10 to 1. The grounds of CPW balun ports are not continuous and are not at the same potential as the common ground. It is difficult to insert CPW baluns into subsystem applications.

This paper presents the design of an ultra-wide bandwidth balun using only one λ/4-coupled line section and provides detailed analysis of the balun [23]. The coupled transmission line is configured in a broadside topology on a multilayer organic substrate to achieve large coupling. We have developed defected ground structures (DGS) and employed them in the balun to obtain high impedance on thin substrates. The coupled line is loaded with an LC circuit to achieve good phase and amplitude imbalance. The experimental results show that the balun achieves good performance over the bandwidth ratio of 23:1. Section II of this paper presents the analysis of the proposed design. In this section, the phase and amplitude imbalances are described, and the impedance transformation bandwidth of the balun is derived and discussed. Moreover, the criterion on how to design DGS and its effects on the balun are also analyzed in this section. The balun prototype and its measurement results are described in section III. Finally, the conclusion is presented in section IV.

2. Analysis of the proposed design

2.1. Balanced bandwidth of the balun

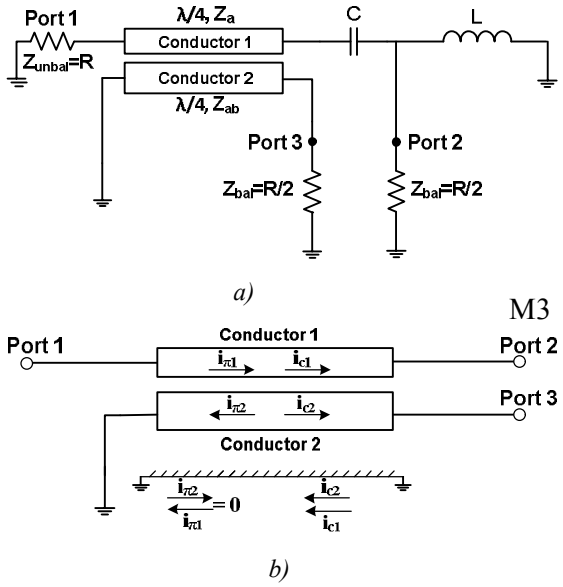
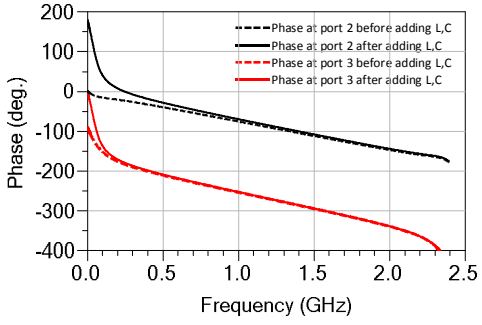


Fig.1*. (a)The schematic diagram of the proposed balun.(b) c- and pi-mode currents in the quarter wavelength (λ/4) broadside coupled line section*

Fig.1a shows the schematic diagram of the proposed balun. This balun is designed using a quarter-wavelength coupled line and a high pass lumped-component compensation network that helps to reduce the phase imbalance of the coupled line in the low frequency region. The broadside asymmetric coupled line consists of top conductor 1 separated by a 50 μm LCP layer from bottom conductor 2 and a ground plane below the two conductors. Fig.1b explains the flow of c- and pi-mode currents on this coupled line

section. In Fig.1b, i_{c1} and i_{c2} are the c-mode currents on conductors 1 and 2, whereas $i_{\pi 1}$ and $i_{\pi 2}$ are the pi-mode currents. In order to form a balun, one termination of conductor 2 is shorted to ground [24] and the currents flowing in the conductors 1 and 2 should be equal in amplitude and 180° out of phase. Therefore, $i_{\pi 1}$ should be equal and in an opposite direction to $i_{\pi 2}$ while i_{c1} and i_{c2} need to be minimized. The above conditions can be realized by designing this coupled line with very high equivalent c-mode characteristic impedance Z_c and appropriate equivalent pi-mode impedance Z_π [25], where Z_c and Z_π are, respectively, the average c-mode and pi-mode characteristic impedances of conductors 1 and 2 in Fig.1. In this case, the ground return currents for $i_{\pi 1}$ and $i_{\pi 2}$ are also anti-parallel and perfectly cancel with each other on the bottom ground plane. Hence, conductor 2 becomes a perfect ground for the conductor 1, since the current on conductor 1 is totally returned by the conductor 2. From [26, 27, 28], the equivalent c-mode characteristic impedance Z_c is large when the characteristic impedance Z_{ab} of conductor 2 with reference to the bottom ground rises. In this paper, we have developed a defected ground structure to increase impedance Z_{ab} to obtain the large equivalent c-mode impedance Z_c of the coupled line. While the DGS improves the amplitude and phase balances of the balun, at low frequency when the coupling becomes weak, the phase imbalance becomes significant.

Fig.2a shows the phase between ports 1 and 2 (Phase at port 2) and between ports 1 and 3 (Phase at port 3) of an asymmetric broadside coupled line constructed in Agilent Advanced Design Systems (ADS) [29]. Z_a, which is the characteristic impedance of conductor 1 with reference to conductor 2, is chosen to match with a 50 Ω unbalanced port and Z_{ab} is 200 Ω to achieve large equivalent c-mode characteristic impedance. The quarter wavelength frequency is set at 1.2 GHz and the terminations for unbalanced port 1 and balanced ports 2, 3 are 50 Ω and 25 Ω, respectively. We can observe from Fig.2a that the simulated phase difference of 180° between ports 2 and 3 of the asymmetric broadside coupled line is degrading rapidly at the lower edge of the frequency band. The phases at port 2 and port 3 at very low frequency (below 10MHz) are around 0° and -90°, respectively. Hence, the phase difference between the signals at these two ports is 90°.



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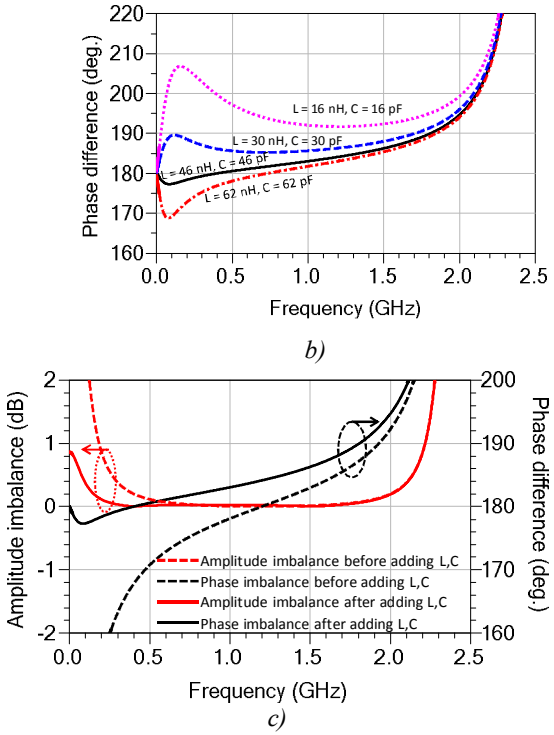


Fig.2.*(a) Phases between ports 1 and 2 and ports 1 and 3 before and after adding a LC circuit to an asymmetric broadside coupled line. (b) Phase differences between ports 2 and 3 versus L and C values. (c) Amplitude and phase differences before and after adding a LC circuit.*

To reduce the phase imbalance of the coupled line at low frequency, a LC-compensation circuit is added to conductor 1 as shown in Fig.1a. Assuming this LC-circuit is a two-port network terminated by 50 Ohm, the phase shift provided by this LC-circuit is calculated from its S-parameters:

$$\Delta\vartheta_{LC} = 90^{o} - \arctan\left[\frac{8(\pi f)^{2} LC - 1}{\frac{\pi f L}{25} + 100\pi f C}\right] \qquad (1)$$

where L and C are the values of shunt inductor and series capacitor in the LC-circuit, f is the frequency.

According to (1), when the frequency f goes to 0, the LC-circuit shifts the phase at port 2 to 180^{0}. At high c-mode impedance (i.e. only pi-mode signal goes through), conductor 2 is the return current path for the conductor 1 and vice versa. The shunt inductor L connecting to the ground from conductor 1 will appear as an inductor connecting between conductor 1 and conductor 2. Assuming the shunt L-circuit is a two-port network terminated by 50 Ohm, the phase shift provided by this network can be calculated from its S-parameters:

$$\Delta\vartheta_{shunt\_L} = 90^{o} - \arctan(\frac{4\pi f L}{50}) \qquad (2)$$

Thus, this shunt inductor will add 90^{0} phase shift to the signal at port 3 when the frequency f approaches 0. The phase at port 3 in this case will reach 0 degree from -90 degrees. After adding the LC-circuit, the total phase difference between the two conductors is corrected to be around 180^{0} at low

frequencies. When frequency *f* goes to infinity, the phase shift created by the LC-circuit at ports 2 and 3 will approach 0 degree according to (1) and (2). The phase difference between ports 2 and 3 will come from the asymmetric coupled line. For the frequencies higher than 1 GHz, the LC-circuit only add less than 6 degree phase shift to ports 2 and 3. For the frequencies lower than 1 GHz, the phase shifting caused by this LC-network is still significant and depends on the value of L and C. Hence, the values of L and C are chosen so that the phase difference of $180^o \pm 10^o$ can be achieved from 10 MHz to around 2 GHz. Fig.2b shows the phase difference between port 2 and 3 for different L and C values. The values of inductor and capacitor are chosen around 46 nH and 46 pF, respectively, for a 180^o phase difference over the widest bandwidth. Fig.2c shows the amplitude and phase differences of the balun before and after adding the LC-compensation circuit. Before adding the LC-compensation circuit, the phase difference of $180^o \pm 10^o$ is only from 470 MHz to 1.93 GHz. With the LC-circuit, the phase balance is improved significantly at frequencies below 500 MHz. The phase imbalance now is within ±10 degrees from 10 MHz to 1.81 GHz. Since the phase balance performance is improved in the low frequency region, the ±1 dB amplitude imbalance bandwidth is also extended from 184 MHz-to-2.2 GHz to 1 MHz-to-2.2 GHz.

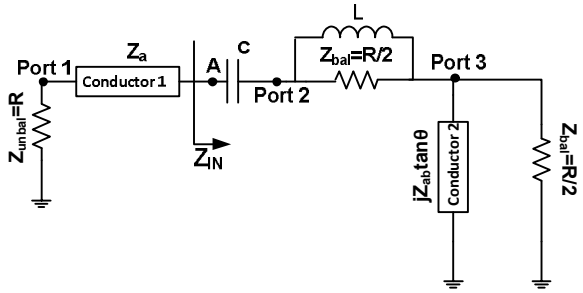


Fig.3. *Equivalent circuit of the proposed balun*

2.2. Impedance transformation bandwidth of the balun

The bandwidth of the balun depends on the impedance matched at the unbalanced port. Since conductor 2 is considered as a ground for conductor 1, the ground of the inductor L and the termination Z_{bal} at port 2 and conductor 2 are at the same node. Conductor 2 is shorted at one end, hence, the input impedance at the other end is $jZ_{ab}\tan\theta$. As a result, we have the equivalent circuit of the proposed balun as shown in Fig.3. Traditionally, Z_a is designed to be equal Z_{unbal}. Hence, the bandwidth of the balun is determined by matching Z_{in} with the unbalanced port termination $Z_{unbal} = Z_a = R$. From the equivalent circuit in Fig.3:

$$Z_{IN} = \left(\frac{jZ_{ab}\tan\theta \times R/2}{jZ_{ab}\tan\theta + R/2} \right) + \left(\frac{jX_L \times R/2}{jX_L + R/2} \right) - jX_C = r + jx \qquad (3a)$$

$$\frac{r}{R}=\frac{2Z_{ab}^2\tan^2\theta}{R^2+4Z_{ab}^2\tan^2\theta}+\frac{2X_L^2}{R^2+4X_L^2}=1-\frac{1}{2+8\frac{Z_{ab}^2}{R^2}\tan^2\theta}-\frac{1}{2+8\frac{X_L^2}{R^2}} \quad (3b)$$

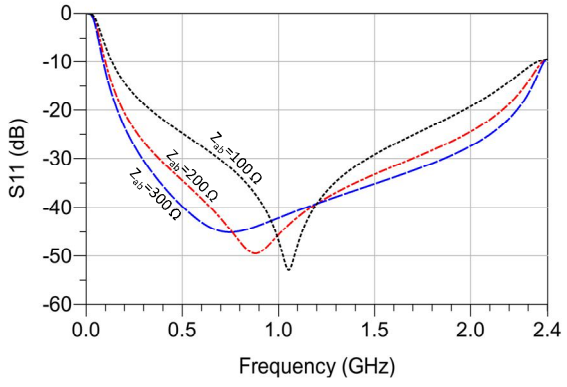
$$\frac{x}{R}=\frac{Z_{ab}\tan\theta\times R}{R^2+4Z_{ab}^2\tan^2\theta}+\frac{X_L R}{R^2+4X_L^2}-\frac{X_C}{R}=\frac{\frac{Z_{ab}}{R}\tan\theta}{1+4\frac{Z_{ab}^2}{R^2}\tan^2\theta}+\frac{\frac{X_L}{R}}{1+4\frac{X_L^2}{R^2}}-\frac{X_C}{R} \quad (3c)$$

where Z_{IN} is the input impedance at point A, $R = Z_{unbal} = 2Z_{bal}$, $X_C = {}^1/_{\omega C}$ and $X_L = \omega L$.

The perfect match will be achieved when $Z_{IN} = Z_a = R$ or

$$\frac{r}{R} = 1 \text{ and } \frac{x}{R} = 0 \qquad (4)$$

From (3b) and (3c), (4) can be satisfied over a wide bandwidth if Z_{ab} and X_L are very large while X_C is small. In otherwords, the matching bandwidth is proportional to the ratios $\frac{Z_{ab}}{R}$, $\frac{X_L}{R}$, and $\frac{R}{X_C}$. Fig.4a shows the simulated S_{11} of the proposed balun using ADS when L = 46 nH, C = 46 pF while Z_{ab} is varied and Fig.4b presents the S_{11} when Z_{ab}= 200 Ω whereas L and C are changed. In Fig.4a, the -10 dB matching bandwidth gets wider when the Z_{ab} is higher. At high frequency, $X_L = \omega L$ is large and $X_C = 1/\omega C$ is small. The matching at high frequencies depends mainly on Z_{ab}. When the frequency is at λ/2 (2.4GHz), tan θ approaches 0 leading to $\frac{x}{R} \approx 0$ and $Z_{IN} \approx r \approx 25$ Ω if R = 50 Ohm. Conductor 1 with $Z_a = Z_{unbal}$= 50 Ω will transform 25 Ω to 100 Ω at the unbalanced port (port 1). The reflection coefficient at port 1 now is -9.54 dB and is independent on Z_{ab} and the values of L and C. In the low frequency region, the values of L and C have significant impacts on the matching bandwidth since ω is small. As shown in Fig.4b, for larger L or C, the S_{11} bandwidth extends further to lower frequency. In short, we need to design high Z_{ab} and choose large values of L and C to achieve wide impedance transformation bandwidth. However, the values of L and C should be chosen appropriately so that we can get the largest bandwidth for a phase difference of $180^o \pm 10^o$.



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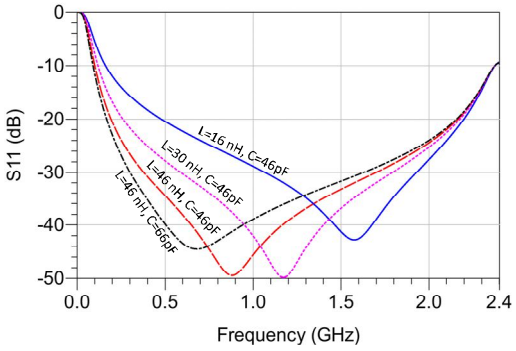


b)

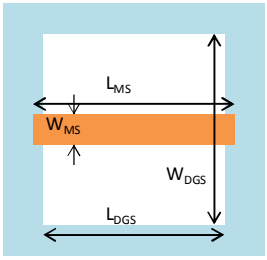
Fig.4.*Simulated S_{11} of the proposed balun in ADS: (a) S_{11} when L = 46 nH, C = 46 pF, and Z_{ab} is a variable. (b) S_{11} when Z_{ab}= 200 Ω, L and C are variables.*

2.3. Defected ground structures for the proposed balun

To achieve wide bandwidth for the balun, one thus needs to increase the characteristic impedance Z_{ab}. Increasing Z_{ab} can be achieved by decreasing the width of conductor 2 and increasing the thickness of the dielectric substrate. Since conductor 2 serves as a ground for conductor 1, its width cannot be too small. Also, it is challenging to increase the thin-film substrate thickness as each layer is about 25 µm to 50 µm thick. Hence, we have developed defected ground structures (DGS) to achieve large Z_{ab} without shrinking the width of conductor 2 or increasing the thickness of the dielectric layers [30]. According to [31], DGS helps to increase the series inductance in the equivalent model of a microstrip line to enlarge its characteristic impedance. To study the characteristic impedance of a microstrip line on a defected ground, we set up a High Frequency Structure Simulator (HFSS) [32] simulation of a DGS microstrip line as shown in Fig.5a. The dielectric substrate is LCP with a relative dielectric constant ε_r= 2.9 and a loss tangent of ~0.002, and the substrate height is 355.6 µm. The metal thickness is 18 µm. The microstrip line width W_{MS} is 1 mm. The length L_{DGS} is varied from 30 mm to 50 mm while L_{MS} of the microstrip line is always 2 mm longer than L_{DGS}. The DGS width W_{DGS} is also varied to observe the change of impedance of the transmission line.

The DGS microstrip line characteristic impedance is extracted from its 2-port simulated S-parameters. Fig.5b shows the characteristic impedance of a DGS microstrip line for different sizes of the defected ground area. A solid ground microstrip line with a width of 1 mm on a 355.6 µm thick LCP substrate has the characteristic impedance of 44.5 Ω. Using the defected ground, the characteristic impedance of the microstrip line on a 355.6 µm thick LCP substrate increases up to 4 times. As shown in Fig.5b, the characteristic impedance of the DGS microstrip line increases to 210 Ω when length L_{DGS} = 40 mm and width W_{DGS} = 40 mm. The characteristic impedance of the DGS microstrip line increases

proportionally to the size of the defected area of the ground and saturates around 210 Ω. The inductance and capacitance per unit length of the DGS microstrip were also extracted. It is observed that the characteristic impedance increases due to the rise of the line's inductance per unit length and a reduction of the capacitance per unit length.



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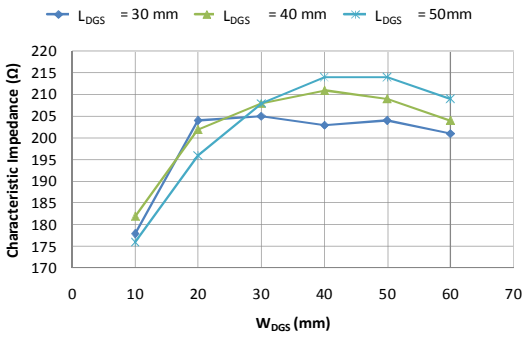


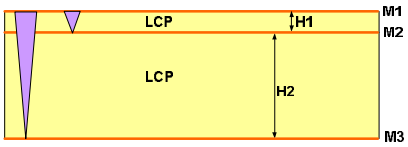
b)

Fig.5.*(a) Defected ground structure microstrip line. (b) Effect of the defected ground area on the characteristic impedance of the microstrip line.*

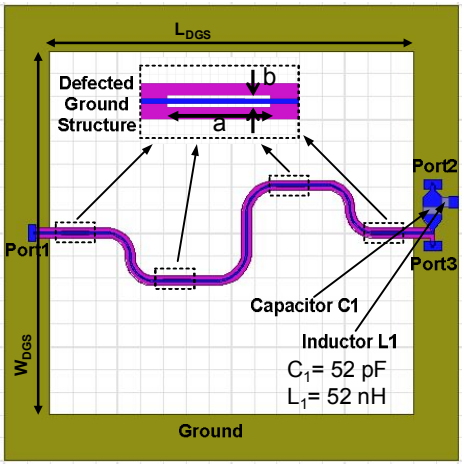
3. Balun design

3.1. The balun design and layout

Fig.6 shows the layout of the proposed balun and the dielectric stack-up. The balun is implemented on a multilayer LCP substrate that has two dielectric layers and three metal layers labeled M1, M2 and M3. The top metal layer M1 is used for conductor 1 of the coupled line section in the balun. In the balun layout shown in Fig.6a, conductor 1 is depicted in blue color. Conductor 2 resides on the metal layer M2 and is depicted in purple color. The ground plane with a large rectangular defected area is on the metal layer M3. The two dielectric layers have thicknesses of H1 = 50 μm and H2 = 304 μm.



a)



b)

Fig.6.*(a) Dielectric stack-up. (b) Balun layout*

In this balun layout, the values of the lumped components C_1=52 pF, L_1=52 nH of the compensation network are used in HFSS simulations. These values are slightly different with ones in ADS simulations because the real 3-D structure in HFSS adds some parasitic. The asymmetric broadside coupled line is designed to have the quarter-wavelength frequency around 900 MHz. The coupled line is meandered to reduce the size of the balun. Since H1 is 50 µm, the width of conductor 1 is ~100 µm to make Z_a ~50 Ohm. To reduce the conductor loss caused by such a small trace width, we create 4 rectangular-shape defected ground structures on conductor 2 to increase conductor 1 width of the 50-Ω line to 177 µm. The width of conductor 2 is chosen to be 1 mm to provide good grounding for conductor 1. Table 1 shows Z_a versus different width b of these 4 small rectangular defected areas on conductor 2 when their length is a = 3 mm. Z_a is closest to 50 Ω when the size of these small defected areas is 3 mm x 0.35 mm.

To achieve high Z_{ab}, the length of the defected area on M3 is L_{DGS} = 40.7 mm to fit the coupled-line and its width W_{DGS} is chosen to get the highest Z_{ab}. Table 2 shows the characteristic impedance Z_{ab} extracted from HFSS simulations when the width W_{DGS} of the defected area is changed and the width of conductor 2 is fixed at 1 mm. With this configuration, Z_{ab} reaches the maximum value of 207 Ω when W_{DGS} is 40.4 mm and the dimension of the defected area for the balun layout is chosen to be 40.7 mm x 40.4 mm.

Table 1 Z_a versus b for the width of microstrip line W_{MS}=177µm

b (mm)	Z_a (Ω)
0	39
0.25	47
0.35	51
0.45	54

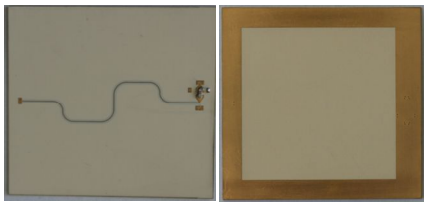
Table 2 Z_{ab} for the microstrip line with W_{MS} =1 mm and different W_{DGS}

W_{DGS} (mm)	Z_{ab} (Ω)
0	40
30.4	195
35.4	204
40.4	207
45.4	199

3.2. Balun prototype, simulation and measurement results

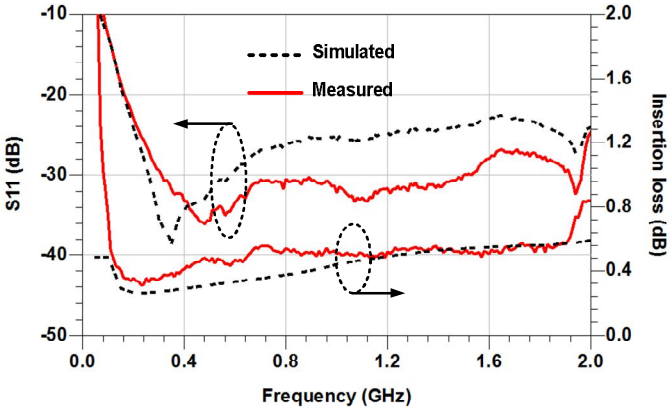
The fabricated prototype of the balun is shown in Fig.7. Co-planar waveguide probe pads are added for on-wafer measurements. The inductor L is realized by two series surface mount components, each having an inductance of 27 nH and a part number of MLK0603L27NJT from TDK Corporation [33]. Since the self-resonant frequency of these inductors is at about 4.5 GHz, it will not have a great effect on the performance of the balun. The capacitor C is realized by 4 parallel surface mount components, each has a capacitance of 13 pF and a part number of 500R07S130GV4T from Johanson Technology Inc [34]. The size of the balun is 40.6 mm x 40.6 mm (and 50.7 mm x 50.7 mm with the whole ground size).

The electrical performance of the balun was measured on a Cascade Microtech probe station with an Agilent E8364 2-port network analyzer. The probes were calibrated by using Thru-Reflect-Line calibration on a Picoprobe CS-9 substrate [35]. Fig.8 shows the measured and simulated results of the balun. As shown in Fig.8a, the balun has a measured input return loss of better than 10 dB from 80 MHz to above 1860 MHz. The measured insertion loss (IL) of the balun in Fig.8a is calculated from the measured S_{12} and S_{13} by the equation $IL = -10log_{10}(|S_{12}|^2 + |S_{13}|^2)$ (dB) [36]. The experimental results demonstrate that the measured insertion loss of the balun is better than 1 dB in the frequency band from 80 MHz to above 1860 MHz. The measured phase imbalance and amplitude imbalance of the proposed balun are shown in Fig.8b. The balun achieves a measured phase imbalance better than ±10 degrees and a measured amplitude imbalance better than ±0.4 dB from 80 MHz to 1850 MHz. Table 3 shows the comparison of this design with published planar PCB broadband compact baluns in terms of bandwidth, phase imbalance, amplitude imbalance and size. In this table, λ_g is the guided wavelength at the center operating frequency of the reported baluns.



a) *b)*

Fig.7.*The balun prototype a) Top b) Bottom*



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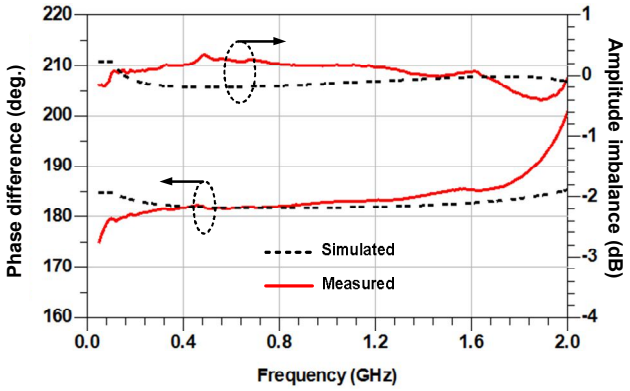


b)

Fig.8.*Measured results of the balun: (a) S_{11} and insertion losses. (b) Phase and amplitude imbalances*

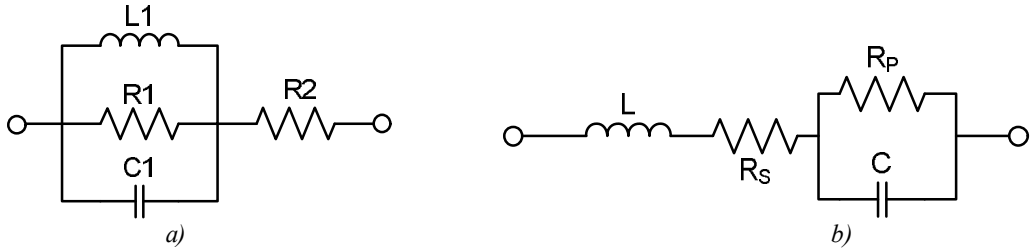
Table 3 Comparison of balun designs

	Bandwidth Ratio	**Amplitude Imbalance (dB)**	**Phase Imbalance (Degree)**	**Size**
[10]	5:1	±0.5	±5	$0.18\lambda_g$ x $0.09\lambda_g$
[11]	2.6:1	±0.69	±1.4	$0.5\lambda_g$ x $0.17\lambda_g$
[12]	1.9:1	±0.5	±1.5	$0.23\lambda_g$ x $0.05\lambda_g$
[21]	10:1	± 0.3	± 6	$0.15\lambda_g$ x $0.11\lambda_g$
[16]	9:1	± 1	± 8	$0.17\lambda_g$x $0.11\lambda_g$
Our work	**23:1**	**± 0.4**	**± 10**	**$0.22\lambda_g$ x $0.22\lambda_g$**

3.3. Parasitic effect of lumped components in LC network

Simple models of a lumped inductor and a lumped capacitor with parasitic effects are shown in Fig. 9. As can be seen, the inductor has parallel parasitic capacitance and the capacitor has series parasitic inductance. In an ideal highpass series C shunt L network, the phase shift from input to output is positive

over frequency. However, due to the parasitic elements, a composite highpass and lowpass network is formed and its phase shift becomes negative as the frequency goes up as shown in Fig. 10. Since ideal lumped components have been used in the simulation, the measured phase imbalance of the prototype is, therefore, slightly worse than that found from the simulation.



a) *b)*

Fig.9. a) Lumped inductor model b) Lumped capacitor model

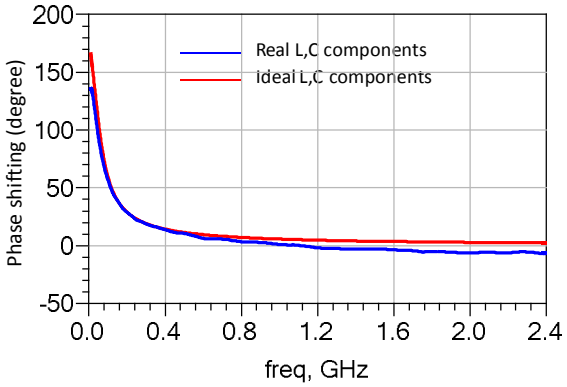
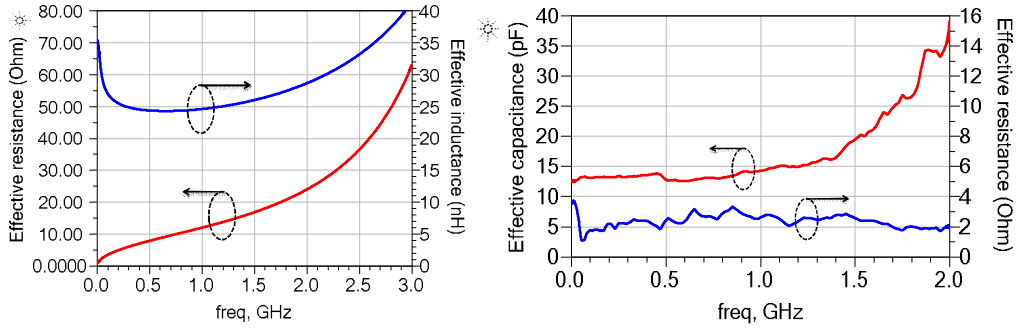


Fig.10. Phase shift of the LC-network in ideal case and real components case

Furthermore, as can be seen in Fig.9, both the lumped inductor and lumped capacitor have series parasitic resistance. The effective resistance, inductance and capacitance of these lumped components are shown in Fig.11. This parasitic resistance adds constructively to the real part of the input impedance and brings the unbalanced port impedance closer to 50 Ohm. Hence, the measured return loss is better than the simulated one.



a) *b)*

Fig.11. a) effective inductance and resistance of the lumped inductor
b) effective capacitance and resistance of the lumped capacitor

4. Conclusion

We present the design and development of a novel wide bandwidth planar balun. This balun achieves ~23:1 bandwidth ratio. The measurement results show that the balun achieves a measured bandwidth from 80 MHz to 1860 MHz. Within this operating band, the balun has phase imbalances better than ±10 degrees and amplitude imbalances better than ±0.4 dB. The wide bandwidth of the balun is achieved by using the defected ground structures and phase compensation circuits.

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