Applications Using One-dimensional Semiconductor Materials

A dissertation submitted in partial satisfaction of the requirements of the degree
Doctor of Philosophy
in
Electrical Engineering (Applied Physics)

by

Ching-Yang Zack Chen

Committee in charge:
Professor Jie Xiang, Chair
Professor Peter M. Asbeck
Professor Prabhakar R. Bandaru
Professor Renkun Chen
Professor Paul Yu

2014
This Dissertation of Ching-Yang Zack Chen is approved, and it is acceptable in quality and form for publication on microfilm and electronically:

_________________________________________________________________________________

_________________________________________________________________________________

_________________________________________________________________________________

_________________________________________________________________________________

_________________________________________________________________________________

Chair

University of California, San Diego
2014
DEDICATION

I dedicate this thesis to my beloved family.

- To my wife Yvonne, without your love and devotion, I am not what I am right now.
- To my son and daughter, Aris and Bethany, your smiles energize me.
- To my parents, thanks for your ceaseless support and love.
# TABLE OF CONTENTS

Signature Page ................................................................. iii
Dedication ........................................................................ iv
Table of Contents .............................................................. v
List of Figures ...................................................................... viii
List of Tables ....................................................................... xiii
Acknowledgements ............................................................. xiv
Vita ...................................................................................... xvii
Abstract of the Dissertation ................................................ xx

## Chapter 1 Introduction ......................................................... 1

1.1 Preliminary: Big things have small beginnings .............. 2
1.2 One-dimensional nanostructures as platforms .............. 4
1.3 Rational synthesis of one-dimensional nanostructures ..... 7
1.4 Organization of dissertation ........................................ 11

## Chapter 2 Origin of Hole Gas in Ge/Si Core/Shell Nanowire Field Effect Transistor .................................................. 19

2.1 Introduction ................................................................... 20
2.2 Experimental section ................................................... 22
2.2.1 Synthesis of Ge/Si core/shell nanowires .......... 22
2.2.2 Fabrication of bottom-gated FETs and characteristic measurements of FETs ........................................... 24
2.2.3 Methods to extract FET properties 24
2.2.4 Poisson-Schroedinger solver 28
2.3 Results and discussions 29
  2.3.1 Device characteristics 29
  2.3.2 Simulation results (Poisson-Schrödinger Solver) 35
  2.3.3 Further mechanisms (Dopant deactivation) 40
2.4 Conclusion 43
References 44

Chapter 3  Nano-Electro-Mechanical Field-Effect-Transistor (NEMFET) 48
  3.1 Introduction 48
  3.2 Static power consumption and subthreshold swing 49
  3.3 Breakthrough of Sub-threshold Swing Limitation 53
  3.4 Nano-Electro-Mechanical System (NEMS) 56
  3.5 Nanowire NEMFET 69
  3.6 Device modeling 75
  3.7 Simulation results 89
  3.8 Device fabrication 95
  3.9 Electrical properties of fabricated devices 103
  3.10 Conclusion 111
References 112
## Chapter 4  Differentially Functionalized Silicon Nanotubes (SiNTs)····  118

4.1 Introduction ................................................................. 119

4.2 Synthesis of SiNTs ........................................................... 120

4.3 Electrical properties of SiNTs ........................................... 123

4.4 Functionalization of SiNTs ............................................... 129

4.5 Conclusion ................................................................. 136

References ................................................................. 137
LIST OF FIGURES

Figure 1.1: Binary phase diagram of Au-Si. Image courtesy of ref. 47

Figure 1.2: Schematic diagram of the nanowire VLS growth process.

Figure 2.1: Ge/Si core/shell nanowires.

Figure 2.2: Comparison of simulation results of Ge/Si core/shell NW gate capacitance over different $D_{\text{core}}$ (10nm ~ 85nm).

Figure 2.3: Temperature-dependent and diameter-dependent hole transport assessment.

Figure 2.4: (a) $I_d$-$V_g$ characteristics of different Ge core diameter ($D_{\text{core}}$) at low drain bias voltages. (b) Normalized $V_{\text{th}}$ histograms and Gaussian fit curves for $V_{\text{th}}$ distribution. (c) Extracted carrier density and simulated hole concentration.

Figure 2.5: Results from three-dimensional Poisson-Schrödinger solver.

Figure 2.6: Effects of fixed surface states and dopant deactivation.

Figure 2.7: Comparisons of band diagram of valence band and carrier distribution of Ge/Si core/shell NW in different $D_{\text{core}}$ (8 nm, 20 nm, 30 nm, and 60 nm) along the radial direction (axis) originating from center of the nanowires.

Figure 3.1: Schematic $V_g$-$I_g$ curve of n-MOSFET. The $I_{\text{off}}$ with same $I_{\text{on}}$ can be decreased with two ways.

Figure 3.2: Comparison of schematic $V_g$-$I_g$ curve between ideal switch and MOSFET.

Figure 3.3: Tunneling Field Effect Transistor with L-shape gate. (a) Schematic structure and band diagram of TFET, (b) Transfer curve of the fabricated TFET. The SS value is 52.8 mV/dec at room temperature.
Table 3.1: Important parameters of NEM switch with suspended NW channel.

Table 4.1: Comparison of the characteristics between the back gate NEMFET and the local metal gate.

Figure 3.4: I-MOS (a) Basic structure and band diagram in the On/Off states of the n-channel I-MOS, (b) Transfer curve of the fabricated device with 7.5mV/dec sub-threshold swing.

Figure 3.5: 3-terminal NEM relay using suspended CNT cantilever, (a) Basic structure, (b) Transfer curve of the fabricated device.

Figure 3.6: 3-terminal NEM switch using suspended CNT channel, (a) 45° tilted SEM image of fabricated NEM switch with triode structure, (b) Transfer curve of the fabricated device with $V_d=0.5V$.

Figure 3.7: 2-terminal NEM switch using suspended TiN Cantilever, (a) 45° tilted SEM image of fabricated NEM switch, (b) Transfer hysteresis curve of the fabricated device with compliance of 10nA.

Figure 3.8: 2 or 3 terminal NEM switch using vertical CNT, (a) 45° tilted SEM image of fabricated NEM switch, (b) Transfer curve of the fabricated device with 3-terminal, (c) Transfer curve of 2-terminal.

Figure 3.9: 4-terminal relay device with suspended metal gate, (a) Schematic of device, (b) Pull-in occurs at $V_g=6.1V$ with $SS=1mV$, (c) Pull-out occurs at $V_g=5V$.

Figure 3.10: Low voltage 2-terminal NEM switch suspended metalized SiC nanowire.

Figure 3.11: Pipe-clip shaped NEM switch using top-down process. (a) Schematic process flow, (b) Cross section TEM image of the device.

Figure 3.12: Large-scale graphene sheet resonator. (a) Angled scanning electron microscopy (SEM) image of Type A suspended graphene membranes over trenches in silicon oxide. (b) Angled SEM of an array of graphene membranes.
Figure 3.13: Direct assembly pattern of SWNT with AFM (a), (b) parallel pattern, (c) Random line structure. ........................................ 66

Figure 3.14: Nanostructure ensemble using a fabric of SWNT, (a) Schematics of process flow, (b) SEM image of fabricated device. ................................................................. 67

Figure 3.15: NW NEMFET structure for the device simulation. .......... 71

Figure 3.16: NW NEMFET operation modes and corresponding band diagrams within the suspended NW. .................................................. 72

Figure 3.17: Normalized restoring and electrostatic forces vs. normalized electrode separation. ................................................................. 73

Figure 3.18: Simulation results of the electrostatic potential distribution of the NW NEMFET. .......................................................... 85

Figure 3.19: Normalized dependence of gap distance vs gate voltage using self-consistent COMSOL simulation and analytical modeling. ................................................................. 90

Figure 3.20: Comparison of simulated $V_g$-$I_d$ curve between NEMFET and MOSFET having same dimension for the same $I_{on}/I_{off}$ ratio. .................................................. 92

Figure 3.21: Comparison of simulated $V_g$-$I_d$ curves of the NW NEMFET with different doping concentrations. ........................................ 92

Figure 3.22: Constant performance device scaling trends between resonant frequency (solid line) & $V_{pi}$ (dotted line). The color map shows constant $V_{pi}$'s as a function of $D$ and $L$. ......... 95

Figure 3.23: Schematic structure of the device, (a) the back gate NEMFET, (b) the local metal gate NEMFET. ........................................... 96

Figure 3.24: Schematic cartoon of process procedure for the back gate NEMFET with suspended i-Ge/Si core/shell nanowire channel. ................................................................. 99

Figure 3.25: HRTEM image of the Ge/Si core/shell nanowire. ................. 100
Figure 3.26: Top-view SEM image of back gate NEMFET, (a) low magnification (scale bar = 50 um), (b) high magnification (scale bar=10 um).

Figure 3.27: SEM image of fabricated back gate NEMFET with suspended i-Ge/Si core/shell nanowire channel, (a) low magnification (scale bar=200um), (b) high magnification (scale bar=1um).

Figure 3.28: Schematics of measurement system, (a) Vd-Id, (b) Vg-Id.

Figure 3.29: Transfer characteristics of NEMFET, (a) Vd-Id curve (SEM image of measured device, scale bar=1um), (b) Vg-Id curve.

Figure 3.30: Comparison of Vpi, Vpo value between 3D COMSOL simulation and measurement results of NEMFET.

Figure 3.31: Pull-in and pull-out switching of other device, Inset is Vd-Id curve.

Figure 3.32: Schematics of measurement system for one-source method.

Figure 3.33: Measurement results of resonant frequency, (a) Frequency vs. Imix plot in different AC drive amplitude. (b) The dependency of resonant frequency f0 and Ipeak vs. AC drive amplitude.

Figure 4.1: (a) Schematics of SiNT synthesis. (b) SiNTs shown in low-resolution TEM image. (c) Individual SiNT. (d) High-resolution TEM shows crystal lattice on the shell of a SiNT. (e) TEM from crystalline SiNT after 28 days exposed in air.

Figure 4.2: Id-V characteristics under four different sets of gate biases from a representative c-Si NT FET with ID of 30 nm, shell thickness of 5 nm.

Figure 4.3: Two-dimensional finite element electrostatic analysis of gate capacitance for NT and NW structure using COMSOL Multiphysics.
Figure 4.4: *I-V characteristics under four different sets of gate biases from a representative a-Si NT FET with ID of 20 nm, shell thickness 40 nm and length of 2 μm between the two inner contacts.*

Figure 4.5: *Schematic illustration of selective biomolecule functionalization. (a) PEGylation process on the outer wall of Si NTs followed by Ge core removal for inner wall functionalization. (b) Two types of biomolecules, Rhodamine and BSA-FITC.*

Figure 4.6: *Demonstration of Rhodamine loading. (a) and (b) Bright field (left) and fluorescent (right) images. (c) Control sample after APTES functionalization and incubation with Rhodamine using a solid core Ge/Si nanowire. Scale bars, 3 μm.*

Figure 4.7: *Demonstration of BSA-FITC functionalization. (a) BSA-FITC-loaded Si NTs from bright field (left) shows green fluorescent (right) signals while (b) control sample of a solid Ge/Si nanowire. Scale bars, 5 μm.*
LIST OF TABLES

Table 1.1: Family of semiconductor nanowires and nanowire heterostructures. ......................................................... 6
Table 3.1: Comparison of the characteristics between the back gate NEMFET and the local metal gate NEMFET. .................. 97
Table 3.2: Important parameters of back gate NEMFET switch with suspended CSNW channel. .................................... 103
I sincerely appreciate my advisor Jie Xiang’s mentoring. During my PhD program at UCSD, Prof. Xiang had been never reluctant to share what he knew. With his encouragement to try and learn, I have not only gained my technical knowledge but also skills to analyze and deal with problems.

Of course, I have to say thank you to all the mentors at UCSD who had instructed me. Thank you, Prof. Peter Asbeck, Renkun Chen, Jennifer Cha, Deli Wang, Prabhakar Bandaru, and Paul Yu. Without your advise, I cannot finish my thesis.

Lastly, I feel blessed doing my graduate program at UCSD, every colleague I had worked with was knowledgeable and passionate about science.
The material in this thesis is based on the following publications.

- Chapter 2 is based on the following publication:

- Chapter 3 is based on the following publications:
    *These authors contributed same.
    *These authors contributed same.
Chapter 4 is based on the following publications:


*These authors contributed same.

My coauthors (Professor Jennifer Cha, Han-Ping Chen, Ji-hun Kim, Soonshin Kwon, Ju Hun Lee, Mr. Hyunwoo Noh, and Professor Jie Xiang, listed in alphabetical order of last name) have all kindly approved the inclusion of the aforementioned publications in my thesis.
VITA

2006  B.S., Electrical and Control Engineering,
      National Chiao Tung University, Hsinchu, Taiwan

2014  Ph.D., Electrical Engineering (Applied Physics)
      University of California, San Diego
All papers coauthored with my advisor Prof. Jie Xiang.

  *These authors contributed same.


  *These authors contributed same.


- **Zack C. Y. Chen**, Matthew C. Wingert, Jie Xiang and Renkun Chen, “Ultra-sensitive thermal conductance measurement of one-dimensional


*These authors contributed same.

- **Zack C. Y. Chen**, Han-Ping Chen, Soonshin Kwon, and Jie Xiang, “Origin and Diameter Dependence of Hole Gas in Ge/Si Core/Shell Nanowires”, submitted to *Nanoscale*.
ABSTRACT OF THE DISSERTATION

Applications Using One-dimensional Semiconductor Materials

by

Ching-Yang Zack Chen

Doctor of Philosophy in Electrical Engineering (Applied Physics)

University of California, San Diego, 2014

Professor Jie Xiang, Chair

One-dimensional (1D) nanostructure has become one of the most exciting
forefronts in nanotechnology fueled by demand for more compact and powerful
devices that could affect people’s lives in many aspects, from simple household
appliances and multimedia systems to communications, computing and medical instruments. In particular, semiconductor nanowires (NWs) and/or nanotubes (NTs) are emerging among the most promising family of platforms since, through controlled chemical growth and specific fabrication, such semiconductor NWs and/or NTs can open up substantial opportunities for novel nanoscale devices, such as electronic devices, mechanical devices, thermoelectric devices, and pharmaceutical devices. In one aspect, understanding the unique nature of 1D electrical transport and the proposed enhancement in performance are crucial to the developments of the nanoscale electric device, mechanical device, or a combination hereof. Yet in another aspect, using the particular structure of the 1D semiconductor heterostructures to synthesize novel 1D nanostructures (e.g., NTs) may provide advantageous benefits to advanced pharmaceutical devices. This dissertation covers topics addressing both critical scientific areas of fundamental understanding of charge transport phenomena of Ge/Si core/shell heterostructure NWs and applications using the core/shell heterostructure NWs and single crystalline Si NTs.
Chapter 1 Introduction

One-dimensional (1D) nanostructure has become one of the most exciting frontiers in nanotechnology fueled by demand for more compact and powerful devices that could affect people's lives in many aspects, from simple household appliances and multimedia systems to communications, computing and medical instruments. In particular, semiconductor nanowires (NWs) and/or nanotubes (NTs) are emerging among the most promising family of platforms since, through controlled chemical growth and specific fabrication, such semiconductor NWs and/or NTs can open up substantial opportunities for novel nanoscale devices, such as electronic devices, mechanical devices, thermoelectric devices, and pharmaceutical devices. In one aspect, understanding the unique nature of 1D electrical transport and the proposed enhancement in performance are crucial to the developments of the nanoscale electric device, mechanical device, or a combination hereof. Yet in another aspect, using the particular structure of the 1D semiconductor heterostructures to synthesize novel 1D nanostructures (e.g., NTs) may provide advantageous benefits to advanced pharmaceutical devices. This dissertation covers topics addressing both critical scientific areas of fundamental understanding of charge transport phenomena and practical applications of semiconductor NWs and NTs. As an introduction, this chapter provides general background knowledge about the nanotechnology and nanoscience, with an emphasis on applications in nanoelectronics. A brief introduction of the bottom-up approach to nanoscale devices using NWs will be given, along with a section
describing the VLS NW growth method, which has established the foundation of our 1D nanostructure study.

1.1 Preliminary: Big things have small beginnings

Back in December 1959, Nobel laureate Richard Feynman gave a visionary talk entitled “There’s plenty of room at the bottom” at the meeting of American Physical Society. Out of Feynman’s intention, his 7,000 words talk does not only set a milestone moment in nanotechnology before anything about nanotechnology appeared on the horizon but also inspired an explosive research effort in the full spectrum of scientific and technical fields at the nanoscale. And, the effort to pursue the future nanotechnology has been only increasingly attempted. For example, the President’s Fiscal Year 2011 Budget provides nearly $1.8 billion for the National Nanotechnology Initiative (NNI), a United States federal nanoscale science, engineering, and technology research and development program.

According to National Nanotechnology Initiative’s definition, nanotechnology is the ability to understand, control and manipulate matter at the nanoscale, at dimensions between approximately 1 and 100 nanometers, where unique phenomena enable novel applications.

Matter at this nanoscale is often awkward to explore because it can exhibit unusual physical, chemical and biological properties, differing in ways from the properties of bulk materials and single atom or molecules1-8. Fortunately, over the
past 50 years after Feynman’s vision, the array of scientific and technical research at this nanoscale has been well established, including but not limiting to, electron-beam and ion-beam fabrication, molecular-beam epitaxy, nanoimprint lithography, projection electron microscopy and chemical vapor deposition\textsuperscript{9-12}.

More specifically, in the area of electronics, nanostructured materials offer a wide choice of crystalline materials with much higher carrier mobility and therefore faster transmission and switching speed for electrical signals than organic molecules in living organisms. The nanometer size scale can be comparable or even smaller than several characteristic length scales related to carrier transport, giving rise to unique low-dimensional physics mechanisms. One notable example pertinent to the experiments described in this thesis occurs when the Fermi wavelength of the carriers becomes comparable to the size of the nanostructure. Similar to the classical case of waveguide modes for electromagnetic waves, confinement of the electron/hole carrier wave function will lead to discontinuities in the density of states in 0D, 1D or 2D, depending on the confinement direction. At 0D, studies have found excitation spectra in these so-called artificial atoms, while at 1D, quantized conductance plateaus have also been extensively explored. Other length scales, such as the electron scattering mean free path, can also be found to be much larger than the device structure, thus provides opportunities to study ballistic transport behavior in semiconductors.

Nanotechnology does have benefit, even revolutionize, many technology and industry sectors: electronics and information technology\textsuperscript{13-17}, energy\textsuperscript{18-21}, environmental science\textsuperscript{22-26}, medicine\textsuperscript{27-31}, among many others.
However, we are certainly nowhere near being able to commercially mass-produce nanosystems—integrated multicomponent nanodevices that have the complexity and range of functions readily provided by modern chips. And, it is becoming increasingly clear that we are still at the beginning step to acquire the detailed knowledge that will be at the heart of future nanotechnology.

Indeed, we still have plenty of things to be discovered at the bottom.

1.2 One-dimensional nanostructures as platforms

Traditionally various lithography methods have been employed to fabricate nanoscale structures out of single crystalline bulk substrates. Such methods are generally referred to as “top-down” approach. The increasing tool cost and physical limitations of lithography due to an increasing scaling-down of size have caused a gradual shift of academia and industry’s attention from such “top-down” approach, to a new “bottom-up” paradigm in the field of nanoscience and nanotechnology. The bottom-up paradigm simply takes the lesson from nature, where systems with complex functionalities have been assembled directly from nanoscale building-blocks\textsuperscript{32}, or simply platforms. This new approach offers distinct advantage over conventional top-down fabrication as it employs virtually any material chemically available and their combination as heterostructure components to achieve better device performance and enable advanced functionalities.
The first task toward realizing applications through a bottom-up paradigm is the rational control of key material parameters, including chemical composition, structure, size, morphology, and doping as it is these parameters that determine, for example, electronic properties critical to predictable device function. Significantly, semiconductor NWs represent the nanomaterial system where these key parameters have been best controlled today. First, an underlying conceptual framework has been developed to enable growth of virtually any uniform composition and structure nanowire, with the wide-range of reported nanowires confirming these models (table 1-1). Second, in many cases controlled p- and n-type doping, which is critical to almost any active device application, has been demonstrated. Third, the control over nanowire growth has enabled the creation of a host of structures with modulated structure and/or doping, including axial and radial heterostructures, where modulation allows functions to be ‘built-in’ at the nanoscale without the need of lithography which dominates many top-down technologies (table 1-1). Lastly, branched and hyper-branched NW structures with homogeneous or heterogeneous materials have offered an additional dimension of device integration than conventional 2D electronics\(^{33,34}\).
### Table 1.1: Family of semiconductor nanowires and nanowire heterostructures available through chemical synthesis. The schematic images and part of the table are adapted from reference 33,35.

<table>
<thead>
<tr>
<th>Homogeneous Structure</th>
<th>Group IV</th>
<th>Group III/V</th>
<th>Group II/VI</th>
</tr>
</thead>
<tbody>
<tr>
<td>Si</td>
<td></td>
<td>Si: B (p-type)</td>
<td>GaN</td>
</tr>
<tr>
<td>Si: P (n-type)</td>
<td></td>
<td>Si: P (n-type)</td>
<td>GaN: Mg (p-type)</td>
</tr>
<tr>
<td>Ge</td>
<td></td>
<td>Ge: B (p-type)</td>
<td>GaN: Mn</td>
</tr>
<tr>
<td>Ge: P (n-type)</td>
<td></td>
<td>Ge: P (n-type)</td>
<td>GaP</td>
</tr>
<tr>
<td>Si$<em>x$Ge$</em>{1-x}$</td>
<td></td>
<td>GaAs</td>
<td></td>
</tr>
<tr>
<td>Axial Heterostructure</td>
<td>n-Si/p-Si</td>
<td>GaAs$<em>y$P$</em>{1-y}$</td>
<td></td>
</tr>
<tr>
<td>n-Si/i-Si/p-Si</td>
<td></td>
<td>InAs$<em>y$P$</em>{1-y}$</td>
<td></td>
</tr>
<tr>
<td>(n-Si/n$^+$-Si)$_n$</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Si/NiSi</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Si/Si$<em>x$Ge$</em>{1-x}$</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Radial Heterostructure</td>
<td>i-Si/p-Si</td>
<td>n-GaN/InGaN/p-GaN</td>
<td></td>
</tr>
<tr>
<td>Si/Ge</td>
<td></td>
<td>n-GaN/InGaN/p-AlGaN/p-GaN</td>
<td></td>
</tr>
<tr>
<td>Si/Ge/Si</td>
<td></td>
<td>n-GaN/(InGaN MQW)/p-AlGaN/p-GaN</td>
<td></td>
</tr>
<tr>
<td>i-Si/Si$_x$O$_y$/p-Si</td>
<td></td>
<td>GaN/AlN/AlGaN</td>
<td></td>
</tr>
<tr>
<td>p-Si/i-Ge/Si$_x$/p-Ge</td>
<td></td>
<td>GaN/AlGaN</td>
<td></td>
</tr>
<tr>
<td>ZnS</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>ZnS: Mn</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CdS</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CdS: Mn</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>ZnSe</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CdSe</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Understanding the physical properties underlying these NW materials at a single device level is the natural next step in the bottom-up paradigm. Electrical transport measurements have been extensively carried out to extract important parameters such as mobility, mean free path and effective mass for these often molecular sized structures. Much focus has been placed on using the NWs in a</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
field-effect transistor (FET) geometry utilizing the high sensitivity of carrier
density inside the NWs to external electrostatic field and have enabled
applications in logic operations\textsuperscript{13,36}, non-volatile memory\textsuperscript{17} and bio-chemical
sensing\textsuperscript{37}.

Finally, in a most crucial component of this new paradigm, novel methods
are being developed to enable large-scale hierarchical assembly of NWs into
dense arrays in order for any practical application. The Lieber group has reported
methods that use confined unidirectional fluid flow\textsuperscript{38} or compression of a
Langmuir-Blodgett film\textsuperscript{39} to align NWs into large arrays along the same direction
with close-pack density, although challenges still remain to improve the end-to-
end registration of these NW arrays. A combination of developments covering all
the aspects above, from NW material synthesis, analysis of fundamental
properties to assembly strategies, should lead to exciting applications within the
field of nanoelectronics and beyond.

\textbf{1.3 Rational synthesis of one-dimensional
nanostructures}

Most nanowires were synthesized using a general and powerful
methodology based on the vapor-liquid-solid (VLS) growth mechanism, which
was first introduced to grow silicon NWs using laser ablation in 1998\textsuperscript{40,41}, while
more recently often implemented using chemical vapour deposition (CVD) for
better control over the growth temperature at milder conditions. In this
mechanism, a metal nanoparticle is used as a catalyst to nucleate and direct the 1D preferential growth of crystalline NWs. The choice of growth temperature and selection of catalyst materials can be guided by the binary phase diagrams between the metal and target NW material, such as the example shown in Fig. 1.1, where Au is chosen as catalyst for Si NW growth as it forms a eutectic liquid Au-Si alloy at temperatures above about 370 °C. In the CVD growth process, a precursor gas such as SiH₄ provides the vapor source (V) for silicon atoms. The temperature and pressure are carefully designed with respect to the decomposition of silane⁴². At this condition the decomposed precursor initially forms a liquid alloy droplet (L) with the Au nanoparticle (For an illustration, see Fig. 1.2). The Au-Si phase diagram predicts that as more and more Si precursors incorporated into the droplet, it will start to become supersaturated and solid phase Si will segregate out, initiating a crystal nucleation process, which breaks the spherical symmetry and further results in an axial growth of the solid nanowire (S), while keeping the eutectic Au/Si droplet at one end which serves as a catalyst particle. A real-time in-situ observation of vapor-liquid-solid or VLS NW growth under a transmission electron microscopy (TEM) has been reported by Wu et.al⁴³. Indeed, using this approach it has been shown early on that a broad range of NWs with homogenous composition and single crystal structures could be prepared as summarized in Table 1-1. In addition, earlier works on homogenous NW materials have demonstrated that NW diameter was indeed controlled by the size of the monodispersed nanoparticle ‘catalyst’⁴⁴, as suggested by the growth model⁴⁰, with molecular scales NWs with diameters as
small as 3 nm realized\textsuperscript{45}, that NW length was proportional to growth time\textsuperscript{46}, and significantly, that specific dopants could be incorporated into NWs to control their electronic properties (see Table 1-1). Such an ability to control the fundamental electronic properties of NWs through doping has been central to much of the progress in developing active electronic and optoelectronic nanodevices in this field.

\textbf{Figure 1.1:} Binary phase diagram of Au-Si. Image courtesy of ref. \textsuperscript{47}. 
Figure 1.2: Schematic diagram of the nanowire V-L-S growth process.

Besides the growth of homogeneous or single-component NWs, another critical breakthrough in the development of NW building blocks has been the recent demonstration of controlled growth of axial\textsuperscript{48-50} and radial heterostructures\textsuperscript{51-53}, where the composition and/or doping is modulated down to the atomic level along or perpendicular to the axes of NWs, respectively (Table. 1-1). The growth of both types of heterostructures was possible due to understanding of the growth mechanism first defined for homogeneous NW structures. In the case of axial heterostructures, one or more hetero-junctions are created within the NW by alternating the flow of different reactants and/or dopants, where this sequence can be repeated to make an arbitrary number of junctions\textsuperscript{48,49}. In the case of radial NW heterostructures, after growth and elongation of a crystalline NW core, conformal radial shell growth is carried out by altering conditions to favor homogeneous deposition on the NW surface.
versus reactant addition at the nanoparticle catalyst\textsuperscript{51-53}. Subsequent introduction of different reactants and/or dopants produces multiple shell structures of nearly arbitrary composition. The ability to prepare controlled and diverse axial and radial heterostructures sets NWs apart from other nanomaterials, such as carbon nanotubes, and combined with the excellent control of NW property in homogeneous structures represent a substantial advantage for fundamental investigation of low-dimensional physical phenomena as well as development of increasingly powerful and unique nanoscale electronic devices crucial to future application, as will be discussed in detail in this thesis.

1.4 Organization of dissertation

This dissertation focuses mainly on the charge transport properties of Germanium (Ge)/Silicon (Si) NW heterostructure and its application as nano-electro-mechanical-system (NEMS) devices. Moreover, this dissertation focuses on exploring charge transport properties and biochemical applications of Silicon NTs. All the NW and NT materials were synthesized in the laboratory at University of California San Diego specifically for this study. Therefore brief discussions on how each material was made are also included at each chapter. An outline is as follows.

Chapter 2 describes a study of exploring the origin of 1D hole gas system in undoped Ge/Si core/shell NW heterostructures. This 1D hole gas system was inspired by band structure engineering in planar 2D electron gas systems.
Transport measurements over a wide temperature range on different diameters of Ge/Si core/shell NWs confirm the formation of the hole gas. More specifically, calibrating the measurement results by using three-dimensional Poisson-Schrödinger modelling leads to a further exploration on the origin of such hole gas in an unintentionally doped NW heterostructures.

In Chapter 3, we introduce a novel three-dimensional nano-electromechanical field-effect-transistor (NEMFET). This NEMFET uses a suspended NW as a conduction channel to eliminate the limit of 60 mV/dec subthreshold-slope (SS) in conventional FETs. Moreover, with proper scaling on the geometry parameters of the NEMFET and electronic properties of the suspended NW, the novel NEMFET may be implemented to operate within sub-1V operating voltage, and within ultra-high frequency range. These two key features may enable this NEMFET as a low-power and high-speed nanoelectric device. This study has been explored theoretically via simulation and experimentally via device fabrication.

Chapter 4 presents experiments that use crystalline silicon nanotubes (Si-NTs) to provide distinctive advantages as electrical and biochemical analysis scaffolds. Through their unique morphology and electrical tunability compared to solid nanowires or amorphous/non-conductive nanotubes. Such potentials are investigated in this chapter. Gate-dependent four probe current-voltage analysis reveals electrical properties such as resistivity to differ by nearly 3 orders between crystalline and amorphous Si-NTs. Analysis of transistor transfer
characteristics yields field effect mobility of 40.0 cm²/V·s in crystalline Si-NTs. The hollow morphology also allows selective inner/outer surface functionalization and loading capability either as a carrier for molecular targets or as nanofluidic channel for biomolecular assays. We present for the first time a demonstration of internalization of fluorescent dyes (Rhodamine) and biomolecules (BSA) in Si NTs as long as 22 μm in length.

References


Chapter 2  Origin of Hole Gas in Ge/Si Core/Shell Nanowire Field Effect Transistor (FET)

Ge/Si core/shell heterostructure nanowires have been widely adopted for a multitude of applications. Recent studies have confirmed the existence of the hole gas in these heterostructures, while the origin and control of high carrier concentration in these undoped nanomaterials remain unaddressed. Here we report a comprehensive study of hole gas concentration in nanowires with varying Ge core diameters. For large core diameter nanowires, the zero-gate voltage hole carrier density increases as diameter reduces, consistent with a volume concentrating effect given the nanowires’ shrinking cross-section area compared to a slower shrinking surface circumference which might contribute to the holes. However, for diameter smaller than 10 nm, an opposite trend was observed as average carrier density drops with reducing diameter. We combine these results with three-dimensional Poisson-Schrödinger modeling to elucidate the role of surface Fermi level pinning as the origin of the hole gas. The result reveals that quantum confinement and dopant deactivation play an important role in the trend reversal of diameter dependence of the hole carrier concentration. We find that an optimum carrier density exists in nanowires with Ge core diameter between 15 and 20 nm.
2.1 Introduction

Heterostructure nanowires\textsuperscript{1-3} have been actively researched in applications such as light-emitting diodes, high-efficiency photovoltaics\textsuperscript{4-6} and high-performance transistors\textsuperscript{7-10} because of the prospect of carrier confinement in the nanoscale channel with dimensions on the same order as the carrier Fermi wavelength. In nanoscale electronic materials, doping becomes increasingly challenging due to the small number of dopant atoms and inherently large number fluctuations. Similar to the concept of two-dimensional electron gas in GaAs/AlGaAs heterostructures\textsuperscript{11} and hole gas in Ge/SiGe heterostructures\textsuperscript{12}, undoped nanowires and nanowire heterostructures rely on “electronic doping” from band bending and Fermi level pinning at the surface to generate free carriers. Therefore detrimental effects such as dopant fluctuation as well as impurity scattering can be avoided\textsuperscript{13}. One particular example, undoped Ge/Si epitaxial core/shell nanowire has exhibited one-dimensional hole gas with high carrier mobility thanks to the silicon shell serving as passivation layer. This material has been widely explored as building blocks for next generation nanoelectronics in high speed logic\textsuperscript{14}, photodetector array\textsuperscript{15} as well as tunable superconductive devices\textsuperscript{16,17}. Besides manifestation in nanowire transistor characteristics\textsuperscript{9,16,17}, experimental evidence for the existence of an one-dimensional hole gas inside the Ge core has also come from enhanced Raman scattering\textsuperscript{18} and off-axis electron holography\textsuperscript{19} and has been
corroborated with recent theoretical models\textsuperscript{20,21}. However, despite these progress, a quantitative picture for the origin of such high concentration of hole carriers in “undoped” Ge core nanowires remains elusive. Here we will use a combination of experimental and theoretical analysis to explain the origin of the hole gas.

Besides doping, another challenge for nanoscale electronic devices has been consistent control of carrier density\textsuperscript{22}. In particular for nanowire transistors, their electronic property becomes increasingly sensitive to surface/interface states and often behaves differently for nanowires of different diameter. For example, in undoped InAs nanowires, Dayeh et. al. have found that carrier density and conductance increases with decreasing diameter as the surface states-induced carriers (with their number proportional to the number of surface atoms) become more concentrated when the volume shrinks much faster than the radial circumference in smaller diameter nanowires\textsuperscript{23,24}. Meanwhile, several earlier reports have found that the same undoped InAs nanowires become increasingly resistive\textsuperscript{25,26} when diameters shrink to less than 40 nm, a complete opposite trend. It is the goal of this study to extend our understanding of diameter dependence of carrier density from core/shell Ge/Si nanowires to undoped nanowires in general and to illustrate the role of quantum confinement effects.

In this article we describe a systematic study combining simulation of quantum-confined undoped nanowire band structure through the use of
three-dimensional cylindrical Poisson-Schrödinger solver and experimental verification by using Ge/Si core/shell nanowire (NW) field effect transistors (FETs). While previous studies on Ge/Si core/shell NWs focused primarily on 10-15 nm and larger core diameters, we present the first study of diameter dependence in the Ge/Si heterostructure nanowire platform with Ge core diameters spanning from below 10 nm to 90 nm. Our results show that contribution of surface Fermi level pinning combined with quantum confinement effect is responsible for the diameter-dependency of carrier density. But to account for the measured high hole gas concentration quantitatively, other mechanisms such as impurity doping inside the Si shell must be considered simultaneously. Furthermore, our Poisson-Schrödinger solver is generalized to predict an optimum diameter for which a maximum carrier concentration can be achieved in heterostructure nanowire materials such as InAs.

2.2 Experimental Section

2.2.1 Synthesis of Ge/Si core/shell nanowires

We synthesized Ge/Si core/shell nanowires (NW) under the vapor-liquid-solid mechanism using a previously described two-step growth process by low-pressure chemical vapor deposition (LPCVD, ET2000, CVD Corporation). For 10 nm diameter Ge core ($D_{\text{core}}$) NWs, gold nanoclusters of 5 nm diameter were first deposited on Si wafers and placed on the quartz holder in the tube furnace. Ge core NWs were grown at 280 °C by flowing 2% GeH$_4$ in H$_2$ [100
standard cm³/ min (sccm)] at a total pressure of 300 torr. After the axial elongation of Ge NWs for 25 min, intrinsic Si shell was grown on the surface of the Ge NWs once the growth wafer temperature reaches 460 °C by using 2% SiH₄ in H₂ (100 sccm) at a total pressure of 100 torr for 10 min. During the transition of ramping the process temperature from 280 °C to 460 °C, 5 sccm of SiH₄ was flowed through the chamber at the total pressure of 5 torr to minimize Au diffusion. The growth rate for intrinsic Si shell at 460 °C is approximately 0.2 nm/ min. For larger core diameters, 10 nm and 20 nm gold nanoclusters were used for 25 nm and 36 nm $D_{\text{core}}$ NWs respectively and both were grown at the temperature of 300 °C during the axial elongation step.

**Figure 2.1:** Ge/ Si core/ shell nanowires.
2.2.2 Fabrication of bottom-gated FETs and characteristic measurements of FETs

NW FET devices were fabricated using the back-gated configuration, as illustrated in Figure 2.1c. All devices are fabricated on top of a degenerately doped Si substrate with a 31 nm thick thermal oxide layer. They have the same dimensions with 3 µm long channel length and 80 nm thick Ni drain/source electrodes defined by photolithography. More than 60 devices were studied from three major groups of NWs with different $D_{\text{core}}$: 10 ± 1.53, 25 ± 1.72, 36 ± 1.84 nm. Additionally, around 30 devices with a scattered $D_{\text{core}}$ distribution ranging from 50 nm to 90 nm were studied. Devices’ $I_d-V_g$ and $I_d-V_d$ characteristics were measured by HP4145B at room temperature 300 K in vacuum environment at a base pressure less than $10^{-5}$ torr using a cryogenic probe station (TTP4, Lakeshore Cryogenics).

2.2.3 Methods to extract FET properties

Device properties, including threshold voltage ($V_{th}$), subthreshold slope (SS), field-effect mobility ($\mu$) and corresponding effective hole concentration were extracted from measured device’s transfer characteristics on the basis of drift equations derived in planar MOSFETs. First, mobility (equation 2.1) at each given $V_g$ was calculated from the the slope of $I_d-V_g$ or transconductance ($g_m$).

$$\mu = \frac{g_m L^2}{V_{ds} C}$$  \hfill (2.1)
The back-gate coupling capacitance used in equation (2.1) was simulated by
a finite-element solver (COMSOL Multiphysics) under no assumption of
equipotential surface on the NWs instead of the previously widely-used
cylinder-on-a-plane analytical model which tends to overestimate the gate
capacitance when the NW diameter is close to the order of gate oxide
thickness.\footnote{28}

To extract the effective hole concentration more precisely, we built
models in COMSOL Multiphysics sharing the same dimensions as our
measured devices in experiments. Ge NW models with 8 different $D_{\text{core}}$
-ranging from 10 nm to 85 nm at doping concentration of $3 \sim 5 \times 10^{18} \text{ cm}^{-3}$
wrapped by 2 nm Si shell in the back-gated configurations were used to
simulate the actual corresponding gate capacitance per unit length at zero
gate bias.

The effective carrier concentration inside the nanowire of back-gate
nanowire FETs was decided by the experimentally measured $I_d-V_g$
transconductive curves. Analytically metallic cylinder-plane equation was
used for back-gate coupling capacitance,

$$C = \frac{2\pi \varepsilon \varepsilon_0}{\cosh^{-1}((R+h)/R)}$$

$\frac{C}{L}$, where $h$ is the gate oxide thickness, $R$ is the nanowire radius and $\varepsilon$ is the
relative dielectric constant of the oxide. Since several assumptions have
been made such as filling of the entire space with oxide and equipotential
surface of nanowire to rationalize the analytical equation, the extracted
mobility would be underestimated which would subsequently lead to the overestimation of effective carrier density on the basis of linear drift equation. To address this issue, finite-element program COMSOL Multiphysics was used to simulate the back-gate coupling capacitance with semiconductor nanowires. Two-dimensional Poisson equation was used to simulate the carrier distribution inside Ge core nanowires. The length of nanowire was assumed to be infinitely long, which means the edge effect near the drain/source electrodes was neglected. Predefined doping level in COMSOL was estimated by using the analytical equation described above. In Figure 2.2, it is clear to see that the simulated capacitances per length depend on the doping level \((5 \times 10^{18}, 3 \times 10^{18} \text{ cm}^{-3})\) of weakly at core diameters from 10 nm to 80 nm. More specifically, at such high doping level, the simulated capacitance is a weak function of the doping level. Meanwhile, the values of capacitance derived from the COMSOL simulation deviate from those based on the analytical equation. For example, at 36 nm Ge core nanowire, the difference percentage of capacitance between the doping level of \(3 \times 10^{18} \text{ cm}^{-3}\) and \(5 \times 10^{18} \text{ cm}^{-3}\) is less than 1%. Notably, the differences between analytical equation and COMSOL simulation are 16.5% for \(3 \times 10^{18} \text{ cm}^{-3}\) and 15.7% for \(5 \times 10^{18} \text{ cm}^{-3}\), respectively. Thus, based on COMSOL simulation to extract the gate-coupling capacitance could lead to more accurate estimation of field-effect mobility and effective carrier density.
Based on the simulated gate capacitance, effective hole concentration inside the core Ge nanowire was derived by,

$$ n = \frac{\sigma}{\mu e} \quad (2.3) $$

where $\sigma$ is the conductivity derived from the slope of $I_d$-$V_d$ using average dimension of the nanowire and $e$ is the elementary charge.

Another method to extract hole concentration is based on measured device’s threshold voltage ($V_{th}$), which is referred to as Vth method hereinafter. For p-type FET with a normally-on behaviour ($V_{th} > 0$), the hole concentration at $V_g = 0$ is proportional to $V_{th}$, and more specifically, with the corresponding gate capacitance simulated by COMSOL Multiphysics, the hole concentration can be derived as,
\[ n = \frac{C_{ox} V_{th}}{eV} \]  

(2.4)

where \( C_{ox} \) is the simulated gate capacitance, and \( V \) is the volume in which the holes are distributed. Assuming holes are confined within the Ge core NW, \( V \) equals \( \pi \left( \frac{D_{core}}{2} \right)^2 L \), where \( L \) is the length of the NW. If not otherwise specified, \( L \) is 3\( \mu \)m for the rest of the discussion.

### 2.2.4 Poisson-Schrodinger solver

To pinpoint the origin of hole gas inside Ge core NWs and the diameter-dependent trend of carrier concentration observed in the experiments, we established a comprehensive Poisson-Schrödinger solver in cylindrical coordinate to calculate the carrier concentration associated with surface Fermi level pinning, unintentional dopants, quantum confinement effect and dopant deactivation (Fig. 2.1a). Here we assumed an isotropic hole effective mass for both Ge and Si, which has previous been shown to yield less than 3% error for the lowest subband position inside a Ge nanowire channel compared to a fully anisotropic model\textsuperscript{29}. To locate \( E_F \) without additional gate bias (at \( V_g = 0 \)), charge neutrality equation, \( n_{core} + p_{core} + n_{shell} + p_{shell} + \text{shell dopants} + Q_f = 0 \), needs to be met (\( n_{core} \) and \( p_{core} \) are electron and hole concentration inside Ge channel. \( n_{shell} \) and \( p_{shell} \) are electron and hole concentration distributed over Si shell which are induced by surface states, \( D_{it} \). Shell dopants and fixed charge \( Q_f \) within the native SiO\textsubscript{x} layer are both set as zero unless otherwise specified).
2.3 Results and Discussions

2.3.1 Device characteristics

The transistor characteristics, $I_d-V_{gs}$, of 10 nm and 25 nm $D_{\text{core}}$ devices exhibit distinctive differences when temperature varies from 300 K to 77 K. As shown in Figure 2a, the threshold voltage $V_{th}$ shifts negatively at lower temperatures. The magnitude of this shift ($\Delta V_{th}$), behaves differently for different diameters. From 300 K to 77 K, $\Delta V_{th} = 2$ V for 10 nm and 4.5 V for 25 nm, respectively. Simply speaking, $V_{th}$ is more sensitive to temperature change in larger core diameter NWs. Furthermore, figure 2b shows that peak field-effect mobility values increase dramatically by 5 fold when temperature is decreased from 300 K to 77 K ($269 \text{ cm}^2/\text{V} \cdot \text{s}$ to $1352 \text{ cm}^2/\text{V} \cdot \text{s}$) for the 25 nm device as a result of decreased acoustic phonon scattering at lower temperatures. In comparison, relatively small mobility increase of ~50% ($101 \text{ cm}^2/\text{V} \cdot \text{s}$ to $152 \text{ cm}^2/\text{V} \cdot \text{s}$) was observed for the 10 nm device. The lack of strong temperature dependence in peak mobility in the $D_{\text{core}} = 10$ nm device suggest that in such smaller diameters surface or impurity scattering is the dominating mechanism while the 25 nm device is dominated by acoustic phonon scattering.
Figure 2.3: Temperature-dependent and diameter-dependent hole transport assessment.

It is important to point out that different from a previous study\textsuperscript{30}, a diameter-dependent mobility has been observed. Our smallest diameter NWs ($D_{\text{core}} = 10$ nm) have on average a mobility of less than 40% of the 25 nm NWs at all temperatures. This dependency of mobility on diameter is
summarized in Figure 2.3c where at 300 K, $\mu$ decreases almost linearly from an average value of 199 cm$^2$/V·s in 36 nm $D_{\text{core}}$ NWs (blue) to 97 cm$^2$/V·s in 10 nm $D_{\text{core}}$ NWs (green), suggesting enhanced surface scattering in these small diameter NWs. Such behavior in small diameter nanowire channel has been previously noted in other NW systems$^{23,25}$. Further studies on the interplay between phonon and boundary scattering in these quantum-confined nanostructures will be needed towards rational design of a high mobility semiconductor nanowire channel.
Figure 2.4: (a) Id-Vg characteristics of different Ge core diameter ($D_{core}$) at low drain bias voltages. (b) Normalized Vth histograms and Gaussian fit curves for Vth distribution. (c) Extracted carrier density (hole concentration) and simulated hole concentration.
At room temperature, $I_d-V_g$ properties of representative field-effect transistors (FETs) with $D_{\text{core}}$ of 10 nm, 25 nm and 36 nm are shown in Figure 2.4a. All devices exhibit excellent Ohmic contact characteristics without post-annealing. For NWs with $D_{\text{core}} = 25$ nm and 36 nm, devices show “normally-on” behaviors at zero gate bias which means nanowires are working in the accumulation mode with hole carriers already populating transistors’ conduction channels. When $D_{\text{core}}$ decreases from 36 nm to 25 nm (red arrow), the threshold voltage ($V_{\text{th}}$) shifts to the left. Such $V_{\text{th}}$ shift from $D_{\text{core}} = 36$ nm to 25 nm may imply that a difference exists between the amount of hole carriers accumulated within the NW with $D_{\text{core}} = 25$ nm and $D_{\text{core}} = 36$ nm respectively. When $D_{\text{core}}$ further decreases from 25 nm to 10 nm (green arrow), $V_{\text{th}}$ further shifts in the negative direction and the device behaves closer to a “normally-off” state or so-called depletion mode: while no gate bias applied, only a relatively small amount of carriers exist inside the conduction channel. Such steep drop-off of $V_{\text{th}}$ shift versus decreasing Ge core diameter is reminiscent of the reports in undoped InAs nanowires as mentioned above.

Moreover, Figure 2.4b illustrates a histogram of $V_{\text{th}}$ distributions for averaged $D_{\text{core}}$ at 10 nm (28 devices) and 25 nm (25 devices). Although the diameter standard deviations are similar for 10 nm (1.53 nm) $D_{\text{core}}$ and 25 nm (1.72 nm) $D_{\text{core}}$ devices, the smaller diameter FETs exhibit a much broader $V_{\text{th}}$ distribution, suggesting that in the case of 10 nm $D_{\text{core}}$ NWs, $V_{\text{th}}$ and the associated hole carrier density are much more sensitive to fluctuations of Ge
Besides large fluctuations for small diameter NWs, our diameter-dependent measurement data of $V_{th}$ in Ge/Si core/shell NWs provides unique evidence on the amount and origin of such hole carriers when no intentional doping was introduced in either the core or the shell layer. Figure 2.4c plots a summary of all the extracted hole carrier concentrations from our measured 25 nm and larger $D_{core}$ devices. The core diameters for each device were individually verified by measuring the total diameters under scanning electron microscope (SEM) and subtracting a nominal shell thickness 2 nm for all. The hole concentrations at $V_g = 0$ are calculated using the $V_{th}$ method is consistent with those from the $n_{\mu}$ method (with a maximum difference of 7% between this two methods). With a reduction of $D_{core}$ from 36 nm to 25 nm, the average concentration increased from $4.11\pm1.11\times10^{18}$ cm$^{-3}$ to $5.26\pm1.14\times10^{18}$ cm$^{-3}$, despite a reduction in $V_{th}$. Such enhancement of concentration is consistent with a volume-concentrating effect previous reported in InAs studies$^{23,26}$ and is a result of the wire cross-section area shrinking more rapidly than surface circumference with diameter. Generally, this increasing concentration with decreasing diameter ($D_{core}$) approximately follows the trend of $1/D_{core}$.

However, by further shrinking diameters to 10 nm or smaller, we find that only part (19 out of 28) of the measured devices exhibit normally-on behaviors (i.e., $V_{th} > 0$). Since the hole concentration of negative $V_{th}$ devices at zero gate bias is nearly zero, we averaged $V_{th}$ for the group of all...
measured 10 nm devices to yield an averaged hole concentration of 3.06±6.46×10^{18} \text{ cm}^{-3} using the $V_{\text{th}}$ method. Therefore shrinking diameters to 10 nm has led to a drop of carrier density compared to 25 nm. Meanwhile, compared to the larger diameter groups, the 10 nm diameter devices also show a much larger standard deviation of the hole concentration. The large fluctuation alludes to a very high sensitivity of hole concentration to diameter variation in such small diameter region. A further exploration on the origin of the hole concentration is needed to explain the drop and the big fluctuation of hole concentration for the 10 nm diameter group.

**2.3.2 Simulation results (Poisson-Schrödinger Solver)**

Hole carriers at room temperature are in principle dictated by the relative position of the Fermi level and valance band top. The observed trend reversal of carrier concentration increasing from those in large diameters to 25 nm core diameter, then decreasing from 25 nm to < 10 nm suggests that a closer look at how the $E_F$ varies relative to $E_V$ inside the Ge core channel at different diameters and the impacts of other possible mechanisms in addition to fixed surface states should be investigated by a comprehensive and general simulator. Therefore we developed a cylindrical, three-dimensional Poisson-Schrödinger solver.
Figure 2.5: Results from three-dimensional Poisson-Schrödinger solver.

Simulation result of $E_F$ (Fermi level) vs. $D_{\text{core}}$ at room temperature (300 K) is shown in Figure 2.5a. We set the surface state density, $D_{\text{it}}$, at the outer surface of Si shell at $3 \times 10^{13}$ cm$^{-2}$eV$^{-1}$ and $E_{\text{neu}}$ (charge neutral energy level of surface states) at negative 0.58 eV (with reference point set at valence band in outer Si shell) to match the experiment results. Note that all energy levels refer to hole carriers, hence Ge valance band appears lower than Si and -0.58 eV is close to silicon mid-gap in our sign convention (Fig. 2.5 insets). $E_F$ value lies close to $E_{\text{neu}}$ for the smallest $D_{\text{core}}$ (top inset, Fig. 2.5) due to Fermi level pinning. As $D_{\text{core}}$ raises, $E_F$ slightly lowers toward the mid-gap, becoming closer to that in bulk Ge. Simply put, effects from surface states on $E_F$ become less important in large diameter wires given the same fixed surface states density. In large diameter devices, to meet charge neutrality, carrier concentration would simply become inversely proportional to $D_{\text{core}}$. 
The bottom inset to Figure 2.5 shows how the topmost valance band position \( E_V \) (typically at center of the nanowire) changes with \( D_{\text{core}} \). For small wires with diameter below \( \sim 18 \) nm, \( E_V \) increases drastically with decreasing \( D_{\text{core}} \) due to the quantum confinement effect. Absent of significant quantum effect with increasing \( D_{\text{core}} \) beyond 15 nm, trend of \( E_V \) becomes relatively flat.

The difference between our calculated \( E_F \) and \( E_V \) or \( E_F - E_V \) (Fig. 2.5, main panel) provides an important clue on the diameter-dependent hole carrier concentration inside the conduction channel under the familiar carrier statistics equation, 

\[
p = N_V \exp\left[ \frac{(E_V - E_F)}{kT} \right],
\]

where \( N_V \) means the effective density of states function in the valence band and \( kT \) is the thermal energy.

\( E_V - E_F \) first descends sharply as \( D_{\text{core}} \) increases from the smallest diameter until the quantum limited condition (\( D_{\text{core}} \sim 18 \) nm). Beyond this small \( D_{\text{core}} \) limit, \( E_V - E_F \) gradually increases as \( D_{\text{core}} \) grows. This trend reversal is in line with the observed trend of decreasing carrier density with increasing \( D_{\text{core}} \) in experiments (Figure 2.4c).

The steep sensitivity of \( E_V - E_F \) vs. \( D_{\text{core}} \) below the quantum confinement limited diameter also sheds light on the observation of a very broad distribution of \( V_{th} \) in smallest wires with \( D_{\text{core}} \) below 15 nm, as shown in Figure 2.3b. Even small fluctuations of \( \sim 2 \) nm in the core diameter will lead to a 60% difference in the resulting hole carrier concentrations. Such diameter fluctuation sensitivity is therefore a direct evidence of quantum effects on performance of nanometer scale devices is region. For \( D_{\text{core}} = 25 \) nm, quantum effect becomes less significant and can be neglected so that the
distribution of $V_{th}$ observed in experiments is comparably much narrower.

Hitherto, the $E_V-E_F$ diameter dependence seemingly follows qualitatively the experimental results based on the simple assumption of the simulation in Fig. 2.5 that the accumulated hold gas inside Ge core NWs directly results from surface charge states. However, upon closer examination there exists quantitative discrepancies between measured and simulated carrier densities. For example, with $D_{core} = 25$ nm, the simulated result using $D_{it} = 3 \times 10^{13} \text{ cm}^{-2}\text{eV}^{-1}$ yields only a hole concentration at $2.1 \times 10^{17}$ cm$^{-3}$, more than an order underestimated than the average extracted value from experiment (by $V_{th}$ method, the average of the extracted hole concentration is $5.26 \times 10^{18}$ cm$^{-3}$; by neµ method, the average of the extracted hole concentration is $4.88 \times 10^{18}$ cm$^{-3}$). The surface states density, $3 \times 10^{13}$ cm$^{-2}\text{eV}^{-1}$, we chose based on experimental conditions for the simulation in Fig. 2.5 is in itself already very high compared to typical semiconductor device standards, presumably due to the quality of our as grown materials.
Yet simulations of carrier density versus $D_{\text{core}}$ with surface state densities $D_{\text{it}}$ pushed up to as high as $10^{14}$ cm$^{-2}$eV$^{-1}$ (Figure 2.6a) still fail to yield carrier densities in the order of $10^{18}$ cm$^{-3}$. In fact the calculated peak density at $D_{\text{core}} = 26$ nm is still 20x smaller compared to extracted experiment data. Although Fermi level pinning caused by surface states has been so far
widely considered as the main and the only contribution to the one-dimensional hole gas accumulation in intrinsic Ge/Si core/shell NWs, our results suggest that other mechanisms may need to be explored to account for the high density hole gas.

2.3.3 Further mechanisms (Dopant deactivation)

It has been reported that even though no intentional dopants was introduced during the VLS growth of intrinsic core/shell Ge/Si or InAs NWs, impurities such as Au atoms may likely form unintentional doping centres affecting device performance\textsuperscript{31,32}. Particularly, in the case of core/shell Ge/Si NWs, a study\textsuperscript{33} has reported the effect of Au diffusion leading to the formation of unintentional Au dopants during depositing Si shell as a result of the disparity in growth temperature for Ge core and Si shell.

But before we model the effect of Au dopants in the intrinsic Si shell, care must be taken in light of the special electrostatic environment these donors reside in, because surrounding each donor atom is less than 2 nm thick Si shell, or only dozens of rows of silicon atoms, outside which is air. The dielectric mismatch between air and Si around each dopant atom will dramatically affect their activation energies. Such so called “dopant deactivation” effect has recently been studied by Diarra\textsuperscript{34} and Björk\textsuperscript{35}. Based on their theoretical model, an expression of the shift in impurity ionization energy can be expressed as equation (2.5),

\[
E_I - E_I^0 \approx \frac{2e^2}{\epsilon_S \epsilon_S - \epsilon_{air}} \frac{\epsilon_S - \epsilon_{air} \epsilon_S + \epsilon_{air}}{F}\left(\frac{\epsilon_S}{\epsilon_{air}}\right)
\]  

(2.5)
where $E_i$ is the diameter-dependent ionization energy, $E_i^0$ is the bulk ionization energy, $\varepsilon_s$ is the semiconductor NW’s dielectric constant, $\varepsilon_{\text{air}}$ is the dielectric constant of surrounding environment, $r$ is the radius of NW, $e$ is the elementary charge, and $F$ is a polynomial function of the dielectric ratio of the wire to the surroundings\textsuperscript{36}. According to ref. 35, dopant deactivation results in a 50% reduction of carrier density for a Si NW with radius of 15 nm compared to in bulk.

Finally, we integrate both the effects of unintentional dopants and dopant deactivation into our Poisson-Schrödinger solver. Dopant density $N_a$, dopant energy level $E_a$ and fixed surface state density $D_{it}$ are all fitting parameters. Figure 2.6b shows the simulated carrier density with and without including dopant deactivation effect respectively by using optimized fitting parameters. First of all, results without dopant deactivation show much higher carrier density (2~3x experimental value) but more importantly all fail to reproduce a drop in carrier density in small diameter nanowires. Only a modest reduction in density for diameters < 10 nm due to very strong quantum confinement was found (red curve, Fig. 2.6b). Dopant deactivation is therefore necessary to be included (blue curve) whose result shows a significant down trend in carrier density while decreasing $D_{\text{core}}$ below ~18 nm, similar to experimental observations (Fig. 2.4, orange dashed curve). The peak density value, at 18 nm, of $5.09 \times 10^{18}$ cm\textsuperscript{-3} also agrees with experiment.
Figure 2.7: Comparisons of band diagram of valence band and carrier distribution of Ge/Si core/shell NW in different $D_{\text{core}}$ along the radial direction (axis) originating from center of the nanowires.

Figure 2.7 shows detailed band diagrams and radial carrier distributions of Ge/Si core/shell NWs in our final simulation results ($D_{\text{core}} = 8$ nm, 20 nm, 30 nm, 60 nm). The blue curve represents the valence band inside of the Ge/Si core/shell NW. The red curve is the Fermi level. For the smallest wire with $D_{\text{core}} = 8$ nm (the tail when $D_{\text{core}}$ below 15 nm), the valence band is relatively flat and the accumulated holes inside the Ge core are confined near the centre of the Ge core. When $D_{\text{core}} = 20$ nm, the valence band of Ge core bends at the Ge/Si interface. The bending of valence band
becomes more significant with increasing $D_{\text{core}}$ (when $D_{\text{core}} = 30 \text{ nm, } 60 \text{ nm}$) due to stronger electric field at the interface and in turn causes the hole charge carriers to be accumulated near the Ge/Si interface.

2.4 Conclusion

In conclusion, an extensive characterization of diameter-dependent properties of Ge/Si core/shell NWs are presented through both experimental transfer characteristics measurements and simulation using a Poisson─Schrödinger solver. Specifically, we observed distinctively different device $V_{\text{th}}$ distributions and carrier densities at room temperature in diameter-dependent $I_d-V_g$ measurements. A comparison with theoretical modelling results suggests that the origin of one-dimensional hole carrier gas inside the undoped Ge nanowire channel is due to a combination of surface states Fermi level pinning, dopant deactivation, and quantum confinement effects. Below $\sim 18 \text{ nm}$, quantum confinement in the Ge core dramatically shifts the Ge valence band, leading to reduction of carrier densities. Above this diameter value, however, the carrier density slowly reduces upon increasing core diameters due simply to the difference in the volume scaling vs. surface area scaling. There therefore exists an optimum diameter range, in this case between 15$\sim$20 nm, for which one can optimize the accumulation of hole carriers in undoped nanowire structures whereby the free carriers come from surface donors/acceptors. Our solver could be generalized to predict
quantum threshold limit for any intrinsic NWs for future thermoelectric and nanoelectronic applications.

Acknowledgments

Chapter 2 is in part a reprint of “Origin and diameter dependent of hole gas in Ge/Si core/shell nanowires“, submitted to Nanoscale (2014).

References


Chapter 3
Nano-Electro-Mechanical Field Effect Transistor (NEMFET)

3.1 Introduction

For over 30 years, advanced logic complementary metal-oxide-semiconductor (CMOS) technology has been enabled to pack twice as many field effect transistors (FETs) onto a chip every 18-24 months, in what has come to be known as “Moore’s law”\(^1\). This scaling technology trend to double devices’ density and performance has resulted in an exponential increase in the information processing capability per unit area on the chip. On the other hand, as CMOS scales from generation to generation, power consumption increases proportionately to increasing trend of density and performance.

More specifically, the power consumption can be divided to the dynamic power consumption and the static power consumption. The dynamic power, which arises from the repeated capacitance charge and discharge on the output of the billions of gates in today’s integrated circuit (IC) chips, can be scaled down with gate length shrinkage successfully with the principle of constant-field scaling\(^2\), but the static power consumption has a limitation as \(I_{\text{off}}\) can’t be scale down due to its thermodynamic nature\(^3,4\).
Controlling \( I_{off} \) is based on sub-threshold swing (SS) value of the device. Generally, conventional CMOS devices have a minimum limitation of SS at 60 mV/dec. A few different types of device was introduced to overcome this thermodynamic limit of CMOS using band to band tunneling, impact ionization, and nano-electro-mechanical system (NEMS).

In this chapter, I will present a nano-electro-mechanical field effect transistor (NEMFET) using a nanowire (NW) as a suspended channel. The suspended channel also functions as a conduction channel of the NEMFET. As such, a mechanical degree of freedom can be integrated into the design of the NEMFET, which may provide a possibility to overcome the 60 mV/dec SS limitation.

### 3.2 Static Power Consumption and Sub-threshold Swing

The static power consumption became one of the key limiting factors on the shrinkage of feature size of VLSI circuit using CMOS technology\(^5\). An equation that T. Mudge presented defines overall power consumption as the sum of dynamic and static power\(^6\),

\[
P = ACV^2 f + V I_{leak}
\]

(3.1)

where the first term is the dynamic power lost from charging and discharging the processor’s capacitive loads, and the second term is the static power lost due to leakage current, \( I_{leak} \). \( V \) is the supply voltage, \( f \) means the operation
frequency, and $I_{\text{leak}}$ is the leakage current in off state. In Equation (3.1), its $V^2$ factor suggests deducing supply voltage as the most effective way to decrease power consumption, and $V_{dd}$ has been scaled down successfully less than 1V with the continuous efforts to shrink the device dimension and circuit perspectives. But, this shrinkage of device geometries exacerbate leakage current, so static power begins to dominate the power consumption equation in IC design. $I_{\text{leak}}$ can be expressed as

$$I_{\text{leak}} = I_{\text{sub}} + I_{\text{ox}}$$ (3.2)

where $I_{\text{sub}}$ is subthreshold leakage current and $I_{\text{ox}}$ is the gate oxide leakage current. $I_{\text{ox}}$ is very important parameters in CMOS technology, but as it’s not a main topic of this thesis, let’s concentrate on $I_{\text{sub}}$ term.
Figure 3.1: Schematic $V_g$-$I_g$ curve of n-MOSFET. The $I_{off}$ with same $I_{on}$ can be decreased with two ways.

Figure 3.1 shows the representative $V_g$-$I_g$ curve of n-MOSFET in semi-log scale. In the figure, $I_{off}$ is the $I_{sub}$ at $V_g=0$. In given $V_g$-$I_g$ curve, there are two simple way to decrease $I_{off}$ current with maintaining same $I_{on}$. The first is increasing $V_{th}$, marked as line (1), and the second is decreasing the sub-threshold swing (SS), marked as line (2). But increasing $V_{th}$, the device speed is decreased in return. The Equation (3.3) shows the relation between operating frequency $f$ and $V_{th}$ of the device$^6$,

$$f \propto \frac{(V-V_{th})^\alpha}{V}$$  \hspace{1cm} (3.3)
where $V$ is the supply voltage, and exponent $\alpha$ is an experimentally derived constant. If we consider the supply voltage $V$ is continuously scaled down, and $V_{th}$ term is inside of exponential term, increasing $V_{th}$ can’t be a solution for the $I_{off}$ decrease.

Sub-threshold swing indicates how fast the channel can be off with the gate signal. SS can be expressed with the equation below

$$SS = \left(\frac{d(\log_{10} I_d)}{dV_g}\right)^{-1} = 2.3 \frac{mkT}{q} = 2.3 \frac{kT}{q} \left(1 + \frac{C_{dm}}{C_{ox}}\right)$$  \hspace{1cm} (3.4)

, and typically SS is between 70-100 mV/dec as $m = 1.1$~1.5 practically. Even for an ideal switch, $m = 1$, SS can’t be decreased under 60 mV/dec at room temperature. Such limitation on the minimum SS value results from the thermally activated diffusion current terms over the channel energy barrier.

Figure 3.2 shows the different switching behavior of ideal switch and real transistor. This thermodynamic limit of SS prohibits the further decrease of $I_{off}$ in CMOS technology.
Referring back to Figure 3.1, the $I_{\text{off}}$ is varied with SS exponentially.

$$I_{\text{off}} = I_{\text{th}} \times 10^{\frac{-V_{\text{th}}}{SS}}$$ \hspace{1cm} (3.5)

And,

$$P_{\text{static}} = V_{\text{leak}} \propto \exp\left(-\frac{V_{\text{th}}}{SS}\right)$$ \hspace{1cm} (3.6)

In conclusion, the static power consumption varied exponentially with SS of the device.

### 3.3 Breakthrough of Sub-threshold Swing Limitation

As discussed above, decreasing SS is the most efficient way to suppress the static power consumption. However, at room temperature, the
sub-threshold swing (SS), the steepest transition rate for turning off the transistor, is limited to 60 mV/decade. This is due to a constant fundamental thermal dynamical limit \((k_B T/q)\) that is not scalable with reduced dimensions. This limitation is inherent to CMOS because its off-state is governed by thermally activated diffusive current over a gate-controlled potential barrier. There have been some demonstrations of novel switches and FETs to overcome the thermodynamic limits of MOSFETs using band-to-band tunneling\(^7\)\(^{-10}\), impact ionization\(^11\)\(^{-14}\), or nano-electro-mechanical–system (NEMS)\(^15\)\(^{-18}\).

Tunneling FET (TFET) is a gated p-i-n diode operating under reverse bias, as shown in Fig 3.3\(^10\). Different from MOSFET using thermal carrier injection, TFET use band-to-band tunneling phenomenon as a source carrier injection mechanism. In OFF state, the gap between conduction band \((E_c)\) and valance band \((E_v)\) is so wide that tunneling current is limited with only very small leakage current. With the increase of gate voltage, \(E_c\) and \(E_v\) come to close enough to allow a huge tunneling current. As the carrier injection mechanism is different from MOSFET, TFET can achieve the steep SS value lower than 60 mV/dec. However, SS increases rapidly with gate voltage and thus steep SS only occurs within limited current, or gate voltage range and the average SS is still relatively high\(^7\). In addition, low \(I_{on}\) is another issue due to the poor tunneling probability of silicon\(^19\).
Figure 3.3: Tunneling Field Effect Transistor with L-shape gate⁸, (a) Schematic structure and band diagram of TFET, (b) Transfer curve of the fabricated TFET. The SS value is 52.8 mV/dec at room temperature.

Figure 3.4: I-MOS¹⁴, (a) Basic structure and band diagram in the On/Off states of the n-channel I-MOS, (b) Transfer curve of the fabricated device with 7.5mV/dec sub-threshold swing.

Impact-Ionization MOS (IMOS) uses modulation of the breakdown voltage of a gated p-i-n structure in order to switch from OFF to ON state and vice versa. Since impact-ionization is an abrupt function of the electric field,
the device has a subthreshold slope much lower than $kT/q^{12}$. Figure 3.4 shows the basic structure and operating principle of the n-channel I-MOS$^{14}$. I-MOS has two big difference compared with MOSFET, opposite doping in the source/drain and the $i$-region which is not completely overlapped by the gate. In the OFF state, when the gate is biased below the threshold voltage, in the source cannot acquire enough energy for impact ionization. Thus, the leakage current is dominated by the reverse current of the $p-i-n$ diode. However, with the gate voltage above the threshold, the ON state utilizes the electrons which acquire the enough energy for the impact ionization that gives rise to avalanche breakdown. As the $p-n$ junction barrier lowering is not the mechanism of current flow control, I-MOS can realize the subthreshold swing less than $60mV/dec$ in room temperature. But, it needs high supply voltage to induce avalanched breakdown and process difficulty in self-aligned fabrication.

### 3.4 Nano-Electro-Mechanical System (NEMS)

NEMS is the device exploiting the mechanical degree of freedom with movable component like gate or channel. NEMS architectures are being explored as components in various applications such as switches, actuators, resonators, and sensors. An emphasis on discussing NEMS switch will be provided as follows in this section.
3.4.1 Variations of NEMS Switch

The NEMS switch is based on an old and common idea in MEMS using pull-in/pull-out movement of suspended components. Taking advantages of such idea, NEMS technologies are being investigated because they offer reduced leakage currents which leads to reduced power consumption and improved $I_{on}/I_{off}$ ratio. Moreover, the NEMS switch is less insensitive to radiation, temperature and external electric field. Thus, NEMS switches are actively explored as components in a plurality of devices, such as transistors, memories, logic and sensor applications.

The previous studies have shown the abrupt on/off switching, and minimized SS with movable gate or channel with various materials like metal, carbon nanotube (CNT), silicon carbide (SiC), nanowire (NW), and various structure like crossbar, cantilever, suspended channel, or vertical pillar.

![Figure 3.5: 3-terminal NEM relay using suspended CNT cantilever](image)

Figure 3.5: 3-terminal NEM relay using suspended CNT cantilever\textsuperscript{18}, (a) Basic structure, (b) Transfer curve of the fabricated device.
Figure 3.5 is 3-terminal CNT nano relay presented by S. Lee\textsuperscript{18}. The CNT channel is suspended (ground) over drain and gate electrode. Drain electrode is maintained to $V_{dd}$, and gate is swept to pull-in and pull-out the suspended cantilever channel. With the gate voltage, the cantilever can touch with drain electrode only, or make a contact with the gate, too. The $V_{sg}$ vs. $I_s(=I_{ds}+I_{gs})$ graph (Figure 3.5(b)) shows this behavior clearly.

\begin{center}
\begin{figure}[h]
\begin{minipage}{0.5\textwidth}
\centering
\includegraphics[width=\textwidth]{figure36a}
\end{minipage}\hfill
\begin{minipage}{0.5\textwidth}
\centering
\includegraphics[width=\textwidth]{figure36b}
\end{minipage}
\caption{3-terminal NEM switch using suspended CNT channel\textsuperscript{16}, (a) 45\textdegree tilted SEM image of fabricated NEM switch with triode structure, (b) Transfer curve of the fabricated device with $V_d=0.5V$.}
\end{figure}
\end{center}
Figure 3.6 illustrates 3-terminal NEM-switch with suspended CNT channel\textsuperscript{16}. The CNT channel supported by drain electrode in both end is suspended in the air, and two symmetrical side electrodes (source and gate) are self-aligned over the suspended CNT channel. The CNT acts as a self-align mask during the source/gate electrode formation process. The drain set to 0.5V and source is grounded. In $V_{gs}$-$I_{ds}$ characteristic (Figure 3.5 (b)), the abrupt switching arises at $V_g$=3.6V with $I_{on}/I_{off}=10^4$. This device can be used as 2-terminal NEMS-switch, too.

W. Jang. presented 2-terminal NEM-switch with suspended TiN thin film cantilever structure\textsuperscript{21}. In Figure 3.7, the thin TiN cantilever is suspended over TiN bottom electrode with 15$nm$ air gap. The switch shows ideal on/off characteristic with $I_{on}/I_{off} = 10^5$. The switch demonstrates the multiple
switching behavior over hundreds of ac and dc bias condition in air ambient. Another advantage of this device is that they use the CMOS process.

**Figure 3.8**: 2 or 3 terminal NEM switch using vertical CNT\(^{22}\), (a) 45\(^{\circ}\) tilted SEM image of fabricated NEM switch, (b) Transfer curve of the fabricated device with 3-terminal, (c) Transfer curve of 2-terminal, Inset of (b),(c) is the SEM image in ON state of each device.

Different from the planar structure NEM-switches, J. Jang suggested NEM-switch architecture with vertically aligned CNT\(^{22}\). Figure 3.8(a) is the schematic of the device. The device uses a pair (2-terminal) or 3 (3-terminal) of vertically aligned CNT pillar as electrode. In case of 2-terminal, one terminal is grounded (source), and the other terminal is biased (gate). With this condition, the top of two electrodes come to contact due to the electrostatic force. As for the 3 terminal device, the adjacent electrodes are biased as same polarity, and the rest electrode is grounded. Because of the repulsive force between two electrodes biased same polarity, the electrode in the middle comes to contact to the grounded electrode. Figure 3.8(b) is the
switching property of 2-terminal device, and Figure 3.8(c) is that of the 3-terminal device. Both graphs show the abrupt switching property of device clearly.

Figure 3.9: 4-terminal relay device with suspended metal gate\textsuperscript{23}, (a) Schematic of device, (b) Pull-in occurs at $V_g=6.1V$ with $SS=1mV$, (c) Pull-out occurs at $V_g=5V$.

Figure 3.9(a) illustrates 4-terminal relay technology for complementary logic circuit presented by R. Nathanael\textsuperscript{23}. NEMS relay technology has been proposed for ultra-low-power digital integrated circuit application. This is because the relay is an ideal switch with abrupt on/off switching and zero off current, so that the operating voltage ($V_{dd}$) can be zero in principle. However, there are two critical problems to solve for conventional 3-terminal NEMS relay: reliability problem comes from surface wear and stiction-induced failure and low switching voltage. They used a highly reliable mechanical contact technology employing tungsten electrodes with TiO$_2$ coating and 4-terminal design adopting body electrode.
Figure 3.10: Low voltage 2-terminal NEM switch suspended metalized SiC nanowire²⁴.

Figure 3.10 shows 2-terminal switch using suspended SiC nanowire channel²⁴. The suspended SiC nanowire and side gate is fabricated top-down process with E-beam lithography and etching process. The nano-beam size is controlled to 55 nm width, 50 nm height, 20 um length including 30 nm Al top metallization layer to gain high $I_{on}$ current. The final gap was 30 nm with various side-gate width like tip (tens of nm) and planar (8 um, 15 um). They demonstrate the sharp pull-in behavior with high $I_{on}/I_{off}$ rate successfully. Furthermore, they showed the possibility of multiple pull-in stage with the various width of side gate in single device.

3.4.2 Scaling Challenges of NEMS Devices
In many types of NEM switches reviewed previous, NEM switch has a limitation in large-scale production due to its bottom-up process scheme or use of special process like manipulator to place nano-structures in proper position. And the use of E-beam lithography technique which is used to form contacts to randomly distributed nanostructures prohibits the NEM switch device from wafer-scale fabrication process. To enhance NEM switch’s application, we need special technique to overcome this issue.

The most straightforward way is to make large-scale array of NEM switch using top-down process which consist of “deposition-patterning-etch” steps. At first, making the pattern of moving part over the fixed bias part covered with sacrificial layer with photolithography and dry etch process. After finishing the top layer, vapor HF etching process can be used to release the moving part of NEM switch. The conventional deposition, photo lithography, and dry etching process are needed. Figure 3.11 is the pipe-clip shape sub-1V NEM switch using top-down process by Lee\textsuperscript{25}. 

In case of Si or metal layer as moving part, the top-down process can be used for NEM switch fabrication, but other nanostructures like carbon nanotube, graphene, or nanowire with various materials are hard to be used with top-down process. The other process like pattern-and-transfer, direct self assemble, or nanostructure ensemble can be an alternative solution for the large-scale array fabrication of NEM switch.

**Figure 3.11**: Pipe-clip shaped NEM switch using top-down process. (a) Schematic process flow, (b) Cross section TEM image of the device.\(^{25}\)
Figure 3.12: Large-scale graphene sheet resonator. (a) Angled scanning electron microscopy (SEM) image of Type A suspended graphene membranes over trenches in silicon oxide. (b) Angled SEM of an array of graphene membranes\textsuperscript{26}. 

A. M. Zande reported large-scale arrays of graphene resonator in 2010\textsuperscript{26}. They realized fabrication of wafer-scale NEMS arrays using array growth and transfer process\textsuperscript{27}. Figure 3.12 shows the SEM images of large-scale graphene sheet resonators. The graphene sheet was deposited on Cu foil using CVD method. Then graphene sheet was transferred to PMMA layer and released on the patterned silicon oxide wafer with appropriate alignment.
Figure 3.13: Direct assembly pattern of SWNT with AFM (a),(b) parallel pattern, (c) Random line structure\textsuperscript{28}.

Direct assembly of nanostructure can be another candidate for the large-scale array fabrication. Y. Wang, et. al. shows the patterned single wall nanotube array using a direct assembly\textsuperscript{28} method. The direct assembling uses the attraction force between the nanostructure and specially terminated substrate surface. They used nanopatterned affinity templates, in this case COOH-terminated self-assembly monolayer (COOH-SAM) and CH\textsubscript{3}-terminated self-assembly monolayer (CH\textsubscript{2}-SAM). The SWNT have attraction to COOH-SAM only, and this property make it possible to place SWNTS in accurate pre-patterned position.
J. W. Ward, et. al. demonstrated NEM switch using nanostructure ensemble. The monolayer of SWNT was spin coated over the pre-patterned electrode layer with sacrificial lay. With the photolithography and lift-off process was used to pattern and form a clamping electrode with alignment process. Figure 3.14 is the schematic of process flown and SEM image of fabricated device.

Many possible ways are being developed for the large-scale fabrication of NEM switch including traditional top-down process, the encapsulation can be the serious obstacle in NEM switch technology. Many of results of NEM switch so far were operated in vacuum. When one considers sticking, oxidation, capillary force from the humidity of air, particles, or contamination, NEM switch in the air is still a big challenge. The
encapsulation increases the device size and the complexity of the process at the same time.

### 3.4.3 Reliability Issue

Reliability is one of the most critical issues of NEM switch as we must consider the mechanical and electrical reliability at the same time. Furthermore, the mechanical motion of moving elements and the repeated contact-detach motion at the same contact position can make various failure modes: stiction, burn-out from electrical discharge, wear (exacerbated easily with electrical discharge), fatigue, fracture, or combinations herein.

Among them, stiction and burn-out are the most common failure mechanism in NEM switch. Stiction is the moving channel which comes to attach to the bias electrode, and doesn’t be detached after removal of bias. In nano-scale device, the relative magnitudes of van Der Waals and elastic forces, and in significance of surface roughness relative to the dimensions of the active elements are should be considered more seriously\(^\text{20}\). Coating the surface of electrode with thin films which can reduce adhesion\(^\text{30}\), or changing of electrode material having less affinity with suspended channel can improve the resistance against stiction problem\(^\text{31}\).

Burn-out is the localized melting of contact point in NEM switch. The charges stored during the off state come to flow through the electrode in “pull-in” moment with higher magnitude in orders compare to steady-state on
current. This huge current in short time can be enough to melt the contact point locally. The best way to prevent burn-out is to decrease the pull-in voltage. The decrease of $t_{\text{gap}}$ or increase of stiffness of moving elements is the easiest way to accomplish it, but these solutions can make “stiction” problem worse. The other solution is to increase contact resistance with thin oxide coating\textsuperscript{32}. But, this method has drawbacks of increasing power dissipation, delay, and decreasing noise margin of device.

3.5 Nanowire NEMFET

Within these previous researches review, NEM switches suffer from the fundamental design limitation that when turned on, the current relies solely on the contact resistance between the two contact surface and the typically large threshold voltage used to pull in the device. Therefore two terminal switches have no control over its on or off current and their performances depend heavily on the nature of the mechanical contacts which is still not well understood\textsuperscript{33}. On the other hand, three terminal suspended gate NEMS field effect transistors are configured as a traditional transistor with the gate voltage used to independently tune the current from source to drain. However the large micrometer sized metal suspended gate electrode in previously reported devices\textsuperscript{15,34} have limited operational speed in several MHz due to their heavy moving mass. Our concept, in contrast, is based on the ultra-small mass and volume of a suspended semiconductor nanowires which has shown to be able to scale to
ultra-high-frequency (UHF) and beyond in mechanical resonance\textsuperscript{35}. Nanowires have also previously demonstrated extreme high performance as field effect transistors with near-ballistic transport\textsuperscript{36}. Therefore, by employing the thin nanowire as the nano-electro-mechanically suspended channel, we will demonstrate near zero SS and high operational speed with combination of mechanical motion and electrical property of core/shell nanowires.

### 3.5.1 Device Structure

Unlike previously reported suspended-gated field-effect transistors, which utilized suspended metal beam anchored at two ends as the moving gate to dynamically control the threshold voltage, we used high performance semiconductor nanowire as the conduction channel. As shown schematically in Figure 3.15, the nanowire with equal width ($W_{NW}$) and length ($L_{NW}$) was suspended with a nanoscale initial airgap ($t_{gap0}$) on the degenerately doped Si substrate as globally bottom-gated electrode covered with SiO$_2$ dielectric layer with thickness ($t_{ox}$). Two ends of the nanowire were clamped by highly p-type doped artificial segments serving as drain/source electrodes. All the designed parameters were shown in the insets of Figure 3.15.
To be more computationally efficient, uniformly p-type doped Si semiconductor nanowire was used in the simulation section of this chapter. However, with respect to experiments, Ge/Si core/shell nanowires which show 0.5 ps intrinsic delay and perfect Ohmic contact with Ni metal electrodes\textsuperscript{36} will be used. In addition, we choose, in the simulation, the cross section of nanowire in square rather than in circular observed in the reality again for the same reason of faster convergence in the computation.

### 3.5.2 Operating Principles – Pull-in & Pull-out

Taking the advantages of heavily doped semiconductor nanowire or Ge/Si core/shell nanowire that is characteristic of normally-on behavior of $I_d$–$V_g$, our device was operating at the accumulation mode, as shown in the band diagrams of Figure 3.16.

**Figure 3.15: NEMFET structure for the device simulation.**
Figure 3.16: NW NEMFET operation modes and corresponding band diagrams within the suspended NW.

Combined with the band diagram at different applied gate voltage, Figure 3.16 also shows a schematic illustration of the operation of the NW NEMFET.

In operation of the NW NEMFET, starting at zero applied gate voltage \((V_g = 0)\), no coupled electrostatic force from the bottom gate yielding \(x = t_{gap0}\), where \(x\) represents the actual distance between the lowest point of nanowire and dielectric layer.

As \(V_g\) increased, a positive charge (and also equal amount of negative charge inside the nanowire) is built up in the gate electrode, giving rise to an electrostatic force pulling down the nanowire and resulting in \(x < t_{gap0}\). Until
the gate voltage reaches the “pull-in voltage” ($V_{pi}$), the coupling electrostatic force between the bottom gate and the nanowire and the counteracting elastic force from nanowire itself were balanced. Once increasing $V_g > V_{pi}$ leading to the collapse of the balance, pull-in occurred and the nanowire was snapped onto the dielectric layer.

![Figure 3.17](image)

**Figure 3.17**: Normalized restoring and electrostatic forces vs. normalized electrode separation$^{37}$.  

Figure 3.17 is the dimensionless plot of a linear counteracting elastic force (solid line), and an electrostatic force (dash line) due to $V_g$$^{37}$. The intersection of the restoring and electrostatic forces indicates an equilibrium position, assuming zero external force. On the electrostatic force curve corresponding to the critical “pull-in” voltage, $V_{pi}$, there is exactly one equilibrium point. Below this voltage, the device has two equilibria; above this
voltage, the electrostatic force dominates the restoring force, and hence, there are no equilibria. This holds true for nonlinear restoring forces provided that they remain finite at $x=0$.

Under the condition that $V_{pi}$ was carefully designed to be smaller than the threshold voltage ($V_t$) while the device was after pulling-in and sitting on the dielectric layer, devices act as ultra-thin layer SOI MOSFETs. Sharing the same principles as fully-depleted SOI MOSFETs\textsuperscript{38}, carriers inside the NW, conduction channel, would be fully depleted. Thus, the fully depleted carriers result in the minimized leakage current while the nanowire was at the pulled-in state. In other words, through the delicate design of operation mode and specification parameters for NW NEMFETs, it is possible to shut down the device at $V_{pi}$ ($V_{pi} = V_{th}$ for NW NEMFET) with zero subthreshold slope (SS) while maintaining the maximum value of the $I_{on}/I_{off}$ ratio. On the other hand, when $V_g$ was swept back from a larger value than $V_{pi}$, pull-out did not occur since the electrostatic force was still larger than the elastic force of nanowire. Pull-out of the nanowire needed further reduction of $V_g$ (while $V_g = V_{pout}$) resulting in the hysteresis of the device’s characteristics and also the effect of adhesion force on $V_{pout}$, which will be discussed in the following sections.
3.6 Device Modeling

3.6.1 Analytical Modeling

To model the pull-in behavior, we started with the force-balance equation (3.7).

\[ \frac{1}{2} WL \frac{1}{\varepsilon_{gap}} Q_{sc}^2 = k(t_{gap0} - x) \]  \hspace{1cm} (3.7)

\[ Q_{sc} = \sqrt{2\varepsilon_{Si} kT N_A \left[ \exp \left( -\frac{q\psi_s}{kT} \right) + \frac{q\psi_s}{kT} - 1 \right]} \]  \hspace{1cm} (3.8)

\[ k = \frac{32E_L h^3}{W^3} \]  \hspace{1cm} (3.9)

\[ V_g = V_{fb} + \psi_s - \frac{Q_{sc}}{C_{ox}} \]  \hspace{1cm} (3.10)

The left-hand side of (3.7) represented the electrostatic attraction force, in which \( \varepsilon_{gap} \) was the gap permittivity and \( Q_{sc} \) was the induced charge density inside the semiconductor nanowire with an equally negative amount at the surface of bottom gate. \( V_g \)-dependent \( Q_{sc} \) (3.8) including the accumulation charge and the depletion charge could be modeled as the function of the surface potential, \( \psi_s \), on the nanowire, where \( \varepsilon_{Si} \) was the silicon permittivity, \( q \) was the elementary charge and \( N_A \) was the nanowire doping concentration. By substituting the term of \( Q_{sc} \) in (3.7) with (3.8), the left-hand side of (3.7) became the function of \( \psi_s \). The right-hand side of (3.7)
meant the elastic force with a linear spring constant. Note that the term in the bracket corresponded the nanowire displacement and was only valid when the nanowire was before pulled in, where $x$ was the actual air gap distance and $t_{gap0}$ was the initial gap distance. This was a simple assumption since the nonlinear stretching component of the spring constant, which can lead to a non-negligible restoring force (and can alter the pull-out behavior) was neglected. For a uniformly distributed electrostatic force along the beam and neglecting the residual stress, the spring constant $k$ was given in terms of the structural parameters as show in (3.9)$^{39}$.

Combined with the gate voltage equation (3.10)$^{40}$, two unknown variables, $x$ and $\psi_s$, could be solved with two equations substituted (3.7) and (3.10). Note that $C_{ox}^* = 1/(t_{ox}/\varepsilon_{ox} + x/\varepsilon_0)$ in (3.10) included the air gap capacitance per area, $x/\varepsilon_0$, in series with the dielectric capacitance per area, $t_{ox}/\varepsilon_{ox}$. Because of the exponential term, $Q_{sc}$ in (3.7), these two equations could be only calculated numerically by iteration.

To solve the equations analytically, depletion approximation was used. The depletion charge inside the nanowire was given as a simple, yet reasonable, function of the surface potential, $Q_{sc} = \sqrt{2\varepsilon_{Si}kTN_A \frac{q\psi_s}{kT}}$. Substituting the approximated depletion charge and (3.8) into (3.7) and solving simultaneous equations (3.7) and (3.10), the onset of nanowire being
pulled-in at the air gap distance, $x_{pi}$, and the corresponding $V_{pi}$ happening once the simultaneous equations would not converge. We would have two sets of analytical solutions and only one had physical meaning, which were shown as (3.11) and (3.12).

$$x_{pi} = t_{gap0} - \frac{1}{36} \left( \varepsilon_0 \sqrt{2 \varepsilon_0 k/WL} \frac{q\varepsilon_{Si}N_A}{q\varepsilon_{Si}N_A} + \frac{2 \varepsilon_0 k/WL}{(q\varepsilon_{Si}N_A)^2} + 12 \left( t_{gap0} + \frac{\varepsilon_0}{\varepsilon_{ox}} t_{ox} \right)^2 \right)^2$$

(3.11)

$$V_{pi} = V_g \text{ (while } x = x_{pi})$$

(3.12)

Equation (3.11) and (3.12) were only valid when the nanowire was in the up state and $V_g \leq V_{pi}$. However, equation (3.12) was a general relationship for $V_{pi}$. It reduced to the well-known pull-in voltage of the simple MEMS switch$^{41}$, $V_{pi(SW)}$, for $N_A \rightarrow \infty$ (metallic switch case) and $V_{fb} \rightarrow 0$ (same material for both electrodes):

$$\lim_{N_A \rightarrow \infty, V_{fb} \rightarrow 0} V_{pi} = V_{pi(SW)} = \frac{6k(t_{gap0} + t_{ox}/\varepsilon_{ox})^2}{27WL_{gap}}$$

(3.13)

By inserting the parameters shown in the inset of Figures. 3.15 & 3.16 and solving equations (3.11) and (3.12), the normalized $x$ versus different $V_g$ could be attained through the iteration at each different $V_g$. Notably, the dimensions used in were in the nanometer scale, and they were about three orders of magnitude smaller than the typical dimensions of MEMS switches (several micrometers for the vertical dimensions and hundreds of
micrometers for the beam length) to actuate the nanowire (pull in) at such low-voltage. As calculated, $V_{pi}$ was only 0.9 V by using the designed parameters, which meant that the threshold voltage for NW NEMFET could be controlled under 1 V while maintaining the low subthreshold current.

When the nanowire was pulled down, the force-balance equation in the nanowire-down state, just before the pull-out, can be expressed as,

$$\frac{1}{2}WL\frac{1}{\varepsilon_{ox}}Q_{sc}^{2} + F_{a} = k_{t}g_{apo}$$  \hspace{1cm} (3.14)

where the first on the left-hand side represented the electrostatic force applied to the nanowire, whereas the term on the right-hand side showed the elastic restoring force of the doubly clamped nanowire. $F_{a}$ was the surface adhesion force, which would not be included in the modeling but would be considered comprehensively in the section 3.5. Again, the spring constant of nanowire was still modeled as (3.9) by structural parameters even though the nanowire was pulled in. The restoring elastic force could be more accurately calculated by taking into account the influence of the nonlinear stretching component on the spring constant$^{42,43}$. Furthermore, the nanowire stayed in contact with the whole gate oxide area until the occurrence of the pull-out in the analytical modeling while only depletion charge has been being considered.

3.6.2 Quasi-static Mechanical Simulation (COMSOL)
To take into account the deformed shape of nanowire in real-time and have the minimal amount of approximations, we utilized finite element simulation solver, COMSOL Multiphysics, coupled with TCAD device-simulation tool, Sentaurus, to handle the electrostatics when semiconductor materials were present coupled with the structural (nano-mechanical) domain. First, we performed the simulation of the mechanical behaviors including pull-in and pull-out in three dimensions at parametric sweep of $V_g$ for semiconductor NW NEMFET in COMSOL. Without equipotential approximation on the nanowire surface, in other words, holes, electrons and acceptors (p-type doped) or donors (n-type doped) were all considered inside the nanowire. Consequently, the simulated data of $x$ vs. $V_g$ functionalized as the input data into Sentaurus to simulate NW NEMFET’s current-voltage characteristics ($I_d-V_g$).

The three-dimensional perspective view of NW NEMFET used in COMSOL was similar to the structure shown in Figure 3.15. Double clamped semiconductor silicon nanowire (material parameters: Young’s modulus, E: 153 GPa; Poisson’s ratio, $\nu$: 0.23) was suspended with an initial air gap on the bottom gate covered with an oxide layer. For the reason of being computationally efficient, the cross section of the nanowire in the circular was substituted by the square and the device was symmetric along the long edge. The dimensions of the device were: length of the nanowire ($L_{NW}$): 1.3 µm; width of the nanowire ($W_{NW}$): 20 nm; width of the bottom gate and oxide layer
(W): 100 nm; initial air gap: 10 nm; dielectric layer thickness: 2 nm. The whole device resided in an air-filled chamber that was electrically insulated except that the bottom side of the oxide layer was applied with the parametric gate voltage, $V_g$, and the bottom side of the air chamber was grounded.

An electrostatic force caused by an applied voltage difference between the nanowire and the bottom electrode bent the nanowire toward the bottom gate. To compute the electrostatic force, the solver calculated the electric field in the surrounding air statically at each step point of applied $V_g$ while the boundary condition of the bottom side of the oxide layer was a parametric sweep of $V_g$ generated by the solver with given interval value and sweeping range. The model comprises a layer of 10 nm thick air below the nanowire which was the initial air gap between the nanowire and the oxide layer and one 40 nm air layer next to the side of the nanowire. As the nanowire bent, the geometry of the air changed accordingly. By using the arbitrary Lagrangian-Eulerian (ALE) method, the solver took the displacement into account while computing the electric field. When the geometry (nanowire and the air gap layer) deformed at each parametric value, $V_g$, the electric field between the nanowire and bottom gate electrode continuously changes as a result of the bending.

Unlike previous proposed planar suspended-gate FETs$^{40}$ having nearly metallic suspended gate, we used suspended semiconductor nanowire as conduction channel. Thus, in our simulation, the electrostatically
metallic approximation on nanowire surface which might result in the underestimation of $V_{pi}$ due to the lack of considering the depletion depth and carrier concentration distribution profile inside the semiconductor nanowires. To address this issue, we integrated the numerical results from solving the classical Poisson’s equation in three dimensions into COMSOL Multiphysics solver. Our model allowed for a uniformly doped semiconducting nanowire channel, core/shell heterostructure nanowire channel, and also a finite nanowire length.

In the COMSOL simulation, we used p-type silicon as the nanowire channel as a representative example in NW NEMFET. The surface of the nanowire was assumed to be fully passivated, such that surface Fermi level pinning and other surface effects can be neglected. The electron and hole concentrations were calculated as a function of local electric potential. This was achieved by integrating the density of states (DOS) in conjunction with the Fermi-Dirac distribution, where $E_f$ was displaced by the local potential, $V$, with respect to conduction band and valence band edges,

$$n(V) = \int_{-\infty}^{\infty} \frac{\rho_c(E)}{1+\exp[(E-E_f-V)/k_BT]} dE = N_c \frac{2}{\sqrt{\pi}} \int_{0}^{\infty} \frac{x^{1/2}}{1+\exp[x-(E_f-V-E_c)/k_BT]} dx$$

(3.15)

$$p(V) = \int_{-\infty}^{\infty} \frac{\rho_v(E)}{1+\exp[(V+E_f-E)/k_BT]} dE = N_v \frac{2}{\sqrt{\pi}} \int_{0}^{\infty} \frac{x^{1/2}}{1+\exp[x-(E_v-V-E_f)/k_BT]} dx$$

(3.16)
\( \rho_c(E) \) and \( \rho_v(E) \) were the DOS of the 6-fold degenerate conduction band minimum and valence band maximum including the contribution from heavy-hole, light-hole as well as spin-orbit split-off valence bands\(^{44} \) respectively. \( E_f \) was given by the charge neutrality condition at \( V = 0: p(0) = n(0) + N_A(0) \).

Two regimes were distinguishable: the nondegenerate regime where \( \log(n) \) and \( \log(p) \) exhibited a linear dependence on \( V \) in comparison with the nonlinear, degenerate regime where the bands were heavily populated. The crossing point of \( \log(n) \) and \( \log(p) \) when \( E_f \) was displaced to mid-bandgap defined an intrinsic free carrier concentration of \( \sim 10^{10} \text{ cm}^{-3} \) in silicon at room temperature. Note that the diameter of the simulated silicon nanowire was larger than 20 nm. Therefore, we reasonably neglected the effect of quantum confinement and only utilized the classical three-dimensional density of states since multiple sub-bands were populated as a consequence of thermal excitation at room temperature.

By integrating the calculated \( V \)-dependent hole and electron concentration profile, into COMSOL electrostatic model, we could obtain the electric potential distribution, \( V(x,y,z) \), through solving the three-dimensional Poisson’s equation (equation below) in our NW NEMFET geometry at each parametric value of applied \( V_g \) self-consistently inside COMSOL solver,

\[
\nabla \cdot [\varepsilon \nabla V(x,y,z)] = \rho(x,y,z) \tag{3.17}
\]
where the space charge density $\rho = q \cdot [p(V) - n(V) - N_a]$ in nanowire and were zero in other subdomains, and $\varepsilon = \varepsilon_0 \varepsilon_r$ with each dielectric material volume with their respective values of $\varepsilon_r$.

In the case of pull-out modeling in COMSOL, we artificially projected the deformed nanowire from the state before being pulled-in to where the nanowire was snapped onto the oxide layer in two dimensions. Subsequently, by using the extruding mesh method available inside COMSOL, three-dimensional NW NEMFET at the pulled-in state could be modeled in a much lower mesh density, which again for the computationally efficient reason.

While keeping the nanowire at the down state, we solved the electrostatic problem without moving mesh and mechanics model through applying parametric $V_g$. The electrostatic force in the vertical direction, which was the main and only driving force pulling down the nanowire, could be obtained at each different supplied $V_g$.

Since there was no nonlinear stretching considered in the simulation of mechanics in our COMSOL model, the counteracting elastic force on the deformed nanowire during pulling-in in the vertical direction would be modeled as a linear function of nanowire’s z-directional displacement.

$$F_{\text{elastic}} = k(t_{gap0} - z) \quad (3.18)$$

where $k$ meant the effective spring constant and $z$ was the actual distance between the lowest point of the deformed nanowire and the oxide layer. Thus,
the projected elastic force of the nanowire at the down state was readily calculable by using the extrapolation.

Pull-out happened once the nanowire’s elastic force was larger than the electrostatic force in z-direction. As shown in, the elastic force was independent with $V_g$ at the down state and consequently the pull-out voltage ($V_{pout}$) could be clearly determined at the onset of the crossover point of two curves.

3.6.3 Advantages Over Planar NEMS Devices

In addition to the flexible properties in mechanics of semiconductor nanowires, adding more dimensionality of electrostatic gate coupling also resulted in better performance of NW NEMFET in terms of designing future low-power devices. Sharing the same principles as the gate-all-around MOSFETs and three-dimensional FinFETs$^{45-48}$, in particular, as the diameter of the nanowire was on the same order of the air gap, electric field lines terminating on the sides of the nanowire, as shown in Figure 3.18, contributed to an enhanced three-dimensional electrostatic coupling and up to 20 % reduction in $V_{pi}$ compared to capacitive coupling in two-dimensional interactions of previously reported MOS-NEMETs$^{40}$. 
3.6.4 Quasi-static Device Characteristics Simulation (Sentaurus)

By incorporating the data of $x$ vs. $V_g$ calculated from COMSOL into TCAD solver, Sentaurus, the quasi-static $I_d$-$V_g$ of NW NEMFET could be obtained. Device characteristics of NW NEMFET was constructed and simulated in three-dimensions by Sentaurus.

We reasonably assumed that the deformed nanowire during pulling-in was flat and in parallel with the bottom oxide and gate electrode in Sentaurus simulation. The maximal error due to the overestimation of capacitive gate-coupling giving rise to the overestimation of drain current was less than 15 % which was justified. Perspective device structure was built and edited in “Sentaurus Structure Editor”, including the calculated distance between the
nanowire and the oxide, all other device dimensions used in the simulation of COMSOL, doping profiles inside the nanowire channel and highly doped drain/source segments. After constructing the device structure at each corresponding \( x \) (the distance between the lowest point of deformed nanowire and the oxide), we simulated the devices’ characteristic \((I_d-V_g)\) by “Sentaurus Device” under the assumption of doping-dependent mobility, no band gap narrowing and no quantum effect being considered.

**3.6.5 Dynamic Modeling**

Different methods were available to describe the dynamic behavior of a vibrating system\(^{49}\). Two most frequently used ones of them were based on:

- Newton’s law of motion, considering that some of forces acting on a moving structure equaled its mass times the acceleration

- Energy conservation method, considering that the total energy of a system was unchanged at all time

To describe in detail the different forces involved in a vibrating beam and the specificity of mode shapes in fixed-fixed beam, the energy method will be used here. Each following equations represented the different kinetic and potential energies associated with the beam deflection.

The stretching of the beam when bending (energy per unit length) was:

\[
U_{\text{stretch}} = \frac{1}{2} EI \left( \frac{d^2 y(x)}{dx^2} \right)^2 
\]  

\( (3.19) \)
The axial deflection of the beam (energy per unit length) was:

\[ U_{axial} = \frac{1}{2} T \left( \frac{\partial y(x)}{\partial x} \right)^2 \]  \hspace{1cm} (3.20)

The external load applied on the beam (energy per unit length) was:

\[ U_{ext} = -P(x) y(x) \]  \hspace{1cm} (3.21)

The kinetic energy of the mass with a certain velocity, per unit length, was:

\[ K_{mass} = \frac{1}{2} \rho A \left( \frac{\partial y(x)}{\partial t} \right)^2 \]  \hspace{1cm} (3.22)

The friction forces acting on the beam while the beam was moving, so-called dissipation function was:

\[ D = \frac{1}{2} y \left( \frac{\partial y(x)}{\partial t} \right)^2 \]  \hspace{1cm} (3.23)

Lagrange function was based on the Hamilton principle claiming that the integral of the energies along the beam length, which was the difference between the kinetic energy \( T \) and potential energy \( U \), is a minimum. The Lagrange function \( L \) was:

\[ L = \frac{1}{2} \int_{0}^{L_{beam}} \left( K_{mass} - U_{stretch} - U_{axial} - U_{ext} + D \right) dx = \int_{0}^{L_{beam}} L^* dx \]  \hspace{1cm} (3.24)

By integrating this function over the time, the Euler-Lagrange equation was defined (3.26). Differentiation with dots and primes meant the differentiation with respect to time and spatial coordinate respectively.
\[ \frac{\partial L^*}{\partial x} - \frac{\partial}{\partial t} \frac{\partial L^*}{\partial \dot{y}} - \frac{\partial}{\partial x} \frac{\partial L^*}{\partial y} + \frac{\partial^2}{\partial x^2} \frac{\partial L^*}{\partial y} = 0 \]  

(3.25)

Considering the external load as the electrostatic force in the case of electrostatic resonators, the equation became,

\[ -\rho A \frac{\partial^2 y}{\partial t^2} = EI \frac{\partial^4 y}{\partial x^4} - T \frac{\partial^2 y}{\partial x^2} - \frac{\varepsilon_0 w V^2}{(d-y)^2} + \gamma \frac{\partial y}{\partial t} \]  

(3.26)

Simplifications of the wave equation (3.24) can be done in the case of the flexural vibrating structure, considering that the displacement of the structure was limited in comparison with its length. It was also assumed that the flexural effect was dominated compared to the shear deformations and the effect of the rotary inertia, which eliminated the third term of (3.27) (Bernoulli assumption). The general expression of the solution was expressed as,

\[ y = A \sin(\lambda_n \frac{y}{L}) + B \cos(\lambda_n \frac{y}{L}) + C \sinh(\lambda_n \frac{y}{L}) + D \cosh(\lambda_n \frac{y}{L}) \]  

(3.27)

, where A, B, C and D were constants determined by the boundary equations. Taking the initial condition at each end of a fixed-fixed beam,

\[ y(0, t) = 0 \]

\[ \frac{\partial y(0, t)}{\partial x} = 0 \]  

(3.28)

the solution of equation (3.26) followed the general form:

\[ y_0 = y(x) \cos(\omega t + \phi) \]  

(3.29)
The expression of the resonant frequencies for the \( n \) Eigen modes was derived from the equation (3.27), without considering axial load:

\[
\omega_n^2 = \lambda_n \frac{Y I}{L^4 \rho A}
\]  

(3.30)

, where \( Y \) was the Young’s modulus for a narrow vibrating beams and \( Y = E/(1 - v^2) \) for a wide vibrating beam \( (W_{beam} >> H_{beam}) \). \( \lambda_n \) corresponded to the value associated with the vibration mode shape number \( (n)^{50} \).

### 3.7 Simulation Results

#### 3.7.1 Zero Subthreshold Slope Field-Effect Transistor

Device’s mechanical behavior coupled with the electrostatically actuating force applying on the semiconductor nanowire, simulated in COMSOL, was shown in Figure 3.19. Device’s dimensions were listed in the inset of Figure 3.15. As seen in Figure 3.19, analytical modeling showed different behavior from the finite element simulation (COMSOL) results especially at the threshold of pulling-in. In the analytical modeling, pull-in happened at \( V_g = 0.92 \) V while the nanowire was at the position of around \( 2/3 \) initial air gap; As for the COMSOL, nanowire was not pulled in until the nanowire was pulled and deformed over the half (47.7 %) of the initial air gap and the pull-in voltage was 0.97 V, 5 % more than the analytical modeling.
Figure 3.19: Normalized dependence of gap distance vs gate voltage using self-consistent COMSOL simulation and analytical modeling.

The difference of the threshold position for pulling-in to be happened and the corresponding $V_{pi}$ was mainly due to the approximation of deformed shape of nanowire during pulling-in. In the analytical modeling, the nanowire was assumed to be flat and additionally the planar capacitance was used. However, in COMSOL, the deformed shape of nanowire which had one biggest deformed distance in the middle and gradually decreasing deformed distance from the middle to two clamped ends was simulated. This difference of the nanowire shapes resulted in the different gate coupling, which meant that the electrostatically coupled gate capacitance crossing the air gap was overestimated in the analytical modeling since in the analytical case, every
point of the nanowire was approximated to be the lowest point of deformed nanowire simulated in COMSOL which meant that the air gap capacitances (illustrating two shade areas on the two sides of deformed NW) were neglected.

We constructed the device in Sentaurus at the same dimensions as in COMSOL, where all the parameters were shown in the inset of Figure 3.15. Through the iteration between COMSOL and Sentaurus, device’s characteristic was shown in Figure 3.20 exhibiting zero subthreshold slope (SS) with $10^{15}$ on/off ration where $V_{pi}$ and $V_{pout}$ happened at 0.97 V and 0.64 V respectively. As illustrated in Figure 3.20, to reach the same on/off ration, NW NEMFET possessing abrupt switching behavior could be reached within 0.5 V $V_{DD}$ window in comparison with the non-suspended MOSFET control device with the same dimensions requiring more than four times the $V_{DD}$ swing.
Figure 3.20: Comparison of simulated $V_g$-$I_d$ curve between NEMFET and MOSFET having same dimension for the same $I_{on}/I_{off}$ ratio.

Figure 3.21: Comparison of simulated $V_g$-$I_d$ curves of the NW NEMFET with different doping concentrations.
With higher doping of the semiconductor nanowire, \( V_{pi} \) can be further reduced (Figure 3.21). Note that several constraints limit the parameter space of doping concentration engineering. For example, \( V_{pi} \) must be larger than the pull-out voltage \( (V_{pout}) \) by a fair margin to ensure the repeated switching operations, while the higher doping nanowire channels also lead to a more positively increased threshold voltage for the device at the pull-down state and thus a reduce on/off ratio. Besides tuning the doping concentration, the design of the structural parameters of the device also play an important role while scaling \( V_{pi} \) and \( V_{pout} \) of NW NEMFET, which will be discussed in detail combined with the design of operating frequency in the next section.

### 3.7.2 Design Map

The speed at which NW NEMFET can operate is essentially determined by the suspended beam’s mechanical resonant frequency. We calculate the fundamental resonant frequency of NW NEMFET by the equation 3.30. For the first mode, the resonant frequency is expressed as

\[
f = 1.027 \sqrt{\frac{E}{\rho} \left( \frac{W}{L^2} \right)} ,
\]

which is a function of the beam’s material characteristics: \( E \) (Young’s modulus) and \( \rho \) (density) and beam’s dimensions: \( W \) (width of beam) and \( L \) (length of beam).

Following the same trend of scaling pull-in voltage as metal-metal switch, \( V_{pi} = \sqrt{\frac{8(\frac{32E W^4}{L^4})}{27\varepsilon_0 W L}} g_0^3 \propto (g_0)^{1.5} \left( \frac{W}{L} \right)^{1.5} \left( \frac{1}{L} \right) \), \( V_{pi} \) of NW NEMFET could be
approximately projected to be a function of material characteristics $E$, air gap thickness $g_0$, and the beam’s dimensions $W$ and $L$, which are approximated as the diameter and length of nanowire respectively. As shown in the equation, in order to minimize the pull-in voltage, shrinking the air gap or using the nanowire as the suspended beam with inherently high aspect ratio, is the possible way.

By choosing the material and tuning the dimensions of nanowire, it is feasible to realize devices with low pull-in voltage and high operational frequency respectively. However, the common dilemma in NEMS switches is higher frequency ($f$ is proportional to aspect ratio) and more rigid usually require much increased pull-in voltage ($V_{pi}$ is proportional to aspect ratio). To explore the design space of NW NEMFET, we plot the constant $V_{pi}$ map for a range of different diameter ($W$)/ length ($L$) nanowires given the same doping profile of nanowire, $x_0$ and $t_{ox}$ (Fig 3.22). The dotted and solid lines represent constant $V_{pi}$ and constant frequency scaling at each corresponding device dimension. It is clear from the crossover of the constant $V_{pi} = 5$ V line and the constant frequency = 320 MHz line that the device operating at frequency higher than 300 MHz with pull-in voltage less than 5 V is achievable using Si nanowires or Ge/ Si core/ shell nanowires with 12 nm diameter. Furthermore, the scaling map suggests sub 1 V operation will require nanowires or nanotubes with diameter smaller than 5 nm. Following the same methodology, we can construct another design map for $V_{pout}$. 
Figure 3.22: Constant performance device scaling trends between resonant frequency (solid line) & Vpi (dotted line). The color map shows constant Vpi’s as a function of D and L. In order to have device to work as a resonator at UHF and to be turned off at a finite voltage, the NW diameter must be scaled down at least to 10 nm.

3.8 Device Fabrication

We have realized the concept of NW NEMFET using two different device structures: local metal gate NEMFET and back gate NEMFET. In this section, however, we only use local metal gate NEMFET as a comparison and put emphasis on the discussion of the back gate NEMFET.

3.8.1 Back Gate NEMFET Scheme

Figure 3.23 is the schematic comparison between back gate NEMFET and local metal gate NEMFET, and Table 3.1 summarize the differences of the back gate NEMFET process comparing to local metal gate one. First, the
critical gate oxide deposition process over suspended nanowire channel or metal gate is not needed. Instead of it, we can use the highly doped silicon substrate covered with gate oxide. The thermal silicon oxide or high-k oxide on planar silicon substrate with atomic layer deposition process is well defined, so don’t need to worry about the quality of the gate oxide. Second, we can skip the one step of E-beam lithography, metal deposition, and lift-off process, so the process step is much more simple than local metal gate process. Third, the gate is global back gate, the source/drain electrode don’t be needed to align to gate electrode. At last, the gate leakage can be minimized between the gate and the source/drain with nanowire channel which is place in unwanted position, as the NW is always isolated with global gate oxide in any position.

*Figure 3.23: Schematic structure of the device, (a) the back gate NEMFET, (b) the local metal gate NEMFET.*
Table 3.1: Comparison of the characteristics between the back gate NEMFET and the local metal gate NEMFET.

<table>
<thead>
<tr>
<th>Gate structure</th>
<th>Back gate</th>
<th>Local gate</th>
</tr>
</thead>
<tbody>
<tr>
<td>Gate material</td>
<td>$p^+\text{Si}$</td>
<td>Metal(Au)</td>
</tr>
<tr>
<td>Gate signal</td>
<td>Global</td>
<td>Individual</td>
</tr>
<tr>
<td>E-beam litho step/Metal deposition step</td>
<td>2/2</td>
<td>3/3</td>
</tr>
<tr>
<td>Gate oxide</td>
<td>On Si</td>
<td>On metal or on NW</td>
</tr>
<tr>
<td>Gate leakage path</td>
<td>Large probing pad and wiring</td>
<td>NW contact area with gate</td>
</tr>
</tbody>
</table>

The back gate NEMFET process has the advantages, but some critical disadvantages can be pointed out. First, as it is the global gate scheme, it can’t control the each device individually. Even though, the isolation process such as isolation trench oxide or ion implantation process can be combined with the back gate scheme to insulating electrically each NEMFET device, but the process complexity will be increased a lot, too. So the back gate NEMFET can be used for the confirmation of NEMFET device scheme only. Second, in practical, the area of the probing pad for the source/drain electrode is extremely larger (60um x 60um) compare to the contact area between suspended nanowire channel and bottom gate (a few nm x a few nm). It means, there is a risk of huge gate leakage from metal – insulator - silicon substrate structure (source/drain probing pad – gate oxide – silicon back gate) specially with high gate voltage which is higher than
breakdown voltage of gate oxide. At last, it’s very hard to decrease the air gap thickness even with critical point dryer process. This acts as an important obstacle for decreasing the pull-in voltage of the device. In the local metal gate scheme, the final air gap thickness may be reduced further with accurate control of gate oxide deposition process precisely.

3.8.2 Device Fabrication of Back Gate NEMFET

Figure 3.24 summarizes the process flow of the back gate NEMFET. I will explain the fabrication process of the back gate NEMFET in short. To realize the back gate NEMFET with suspended nanowire channel, we used intrinsic Ge/Si core/shell nanowire as suspended channel, and fabricate metal electrode array as source/drain electrode to support the suspension of nanowire channel over the $p^+$ silicon substrate as back gate covered with 40nm ALD ZrO$_2$ as gate oxide.
Figure 3.24: Schematic cartoon of process procedure for the back gate NEMFET with suspended i-Ge/Si core/shell nanowire channel.

Intrinsic Ge/Si core/shell nanowires were grown by vapor-liquid-solid process using previously described two-step growth process. For the intrinsic Ge/Si core shell nanowire, the intrinsic Ge core was grown first using gold colloids (Ted Pella) with diameters ranging from 10~15nm as catalyst seeds. The Ge nanowire was grown at 287°C for 60min using GeH\textsubscript{4} gas with total pressure of 300Torr, then the chamber heated up to 460°C which is the Si shell growth temperature within H\textsubscript{2} ambient. The silicon shell of thickness 2~3nm was grown at 460°C for 17min using SiH\textsubscript{4} with total pressure of 100Torr. No dopant was added during the whole process. After finishing the growth, the chamber was cooled down to room temperature with no gas flow. The target diameter was set to 25~30nm with 5nm silicon shell thickness.
Figure 3.25: HRTEM image of the Ge/Si core/shell nanowire.

Figure 3.25 shows a representative high-resolution TEM (HRTEM) image of the Ge/Si core/shell nanowire. As shown in the figures and based on extensive TEM observations, the Ge cores have diameters of 10~25 nm while the Si shells are typically 2~3 nm thick, and the Si-Ge interface is epitaxial with no dislocations. The cross section of the wire is circular. The NWs typically exhibit a layer of ~1 nm thick amorphous native SiO₂.

The p+ Si substrate covered with gate oxide (40 nm ALD ZrO₂) is cut and cleaned in appropriate sizes. The high-k oxide is always favorable in terms of low $V_{th}$ and small sub-threshold swing with better gate coupling, but usually suffer from low breakdown voltage. We designed the straight and parallel source/drain electrode arrays without gate electrode.
Figure 3.26: Top-view SEM image of back gate NEMFET, (a) low magnification (scale bar = 50 um), (b) high magnification (scale bar=10 um).

Figure 3.26 shows the design of the back gate NEMFET device. Another different point with NEMS switch design excepting gate-electrode-less is the wiring which connects the selected source/drain electrode to external probing pad was formed at the stage of patterning the source/drain electrode. This is for minimizing the parasitic conduction of unwanted nanowire channel among source and drain. If the wiring was formed after the nanowire channel transfer, the parasitic channel makes firm connection electrically and mechanically with the wiring metal. Furthermore, as I mentioned, the transfer process is random in density and position, there are a lot of nanowire on the substrate outside the electrode area. So, the parasitic conduction can screen out the electrical current of selected device severely. Different from this, the pre-formation of the wiring line in the step of
the source/drain electrode fabrication, the unwanted transferred nanowire channel was just placed on the wiring line without electrical and mechanical contact.

![Figure 3.27: SEM image of fabricated back gate NEMFET with suspended i-Ge/Si core/shell nanowire channel, (a) low magnification (scale bar=200um), (b) high magnification (scale bar=1um).](image)

As the gate electrode is not needed in the back gate NEMFET, the source/drain electrode as supporting suspended nanowire channel was patterned with E-beam lithography process without aligned to gate electrode, and Cr 5nm + Au film was deposited and lift-off in same way. The thickness of Au film is important as the air gap thickness, $t_{gap}$, is simply controlled by the Au deposition thickness. The $L_{ch}$ was chosen with the results of NEMS switch. After finishing the source/drain electrode array fabrication, the nanowire channel is transferred perpendicularly on the electrode array with dry transfer method. As the suspension rate of nanowire channels was varied,
just same as NEM switch, we picked up the best suspended nanowire channel with plan-view and tilt-view SEM observation. After transferring the nanowire channel, anchor electrodes process was followed. Different from the NEM switch, Ni 10 nm was used as anchor electrode only for the ohmic contact to Ge/Si core/shell nanowire, and the wiring was formed with the source/drain already, so the adhesion with oxide is not a concern anymore. The NEMFET was selected after critical point dryer process with SEM observation.

Fig 3.27 shows the SEM image of the back gate NEMFET after whole process. The source/drain and anchor electrodes were patterned well with E-beam lithography, and the nanowire channel was suspended successfully after whole process.

3.9 Electrical Properties of Fabricated Devices

3.9.1 DC Properties

| Table 3.2: Important parameters of back gate NEMFET switch with suspended CSNW. |
|--------------------------------|-----------------|-----------------|-----------------|
| S/D height                     | 120nm(Cr+Au)    | Anchor Electrode| 60nm(Ti+Au)     |
| Gate height                    | 40nm(Cr+Au)     | NW channel      | i-CSNW          |
| $t_{gap}$                      | 80nm            | NW diameter     | 28nm            |
| $L_{ch}$                       | 1.62um          | Gate Oxide      | 40nm ZrO$_2$    |
To measure the electrical property of NEMFET, we used the Lakeshore vacuum probe station with HP4145B for $V_d-I_d$ measurement, and DEQ of National instrument with Stanford SR570 current amplifier for $V_g-I_d$ measurement at room temperature with the $\sim 10^{-5}$torr vacuum level. Figure 3.28 is the schematic of measurement system.

**Figure 3.28:** Schematics of measurement system, (a) $V_d-I_d$, (b) $V_g-I_d$.

**Figure 3.29:** Transfer characteristics of NEMFET, (a) $V_d-I_d$ curve (SEM image of measured device, scale bar=1um), (b) $V_g-I_d$ curve.
Figure 3.29(a) is the $V_d$-$I_d$ plot of NEMFET device with different $V_g$. The important parameters of device are summarized in Table 3-2. The top-left inlet of Figure 3.29(a) shows the tilt SEM image of device. The good ohmic contact and hole gas formation are achieved, and the small gate dependency of $I_d$ can be an electrical evidence that the CSNW channel is suspended. As the CSNW channel is suspended over 80nm vacuum (same to 312nm SiO2), the coupling with gate is very small, so the channel is still remain on-state till large $V_g$ (10V). With $V_g$ sweep over the pull-in voltage, the $V_g$-$I_d$ plot (Figure 3.29(b)) shows the abrupt transition from on-state to off-state at the pull-in voltage. The suspended CSNW channel abruptly touches the gate oxide due to electrostatic force from gate, then the CSNW is depleted with large coupling with positive gate voltage effectively. The pull-in occurs at $V_{pi}$=10.8V, and the on/off ratio ~10.7 with SS=15mV/dec. As the abrupt $I_{on}/I_{off}$ transition of device comes from the mechanical motion, the SS is determined by the $V_g$ sweep step only, and we can point out the SS can be almost zero if the $V_g$ sweep step is small enough as

$$SS = \frac{Gae\ Sweep\ Step}{Log(I_{on} / I_{off})}.$$  \hspace{1cm} (3.31)
Figure 3.30: Comparison of Vpi, Vpo value between 3D COMSOL simulation and measurement results of NEMFET.

Figure 3.31: Pull-in and pull-out switching of other device, Inset is Vd-Id curve.
The $I_{on}/I_{off}$ at $V_{pi}$ is smaller than simulation results, but it comes from large SS of stuck CSNW-FET (8V/dec). In back gate FET structure, the surface/interface state can increase SS of device with considering, because SS is $60mV \times (C_{total}/C_g)$ at room temperature and $C_{total}$ is the sum of all capacitances to the channel including parasitic contributions from intrinsic quantum capacitance of the semiconductor, charge traps, and source and drain electrodes. The on/off ratio can be increased significantly with local gate device with passivation process which will discuss in chapter 5 in detail. The back gate NWFET shows the $V_{th} \sim 5V$, and the expected SS is 1.5V/dec in local gate device, which is extracted from back gate planar NW-FET using same nanowire with passivation, then the possible on/off ratio with local back gate NEMFET is $10^4$ with $I_{off} = 40pA$. We sweep down the $V_g$ right after pull-in to confirm the pull-out behavior of device, and the pull-out occurs at $V_{po} = 6.5V$. The $V_{po}$ is smaller than $V_{pi}$ as expected. The COMSOL simulation shows the $V_{pi}$ matches well with measured data, but $V_{po}$ shows a value 16.4% smaller than simulation (5.4V). This can be explained with the residual tensile surface stress might come from the lattice mismatch and the clamping method of the device. The surface stress is added up to restoring force, so the $V_{pi}$ can have a greater value than the simulation. The similar NEMFET operation is demonstrated repeatedly with other device, and Figure 3.31 shows the results of it.
In back gate NEMFET measurement, we failed to get a multiple switching with this NEMFET, and there’s misfit of $I_d$ between sweep-up and sweep-down. This can be explained with the mechanical hardening effect of suspended channel with change of slack.

### 3.9.2 AC Properties

One of the important factors to determine the performance of the NEMFET is operational speed. The speed at which NEMFET can operate is essentially limited by the suspended beam’s mechanical resonant frequency. For a suspended beam, the resonant frequency $f_o$ can be expressed as\(^5\)

$$f_o = 1.03 \frac{d}{L^2} \sqrt{\frac{E}{\rho}}, \quad (3.32)$$

where $E$ is Young’s modulus, $\rho$ is the mass density, $d$ is the thickness of the beam (in this case, the diameter of CSNW) in the direction of motion, and $L$ is the length of the suspended beam. As the suspended channel is core/shell structure of Ge/Si, it’s not easy to calculate the exact resonant frequency, but it should be a value between Ge-only $f_o$ 34MHz and Si-only $f_o$ 70MHz in same device dimension. So, we use the so-called single source method which measured $I_{\text{MIX}}$ current using a NEMFET as a signal mixer.
Figure 3.32 illustrate the concept of measurement. The signal $V_d^{ac}$ with frequency $\omega$ and amplitude modulated at $\Delta\omega$ is applied to drain electrode, while the gate electrode is held at a constant DC voltage $V_g^{dc}$. The intermediate band width mixing signal (AM 400Hz) by NEMFET is detected by low frequency lock-in amplifier. The mechanical motion of suspended NW channel cause a modulation of the capacitance between NW and the gate, making a modulation of output current at the drive frequency $\omega$, and it shows the maximum value at the resonant frequency $f_0$. The shape of peak can be a various shape depending on the phase difference between reference signal and $I_{mix}$ signal. The $I_{mix}$ follows the equation listed below:
\[ I_{\text{mix}}(\omega) = A + B\omega + \frac{H\cos(\arctan\left(\frac{f_0^2 - \omega^2}{f_0\omega}\right) + \Delta\phi)}{\sqrt{\left(1 - \left(\frac{\omega^2}{f_0^2}\right)\right)^2 + \left(\frac{\omega}{f_0}\right)^2}} \]  

(3.33)

where, \(A, B, H, f_0, Q\) and \(\Delta\phi\) are the independent fitting parameters. \(\omega\) is the drive frequency, \(f_0\) is resonant frequency, and \(Q\) is quality factor. Figure 3.33 (a) is the plot of \(I_{\text{mix}}\) vs. drive frequency in different drive amplitude at \(V_g^{dc}\) is held to 1V. The \(I_{\text{mix}}\) peak shows \(f_0\) is 57MHz with drive amplitude 20mV, and the \(f_0\) increase non-linearly with increase of drive amplitude (Figure 3.33 (b)).

![Figure 3.33: Measurement results of resonant frequency. (a)Frequency vs. \(I_{\text{mix}}\) plot in different AC drive amplitude. The data was taken at \(V_g^{dc}=1V\). The each line is the fitted value with the analytical equation of \(I_{\text{mix}}\). (b) The dependency of resonant frequency \(f_0\) and \(I_{\text{peak}}\) vs. AC drive amplitude.](image)

The measured point fits well with Equation 3.33. The shape of peak can be varied with phase difference \(\Delta\phi\). The measured resonant frequency 57MHz is fit very well with Ge/Si CSNW COMSOL simulation with bulk value of Young's modulus and density. In general, NW resonator shows smaller
Young’s modulus due to compress stress in the surface with small diameter NW less than 100 nm\textsuperscript{53,54}, but Si shell has smaller lattice constant than core Ge. This lattice mismatch makes tensile stress in the surface of CSNW resonator, which is not released due to very thin shell thickness (2.5 nm), so the simulation results with continuum elastic theory equations fit very well with experimental results. The quality factor $Q$, which is defined as the ratio of the energy stored to the energy lost per cycle, of device is 201 with drive amplitude 20 mV. The resonant frequency is inversely proportional to the scale of the structure, but $Q$ factor decreases with increasing of resonant frequency. The $Q$ factor of our device is comparable to the previous study using 30 nm diameter and 1.8 um length double-clamped SiNW resonator\textsuperscript{35} with resonant frequency 75MHz and $Q$ factor 700, considering the smaller diameter and core Ge with lower Young’s modulus of our device. Figure 3.33 shows the typical non-linear increase of $I_{\text{peak}}$ with increase of drive amplitude. This behavior arises because the $V'_d^{dc}$ driving term contributes to an AC force term that is proportional to $(V'_d^{dc2} + V'_d^{ac2})/2$, which follows the description of the reference\textsuperscript{35}. The non-linear shift of $f_0$ with drive amplitude tells the resonator operates in the elastic hardening types of frequency tuning for vibration in plane of the gate\textsuperscript{51}.

### 3.10 Conclusion

In summary, we studied, via simulation and fabrication, NW NEMFET which utilizes the mechanical degree of freedom to overcome the 60 mV/dec
SS limit of MOSFET. Also, we achieve smaller $V_{pi}$ than the planar SGFET due to enhanced electrostatic coupling. Compared to traditional MEMS mechanical switches and NEM switches, a suspended field-effect channel does not rely on mechanical contacts with the gate electrode thus offers a potential of high reliability. Future scaling trends toward high speed UHF operation can be enabled by rational design and fabrication of nanoscale structures with further reduced dimensions.

Acknowledgements


References


Chapter 4
Differentially Functionalized Silicon Nanotubes (SiNTs)

Crystalline silicon nanotubes (Si-NTs) provide distinctive advantages as electrical and biochemical analysis scaffolds through their unique morphology and electrical tunability compared to solid nanowires or amorphous/non-conductive nanotubes. Such potentials are investigated in this chapter. Gate-dependent four probe current-voltage analysis reveals electrical properties such as resistivity to differ by nearly 3 orders between crystalline and amorphous Si-NTs. Analysis of transistor transfer characteristics yields field effect mobility of 40.0 cm²/V·s in crystalline Si-NTs. The hollow morphology also allows selective inner/outer surface functionalization and loading capability either as a carrier for molecular targets or as nanofluidic channel for biomolecular assays. We present for the first time a demonstration of internalization of fluorescent dyes (Rhodamine) and biomolecules (BSA) in Si NTs as long as 22 μm in length.
4.1 Introduction

In depth understanding of biomolecular interactions has led to more sophisticated diagnostics and therapeutic systems in the field of bioanalysis and biomedicine\(^1\) and prompted the development of biosensors with ever improving specimen selectivity, signal-to-noise sensitivity, and variety of detectible biomaterials\(^2-5\). Silicon nanowires have shown their potential as an advanced biosensor platform\(^6-10\) with real-time electrical readouts thanks to their reduced dimensionality, large surface-to-volume ratio, amplification of signal as an active field-effect device, selective surface modification for detecting specific targets, and abundant material processing knowledge derived from semiconductor manufacturing techniques.

Considerable efforts have been devoted to improve the performance of nanowire (NW) field-effect transistor (FET) biosensors. Point-like localized detection area along the NW axis via either dopant modulation\(^11\) or p-n heterostructures\(^12\) can enable finer spatial resolution and faster response. Multiplexing from nanowires array networks\(^13,14\) have paved the way toward extreme sensitivity in the range of femtomolar precision since multiple sensor arrays on a single chip correlate effectively to discriminate electrical false-positive signals. Meanwhile, series of techniques involving modification of NW structure\(^15,16\), device geometry\(^17\) and functionalization of NW surfaces\(^18\) have been demonstrated to further enhance the detection performance of NW FET biosensors. Beyond solid NWs, crystalline silicon nanotube\(^19\) (c-Si
NT) provides two distinctive inner and outer surfaces for analyte detection thus offering a new platform for novel applications as a biosensor. Unique morphology and non-cytotoxicity\textsuperscript{20,21} of Si NTs endow them with potential functionality for intravascular drug delivery/imaging by using their inner cavity to load biomolecular species\textsuperscript{21,22}. Previously, Shi et al. has examined the mechanism of one-dimensional nanostructure-cell interaction\textsuperscript{23} while Ben-Ishai et al. has shown selective binding of metal nanoparticle either on inner or outer surfaces of Si NTs\textsuperscript{24}. Meanwhile, electrically active high-quality c-Si NT themselves possess additional functionality as an FET channel sensitive to potential and charge modulations from environments both inside and outside. A combination of these traits makes c-Si NTs an attractive material for novel biosensor FET devices as recently demonstrated by R. Gao\textsuperscript{25}.

In this report, we present a fundamental study of c-Si NT properties as a platform for electrically and biochemically functional devices. Synthesis of Si NTs shows well-controlled inner diameter (6~90 nm) and wall thickness (4~40 nm) by selectively etching core/shell Ge/Si nanowires (NWs).

### 4.2 Synthesis of SiNTs

We used Ge/Si core/shell NWs as sacrificial templates to synthesize crystalline and amorphous Si NTs, as depicted in Figure 4.1, Ge/Si core/shell NWs were grown using a two-step process\textsuperscript{26,27}. The Si shell can be controlled to be epitaxially grown or amorphous by the process temperature. Ge/Si core/shell NWs were grown on Si (100) wafers by the well-known
vapor-liquid-solid (VLS) process using low-pressure chemical-vapor-deposition (ET-2000, CVD Corporation). Colloidal Au nanoparticles of 5-80 nm were dispersed on Si substrates as catalyst for Ge core growth using 1.8% GeH\textsubscript{4} in H\textsubscript{2} (300 Torr total pressure, 290°C). Subsequently, in-situ deposition of epitaxial, crystalline Si shells was carried out using 2% SiH\textsubscript{4} (30 Torr, 600°C) with varying growth duration depending on the desired shell thickness. During Si shell growth diborane (B\textsubscript{2}H\textsubscript{6}) was used as in-situ doping source at a flow rate of 20 sccm and a B:Si atomic ratio of 1:560. As a comparison, amorphous Si shells were grown using a lower temperature at 490 °C.

Following growth of core/shell NWs, Si NTs were synthesized by selective wet etching of Ge cores (see Supporting material for details). Figure 4.1b shows transmission electron microscope (TEM) image of as-synthesized c-Si NTs with inner diameter (ID) of 88±16 nm and 10 nm shell thickness. The ID is solely determined by the Ge core diameter during synthesis based on choice of the Au catalyst diameters. Using this method, NT with ID from 50 nm (Figure 4.1c) and, by using 5 nm diameter catalysts, to as small as 6.5 nm surrounded by 4 nm thick Si shell can be synthesized (inset of Figure 4.1c). The NT shells have relatively uniform thickness with 1~2 nm fluctuations. High-resolution TEM (Figure 4.1d) and fast Fourier transform (FFT) images (inset of Figure 4.1d) further reveal the highly crystalline nature of the c-Si NTs. The FFT shows the NT’s <112> growth
orientation with the measured 0.11 nm interatomic distance matching that of Si \{224\} planes\textsuperscript{28}. The 6 sharp diffraction spots around the centre indicate epitaxial deposition of Si layer following the Ge core. As shown in Figure 4.1e, we found these crystalline NTs to preserve their crystallinity even after been exposed in air at room temperature for 28 days. There is also little discernable change in their oxide layer thickness (shown as the light contrast layers on the outer surface of the TEM images)\textsuperscript{29}. Such stability is ideal for nanoelectronic and biomedical applications.
Figure 4.1: (a) Schematics of Si NT synthesis steps. (b) SiNTs shown in low-resolution TEM image and (c) Individual SiNT. (d) High-resolution TEM shows crystal lattice of a SiNT. (e) TEM from crystalline SiNT after 28 days exposed in air.

4.3 Electrical Properties of SiNTs

To establish the fundamental electrical properties of c-Si NTs, we performed four point probe measurement on c-Si FETs with 100 nm thick
thermal oxide layer as the back-gate dielectrics (Figure 4.2a). The devices were fabricated using standard e-beam lithography, metallization, and lift-off techniques. Four metal contacts of 1 μm width were deposited on each NT FET with 150/30 nm thick Ni/Au bilayer followed by rapid thermal annealing at 400°C for 30 seconds to improve electrical contacts between Si and Ni. Four-probe measurements were carried out using HP 4155A semiconductor parameter analyzer and SR560 voltage pre-amplifier to monitor the inner voltage drop $V_{D23}$ while capturing $I_D-V_{D14}$. First, gated two-probe I-V measurement across electrodes 1 and 4 (top inset, Figure 4.2b) shows typical p-type FET behavior, where the drain current increases with more negative gate voltages and begins to saturate at negative bias voltage. Meanwhile the four probe $I_D-V_{D23}$ measurement result (Figure 4.2b) shows clear linear $I$-$V$ curves indicating contact barriers are effectively eliminated. At $V_G = -20$ V, the two-probe resistance of the NT is 180 MΩ while only 4.4 MΩ when measured using the four-probe method, suggesting an average contact resistance of 88 MΩ which dominates the two-probe measurement results. Therefore, four-probe current-voltage ($I$-$V$) measurements are necessary in order to eliminate the effects from Schottky contact barriers at the Ni-Si contact interfaces and to represent intrinsic $I$-$V$ characteristics of the NT material.
**Figure 4.2:** $I_D$-$V$ characteristics under four different sets of gate biases from a representative c-Si NT FET with ID of 30 nm, shell thickness of 5 nm.

From the dimension of the NT and slopes of the linear $I_D$-$V_{D23}$, we can obtain the resistivity of crystalline Si NT to be 0.032, 0.069, 0.22, and 0.68 $\Omega \cdot $cm from gate voltage of -20 (red) to -5 V (green) with 5 V steps.

With decreasing gate bias, the four-probe NT conductance rises, representative of the linear-region transfer characteristics of a p-type FET\(^{30}\) (top right inset, Figure 4.2b), with transconductance ($g_m = dI/dV_G$) of 2.78 nS at $V_{D23} = 0.11$ V and an extrapolated threshold voltage of $V_T = -9.9$ V. From these values we can extract the low-field mobility $\mu$ based on a long channel.
transistor model using $\mu = g_m L^2 / C_G V_{DS}$. For estimation of the gate capacitance $C_G$ we used finite-element modelling similar to a previous study on the dielectric screening effect from low carrier density Si NWs and found that back gate capacitance coupling to NTs is near identical to NWs across a wide range of carrier concentrations.

To find $C_G$ we used finite element electrostatic simulation coupled with the equation,

$$\varepsilon, \varepsilon_0 \nabla^2 V(x, y) = q[p(V) - n(V) + N_A]$$

(4.1)

to evaluate the potential $V$ and hole carrier distribution in the cross-section of the NT or NW at different back-gate voltages in order to extract the gate capacitance. Here $p$, $n$ and $N_A$ represent hole density, electron density and unintentional doping/impurity doping density in the Si shell, respectively.

A cross-sectional view of the equipotential and hole carrier distribution is presented in Figure 4.3b and c, for the cases of a nanowire and a nanotube, respectively. Both cases have the same outer diameter (40 nm), with the difference being the NT is hollow inside its 30 nm ID. If we assume a doping level $N_A$ at $1 \times 10^{17}$ cm$^{-3}$, Figure 4.3b,c show that the hole carriers are mostly concentrated at the bottom surface and the outer circumference for both cases, regardless whether there is a void inside the NT. Indeed, as we experimented through a wide range of $N_A$ levels, the resulting gate capacitance $C_G$ is identical between NT and NW (Figure 4.3a inset) and
does not depend on $N_A$ at on state ($V_G = -20 \text{ V}$). This is a result of the screening effect from large amount of hole carriers distributed on the outer surface of the NW or NT, making both materials behave similar to a metallic cylindrical conductor. As Figure 4.1a shows, $C_G$ also remains relatively constant with $V_G$ throughout most of the on-state and only decreases significantly at $V_G > -3 \text{ V}$ when the hole carriers are beginning to be depleted. Although in our experiments, the exact activated dopant level $N_A$ is yet to be determined due to the c-Si FETs exhibiting enhancement mode (normally-off) FET behavior, since $C_G$ is insensitive to $N_A$ as our simulation shows, we can use $C_G = 3.37 \text{ fF}$ to extract the on-state field effect mobility of the device in Figure 4.2.

![Figure 4.3](image)

**Figure 4.3:** Two-dimensional finite element electrostatic analysis of gate capacitance for NT and NW structure using COMSOL Multiphysics.

Field-effect mobility for the c-Si NT in Figure 4.2 is $40.0 \text{ cm}^2/\text{V} \cdot \text{s}$, which is comparable to values reported in bulk polycrystalline Si with large
grain sizes\textsuperscript{32-34}. One can also obtain mobility from the Ohm’s law using the Drude model: \( \sigma = n_e \mu = (V_G - V_T)C_G\mu/L^2 \) which yields \( \mu = 40.6 \text{ cm}^2/\text{V} \cdot \text{s} \).

These robust performances attest to the highly crystalline nature of the electronically active Si nanotube channels.

**Figure 4.4:** *I-V characteristics under four different sets of gate biases from a representative a-Si NT FET with ID of 20 nm, shell thickness 40 nm and length of 2 \( \mu \)m between the two inner contacts.*

The high conductivity of our c-Si NTs is also evident when compared with *I-V* measurement of amorphous Si NT (a-Si NT) FETs. We intentionally synthesized a-Si NTs using a modified growth recipe with Si shell growth at a lower temperature for 2 hrs which produced 40 nm thick amorphous shells as
confirmed by TEM and the lack of distinctive spots from selected area electron diffraction (SAED) patterns (Figure 4.4b). Compared to the thin, 4~5 nm thick c-Si NTs, here a thick a-Si shell thickness was necessary to achieve measurable conductance above the noise level of our measurement system. a-Si NTFET device was fabricated with four 2 μm wide Ni/Au contacts and an inner channel length of 2 μm (Figure 4.4a). Two probe $I_D-V_D$ measurement (top inset of Figure 4.4b) shows non-linear, Schottky contact behaviour and p-type characteristics with a maximum on current of less than 50 pA under 30 V bias with $V_G$ as small as -40 V. Four-probe conductance in Figure 3b shows an intrinsic resistivity of 28.8, 24.8, and 22.7 Ω·cm for -20, -30, and -40 V gate bias respectively with more apparent noise in the $I-V$ curves due to the low current level. These values in a-Si NT are nearly 3 orders more resistive than the on-state resistivity from c-Si NTs. Such difference is a direct result of their respective morphologies.

### 4.4 Functionalization of SiNTs

Previously extensively studies have shown decoration of Si NWs with a wide selection of biomolecules with help from covalently bonded silane chemistry. To explore the potential integration and compatibility of our c-Si NTs with bio-specimens, in particular the capability of introducing analytes on the inner surface and cavity of the NT, we have further studied selective
surface functionalization on the NT’s inner and outer surfaces (Figure 4.5). The outer silicon surface was first selectively functionalized with polyethylene glycol (PEGylation) as a stealth moiety. We begin with outer surface PEGylation of the as-grown core/shell NWs using trimethoxysilane PEG (2 kDa, ProChimia) upon immediate cool-down and removal from the growth chamber.

The surface of as-grown Ge/Si core/shell NWs was first cleaned and activated by a UV cleaner (Jelight, model 42) for 20 min. The growth wafer then reacted in trimethoxysilane PEG solution (2 mg in 200 µl toluene) for 30 minutes, followed by rinsing with toluene and acetonitrile for three times. It is worth noting that both the growth substrate and the NWs outer surface were covered in this step during PEGylation. The entire growth substrate was then sonicated in isopropyl alcohol (IPA) to break off the PEG-encapsulated NWs from the substrates and to expose clean, naked terminals of the Ge core to allow for the subsequent Ge core etching. The etching step was performed in the solution of IPA/30% hydrogen peroxide 3:1 v/v at 60 °C for 3 hours.
Figure 4.5: Schematic illustration of selective biomolecule functionalization. (a) PEGylation process on the outer wall of Si NTs followed by Ge core removal for inner wall functionalization. (b) Two types of biomolecules, Rhodamine and BSA-FITC, loading inside the cavity of Si NTs.

PEGylated NWs are cleaved and suspended in solvent using an ultrasonicator to expose the fresh Ge on the ends. This is followed by etch removal of the Ge core to form hollow SiNTs with the inner surface being fresh Si while outer surface protected by PEG (Figure 4.5a).

Here we demonstrate loading of two different molecules, Rhodamine (Figure 4.5b) and bovine serum albumin (BSA)-fluorescein isothiocyanate (FITC) conjugates (Figure 4.5c) into Si NTs. The Rhodamine and FITC are
red and green fluorescent respectively and are used to help visualize the loading results. The average ID size of NTs used is 30 nm.

First, for loading of Rhodamine molecules, 3-aminopropyltriethoxysilane (APTES) was used as a self-assembled monolayer on the inner surface of the SiNT to enable covalent bonding to the carboxylic group on Rhodamine. More specifically, Si NTs with PEG on the outer surface were centrifuged to exchange buffer solution with DI water using a 30K MWCO centrifuge filter. Subsequently, inner surfaces of Si NTs were hydraoxylated with 2M nitric acid, then coated with 3-aminopropyltriethoxysilane (APTES) as a self-assembled monolayer to enable the covalent bonding to the carboxylic group on Rhodamine. 2% (v/v) APTES was added to the Si NTs solution and reacted for 4 hours. Excessive APTES was removed by a 100K MWCO centrifuge filter. The purified solution was mixed with 5 mM Rhodamine dye (Sigma-Aldrich) in methanol and kept reacting overnight. After reaction, excess Rhodamine dye was removed by using 30K MWCO centrifuge filter and the functionalized Si NTs were dispersed in DI water.

Far-field fluorescent optical images (Figures 4.6a and b right panels) along with corresponding bright-field images (Figures 4.6a and b left panels) of functionalized Si NTs show a fluorescent rod-shaped structure 5 µm in length suggesting the successful functionalization of Rhodamine in the Si NTs. As a control experiment and to verify that Rhodamine is not attached to
the outer surfaces, we performed the same functionalization procedures on solid core Ge/Si core/shell NWs. The solid NW surfaces are identical to the outer surface of hollow NTs and are PEGlyated via the same procedure. Absence of fluorescence (Figure 4.6c right panel) compared to the NW in the corresponding bright-field image (Figure 4.6c left panel) confirms the high selectivity of functionalization on the nanotube inner surface only and demonstrates the high quality PEGylation on the outer Si surface preventing any side reaction with APTES or fluorescent molecules which could be attached directly onto Si. Therefore we have shown that with protective PEGylation of the outer surface, the inner surface of the Si NT can be selectively functionalized and loaded with small molecules.
Figure 4.6: Demonstration of Rhodamine loading. (a) and (b) Bright field (left) and fluorescent (right) images showing red fluorescent signals in Rhodamine-loaded Si NTs. (c) Control sample after APTES functionalization and incubation with Rhodamine using a solid core Ge/Si nanowire. Scale bars, 3 μm.

Beyond fluorescent dyes, we further experimented with a larger, FITC decorated BSA molecule loaded inside Si NTs (Figure 4.7). BSA is a single polypeptide chain with 580 amino acid residues, and contains 17 intrachain disulfie bridges and 1 sulfhydryl group.$^{36}$ A BSA protein is approximately 14 nm x 4 nm x 4 nm in size.
To synthesize BSA-FITC conjugates, thiol-maleimide coupling chemistry was used. BSA was dissolved at 20 mg/mL in pH 7.0 10 mM phosphate buffer. Disulfide bonds in BSA were reduced by 100 fold excess of dithiothreitol (DTT) for 20 min. Excessive DTT was removed by desalt column (Thermo Scientific). DTT treated thiol-BSA was then reacted with maleimide-FITC for overnight, and the resulting BSA-FITC was purified by 30K MWCO centrifuge filtration.

From the right panel of Figure 4.7a, rod-shaped green fluorescence signals are clearly observed in NTs shown in the bright field image (Figure 4.7a, left), indicating fluorescently functionalized proteins (BSA) are successfully loaded within Si NTs. Significantly, Figure 4.7a shows loading of BSA in an NT as long as 22 µm. Similar to the case with Rhodamine, a control experiment loading BSA-FITC into solid core/shell Ge/Si NWs shows no fluorescence from its outer surface (Figure 4.7b, right) of the corresponding NWs in the bright-field image (Figure 4.7b, left), which again demonstrates the lack of leakage path or side reaction through the encapsulated PEG layers on the outer surface of Si NTs or NWs and most importantly, the successful selective functionalization of the inner walls of Si NTs by relatively large protein molecules.
Figure 4.7: Demonstration of BSA-FITC functionalization. (a) BSA-FITC-loaded Si NTs from bright field (left) shows green fluorescent (right) signals while (b) control sample of a solid Ge/Si nanowire functionalized in the same condition presents no fluorescent signal. Scale bars, 5 μm.

4.5 Conclusion

In summary, we have explored the potential of crystalline Si NTs as an electrically active and biochemically compatible material in ways that distinguish them from solid NWs. TEM analysis reveals the crystalline nature of the as-synthesized NTs. Four probe transport analysis yields field effect mobility of 40 cm²/V·sec for the c-Si NT and a resistivity as small as 0.032 Ω·cm, nearly 3 orders more conductive than that of amorphous Si NTs. Such demonstrated electrical property in c-Si NTs may extend to much broader applications such as high
efficiency thermoelectric modules due to phonon confinement effects in Si NTs\textsuperscript{37,38}. Moreover, by selectively functionalizing the inner/outer surfaces, we demonstrated uptake of molecules from small dye molecules to proteins bonded on the NT inner surface, which when combined with the electrically active NT channel have the potential to lead to a range of novel therapeutic drug delivery or diagnostic detection applications\textsuperscript{39-41}.

**Acknowledgments**

Chapter 4 is in part a reprint of “Selective functionalization and loading of biomolecules in crystalline silicon nanotube field-effect transistors”, *Nanoscale* (2014).

**References**


